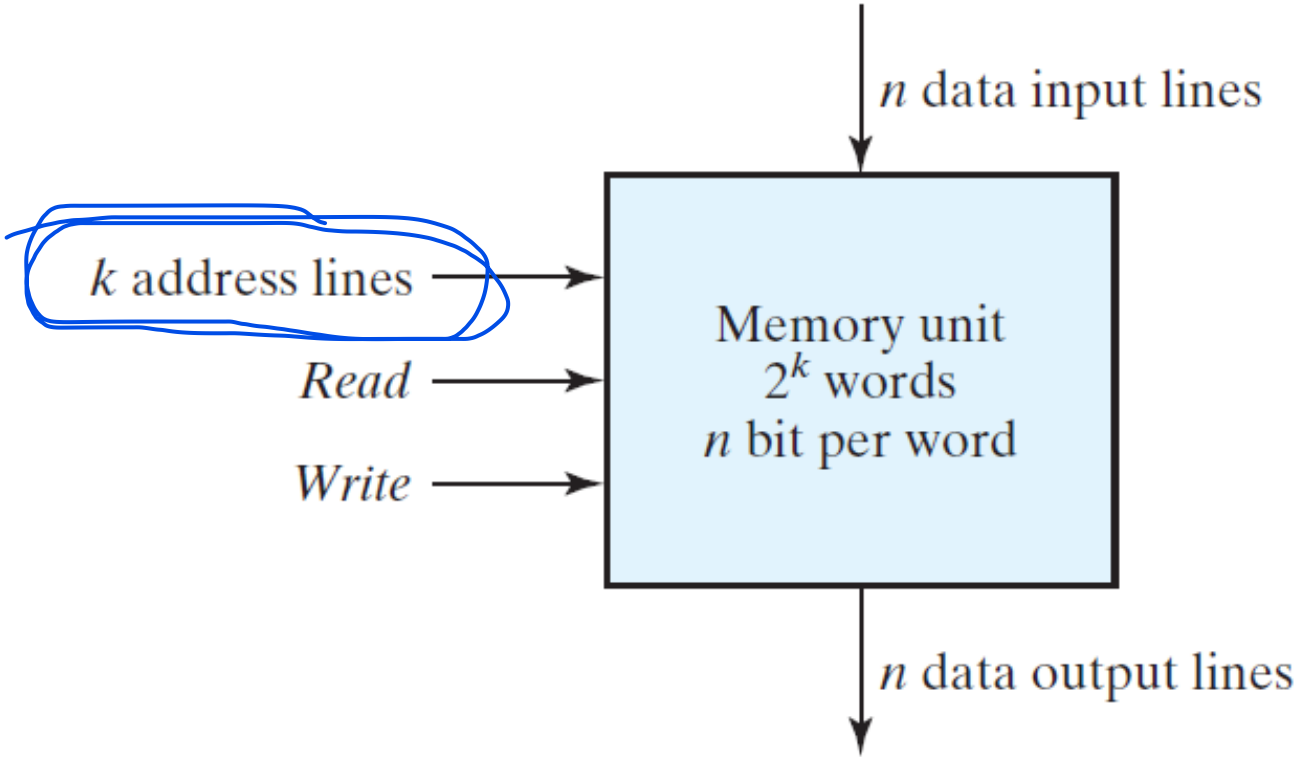
Chapter 7: Memory

Memory

- **RANDOM-ACCESS MEMORY (RAM)**
  - A memory unit is a collection of storage cells together with associated circuits needed to transfer information in and out of the device.
  - Memory cells can be accessed for information transfer to or from any desired random location and hence the name *random access memory, abbreviated RAM.*
  - The capacity of a memory unit is usually stated as the total number of bytes that it can store.

Memory

- **RANDOM-ACCESS MEMORY (RAM)**



Memory

- **RANDOM-ACCESS MEMORY (RAM)**
  - A memory unit with a capacity of 1K words of 16 bits each. What is the total memory size?

Memory address		Memory content
Binary	Decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Memory

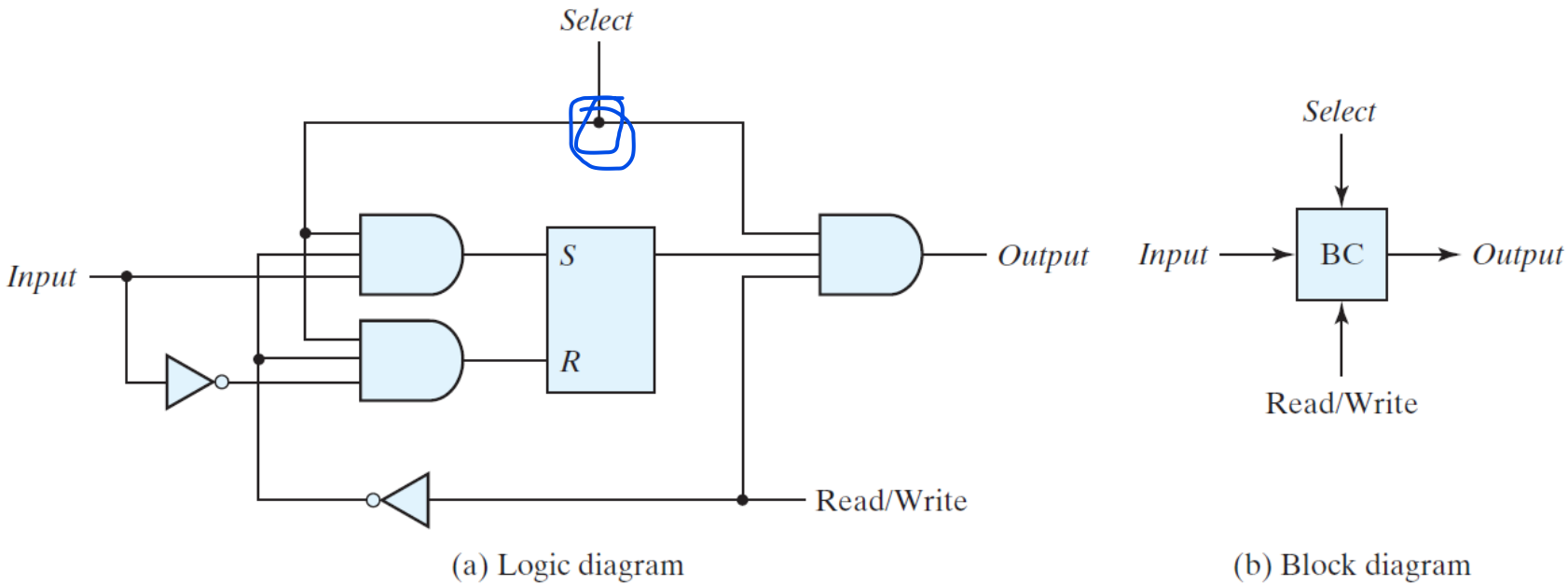
- **Write and Read Operations**
  - The steps required for write operation
    - Transfer the binary address of the desired word to the address lines.
    - Transfer the data bits that must be stored in memory to the data input lines.
    - Activate the *write input.*
  - The steps required for read operation
    - Transfer the binary address of the desired word to the address lines.
    - Activate the *read input*

Memory

- **Properties of Memory**
  - Integrated-circuit RAM may be either static or dynamic
  - Static RAM (SRAM) consists of internal latches that store the binary information
  - Dynamic RAM (DRAM) stores the binary information in the form of electric charges on capacitors
  - Both SRAM and DRAM are volatile memory
  - Magnetic disk and ROM are non-volatile memory

Memory

- **Internal Construction (1x1 SRAM)**

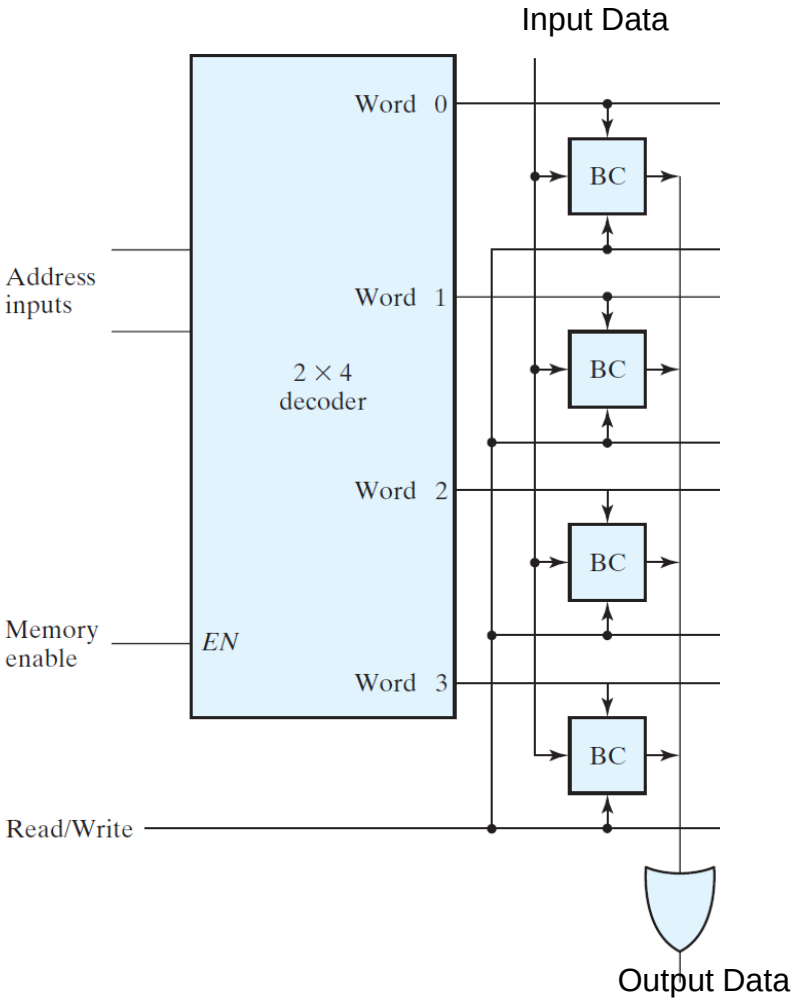


(a) Logic diagram

(b) Block diagram

Memory

❑ Logic Construction of a 4x1 SRAM



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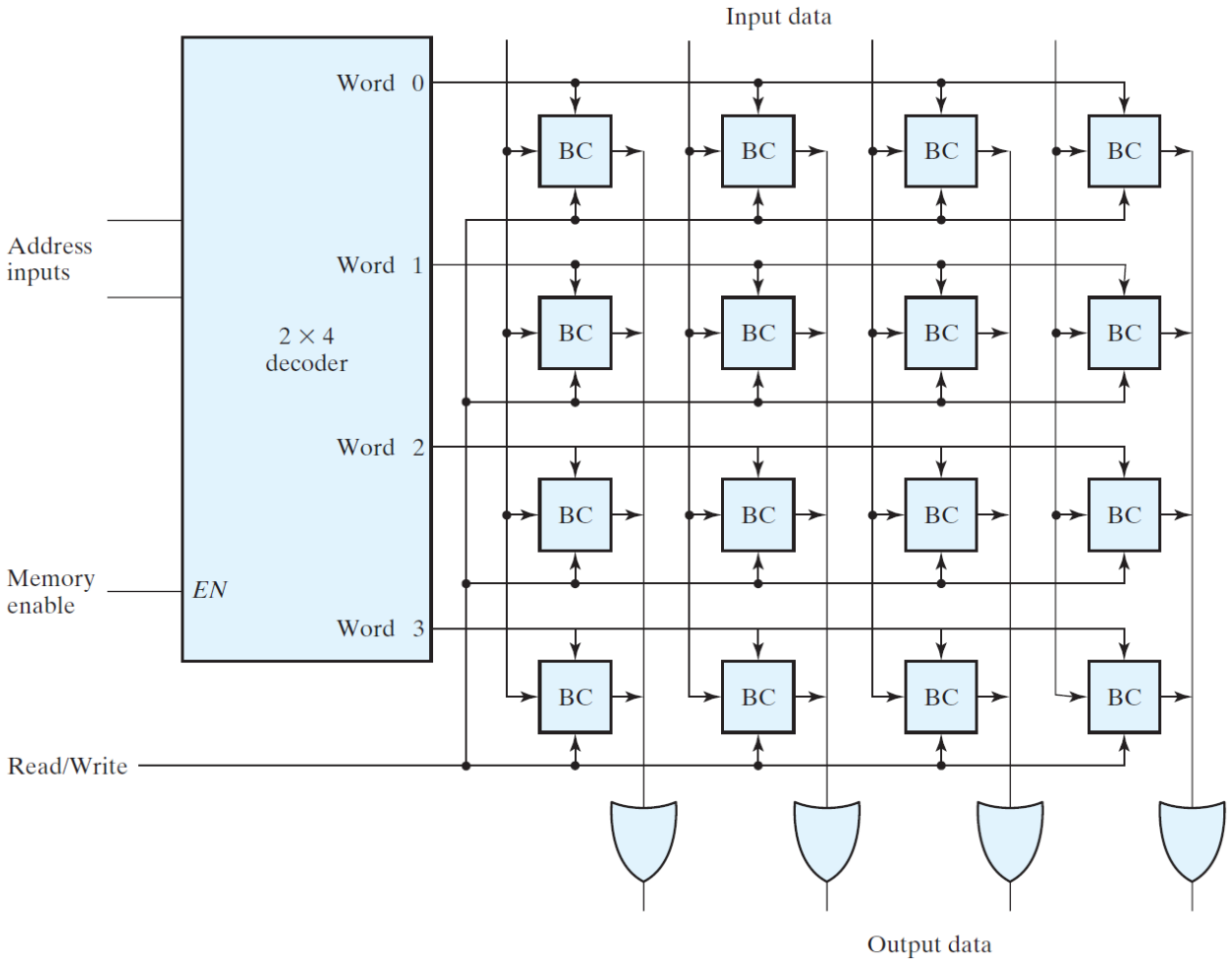
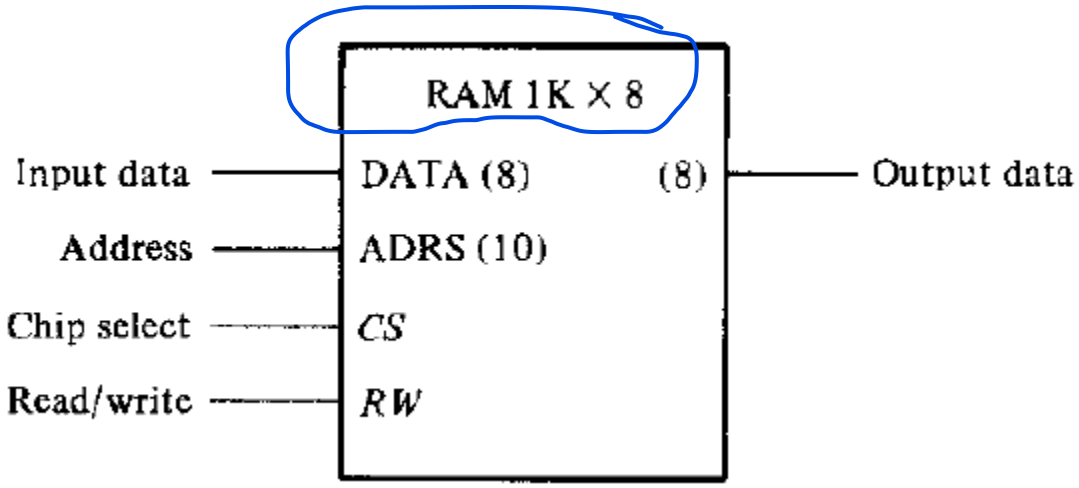
❑ Logic Construction of a 4x4 SRAM



Memory

❑ SRAM Chips



- RAM chips are available in verity of sizes.
- The capacity of RAM depends on two parameters
  - Address size
  - Word size

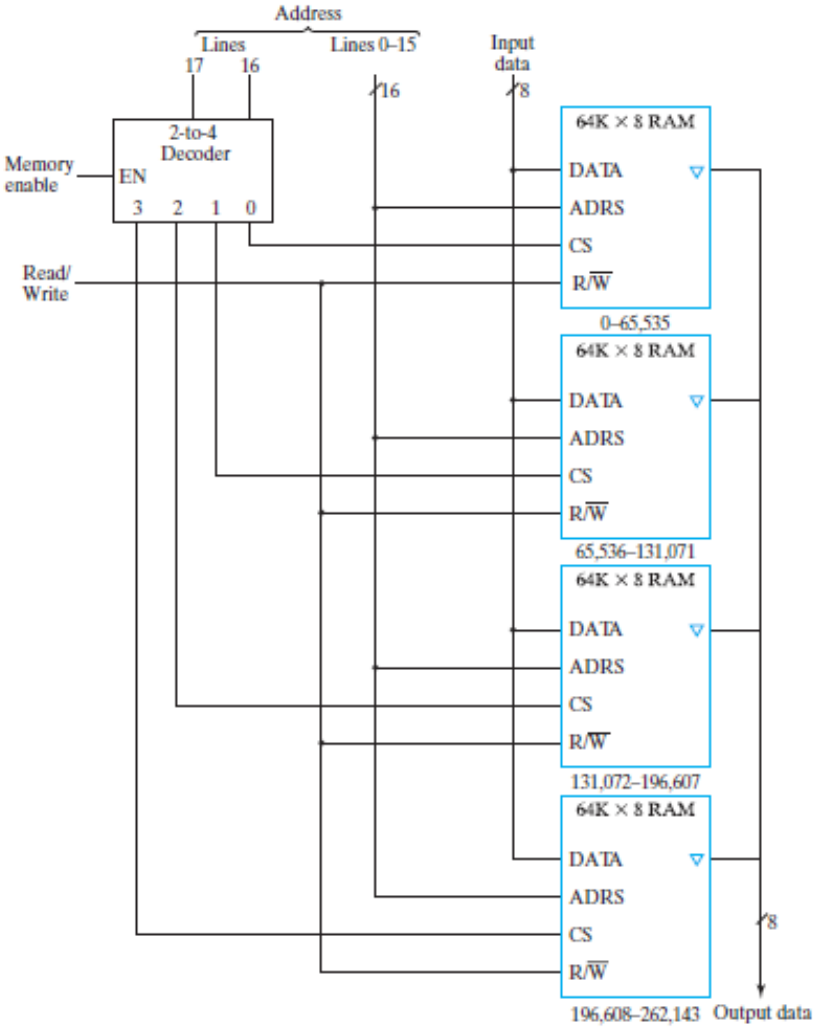
Memory

- **Array of SRAM Chips**
  - We have many RAM chips of small size but we want a RAM with larger size
  - How to increase the RAM size?
    - Increasing the address size
      - Increasing 1 bit of address size doubles the memory size

      and/or
    - Increasing the word size.
      - Increasing one bit of word size increases the memory size with the amount of the address.
    - How to make array of RAM chips.

Memory

- **Array of SRAM Chips**
  - Increasing address size
  - Block Diagram of a 256K * 8 RAM



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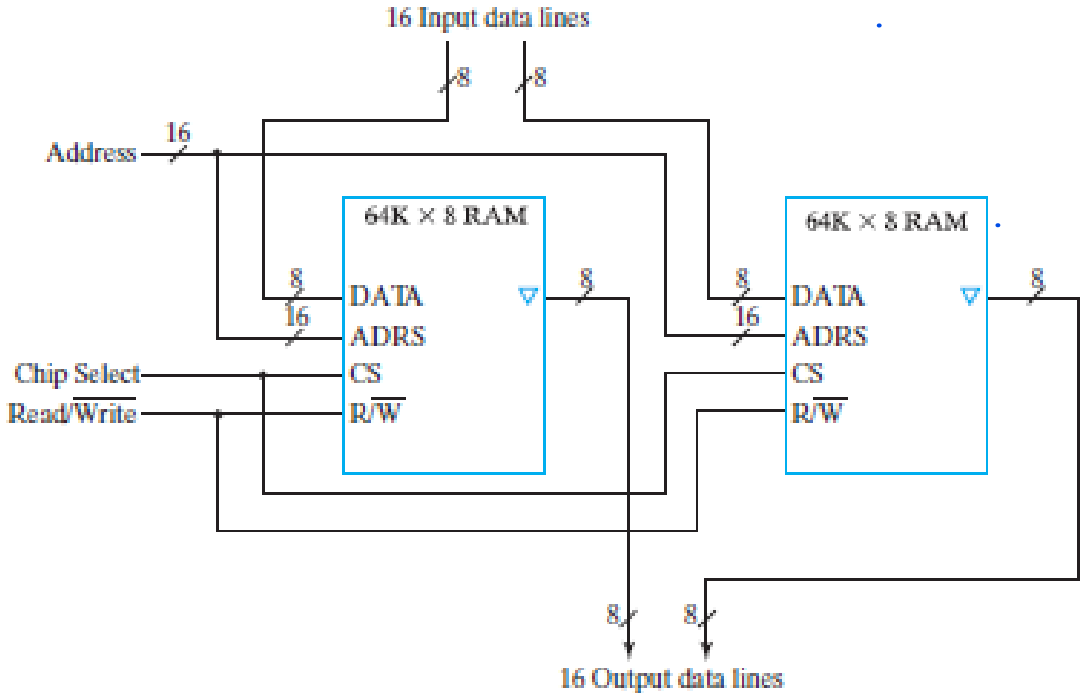
- **Array of SRAM Chips**
  - Increasing word size
  - Block Diagram of a 64K * 16 RAM



Memory

- **ERROR-CORRECTING CODE**
  - The complexity level of a memory array may cause occasional errors in storing and retrieving the binary information.
  - The reliability of a memory unit may be improved by employing error-detecting and correcting codes.
  - The most common error-detection scheme is the parity bit.
  - Other error correcting codes for example hamming code can also be used.

Memory

❑ Problems

7-35 (a) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(b) How many lines of the address must be used to access 2048 bytes? How many of these lines are connected to the address inputs of all chips?

(c) How many lines must be decoded for the chip-select inputs? Specify the size of the decoder.

7 -36 A computer uses RAM chips of 1024 x I capacity.

(a) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?

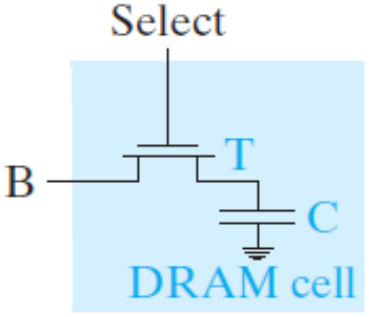
(b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected.

Memory

- Dynamic RAM
  - The name “dynamic” implies, the storage of information is inherently only temporary.
  - The information must be periodically “refreshed”
  - Provide high storage capacity at low cost
    - Dominates the high-capacity memory applications, including the primary RAM in computers.
  - Logically, DRAM in many ways is similar to SRAM.
  - Its electronic design is considerably more challenging.
  - Need for refresh is the primary logical difference in the behavior of DRAM compared to SRAM.

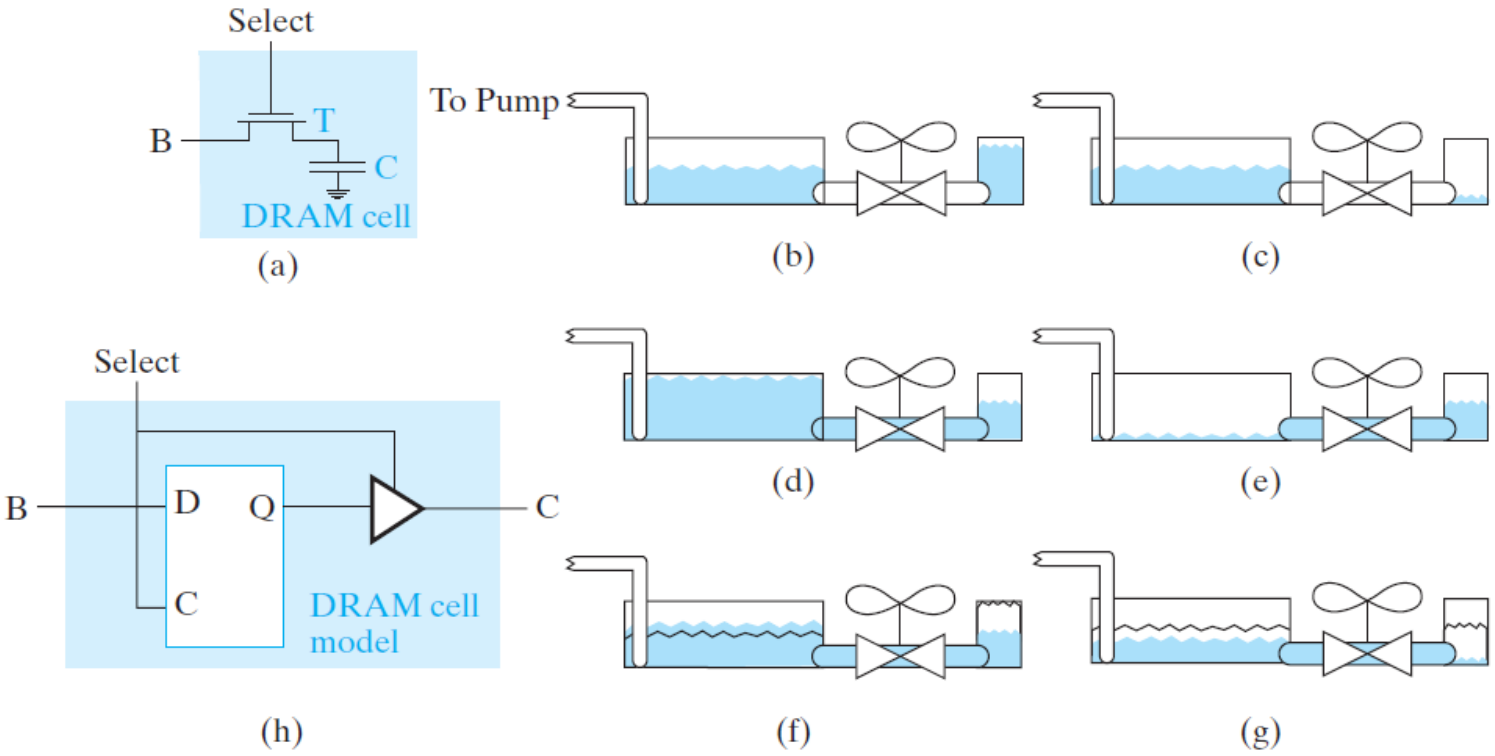
Memory

- DRAM Cell
  - The DRAM cell consists of a capacitor C and a transistor T.
  - The capacitor is used to store electrical charge.
    - If sufficient charge is stored, it can be viewed as storing a logical 1.
    - If insufficient charge is stored, it can be viewed as storing a logical 0.
  - The transistor acts much like a switch,
    - When the switch is “open,” the charge on the capacitor roughly remains fixed—in other words, is stored.
    - When the switch is “closed,” charge can flow into and out of the capacitor from the external Bit (B) line.
  - This charge flow allows the cell to be written with a 1 or 0 and to be read.



Memory

- DRAM Operation



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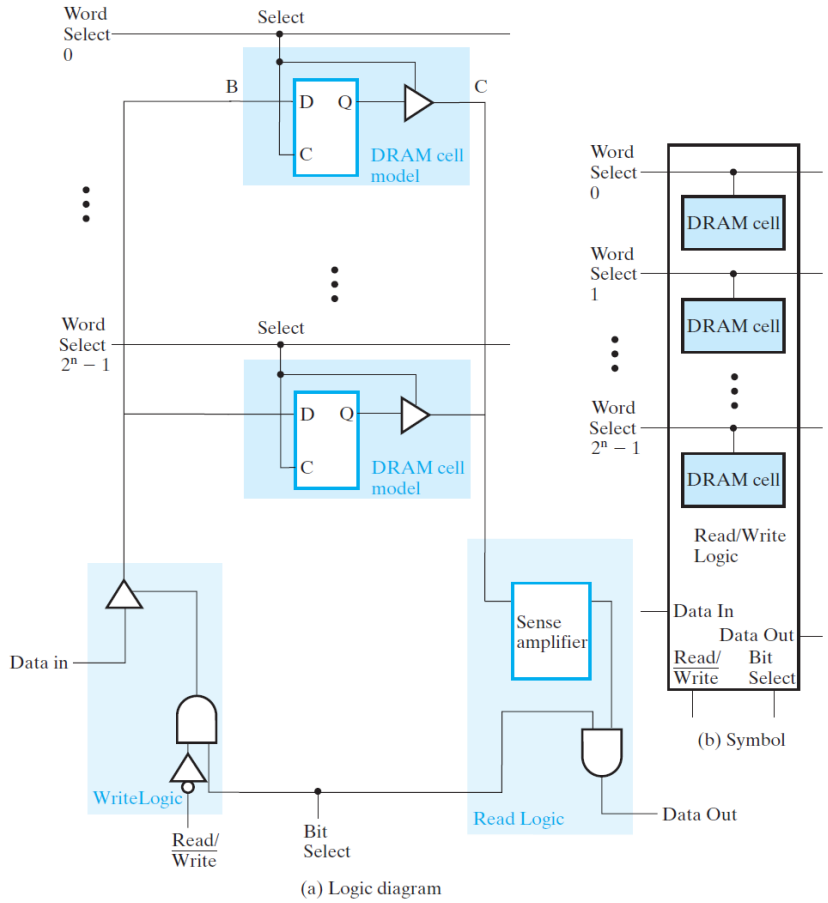
- DRAM bit Slice model



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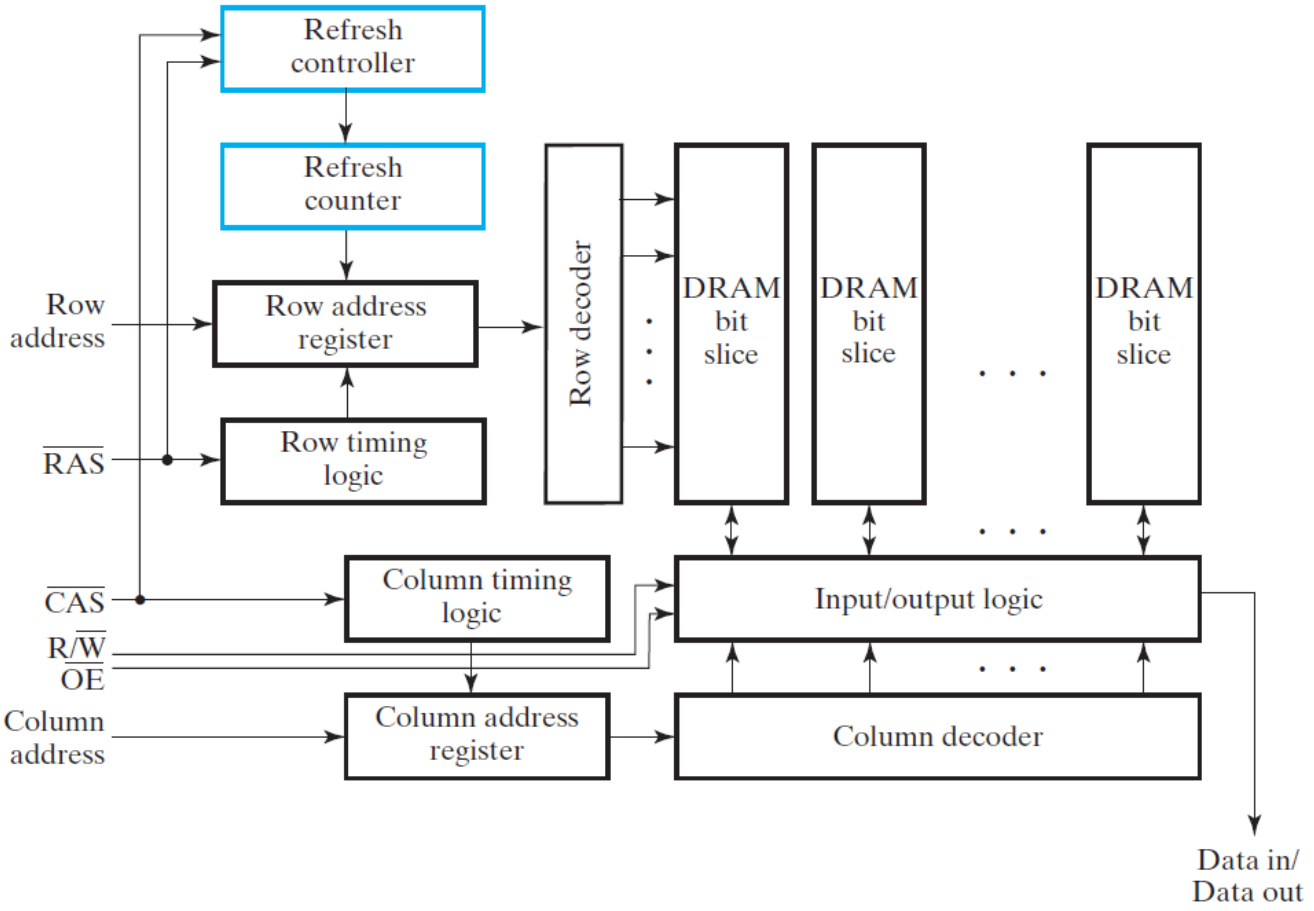
- Block Diagram of a DRAM Including Refresh Logic



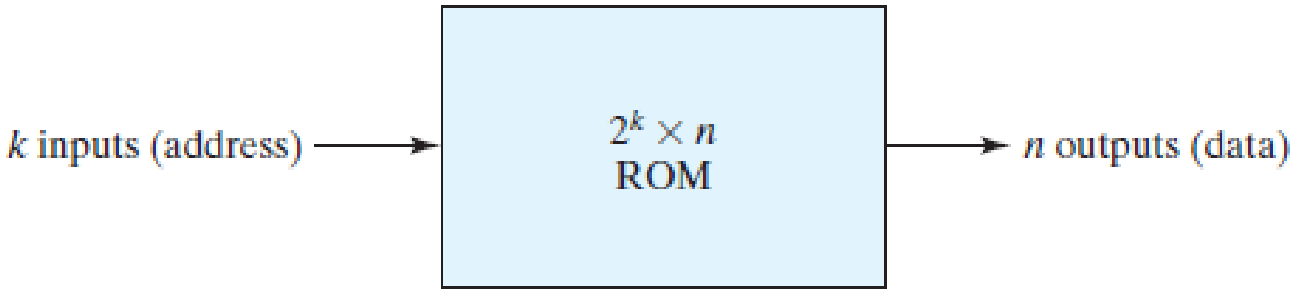
Memory

- Types of DRAM
  - Fast page mode DRAM (FPM DRAM)
  - Extended data output DRAM (EDO DRAM)
  - Synchronous DRAM (SDRAM)
  - Double-data-rate synchronous DRAM (DDR SDRAM)
  - Rambus DRAM (RDRAM)

Type	Abbreviation	Description
Fast page mode DRAM	FPM DRAM	Takes advantage of the fact that, when a row is accessed, all of the row values are available to be read out. By changing the column address, data from different addresses can be read out without reapplying the row address and waiting for the delay associated with reading out the row cells to pass if the row portions of the addresses match.
Extended data output DRAM	EDO DRAM	Extends the length of time that the DRAM holds the data values on its output, permitting the CPU to perform other tasks during the access, since it knows the data will still be available.
Synchronous DRAM	SDRAM	Operates with a clock rather than being asynchronous. This permits a tighter interaction between memory and CPU, since the CPU knows exactly when the data will be available. SDRAM also takes advantage of the row value availability and divides memory into distinct banks, permitting overlapped accesses.
Double-data-rate synchronous DRAM	DDR SDRAM	The same as SDRAM except that data output is provided on both the negative and the positive clock edges.
Rambus® DRAM	RDRAM	A proprietary technology that provides very high memory access rates using a relatively narrow bus.

Memory

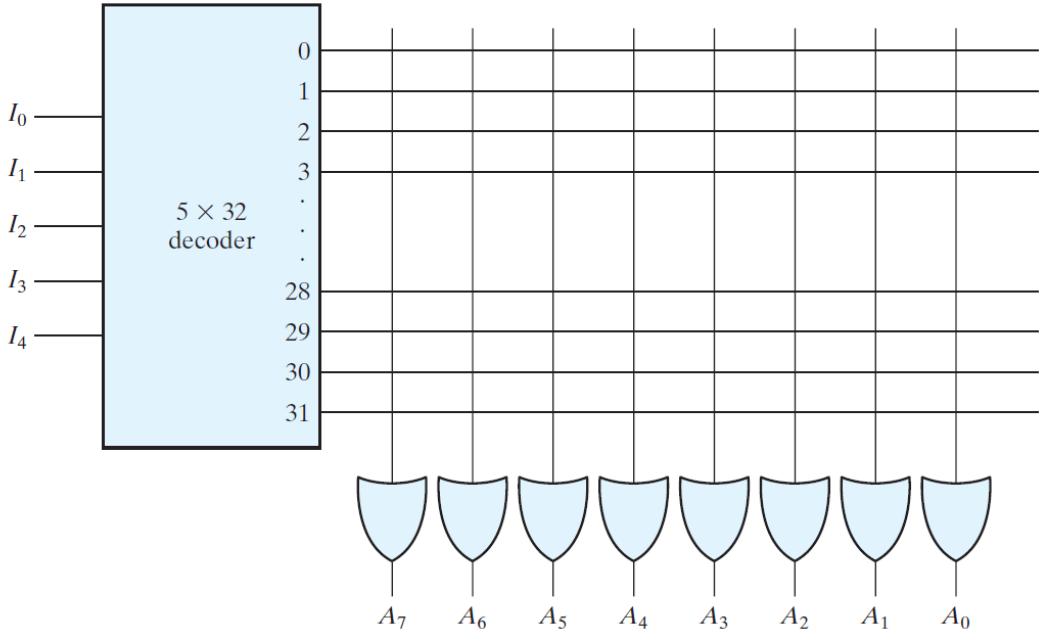
- ROM
  - A read-only memory (ROM) is essentially a memory device in which permanent binary information is stored.
  - The binary information must be specified by the designer and is then embedded in the unit to form the required interconnection pattern.
  - Once the pattern is established, it stays within the unit even when power is turned off and on again.



Block Diagram of ROM

Memory

- ROM
  - Internal logic
    - Each OR gate has 32 inputs.
    - Each output of decoder is connected to one of the inputs of OR gate.
    - The ROM contains 32 * 8 = 256 internal connections.
    - In general, a 2^k x n ROM will have an internal k x 2^k decoder and n OR gates. Each OR gate has 2^k inputs



Memory

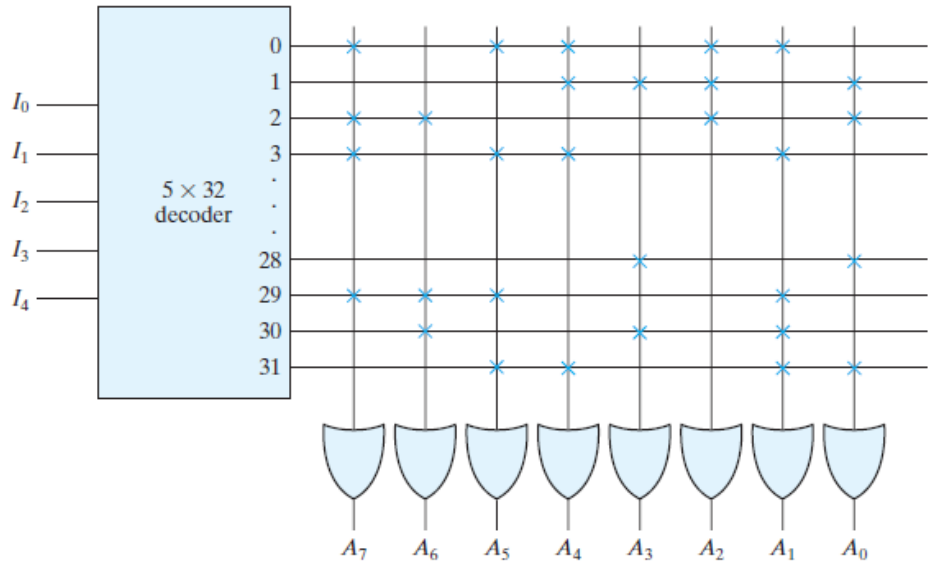
- ROM
  - Crosspoint
    - The 256 intersections are programmable.
    - A programmable connection between two lines is logically equivalent to a switch that can closed or open
    - The programmable intersection between two lines is sometimes called a *crosspoint* .
    - Various physical devices are used to implement crosspoint switches.
    - One of the simplest technologies employs a fuse that normally connects the two points, but is opened or “blown” by the application of a high-voltage pulse into the fuse.

Memory

- ROM
  - Programming

ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮							⋮			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1



Memory

- Memory Unit