Chapter 12

Lesson-34:

Topic	Lesson Learning Outcomes	Teaching-Learning Methodology	Assessment Method
Bus and Memory of Microprocessor based system	• to design Buffer based bus • To design memory systems	Class Lecture Question and answer	Test, exams, quiz, etc

Memory

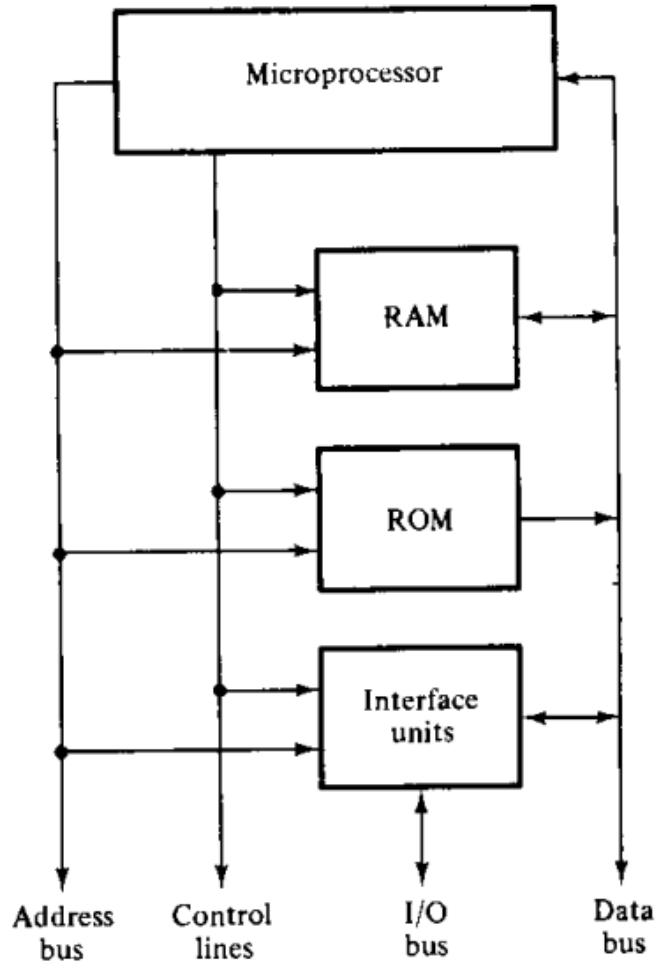
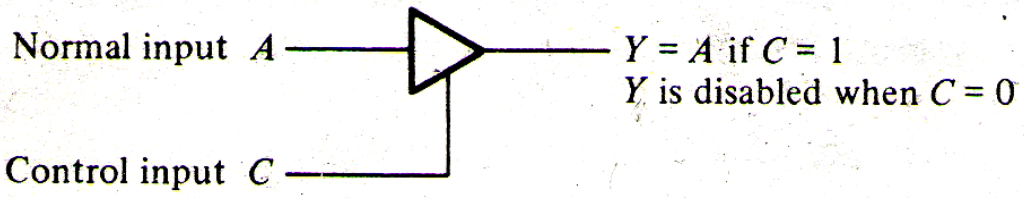


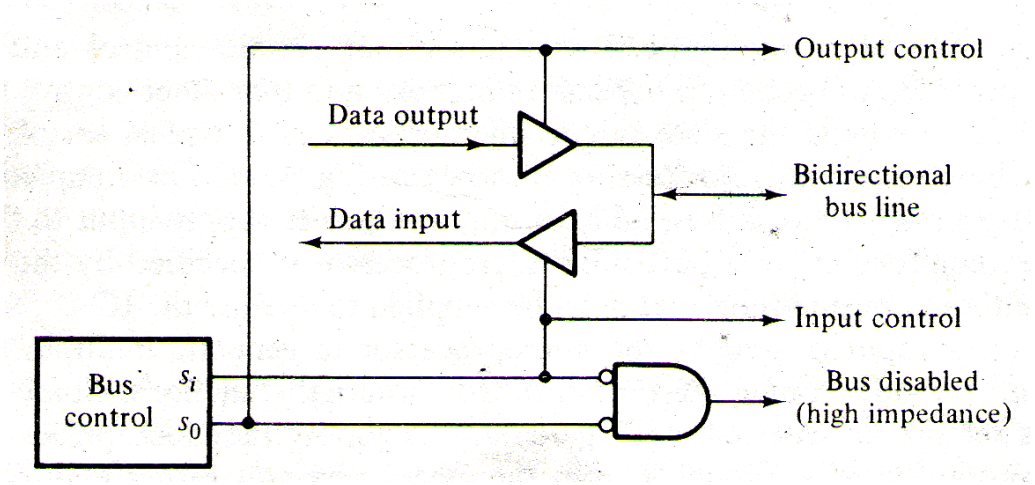
Figure 12-1 Microcomputer system block diagram

Memory

- Bus Design
  - 3 state unidirectional buffer can be used as address bus



  - 3 state bidirectional buffer can be used as data bus

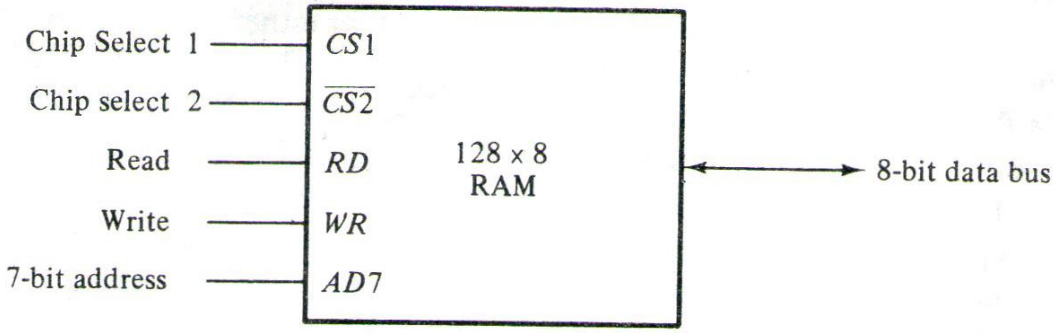


Memory

- Memory Organization
  - Microprocessor must communicate with memory
    - Both RAM and ROM
      - Distinguish between them in terms of computer design.
    - Is computer hard-disk a memory?
  - Size of memory
    - Depends on manufacturer of IC package
      - Data-word × address
    - Depends on the micro computer architecture specially address bus
      - 16 bit address line can accommodate up to 64K bytes

Memory

- RAM and ROM chips
  - Typical RAM chip



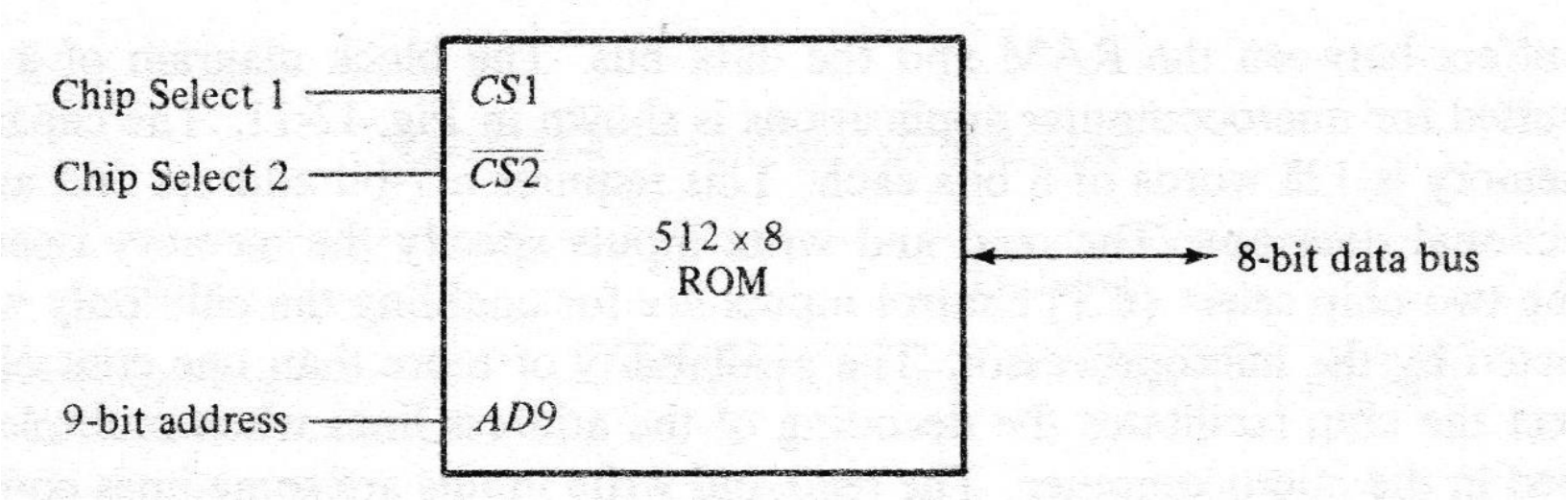
(a) Block diagram

$CS1$	$\overline{CS2}$	RD	WR	Memory function	State of data bus
0	0	X	X	Inhibit	High-impedance
0	1	X	X	Inhibit	High-impedance
1	0	0	0	Inhibit	High-impedance
1	0	0	1	Write	Input data to RAM
1	0	1	X	Read	Output data from RAM
1	1	X	X	Inhibit	High-impedance

(b) Function table

Memory

- RAM and ROM chips
  - Typical ROM chip



Memory

- Memory Address Mapping
  - A microprocessor system need
    - RAM 512 bytes
      - You have RAM chips of 128 bytes
    - ROM 512 bytes
      - You have ROM chips of 512 bytes

    How many chips are needed and how to map the address?

Memory

- Memory Address Mapping

Component	Hexadecimal address	Address bus									
		10	9	8	7	6	5	4	3	2	1
RAM 1	0000–007F	0	0	0	x	x	x	x	x	x	x
RAM 2	0080–00FF	0	0	1	x	x	x	x	x	x	x
RAM 3	0100–017F	0	1	0	x	x	x	x	x	x	x
RAM 4	0180–01FF	0	1	1	x	x	x	x	x	x	x
ROM	0200–03FF	1	x	x	x	x	x	x	x	x	x

Memory

- Memory connection to the microprocessor

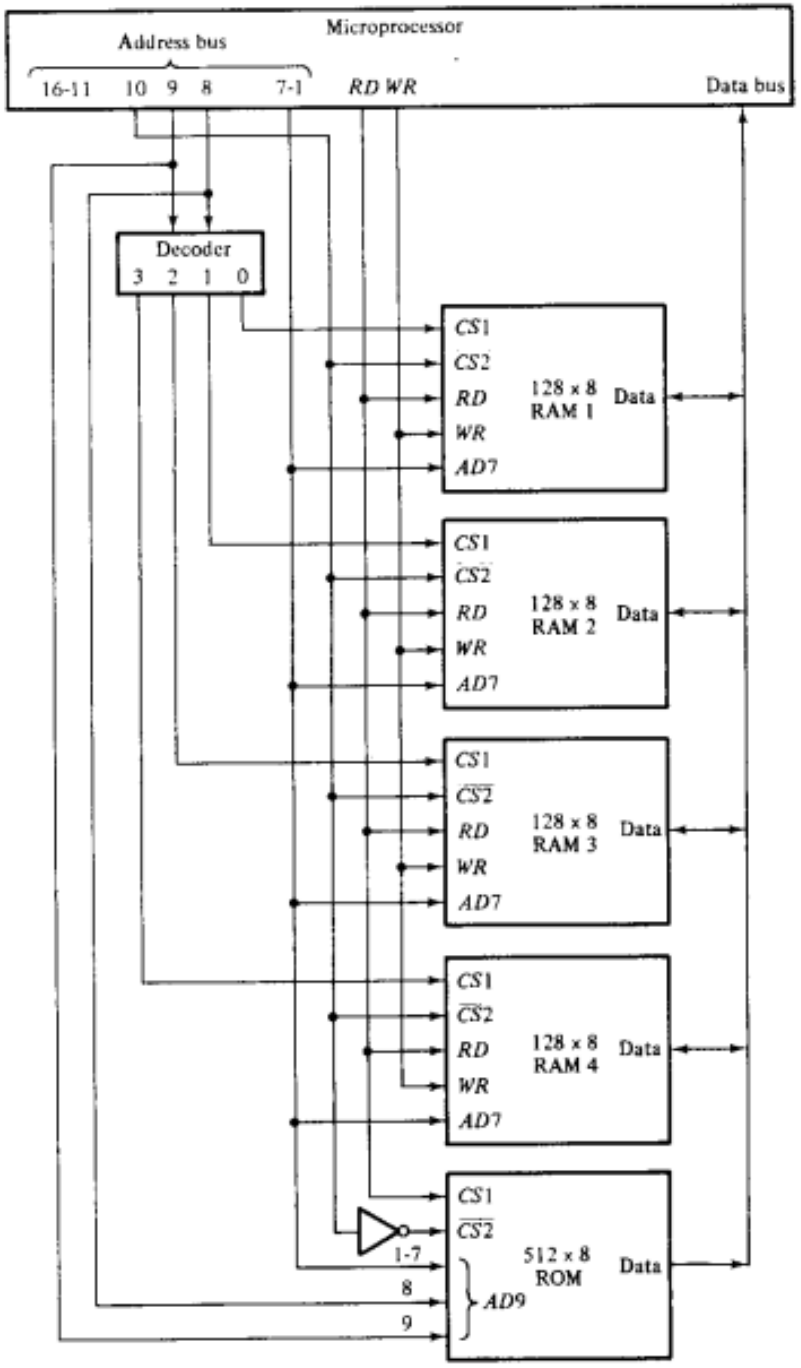


Figure 12-13 Memory connection to the microprocessor

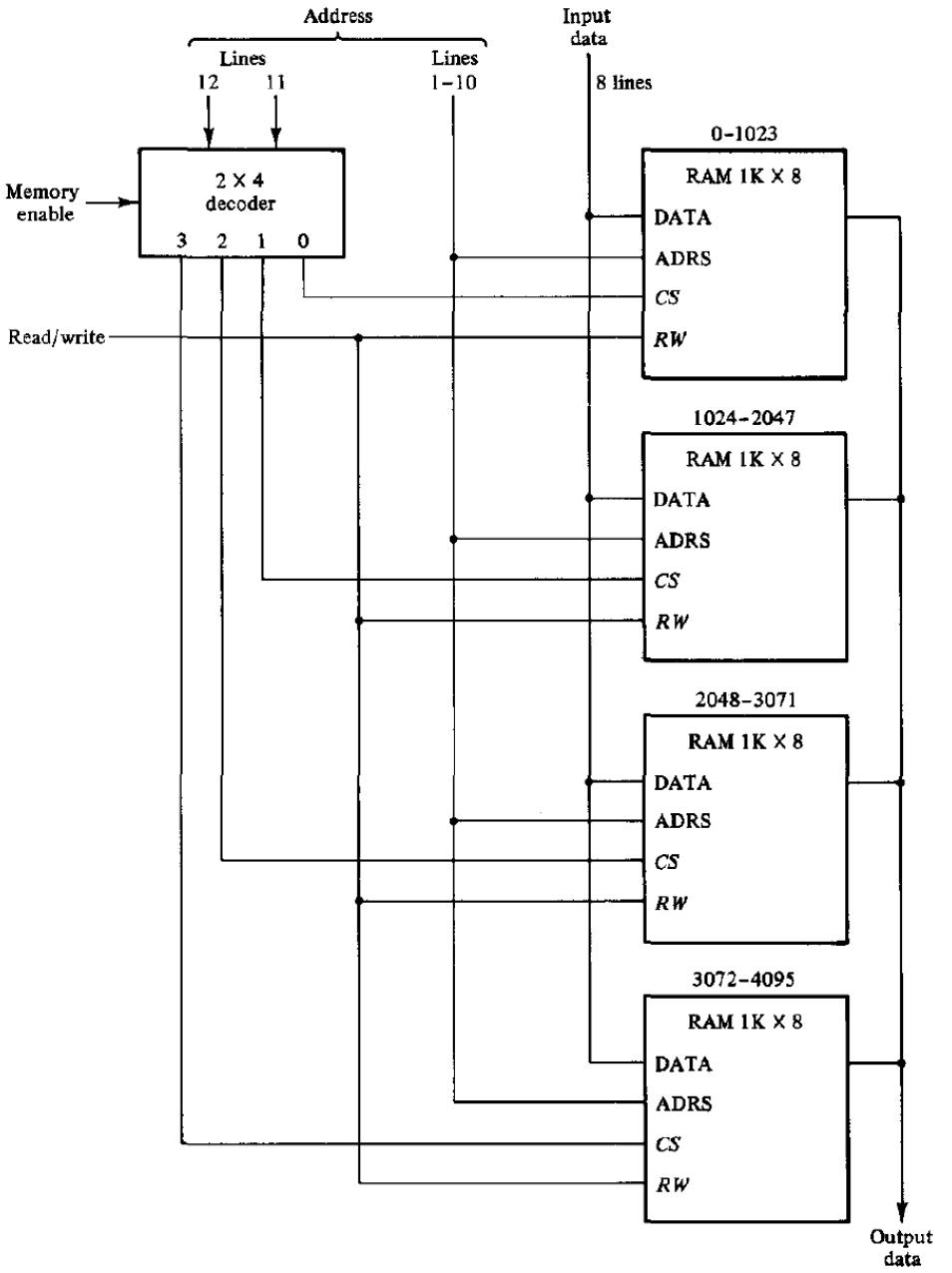
Memory

- **Array of RAM Chips**
  - We have many RAM chips of small size but we want a RAM with larger size
  - How to increase the RAM size?
    - Increasing the address size
      - Increasing 1 bit of address size doubles the memory size

      and/or
    - Increasing the word size.
      - Increasing one bit of word size increases the memory size with the amount of the address.
    - How to make array of RAM chips.

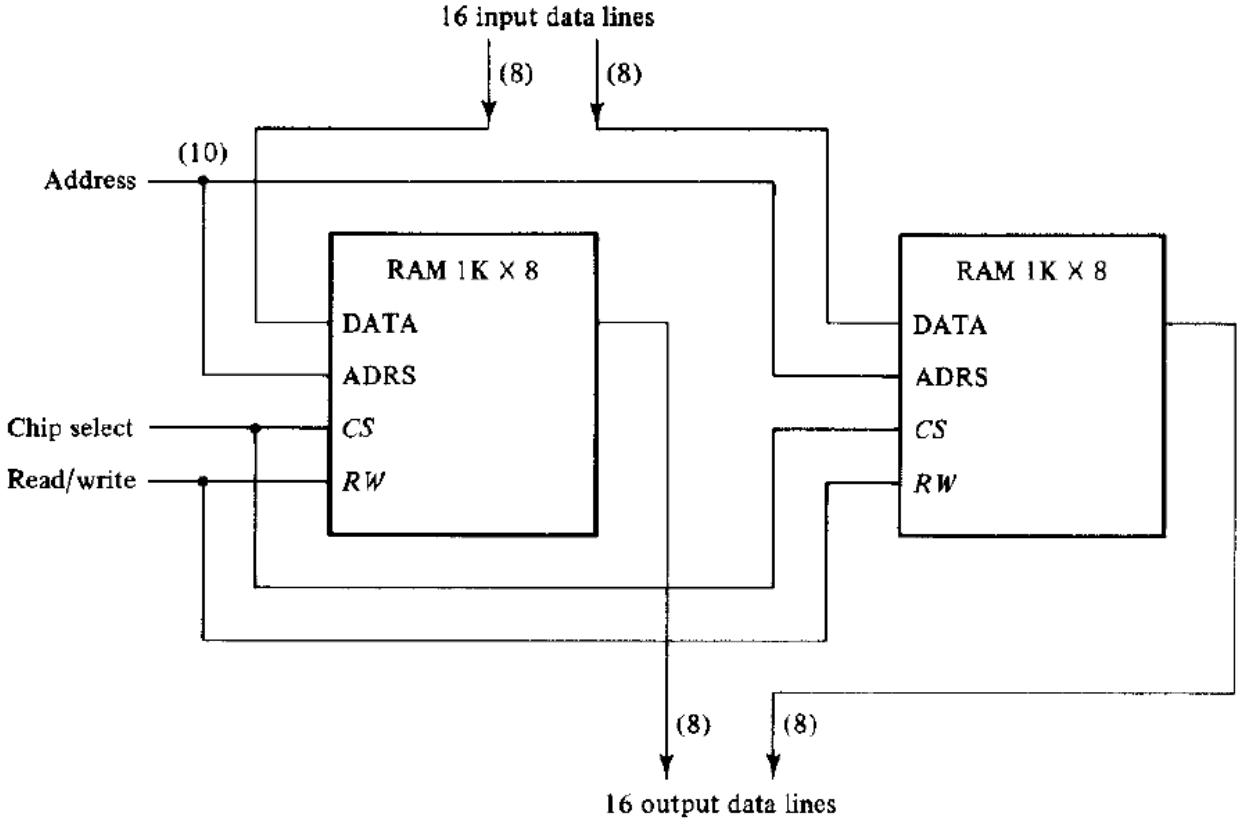
Memory

- **Array of RAM Chips**
  - Increasing address size



Memory

- **Array of RAM Chips**
  - Increasing word size



Memory

12-29. A microprocessor employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The microcomputer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(a) How many RAM and ROM chips are needed?

(b) Draw a memory-address map for the system.

(c) Give the address range in hexadecimal for RAM, ROM, and interface.

Memory

- Given, RAM ROM and 4 interface unit
  - RAM chips of 256×8,
  - ROM chips of 1024×8,
  - 4 interface unit with 4 registers
- Solution
  - 2K bytes RAM requires 2K/ 256= 8 chips
    - Address for 2K words requires 11 bits
      - 8 bits for each chip and 3 bits to select 8 chips
      - Address range 0000 – 07FF (0000 0111 1111 1111)
  - 4K bytes ROM requires 4K/1024=4 chips
    - Address for 4K words requires 12 bits
      - 10 bits for each chip and 2 bits to select 4 chips
      - Address range 2000 (0010 0000 0000 0000) – 2FFF (0010 1111 1111 1111)
  - 4 interface unit with 4 registers requires 4×4=16 address
      - Address range 4000 (0100 0000 0000 0000) – 400F (0100 0000 0000 1111)

Memory

- Example:
  - Core i-5 processor with maximum memory size 32GB
  - 4-GB RAM
  - 32 bit OS has addressing capability 2^{32} = 4 GB
    - Processor cache memory 6MB
    - Graphics Card memory 1GB
    - Address for peripheral interface
      - I/O, USB, PCI, etc
  - The remaining address will be assigned to the RAM
    - Hence if you connect 4GB RAM to the system you will get a much less useable memory

Memory

- **Problems**

7-35 (a) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(b) How many lines of the address must be used to access 2048 bytes? How many of these lines are connected to the address inputs of all chips?

(c) How many lines must be decoded for the chip-select inputs? Specify the size of the decoder.

7 -36 A computer uses RAM chips of 1024 x 8 capacity.

(a) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?

(b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected.

Problems of Chapter 12 :

12-25, 12-26, 12-27, 12-28, 12-29, 12-30.

Lesson-35:

Topic	Lesson Learning Outcomes	Teaching-Learning Methodology	Assessment Method
I/O and interrupt design	• Design I/O interface • Design DMA and interupt	Class Lecture Question and answer	Test, exams, quiz, etc

I/O interface

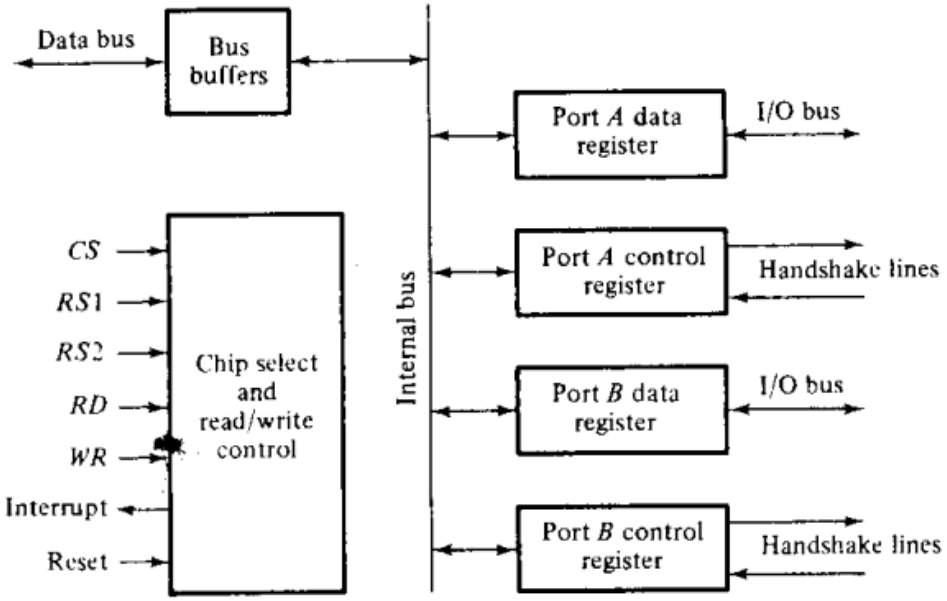
- Addressing I/O
  - Memory-mapped I/O
  - Isolated I/O

I/O interface

- 4 Types of Input-Output Interface
  - Parallel Peripheral Interface
  - Serial Peripheral Interface
  - Special Dedicated Interface
  - Direct Memory Access (DMA) Interface

I/O interface

- Parallel peripheral Interface

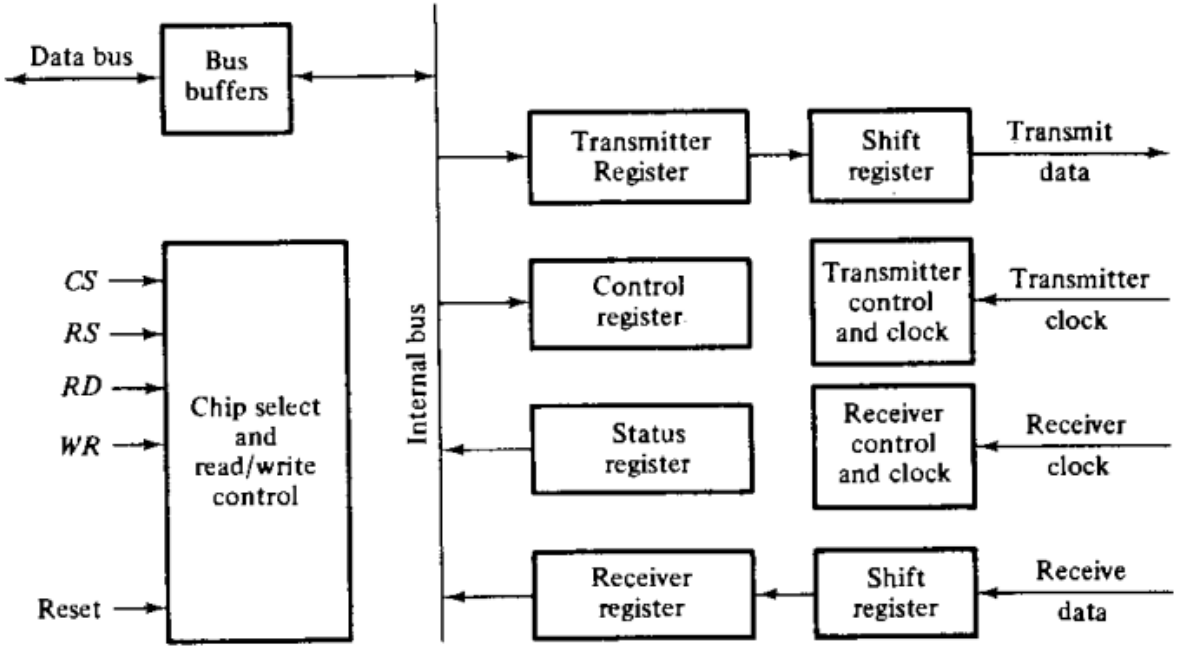


CS	RS1	RS2	Register selected
0	X	X	None - data bus in high-impedance
1	0	0	Port A data register
1	0	1	Port A control register
1	1	0	Port B data register
1	1	1	Port B control register

Figure 12-14 Block diagram of parallel peripheral interface

I/O interface

- Serial communication Interface

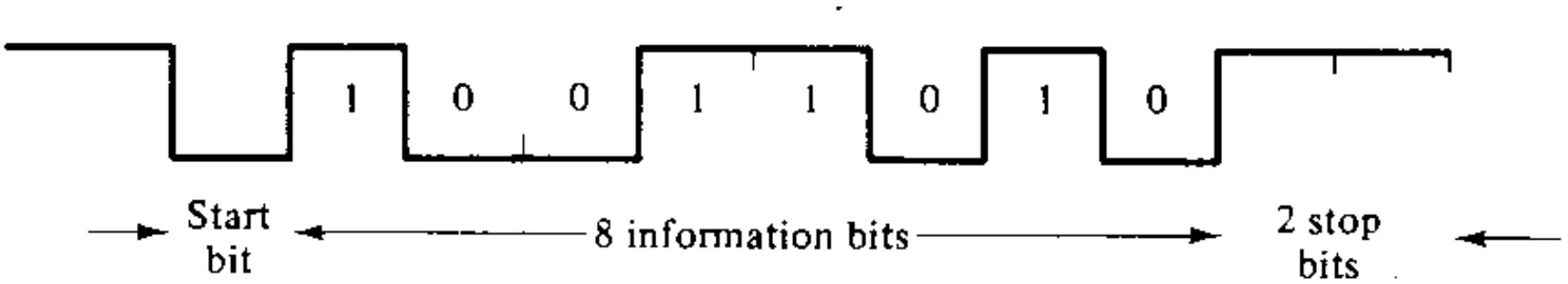


CS	*RS*	Operation	Register selected
0	*X*	*X*	None
1	0	*WR*	Transmitter register
1	1	*WR*	Control register
1	0	*RD*	Receiver register
1	1	*RD*	Status register

Figure 12-15 Block diagram of a typical serial communication interface

I/O interface

- Serial communication Interface
  - Asynchronous serial transmission of a character



I/O interface

- Dedicated interface components

Floppy disk controller

Keyboard and display interface

Priority interrupt controller

Interval timer

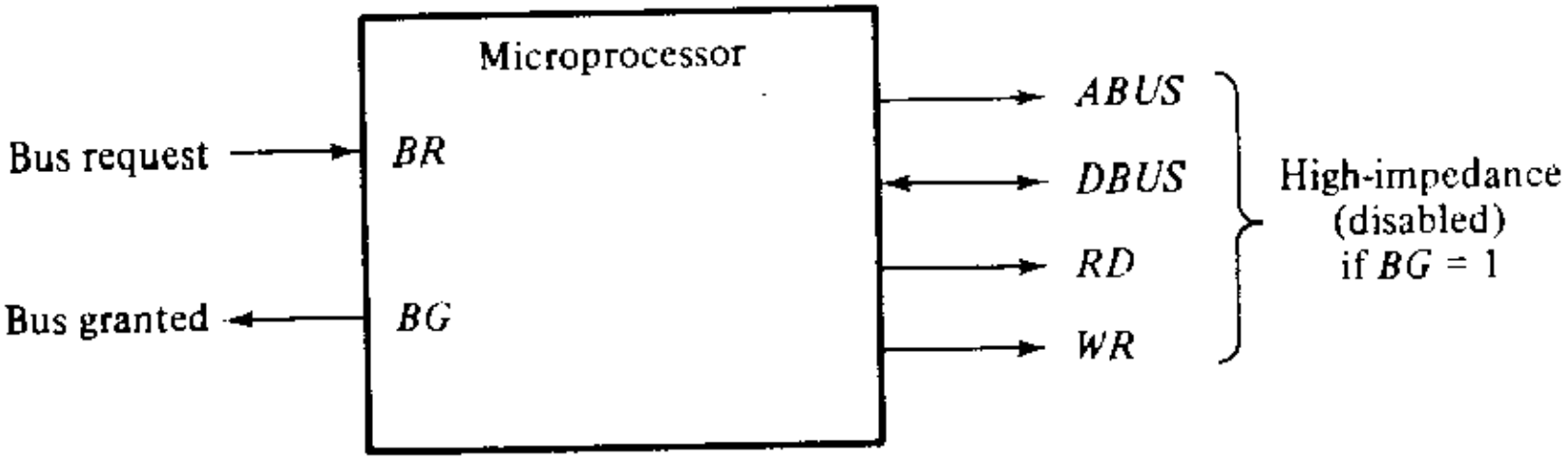
Universal peripheral interface

DMA

- Commonly used for data transfer in storage devices
  - Storage devices ex, magnetic-disk, magnetic-tape, CD, etc limited by speed
  - Processor spent most of its time for transferring data to these devices
  - The solution is to bypass the processor in such transfer
    - Peripheral device that can do this is the Direct Memory Access (DMA)
  - Processor is idle during DMA transfer
  - A DMA controller takes over the busses to manage the transfer directly between peripheral devices and memory.

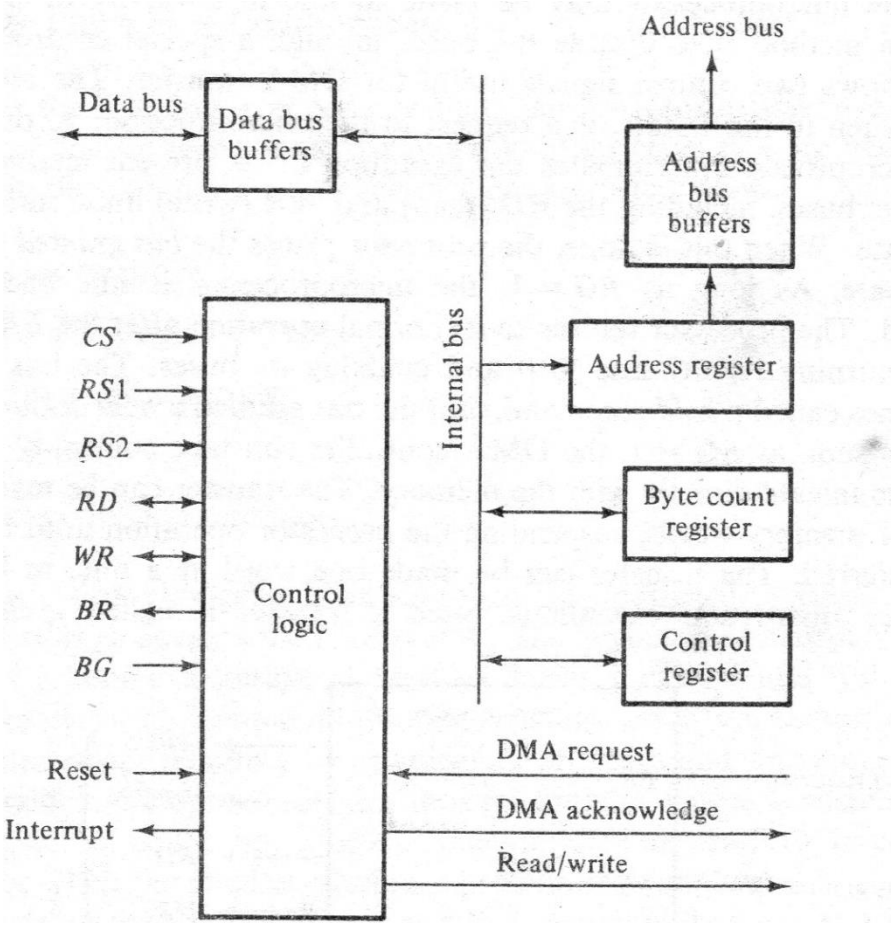
DMA

- Control Signals for DMA Controller



DMA

- Block Diagram of DMA Controller



DMA

- The microprocessor initializes the DMA by sending the following information through the data bus:
  1. The starting address of the memory block where data are available (for read) or where data are to be stored (for write).
  2. The byte count, which is the number of bytes in the memory block .
  3. Control bits to specify a read or write transfer
  4. A control bit to start the DMA.

DMA

- DMA transfer in microcomputer system

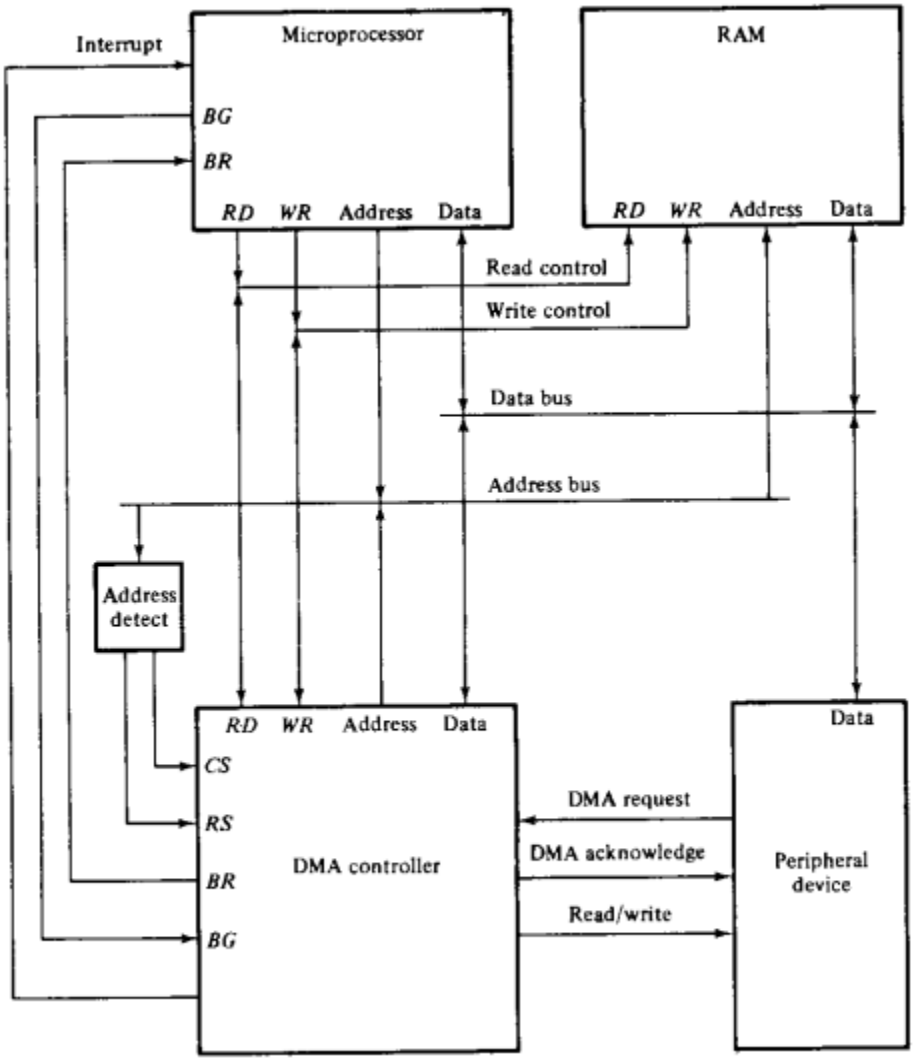
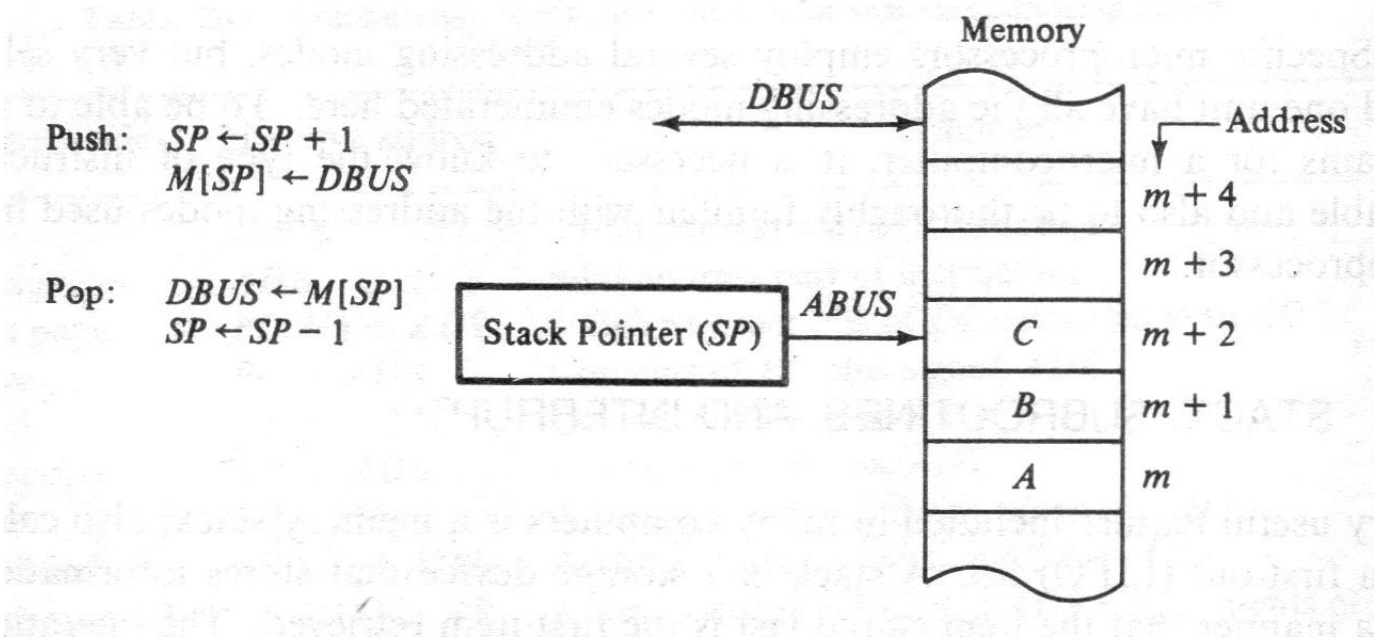


Figure 12-19 DMA transfer in a microcomputer system

Stack Subroutine and Interrupt

- Memory Stack Operation



Stack Subroutine and Interrupt

- Example of Call Subroutine