



**NTNU – Trondheim**  
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# Energy Efficiency Experiments on Mali Powered Exynos 5 using OmpSs

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PILOT PROJECT FOR MASTER THESIS

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## **Problem statement**

Here is the problem statement.

## **Acknowledgements**

Here are the acknowledgements.

## **Abstract**

This is the abstract.

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# Chapter 1

## Introduction

### 1.1 Motivation

Increase of performance and power efficiency are the main goal of processor designers. Unfortunately we are currently reaching the limits of the current strategies for further development. For some time, our processors have been struggling to achieve increased performance. Heat stops us from driving the clock frequency higher, while memory is lagging more and more behind. A solution to enable continued performance growth is multicore processors, and for the last decade this has been the focus. Unfortunately adding cores will not be a sustainable solution forever. As the amount of cores grow, they are still competing for the same system resources and may have to wait for each other to complete calculations on data with dependencies.

A promising solution to this issue is heterogeneous multi-processor systems. Heterogeneous multi-processor systems utilize multiple different processor cores in the same system. This allows different parts of a program to be executed on a suitable processor. By using a suitable core for each part of the program it is possible to achieve better performance than homogeneous multi-processor systems.

### 1.2 Project Scope and Goal

This pilot project's main goal is to do preliminary research and experiments on the energy efficiency of the Exynos 5 processor, with the intent to use the results next spring in my master

thesis. The goal of this research is to explore the potential of the task based programming model heterogenous multi-processor systems.

### 1.3 Problem Statement Interpretation and Approach

- Task 1: Implement or adapt suitable experiment applications for testing energy efficiency.
- Task 2: Implement some energy efficiency measurement application for both Arendale duo and Odroid-xu3.
- Task 3: Optimize experiment applications for both platforms.
- Task 4: Gather performance and energy efficiency results from the experiment applications on both platforms.
- Task 5: Analyze and evaluate experiment results.

TODO: Introduce how these tasks were solved.

### 1.4 Outline

TODO: This section need to be completed after the outline of the report is done.



## **Chapter 2**

### **Related work**

The heterogen property of this

# Chapter 3

## Background

### 3.1 Energy measurement

### 3.2 NEON

NEON is a general-purpose single input multiple data (SIMD) technology implemented in the ARM Cortex A series of processors. It is able to run SIMD instructions on 128bit registers. By utilizing the NEON unit of the ARM processors, it is possible to achieve parallelism in each separate core. This will often open for great performance boost on problems like the ones explored in this paper. Each register may be filled with single precision floating point numbers ranging from 8 to 64 bit each. In future generations of the ARM ISA there will be support for other data types as well. Different implementations of NEON exist in the Cortex A cores, and while the even the simple implementations in smaller cores like the A7 can give great performance boost, the implementations present in the newest cores are performing even better. The A15 offer two NEON units, and the instruction pipeline to start the cores are shorter than in simpler implementations.

### 3.3 Task based programming

Task based programming allow a programmer to work with parallel programs, with an abstraction from the parallelization itself. When programming with this model, the program can be

split into tasks which can run in parallel. When the program runs, it will run a task manager as part of the program. This task manager can dynamically assign tasks to the processors, and the programmer does not have to handle all the time-consuming tasks related to manual parallelization. As long as the programmer correctly handles dependencies in the parallelized code, it will be possible to write this kind of code as if it was serial.

The task-based programming model also allows simpler development of portable programs. When the program is running tasks on available CPUs, it is not a problem to allow it to run on larger or smaller numbers of processors, and even clusters can support the program. This model even allows the tasks to run on different types of processors in a heterogeneous environment.

### **3.4 OpenMP Super scalar**

OpenMP Super scalar (OmpSs) is an extension of the OpenMP API to integrate features from the StarSs programming model. It is currently under development at the Barcelona Supercomputing Center. The goal of OmpSs is to extend the programming model to support a wide range of processors. The OmpSs programming model will run on a wide variety of different systems, such as traditional personal computers, clusters, shared memory systems and heterogeneous processors. While the software is not yet completed or fully tested, there have been several reports exploring its potential. The results have proven OmpSs as an efficient solution on both clusters and heterogeneous systems utilizing OpenCL and CUDA.

### **3.5 Heterogeneous multi-processor**

Heterogeneous multi-processor systems have multiple different processors, opposed to traditional multi-processor systems. A typical modern processor has several processors, and a program can run effectively by having threads running parts of their work on each of them. This work is often of such a nature that it can run better on a different processor. Sometimes it can run just as well on multiple simple processors, while using less die space and energy. In other instances, an advanced processor with some special capabilities, like vector instructions, can be more efficient.

This kind of processors have a potential to help us overcome the challenges that are emerging in processor development. Unfortunately they also introduce several new challenges.

## 3.6 Experiment platforms

### 3.6.1 Arendale Board

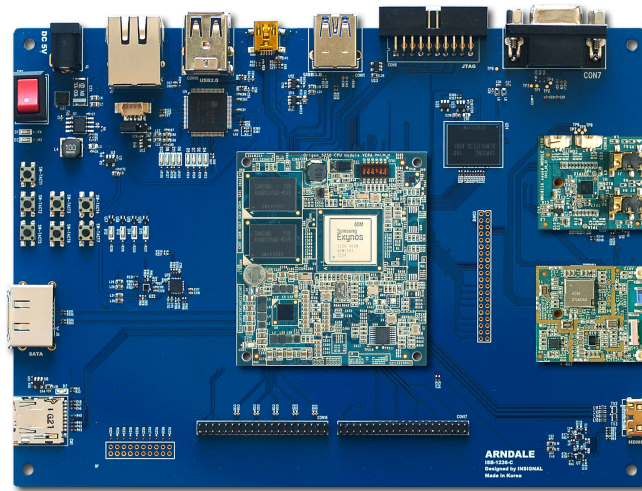


Figure 3.1: Arendale Duo

The Arendale Duo is a computing system mounted on a single board. It is fitted with an Exynos 5250 SoC, which contain a dualcore Arm Cortex-A15 , as well as an ARM Mali T-604 GPU. This computer offer a range of supported linux distributions, as well as the OmpSs programming model. The computer was used in the 2014 master thesis "Acceleration with OmpSs and Neon/OpenCL on ARM Processor" by Trond Inge Lillesand. The thesis lay alot of the ground for this pilot project and planned master thesis.

### 3.6.2 ODROID-XU3

The ODROID-XU3 is a new single-board computing system, offering interesting properties for these experiments. The system has an Exynos 5422 heterogenous Soc. Exynos 5422 has a quad-core ARM Cortex-A15 CPU and a ARM Mali T-628 GPU, but also a smaller quadcore ARM Cortex-

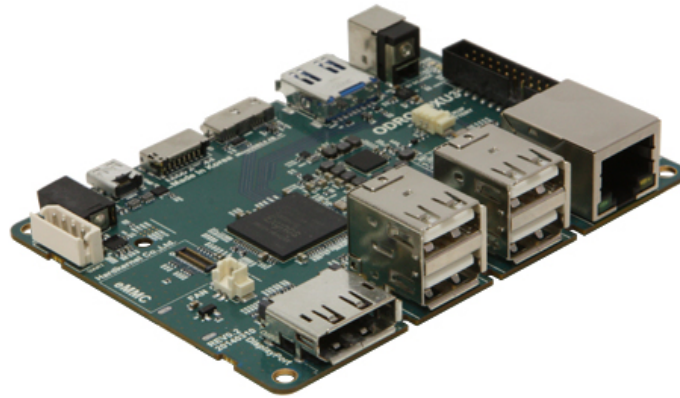


Figure 3.2: ODROID-XU3

A7 coprocessor. These 3 different processing units can be used simultaneously to solve problems. In this paper, and the planned master thesis following it, the potency of this kind of heterogeneous processor will be explored.

TODO: Write this in a better fashion. A key feature making this card suitable for this research-project, is the presence of 4 separate current sensors. The sensors can do realtime measurement of the big CPU, little CPU, GPU and DRAM, respectively.

### 3.6.3 ARM Cortex-A15

Performance	1.0 GHz to 2.5GHz
L1 Cache	64KB
L2 Cache	4 MB
L3 Cache	None in core, may be implemented shared in multicore system.
Architecture	ARMv7-A
Supported features	ARM Thumb-2 TrustZone® security technology NEON™ Advanced SIMD DSP & SIMD extensions VFPv4 Floating point Hardware virtualization support Integer Divide Fused MAC Hypervisor debug instructions
Memory management	40-bit ARMv7 Memory Management Unit

### 3.6.4 ARM Cortex-A7

The ARM Cortex-A7 is designed to be a low power alternative to the ARM Cortex-A15 and ARM Cortex-A17, with the same supported ISA and features. This enable the ARM Cortex to be paired with it's largers relatives in a ARM big.LITTLE configuration.

Performance	1.2 GHz to 1.6GHz
L1 Cache	8-64KB
L2 Cache	up to 1 MB
L3 Cache	None in core, may be implemented shared in multicore system.
Architecture	ARMv7-A
Supported features	ARM Thumb-2 TrustZone® security technology NEON™ Advanced SIMD DSP & SIMD extensions VFPv4 Floating point Hardware virtualization support Integer Divide Fused MAC Hypervisor debug instructions
Memory management	40-bit ARMv7 Memory Management Unit

### 3.6.5 ARM Mali T604

Performance	533 MHz 17 GFLOPS
Multicore support	1-4 cores
API Support	OpenGL 1.1, 2.0, 3.0 and 3.1 OpenCL 1.1 DirectX 11 RenderScript
Anti-Aliasing	4xFSAA with minimal performance drop 16xFSAA
Cache	32-256KB L2 cache



### 3.6.6 ARM Mali T628

Performance	533/695 MHz 17/23.7 GFLOPS
Multicore support	1-8 cores
API Support	OpenGL 1.1, 2.0, 3.0 and 3.1 OpenCL 1.1 DirectX 11 RenderScript
Anti-Aliasing	4xFSAA with minimal performance drop 16xFSAA
Cache	32-256KB L2 cache

## 3.7 Algorithms

Here I will write about the algorithms used in the experiments.

# Chapter 4

## Setup and Methodology

### 4.1 Test platfoms

#### 4.1.1 Arendale Duo

The Arendale Duo board was used for some perliminary research in this thesis. It was chosen because we had experience from earlier student projects using this board. It's feature set and properties are elaborated in section [3.6.1 Arendale Board](#).

<b>SoC</b>	Samsung Exynos 5250
<b>CPU</b>	
Model	ARM Cortex-A15
Manufacturing process	32nm
Maxiumu clock frequency	1.7GHz
Number of cores	2
L2 Cache	1MB
L1 Cache	32KB
<b>GPU</b>	
Model	ARM Mali-T604
Number of cores	4
<b>Memory</b>	
Available memory	2 GB
Maxiumu clock frequency	800MHz
<b>Operating system</b>	
Distriubtion	Linux Ubuntu
Version	TODO

Table 4.1: Arendale Duo Spesifications

### 4.1.2 ODROID-XU3

The ODROID-XU3 single board computing system was used for most of the experiments of this thesis. Fitted with an Samsung Exynos 5422 SoC it offer the heterogenous properties that will be explored in detail in the planned master thesis. In addition, the board offer multiple energy monitors, enabling precise data gathering. It's feature set and properties are elaborated in section [3.6.2 ODROID-XU3](#).

<b>SoC</b>	Samsung Exynox 5422
<b>CPU 1</b>	
Model	ARM Cortex-A15
Manufacturing process	32nm
Maxiumu clock frequency	2.0GHz
Number of cores	4
L2 Cache	1MB
L1 Cache	32KB
<b>CPU 2</b>	
Model	ARM Cortex-A7
Manufacturing process	32nm
Maxiumu clock frequency	TODO
Number of cores	4
L2 Cache	TODO
L1 Cache	TODO
<b>GPU</b>	
Model	ARM Mali-T628 MP6
Number of cores	4
<b>Memory</b>	
Available memory	2 GB
Maxiumu clock frequency	933MHz
<b>Operating system</b>	
Distriubtion	Linux odroid
Version	3.10.54+

Table 4.2: ODROID-XU3 Spesifications

## 4.2 Software

## 4.3 Compilation and running of test benches

Mention frequency scaling here.

<b>Software</b>	<b>Version</b>
Nanos++	0.9a
Mercurium	1.99.4
Papi	5.3.2
Extrac	3.0.1
gcc	4.8.2

Table 4.3: Third party software and frameworks used in the experiments.

## 4.4 Performance measurement

In the experiments being run in this pilot project, execution time was used as the primary metric for performance. While running the experiments, the POSIX function `gettimeofday()` is used before and after running the main part of the application. The time difference is used as a measurement of how good the performance is.

In the planned master thesis, PAPI (Performance API) may be used to measure more detailed aspects of the performance. PAPI is able to access a lot of different performance measurements from systems. The available metrics include among others; Cache utilization and hit rate, memory utilization and bus utilization.

## 4.5 Energy efficiency measurement

# **Chapter 5**

## **Implementation**

## **Chapter 6**

### **Result and Discussion**

## **Chapter 7**

## **Conclusion**

# Chapter 8

## Future Work

These are some suggestions for future work that may build upon the work in this thesis.

### 8.1 Experiment with heterogeneity

In this thesis, there have been done experiments with the Exynos 5, which support ARM big.LITTLE. The heterogeneity properties of this processor was outside of the scope of this pilot project. The same applications can be adapted and optimized to explore the potential of this processor architecture. This is planned for the master thesis following this pilot project.

### 8.2 OmpSs with OpenCL kernels

A new feature of OmpSs is its ability to manage OpenCL kernels as tasks. It is possible to issue OpenCL kernels as OmpSs tasks, and have the task manager assign them to GPUs and CPUs. This allows for portable code that can run effectively on a range of different systems. It would be interesting to examine the potency of this way of utilizing the GPU, as it saves the programmer from the job of manually tuning the load balance between GPU and CPU.



### **8.3 ARMv8-A 64-bit processors**

ARM have created the next generation ARM processors. They run a new instruction set, with support for both 32- and 64-bit instructions. Running similar experiments on such a processor would be interesting.

### **8.4 Performance measurement**

In this project, only simple forms of performance measurement was used. Running the same or similar experiments with access to other performance counters would be interesting. Cache hit rate and utilization, memory utilization, bus utilization and other counters could help understanding the strengths and weaknesses of the system.

# **Appendix A**

## **Implementation**

### **A.1 Introduction**

#### **A.1.1 Program 1**

# Bibliography

Rausand, M. and Høyland, A. (2004). *System Reliability Theory: Models, Statistical Methods, and Applications*. Wiley, Hoboken, NJ, 2nd edition.

# **Curriculum Vitae**

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