Synthesis Schematics

Introduction

This document presents the schematics from synthesizing the Liasion System in the Term Assignment[1] from the course TFE4140 Modelling and Analysis of Digital Systems. As part of the project, the system that is implemented using VHDL is synthesized in Synplicity Synplify Pro C-2009.06.

The schematics from the RTL view are presented first, then the schematics from the Technology view. The modules are both presented in the following order: Liasion, Onebit-voter, controller, registers and ECC.

RTL view Schematics

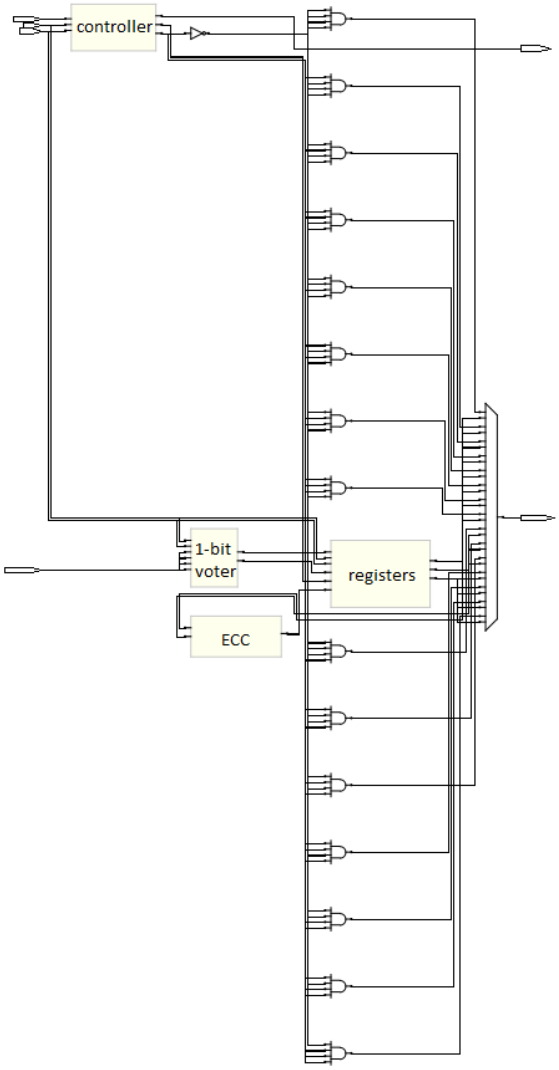

Figure 1 – Liaison (RTL)

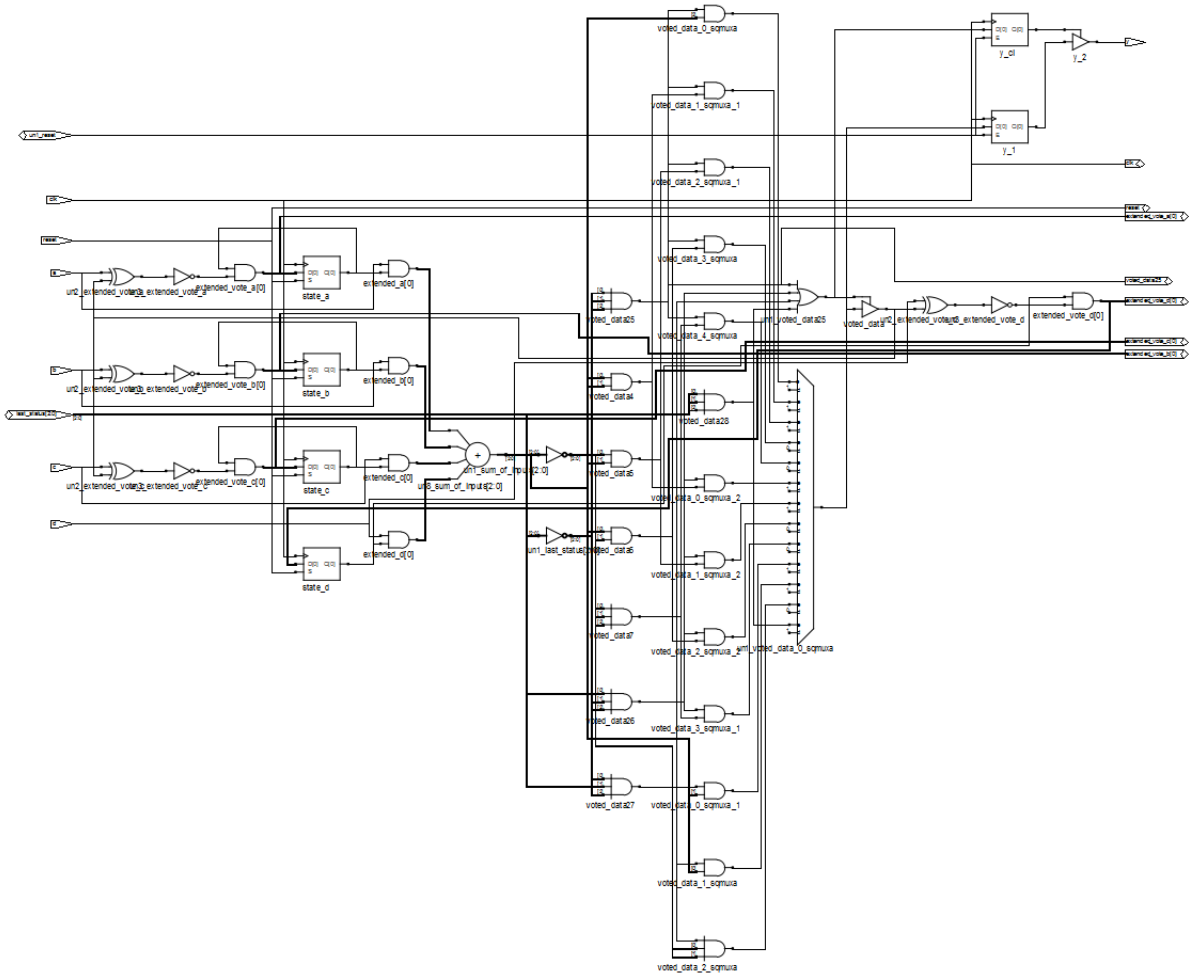

Figure 2 - 1-Bit Voter (RTL)

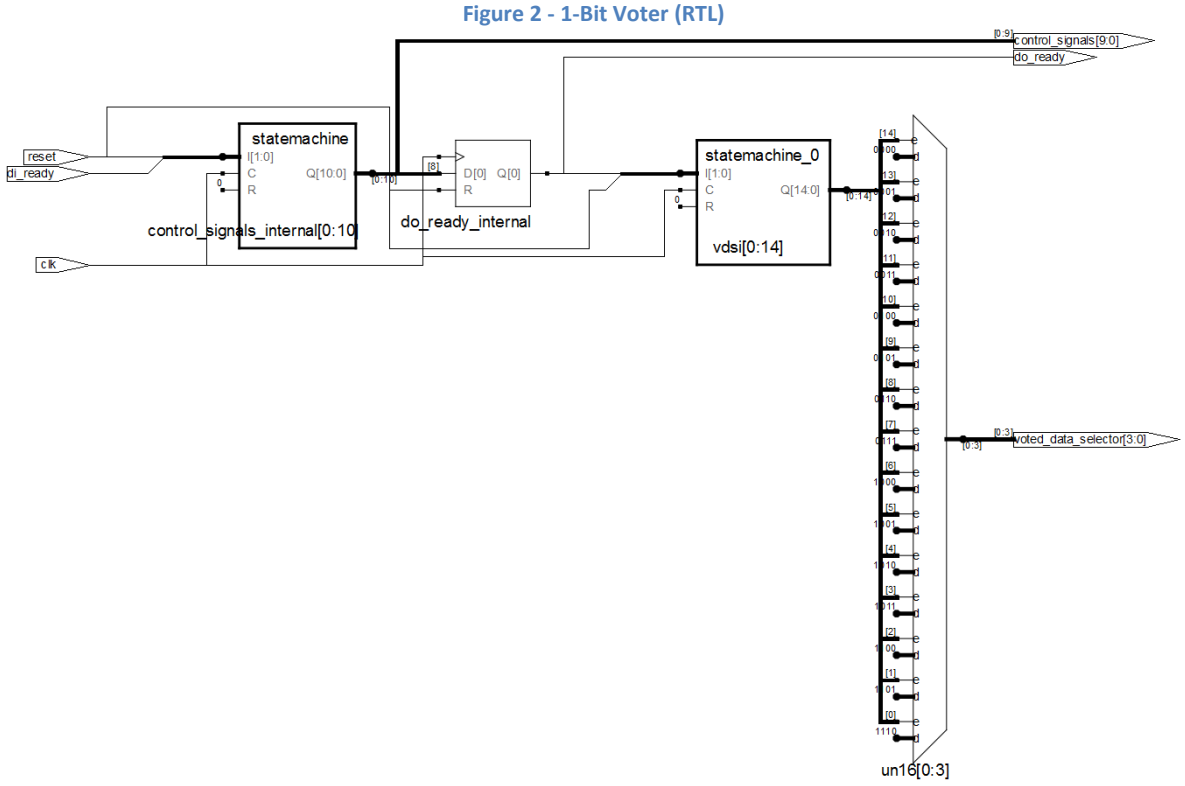

Figure 3 – Controller (RTL)

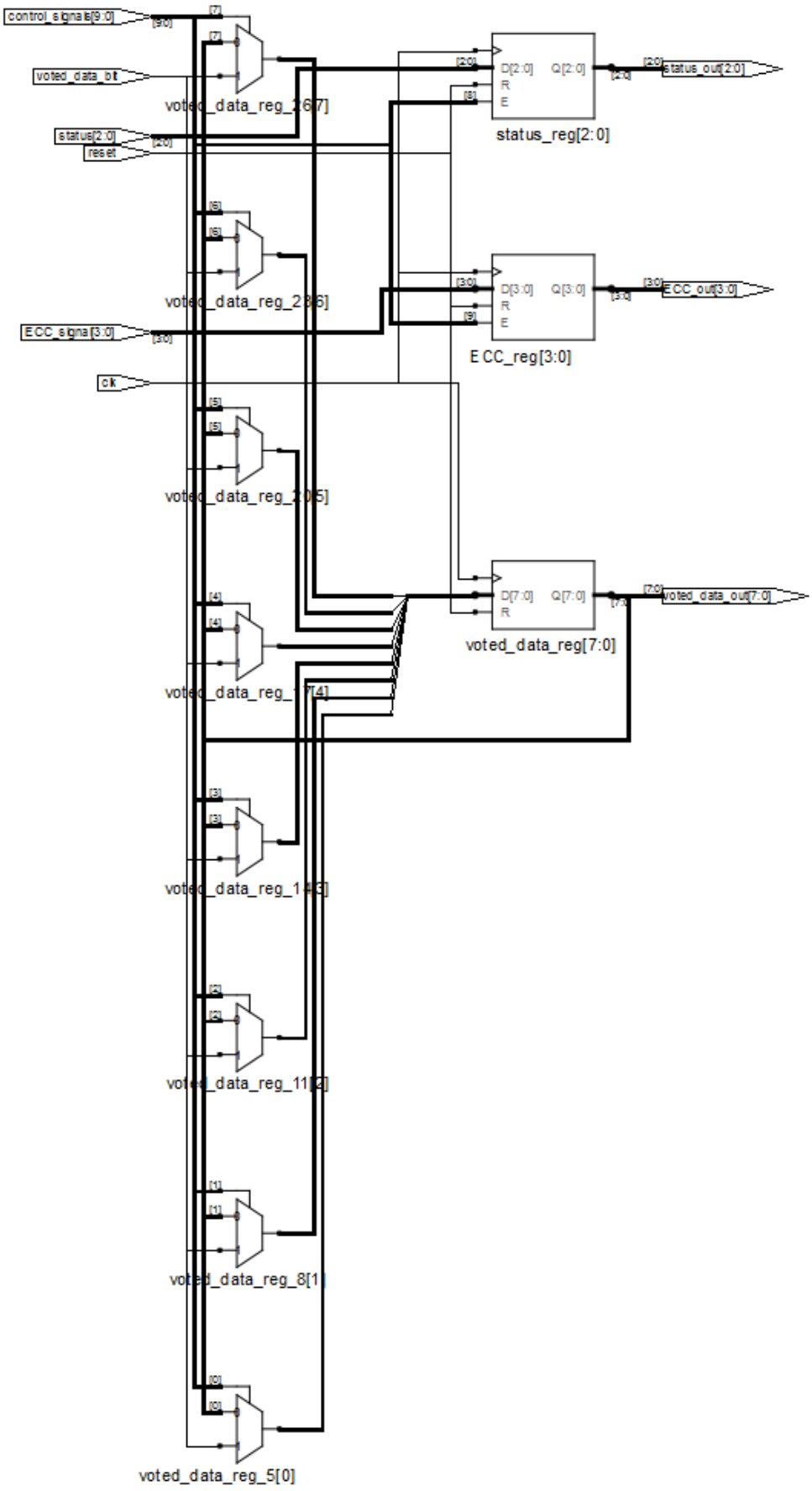

Figure 4 – Registers (RTL)

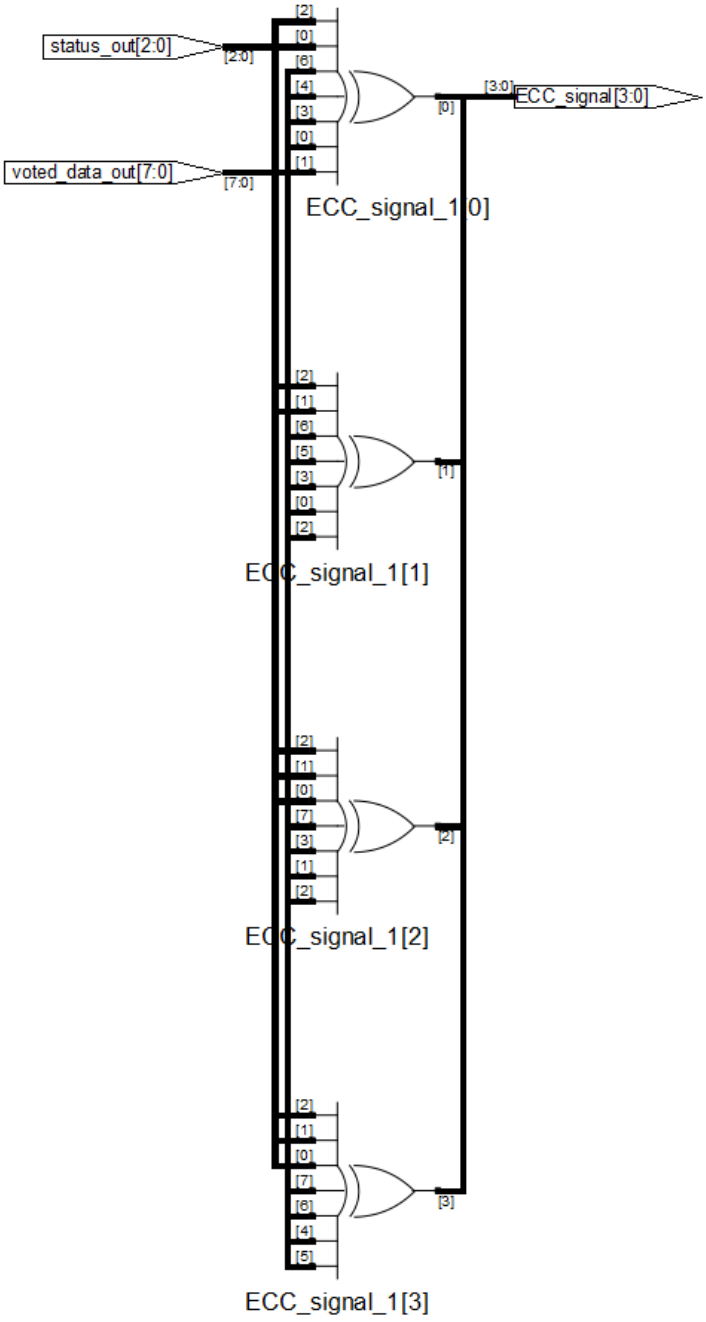

Figure 5 – ECC (RTL)

Technology-view Schematics

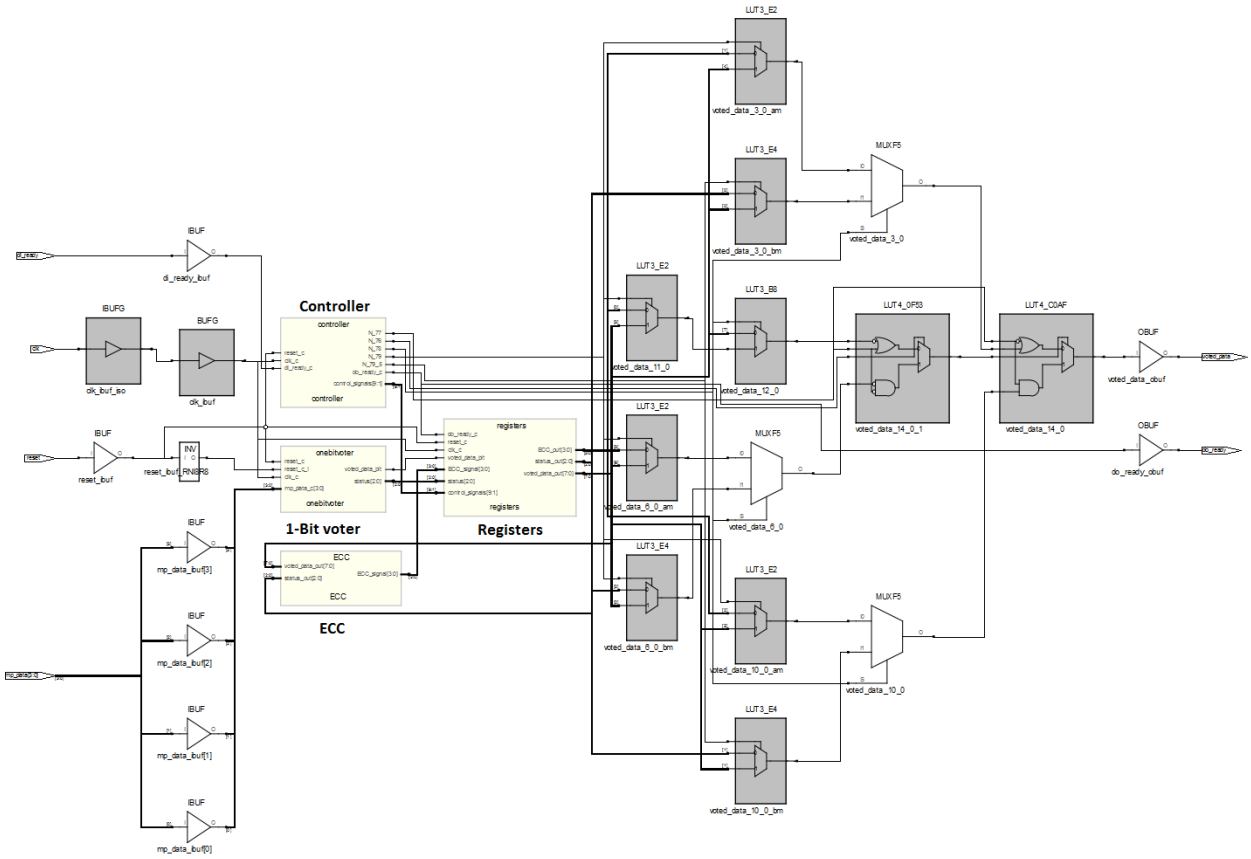

Figure 6 – Liaison (Technology)

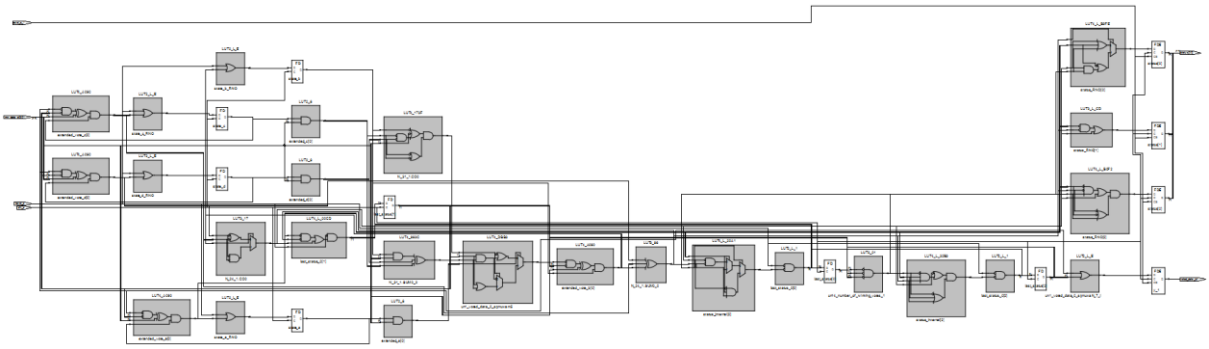

Figure 7 – 1-Bit Voter (Technology)

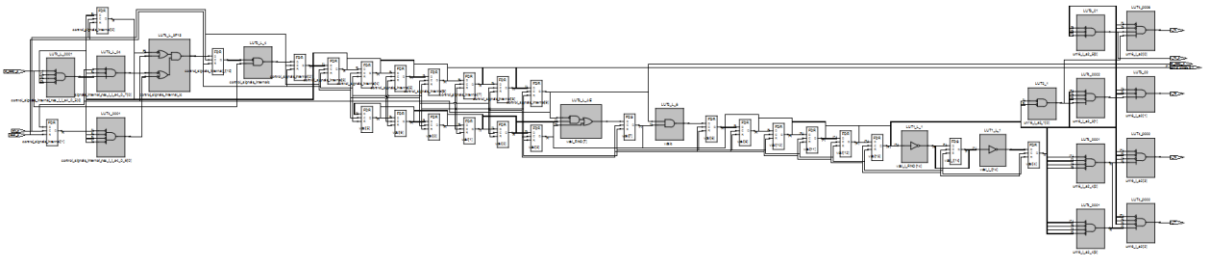

Figure 8 – Controller (Technology)

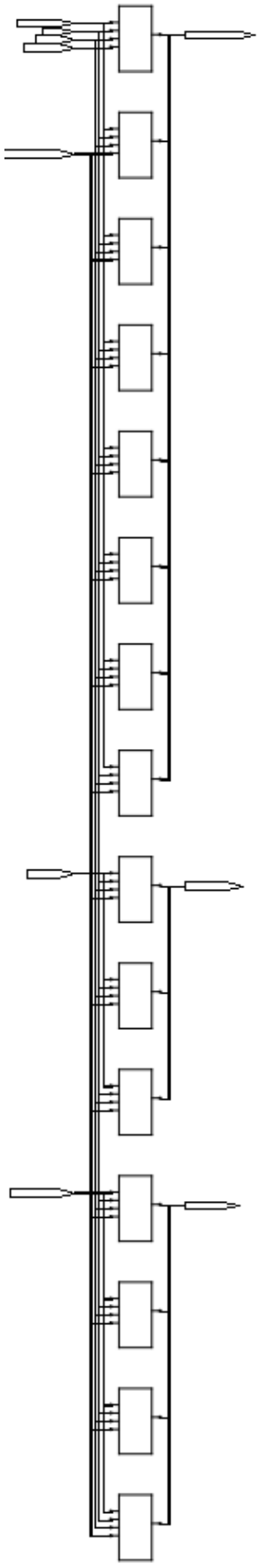

Figure 9 - Registers (Technology)

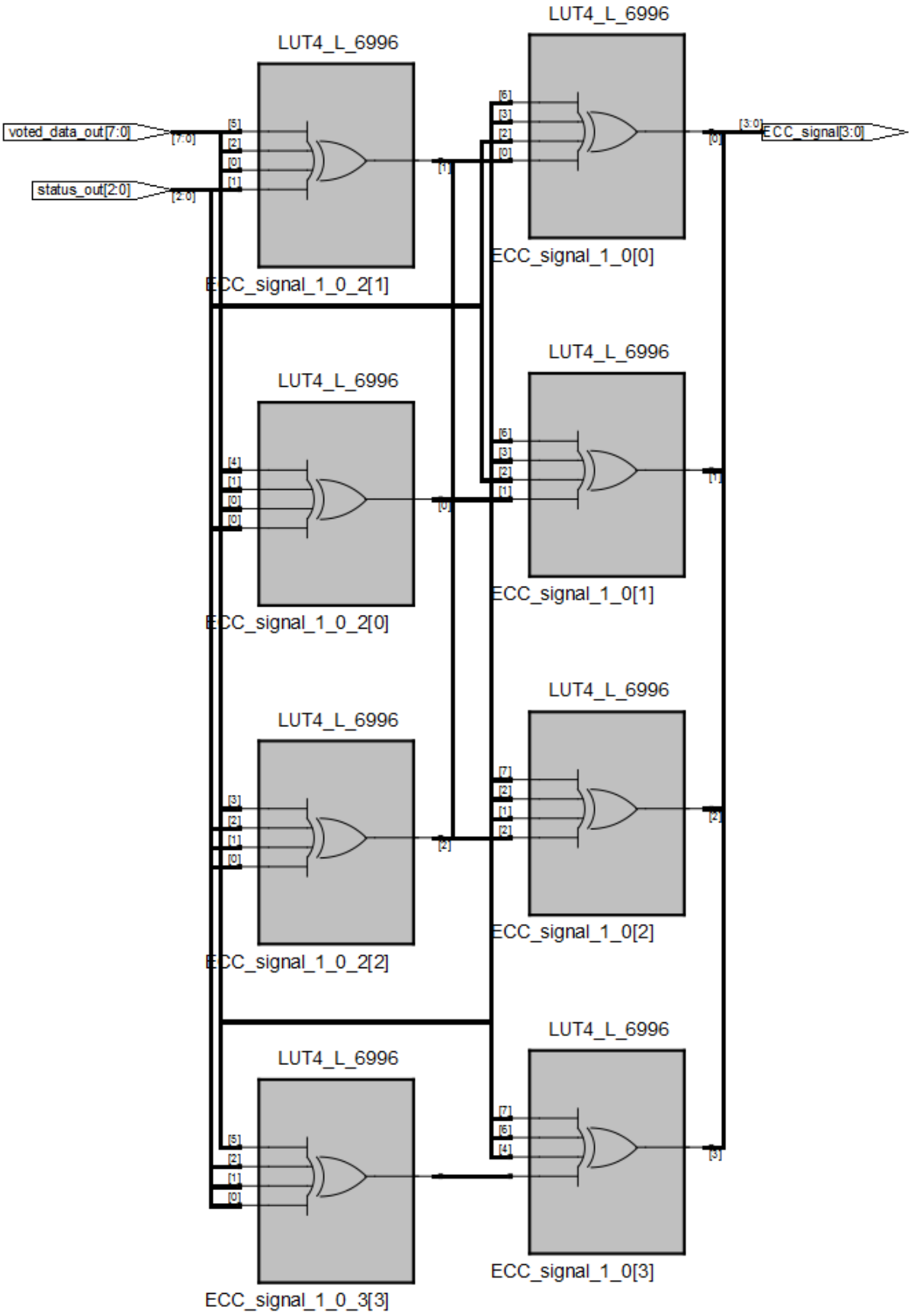

Figure 10 - ECC (Technology)

Figure list

Sources:

[1] TFE4140 Modelling and Analysis of Digital Systems Term Assignment 2014