Fatima Jinnah Women University

Sawaira saeed

2022-BSE-067

Rabia Batool

2022-BSE-064

Hafsah tahir

2022-BSE-052

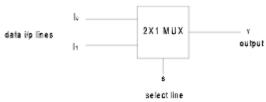
Group#B

Computer architecture and logic design

LAB#03

Submitted to Sir Shoaib

Block diagram of 2x1 MUX

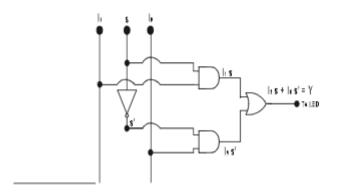


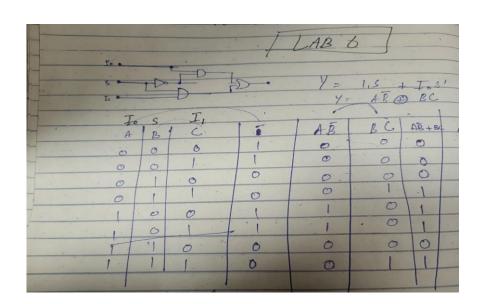
The function table of 2x1 Mux is

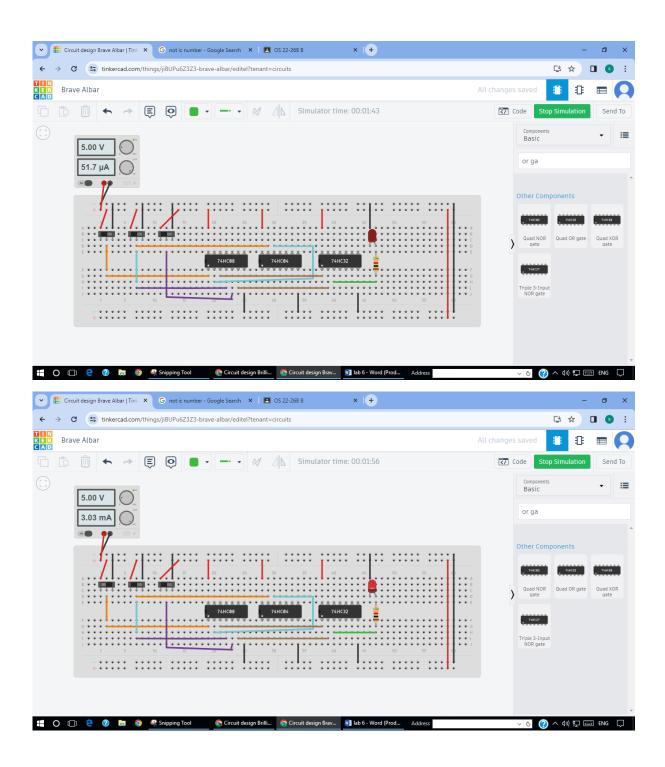
Select line	o/p
S	Y
0	I_{σ}
1	$I_{\scriptscriptstyle \parallel}$

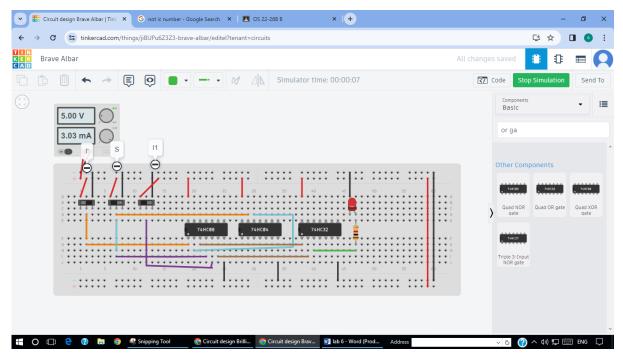
The Boolean function for 2x1 Mux is: $Y = I_t s + I_0 s'$

Logic Diagram of 2x1 Mux is

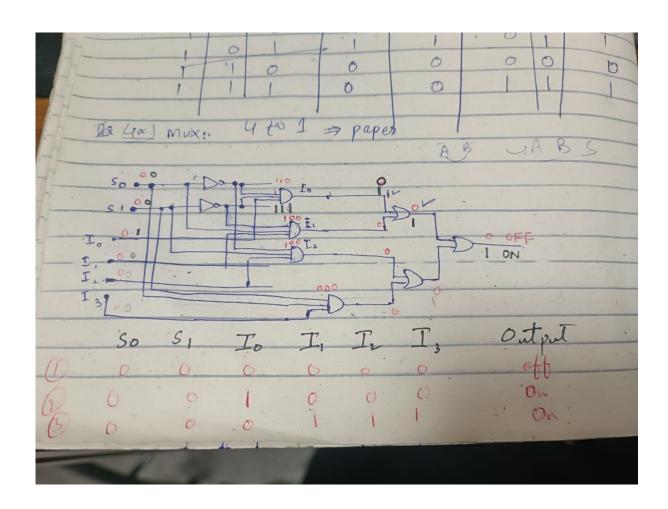




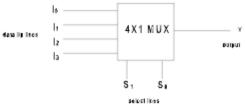




Multiplexer 4 to 2:



Block diagram of 4x1 MUX

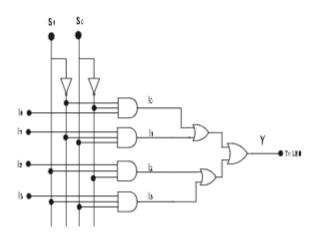


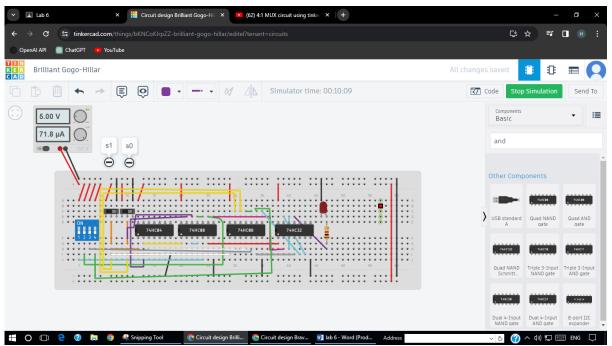
I₀, I₁, I₂ and I₃ are inputs of Mux S₁ and S₂ are select lines Y is output

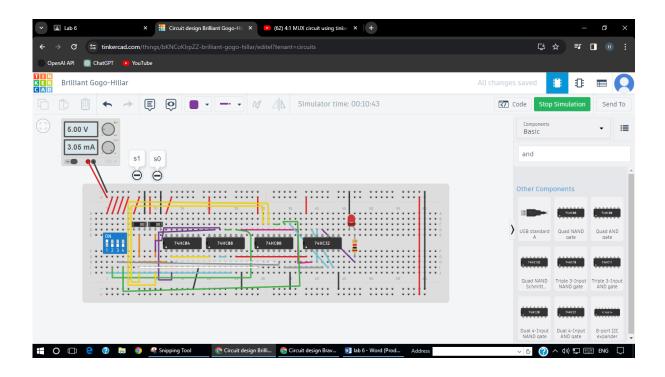
The Boolean function for 4x1 Mux is

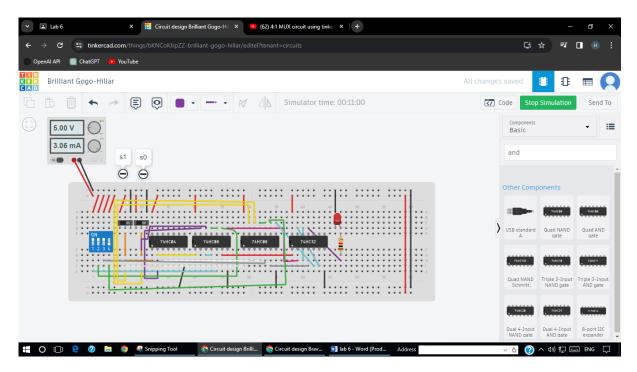
 $Y = I_4 S_1' S_0' + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$

Logic Diagram of 4x1 Mux is

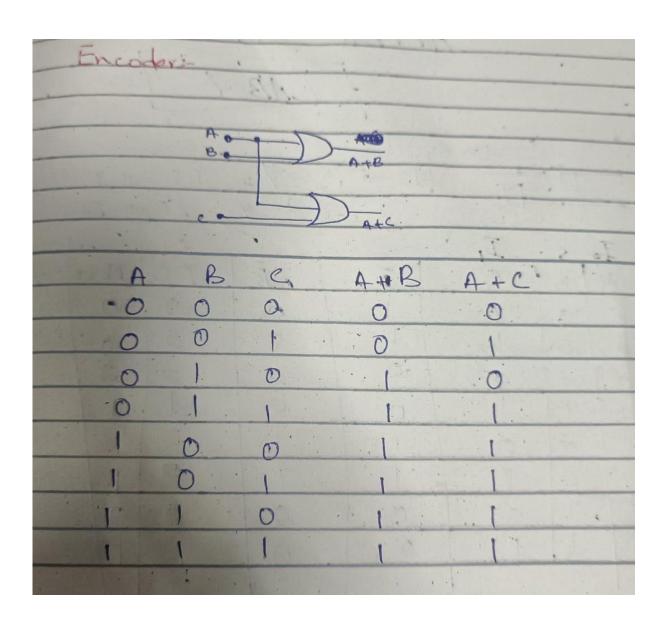


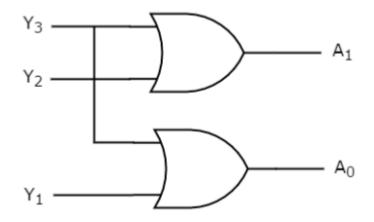


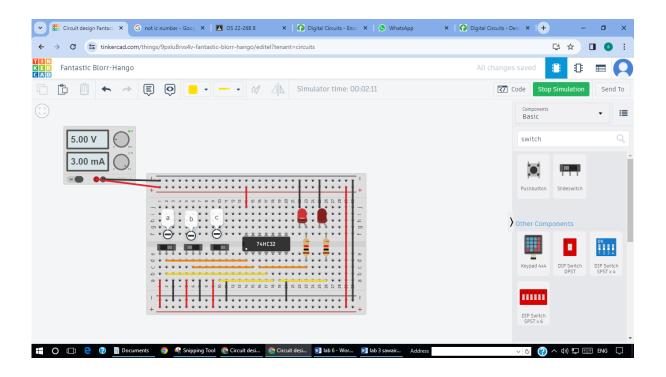


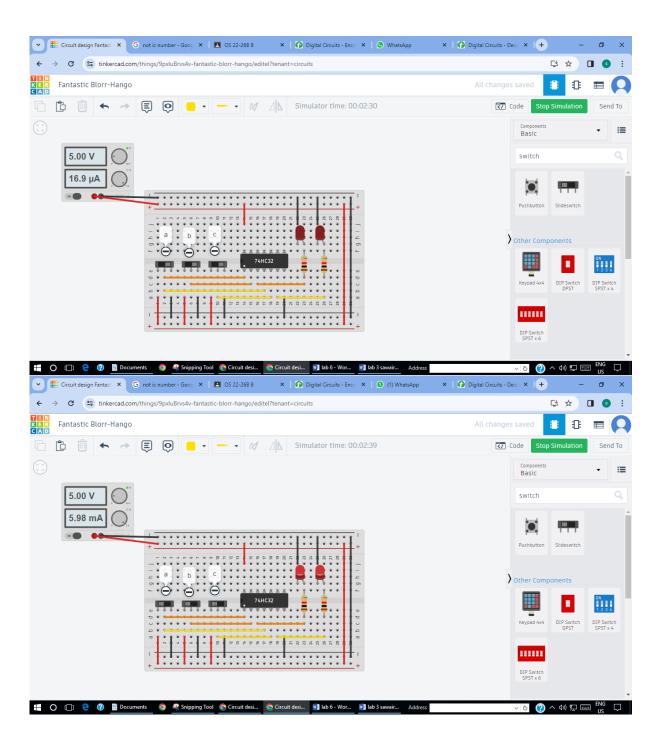


Encoder:









Decoder:

