



Sawaira saeed

2022-BSE-067

Rabia Batool

2022-BSE-064

Hafsah tahir

2022-BSE-052

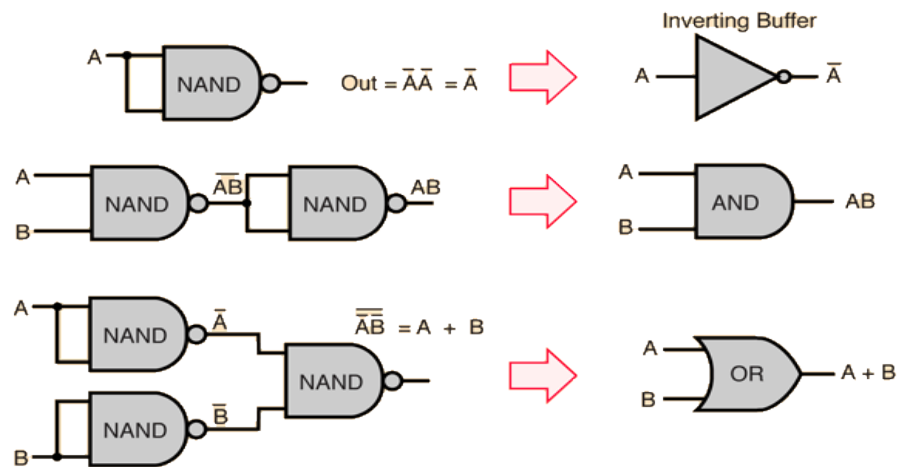
Group#B

Computer architecture and logic design

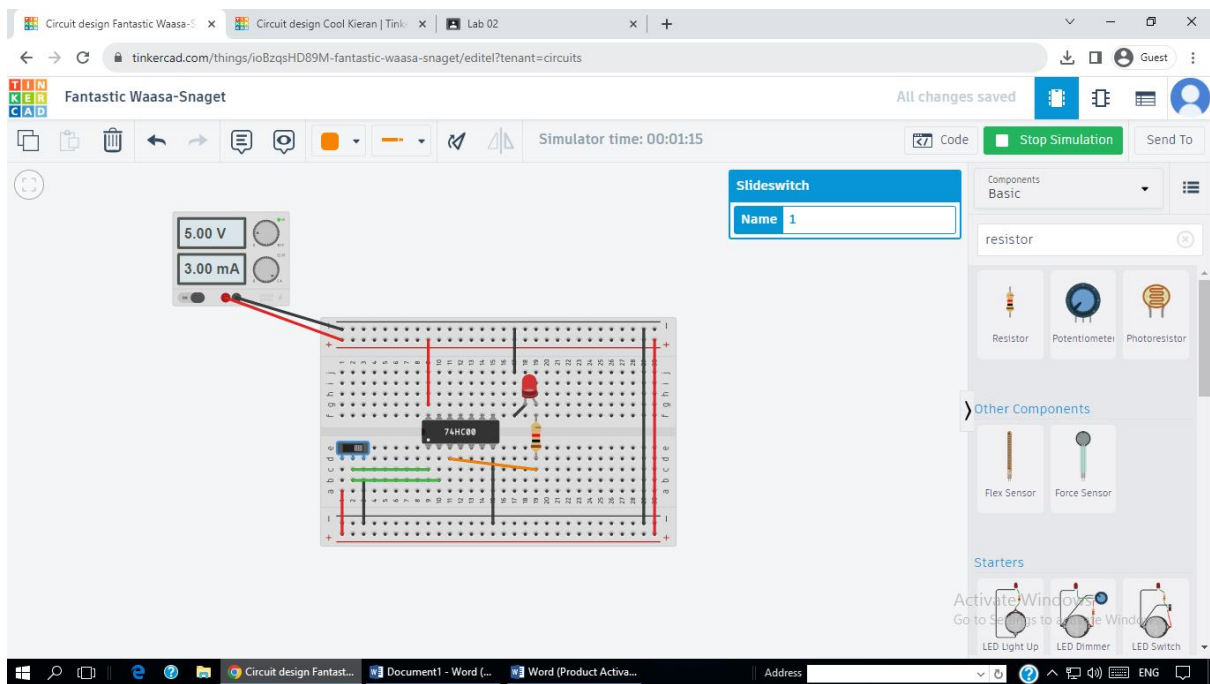
LAB#02

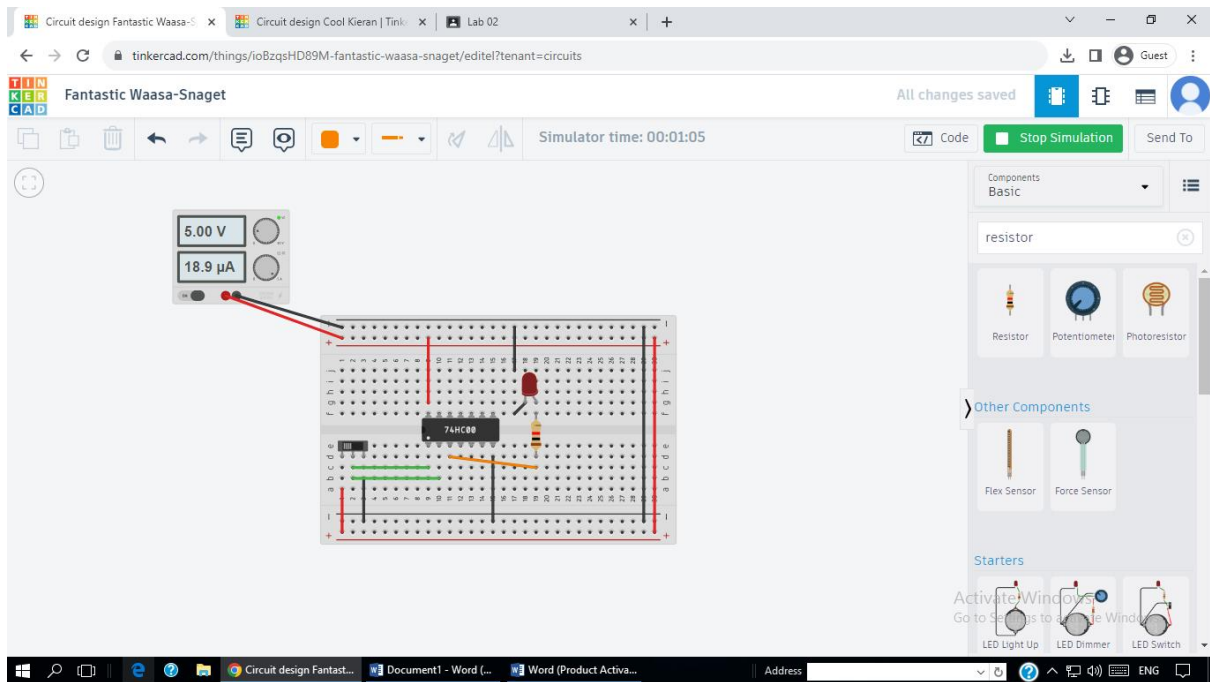
Submitted to Sir Shoaib

3.1. Working with NAND Gate:

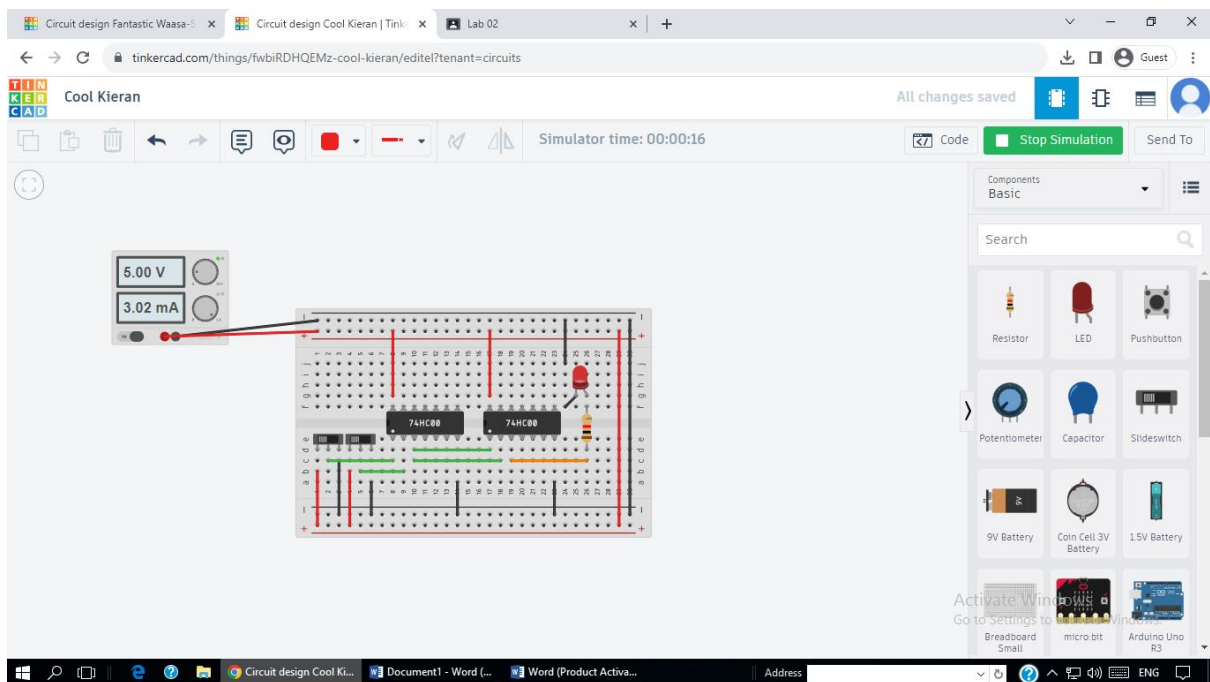


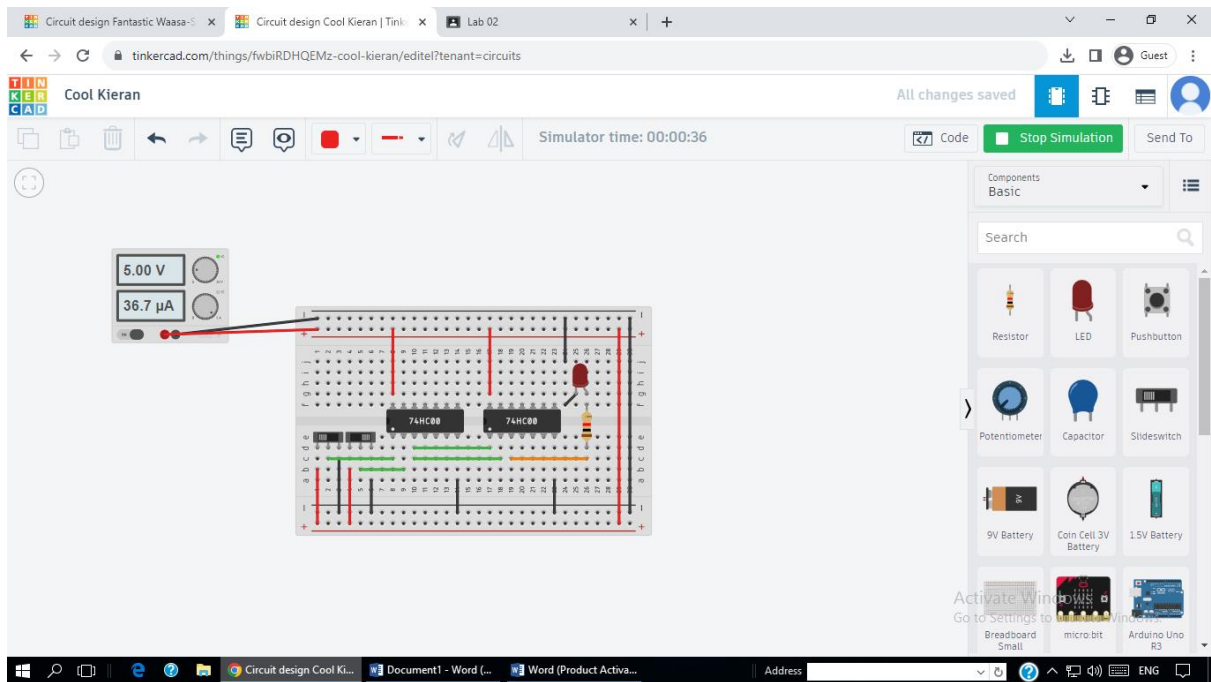
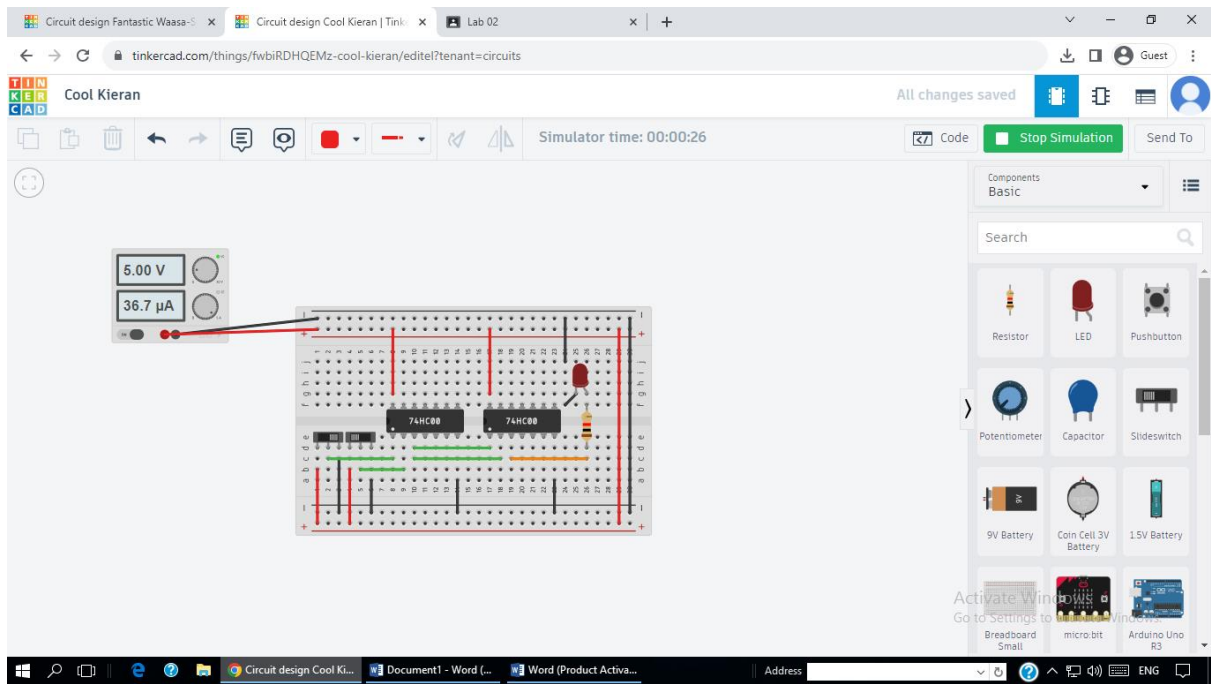
1a)- NAND to NOT :

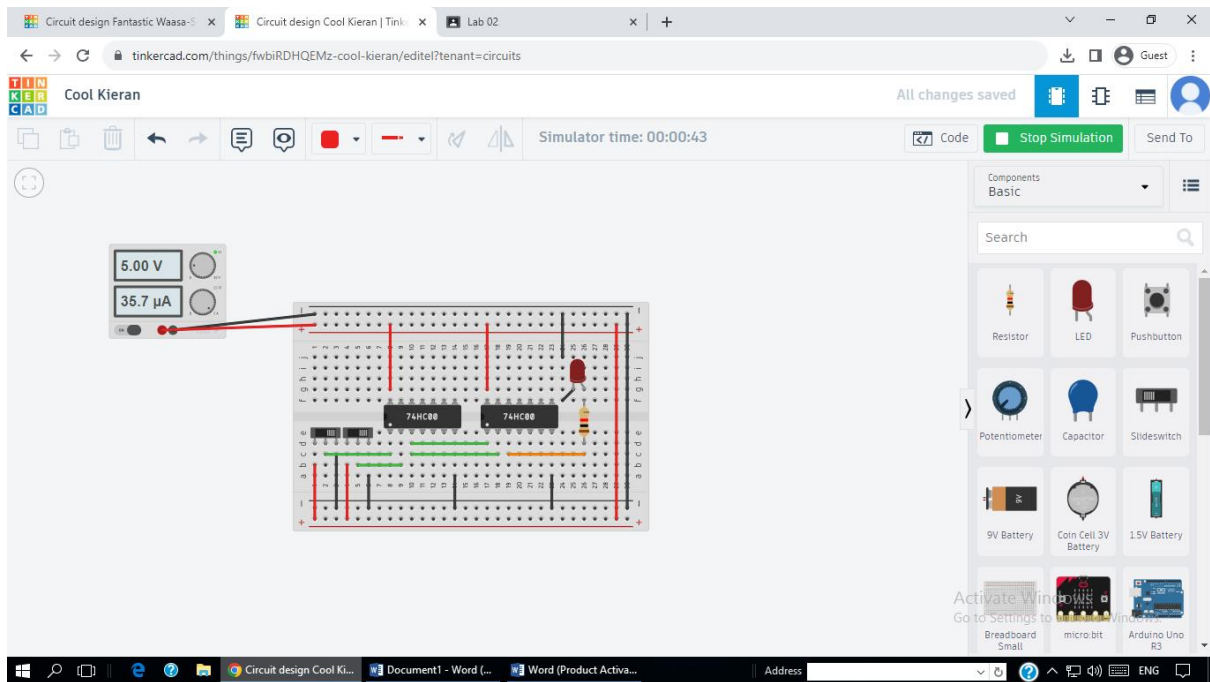




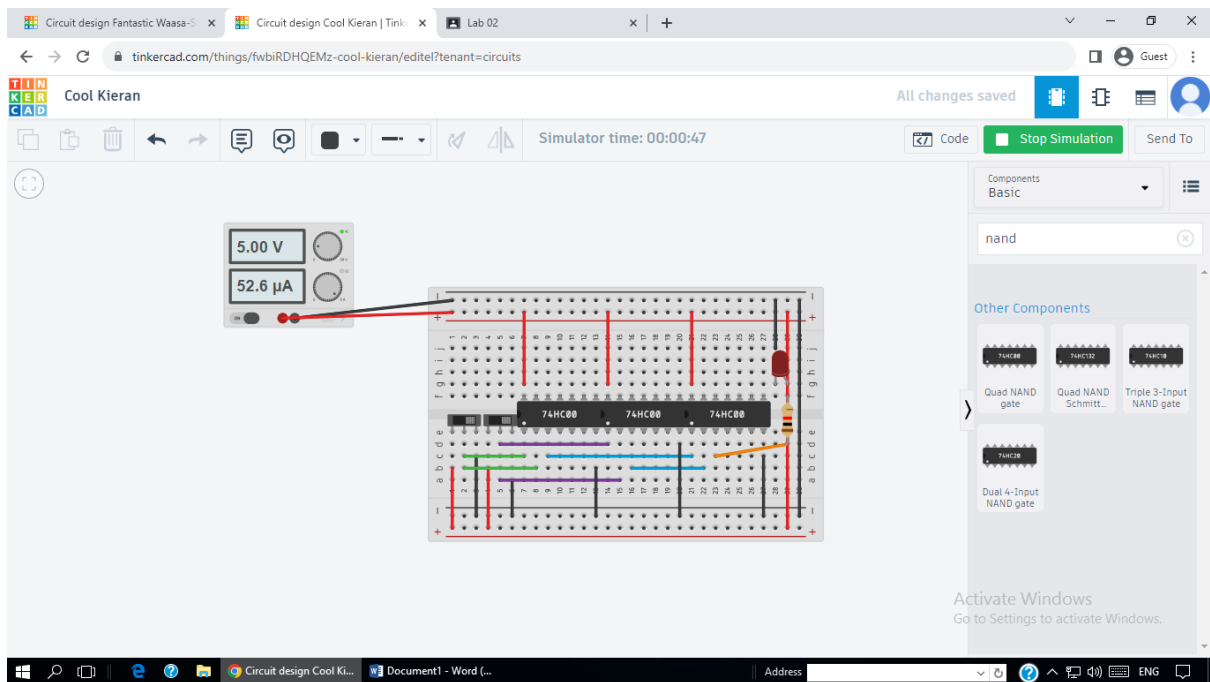
3b) NAND to AND

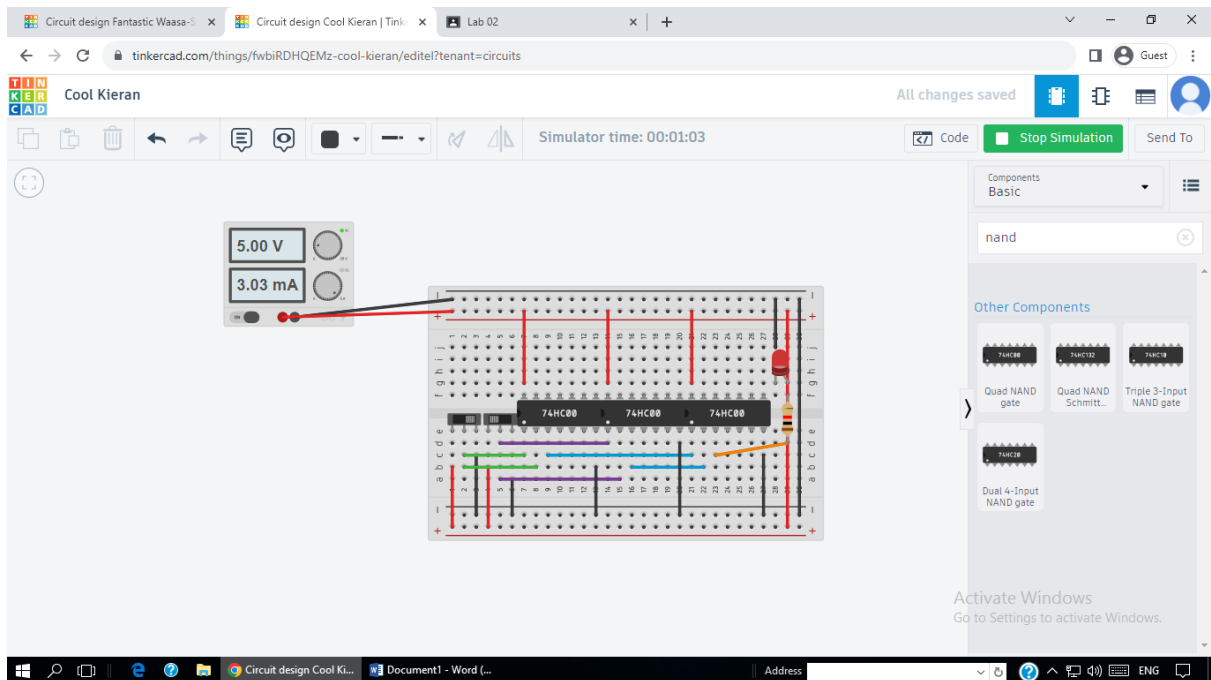
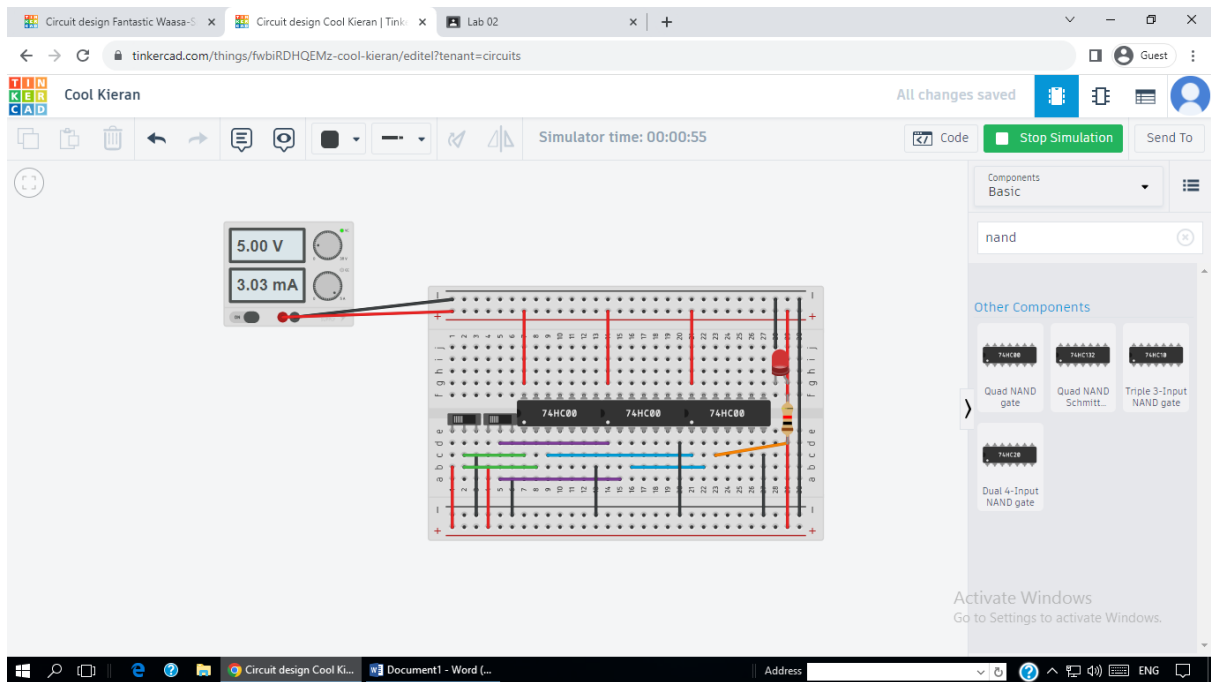


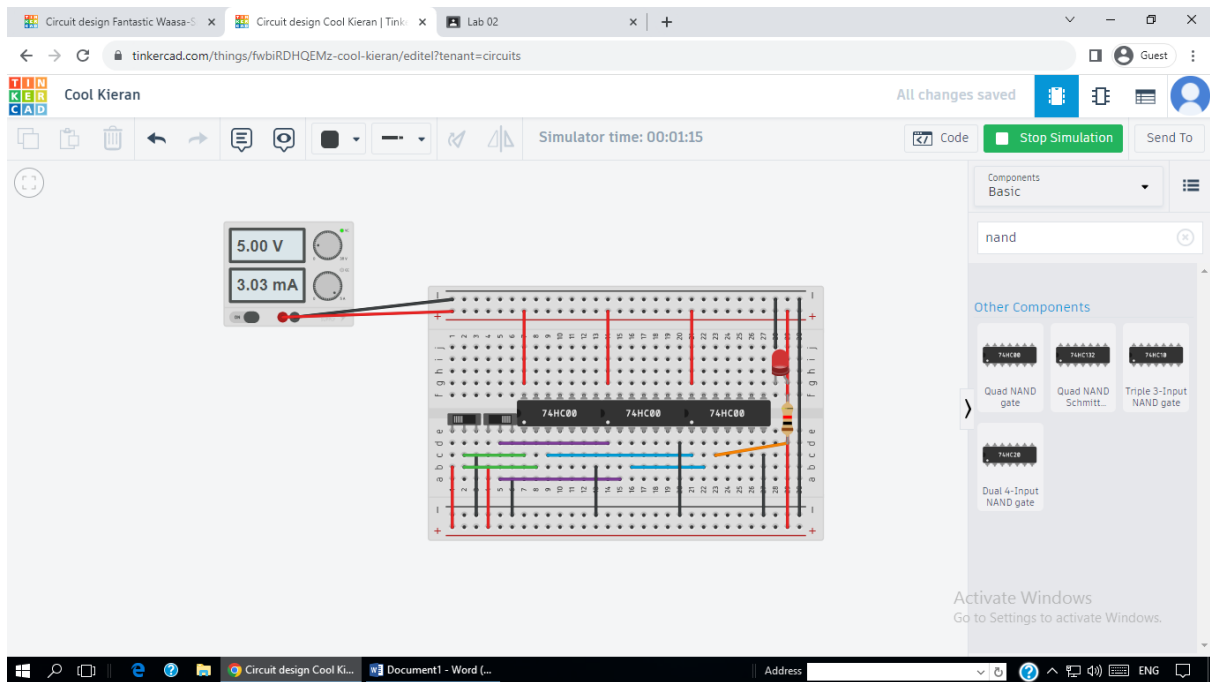




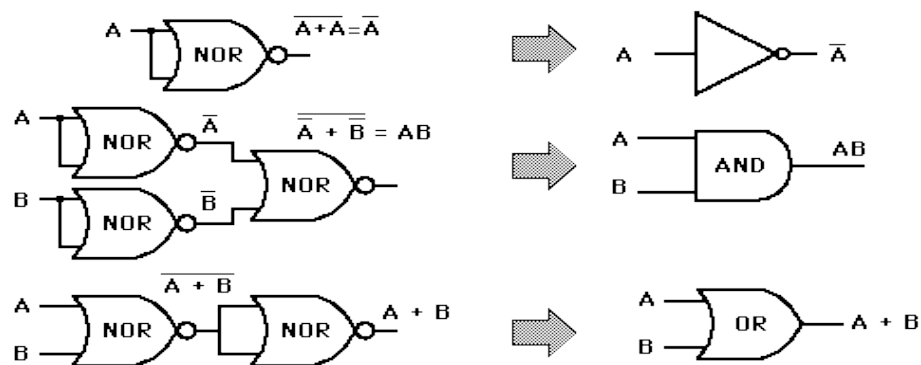
3b) NAND to OR



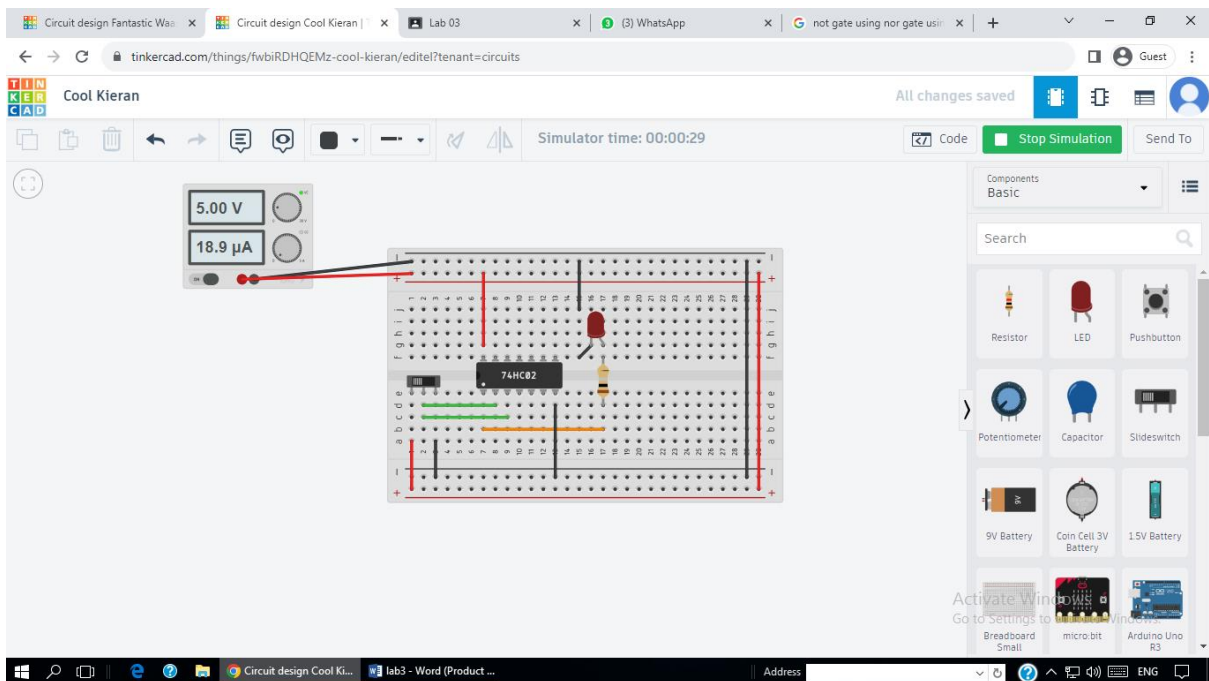
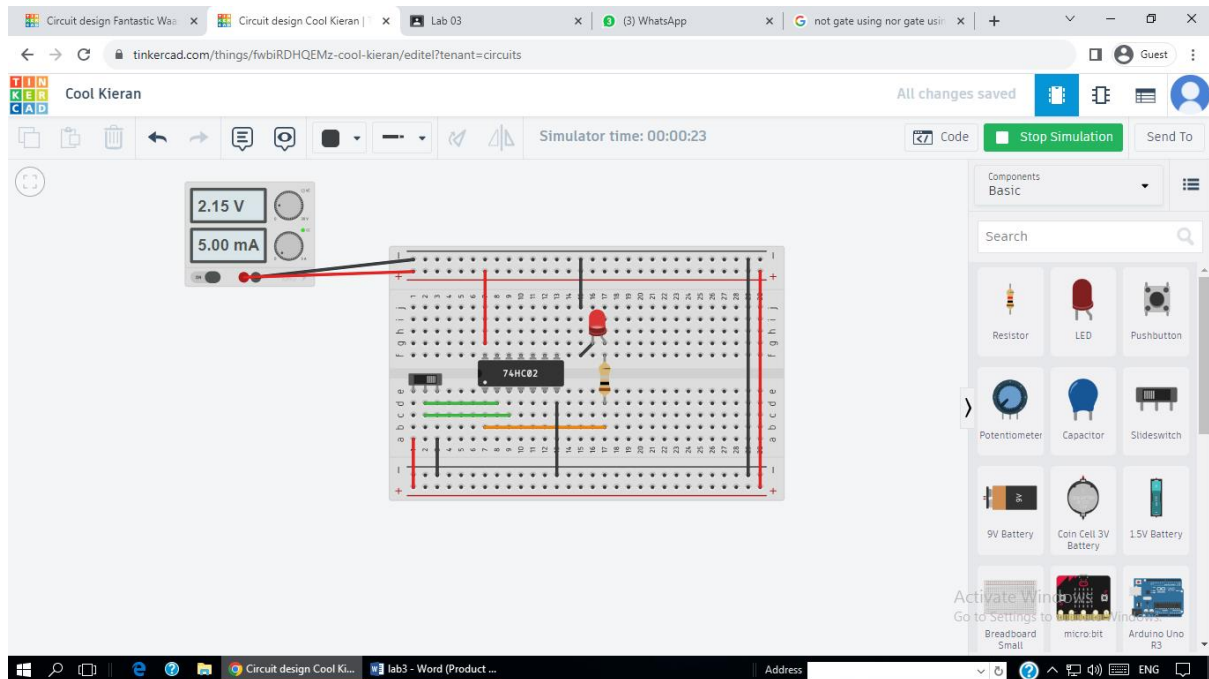




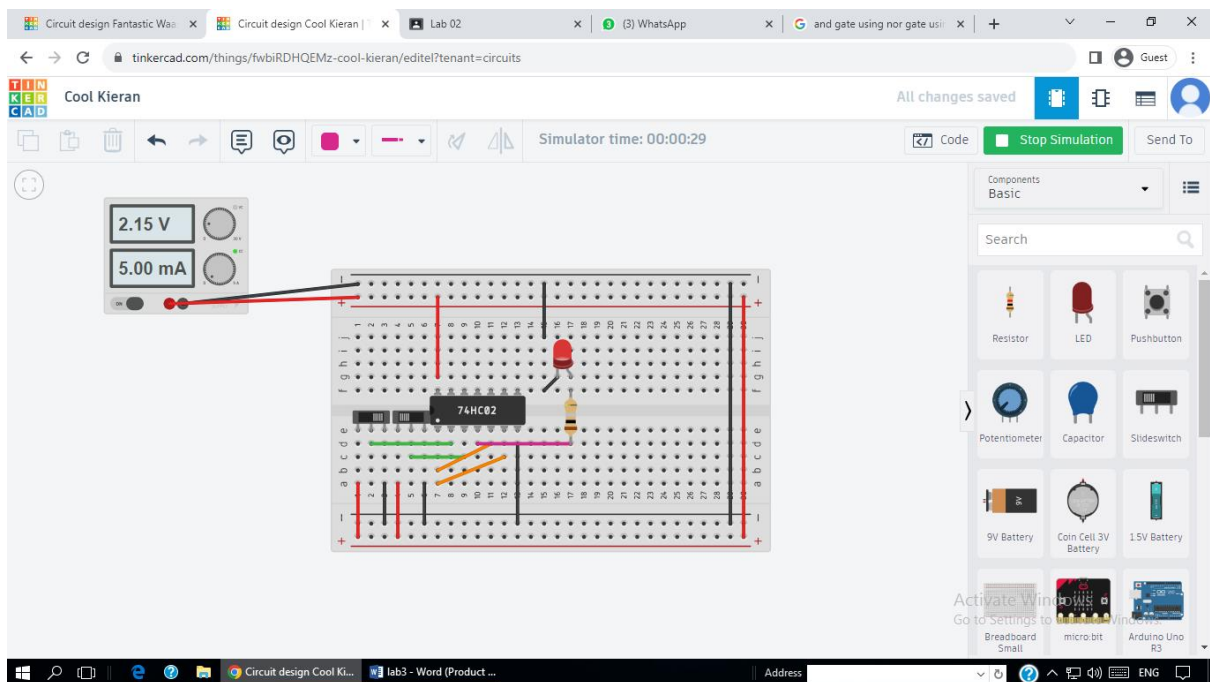
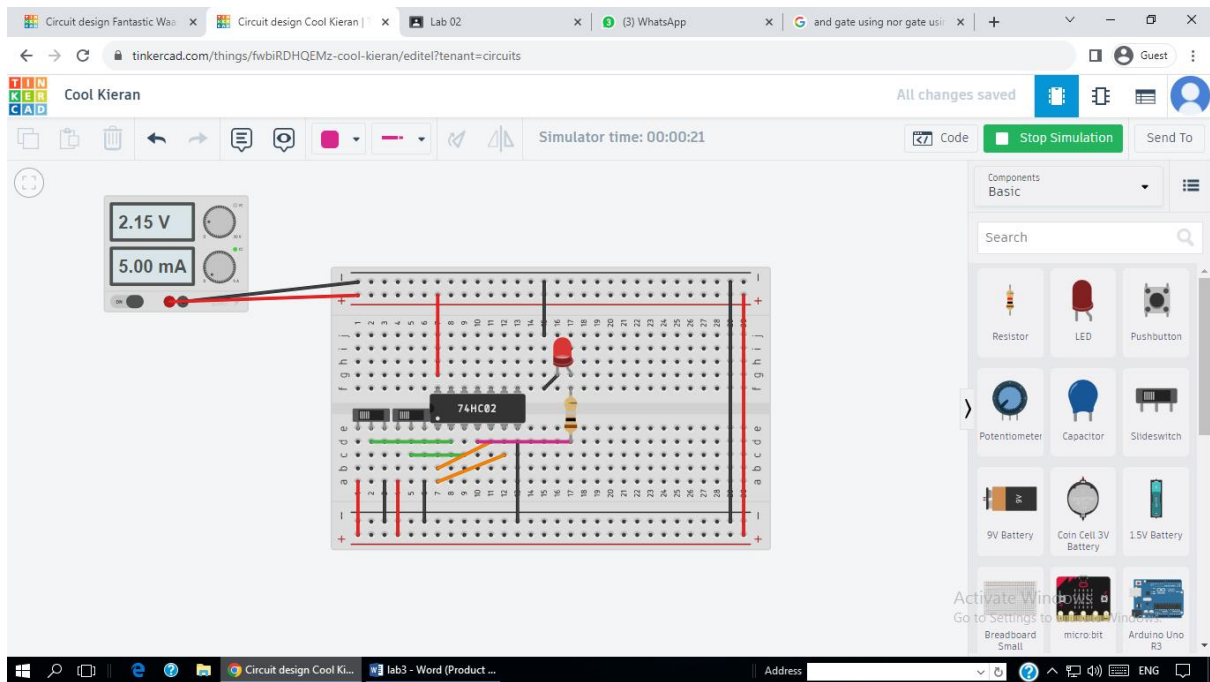
3.2. Working with NOR GATE

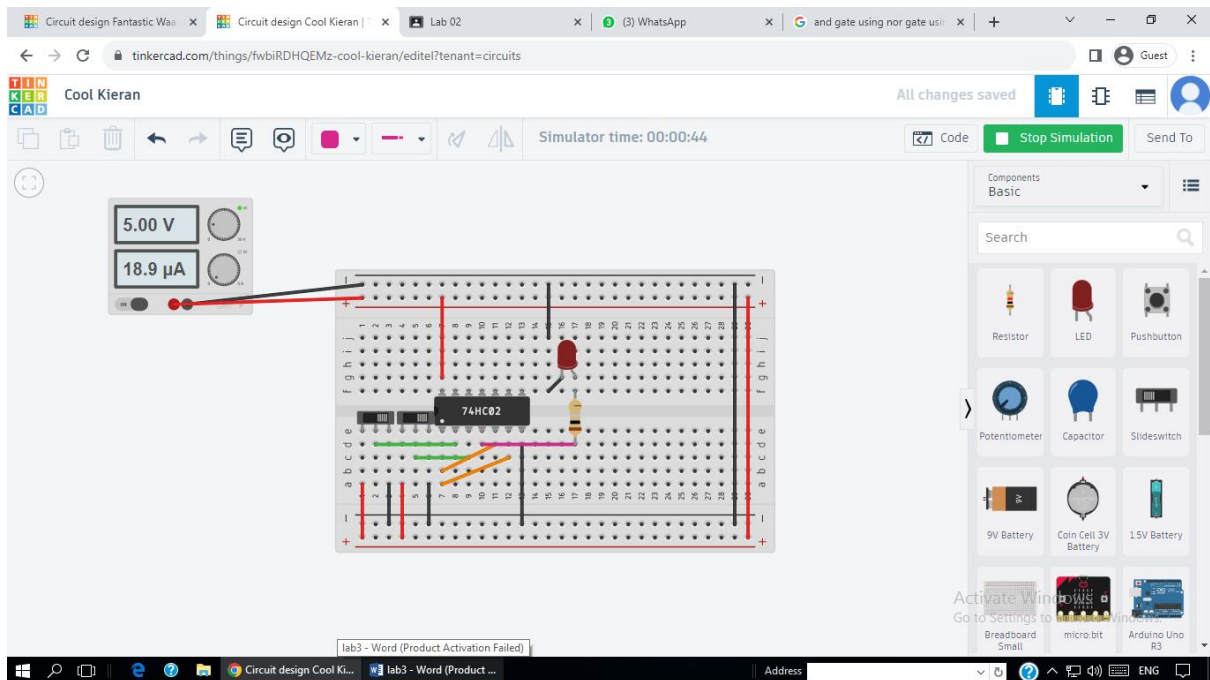
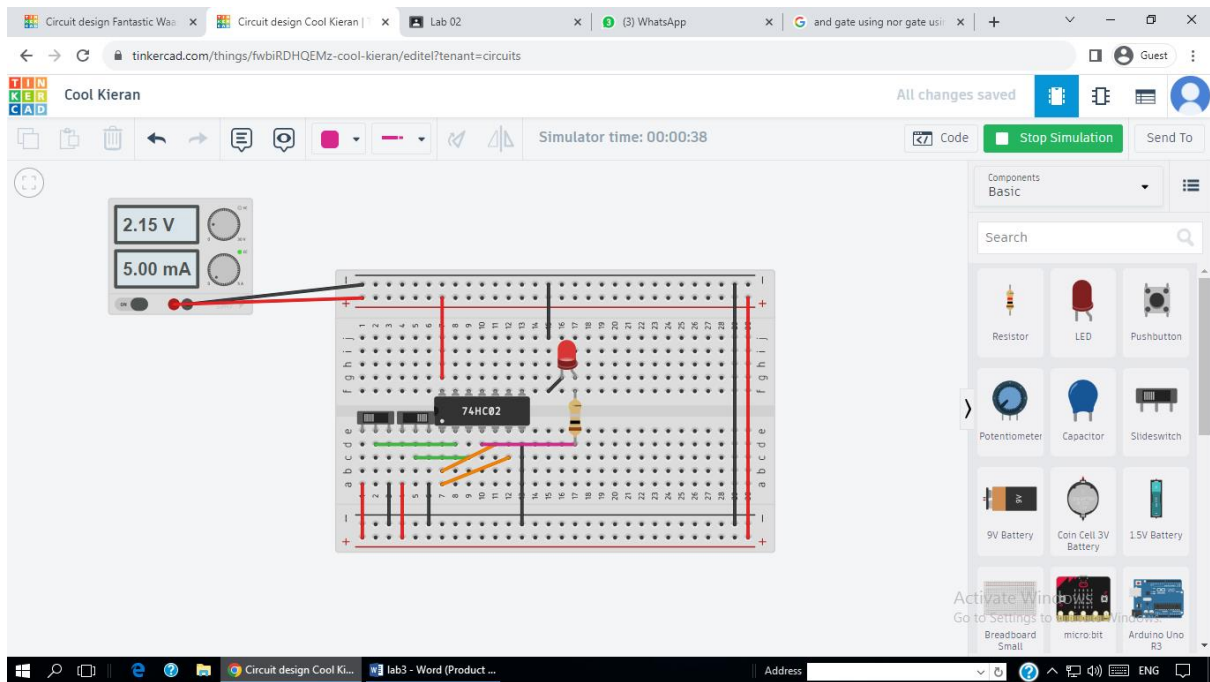


3.4 a Nand to NOT:



3.4 b) Nand to OR





3.4 b) Nand to AND

