# Department Of Software Engineering Computer Architecture & logic design Lab # 01

Submitted to:

Sir Shoaib

Submitted by:

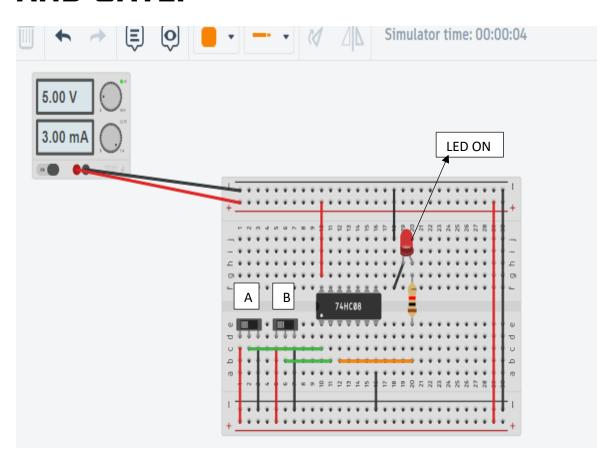
Rabia batool (2022-BSE-064)

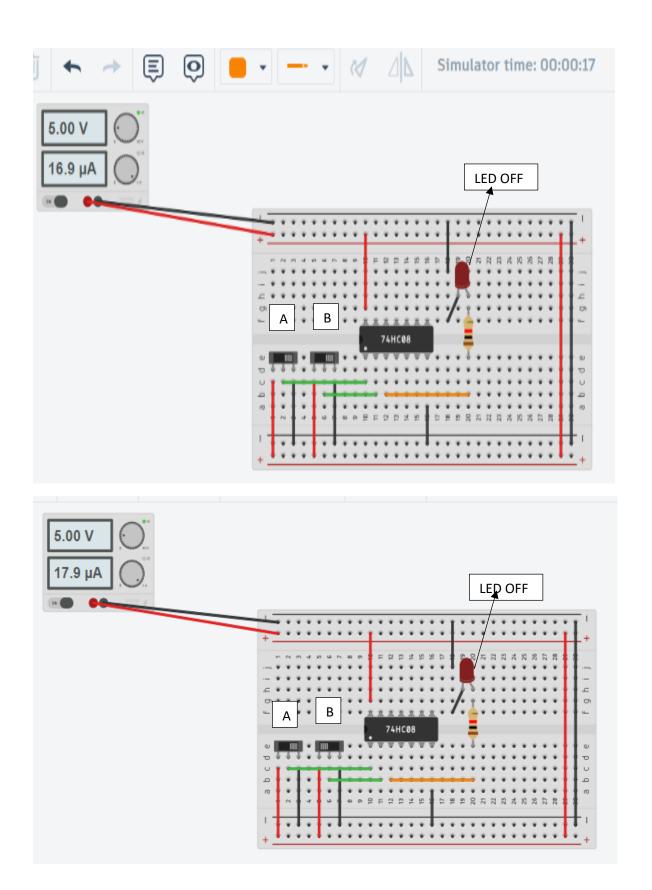
Sawaira Saeed (2022-BSE-067)

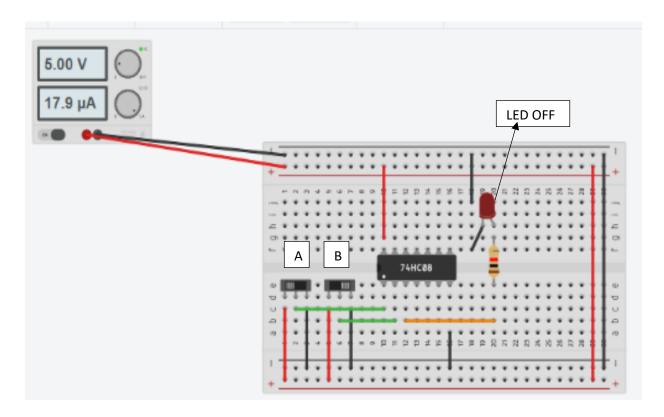
Hafsah Tahir (2022-BSE-052)

# FAMILIARIZATION WITH LOGIC TRAINER AND VERIFICATION OF TRUTH TABLE OF BASIC LOGIC GATES.

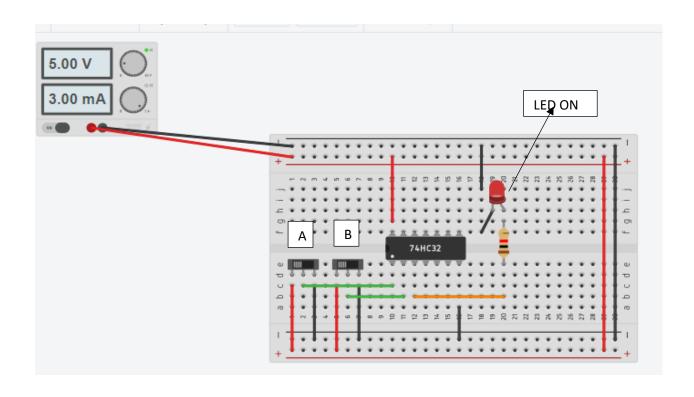
## **AND GATE:**

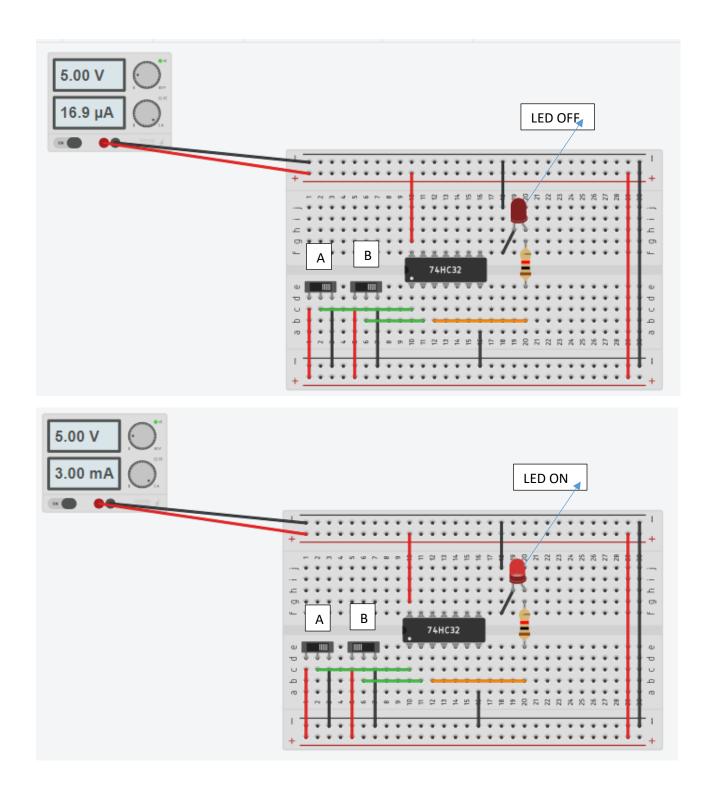


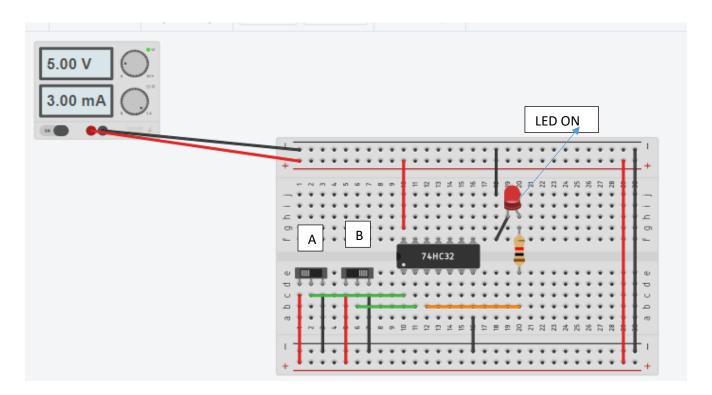




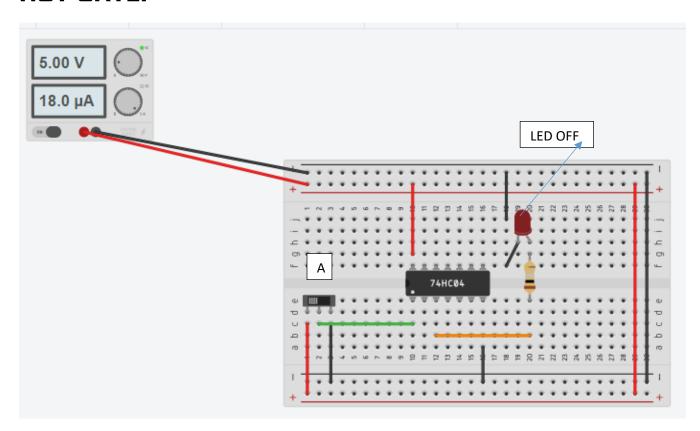
#### OR GATE:

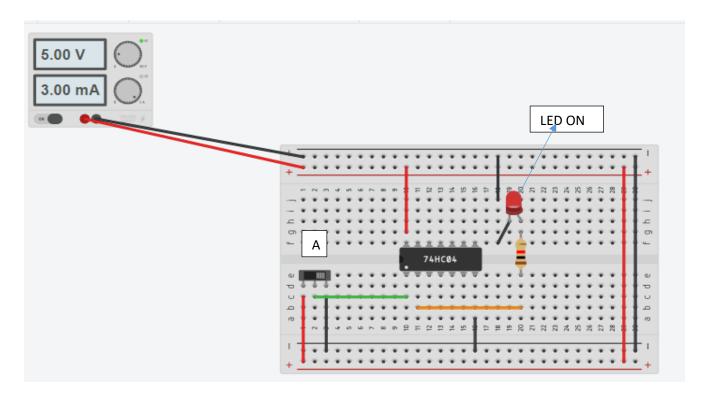




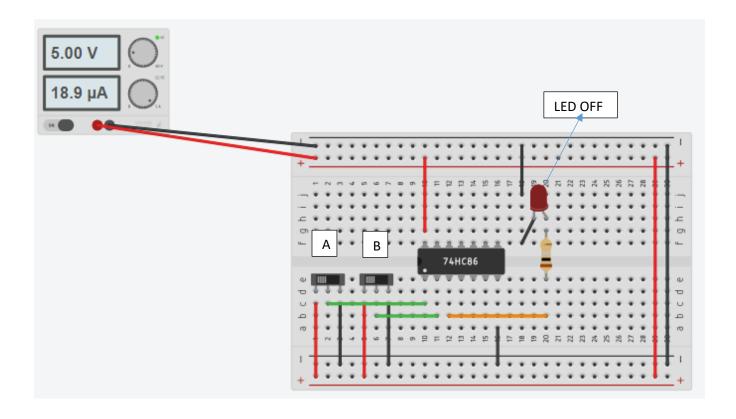


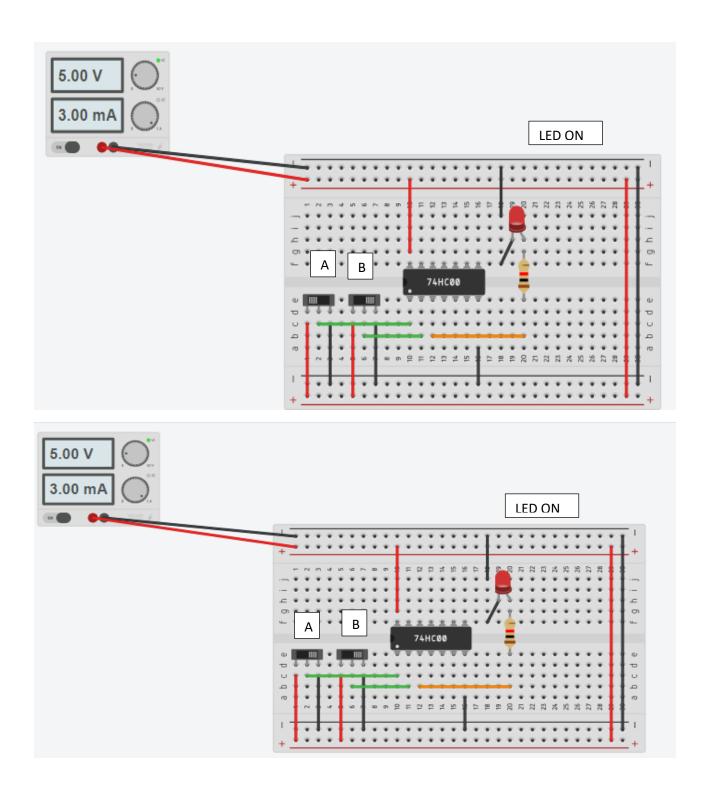
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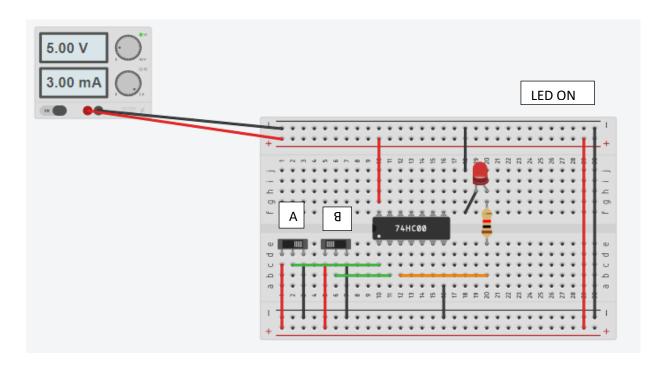




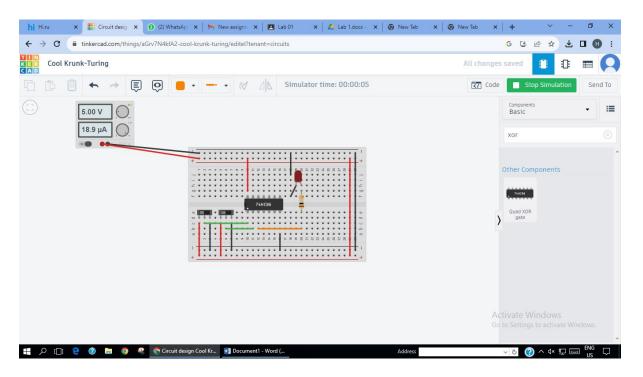
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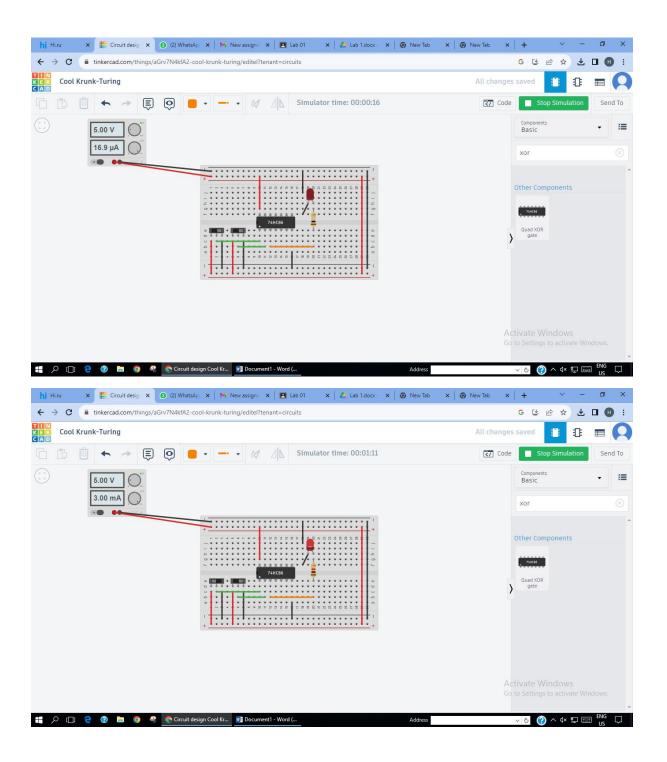


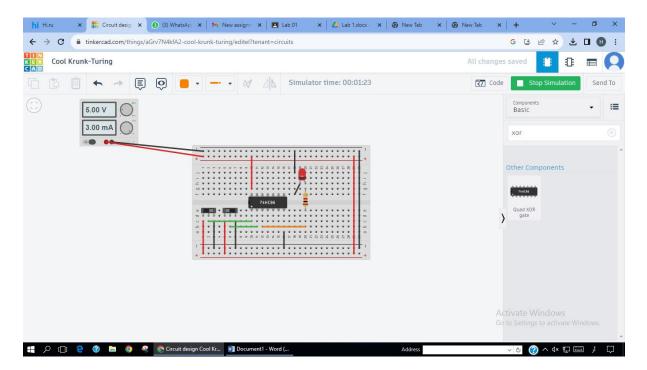




#### **EX-OR**







#### **NOR GATE:**

