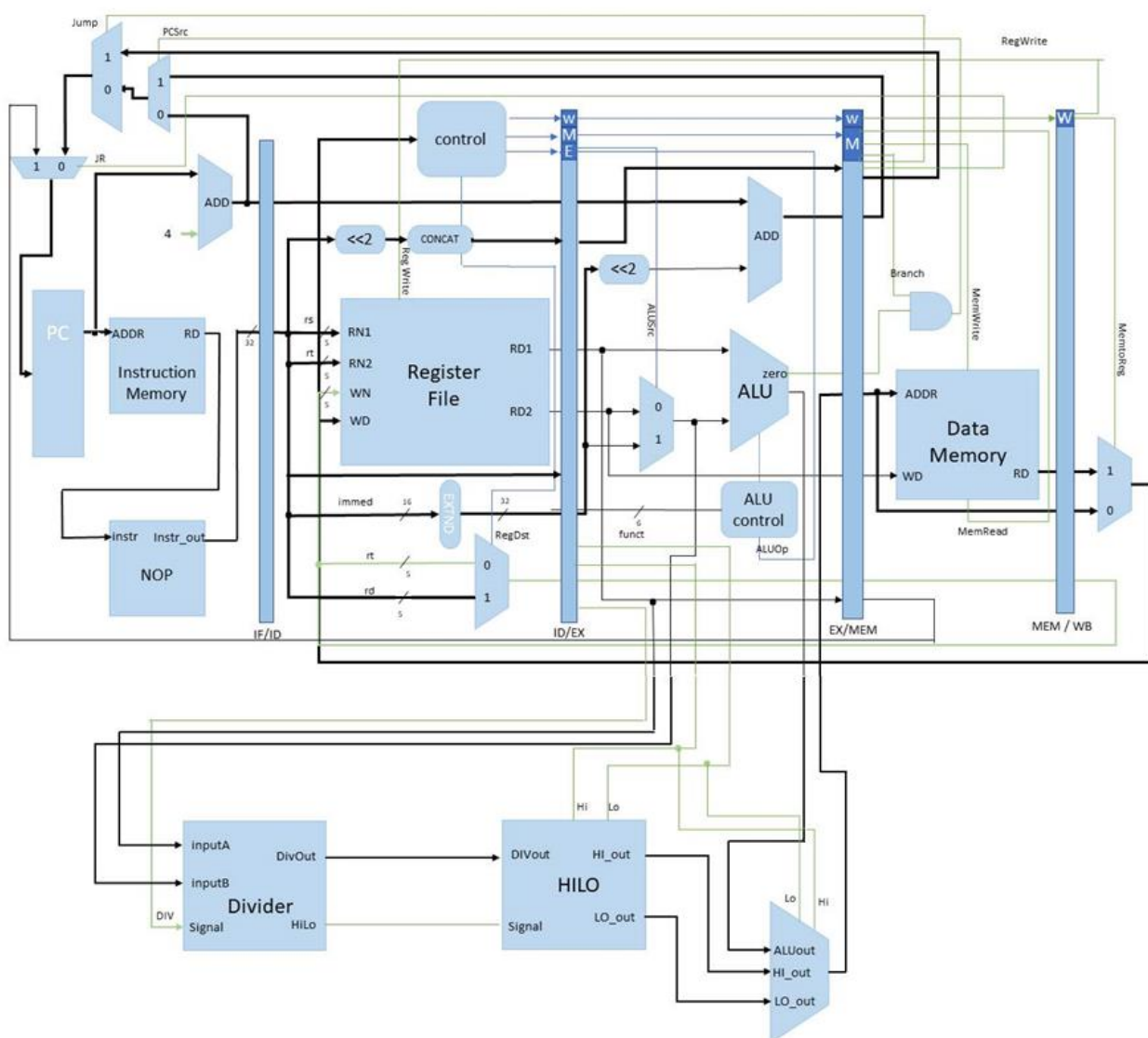


5-Stage-Pipeline-CPU 報告

負責部分：code、架構圖、Waveform 驗證結果

一、架構圖



二、程式說明

1. IF

計算 PC 並抓取指令，且判斷是否需要 NOP，若需要 NOP 就將指令輸出為 32bits 的 0，若不需要就輸出抓到的指令與 PC+4 的值

2. IF_ID

暫存從 IF 傳來的 PC+4 與指令

3. Sign_extend

將 16 bits 的 input extend 至 32 bits

4. Reg_file

判斷 RN1 和 RN2，把 RD1 和 RD2 放好，如果 RN1 或 RN2 為 0，就將 RD1 或 RD2 歸零，如果有東西就寫入 RD1 和 RD2。判斷從 memory 是否有寫東西回來，有的話就寫入 WN

5. Control_single

定義每一指令的訊號，並且定義每一指令的控制訊號

6. ID

將讀入的指令的切成一塊一塊並且 assign 給分別該有的 wire，例如 rs, rt, opcode 等等，先使用 Sign_extend，然後使用剛剛切好並放入的東西寫入 reg_file，最後使用 controll_single 定義訊號，並選擇 WN 的數值

7. ID_EX

先判斷是否 reset，如果是，將所有東西歸零，接下來判斷指令，並且寫好所有的控制訊號，且暫存 ID 所傳入的值

8. EX

負責判斷從不同地方傳來的值該如何處理的地方。EX 裡的元件有 Divider、HILO、ALU、ALU control、ADD 及兩個 MUX。Divider 計算完後將資料存入 HILO，需要時再使用 mfhi 及 mflo 指令使用。ALU control 控制 ALU 應使用的功能。MUX 決定要輸出哪個訊號。

9. EX_MEM

先暫存從 EX 傳來的訊號，再傳送到 Memory 區域

10. Memory

存取資料的地方，控制資料的讀入及寫入記憶體。接收 control signal 的訊號決定 MEM_WRITE、MEM_READ 的訊號。此區域也連接 Branch，不須使用記憶體時，像 jump 指令時可使用 Branch 將訊號送回 IF 區。

11. MEM_WB

暫存從 Memory 傳來的訊號，再傳送到 WB 區域

12. WB

接收訊號後，接收 control signal 的訊號確認 MemtoReg 的訊號來判斷是否需要將資料寫回 Register File，若需要就寫回。

輸入指令為

```
slt $s3, $s2, $s4
```

j 3

```
beq, $s1, $s4, 2
```

```
lw    $t7, $s1, 0
```

```
beq $s1, $s1, 4
```

```
add $s2, $s0, $s2
```

```
sub    $s2, $s0, $s2
```

```
add $s1, $s0, $s1
```

```
add $s1, $s0, $s1
```

divu, \$t0, \$a2

or `$s2, $s0, $s2`

mfhi, \$s6

mflo, \$s5

```
add $s1, $s0, $s1
```

```
sub  $s2, $s0, $s2
```

```
ori $s3, $s2, 4
```

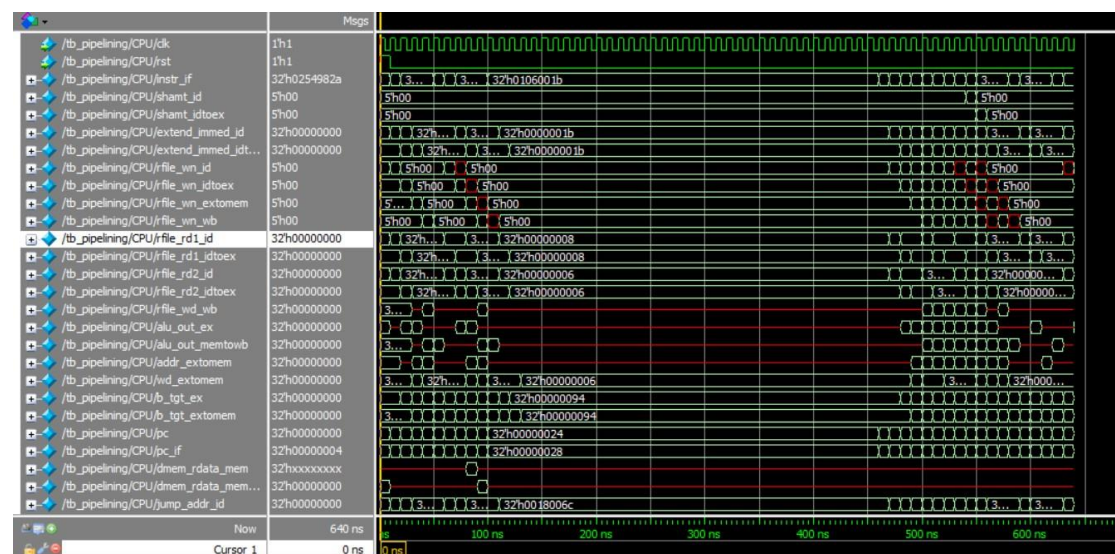
```
sw    $zero, $s2, 24
```

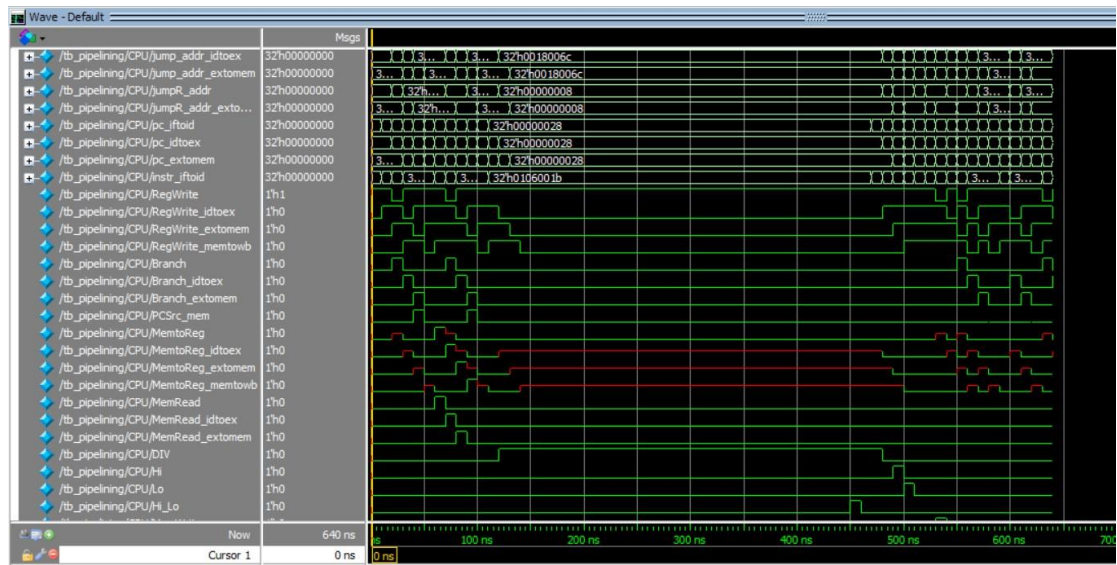
```
srl $s3, $s7, 2
```

```
beq, $s1, $s4, 2
```

jr, \$s7

Waveform :





驗證結果：

1	#	0, reading data: Mem[x] =>	x
2	#	18446744073709551615, PC:	x	
3	#	0, reading data: Mem[0] =>	39098410
4	#	0, reg_file[0] =>	0 (Port 2)	
5	#	0, reg_file[0] =>	0 (Port 1)	
6	#	0, PC:	0	
7	#	0, NOP		
8	#			
9	#	1, reading data: Mem[4] =>	134217731
10	#	1, reg_file[20] =>	5 (Port 2)	
11	#	1, reg_file[18] =>	3 (Port 1)	
12	#	1, PC:	4	
13	#	1, wd:	0	
14	#	1, SLT		
15	#			
16	#	2, reading data: Mem[8] =>	305397762
17	#	2, reg_file[0] =>	0 (Port 2)	
18	#	2, reg_file[0] =>	0 (Port 1)	
19	#	2, PC:	8	
20	#	2, J		
21	#			
22	#	3, reading data: Mem[12] =>	2385444864
23	#	3, PC:	12	
24	#	3, NOP		
25	#			
26	#	4, reading data: Mem[16] =>	305201156
27	#	5, reg_file[19] <=	1 (Write)	
28	#	4, PC:	16	
29	#	4, NOP		
30	#			
31	#	5, reading data: Mem[12] =>	2385444864
32	#	5, PC:	12	
33	#	5, NOP		
34	#			
35	#	6, reading data: Mem[16] =>	305201156
36	#	6, reg_file[15] =>	21 (Port 2)	
37	#	6, reg_file[17] =>	2 (Port 1)	
38	#	6, PC:	16	
39	#	6, LW		
40	#			

```

41 # 7, reading data: Mem[ 20] => 38834208
42 # 7, reg_file[17] => 2 (Port 2)
43 # 7, PC: 20
44 # 7, BEQ
45 #
46 # 8, reading data: Mem[ 24] => 38834210
47 # 8, reg_file[ 0] => 0 (Port 2)
48 # 8, reg_file[ 0] => 0 (Port 1)
49 # 8, reading data: Mem[ 2] => 256
50 # 8, PC: 24
51 # 8, NOP
52 #
53 # 9, reading data: Mem[ 28] => 36735008
54 # 10, reg_file[15] <= 256 (Write)
55 # 9, PC: 28
56 # 9, NOP
57 #
58 # 10, reading data: Mem[ 36] => 17170459
59 run
60 # 10, PC: 36
61 # 10, NOP
62 #
63 # 11, reg_file[ 6] => 6 (Port 2)
64 # 11, reg_file[ 8] => 8 (Port 1)
65 # 11, PC: 36
66 # 11, wd: x
67 # 11, DIVU
68 #
69 # 12, PC: 36
70 # 12, wd: x
71 # 12, DIVU
72 #
73 # 13, PC: 36
74 # 13, wd: x
75 # 13, DIVU
76 #
77 # 14, PC: 36
78 # 14, wd: x
79 # 14, DIVU
80 #
81 # 15, PC: 36
82 # 15, wd: x
83 # 15, DIVU
84 #
85 # 16, PC: 36
86 # 16, wd: x
87 # 16, DIVU
88 #
89 # 17, PC: 36
90 # 17, wd: x
91 # 17, DIVU
92 #
93 # 18, PC: 36
94 # 18, wd: x
95 # 18, DIVU
96 #
97 # 19, PC: 36
98 # 19, wd: x
99 # 19, DIVU
100 #
101 run
102 # 20, PC: 36
103 # 20, wd: x
104 # 20, DIVU
105 #
106 # 21, PC: 36
107 # 21, wd: x
108 # 21, DIVU
109 #
110 # 22, PC: 36
111 # 22, wd: x
112 # 22, DIVU
113 #
114 # 23, PC: 36
115 # 23, wd: x
116 # 23, DIVU
117 #
118 # 24, PC: 36
119 # 24, wd: x
120 # 24, DIVU

```

121	#		
122	#	25, PC:	36
123	#	25, wd:	x
124	#	25, DIVU	
125	#		
126	#	26, PC:	36
127	#	26, wd:	x
128	#	26, DIVU	
129	#		
130	#	27, PC:	36
131	#	27, wd:	x
132	#	27, DIVU	
133	#		
134	#	28, PC:	36
135	#	28, wd:	x
136	#	28, DIVU	
137	#		
138	#	29, PC:	36
139	#	29, wd:	x
140	#	29, DIVU	
141	#		
142	run		
143	#	30, PC:	36
144	#	30, wd:	x
145	#	30, DIVU	
146	#		
147	#	31, PC:	36
148	#	31, wd:	x
149	#	31, DIVU	
150	#		
151	#	32, PC:	36
152	#	32, wd:	x
153	#	32, DIVU	
154	#		
155	#	33, PC:	36
156	#	33, wd:	x
157	#	33, DIVU	
158	#		
159	#	34, PC:	36
160	#	34, wd:	x
161	#	34, DIVU	
162	#		
163	#	35, PC:	36
164	#	35, wd:	x
165	#	35, DIVU	
166	#		
167	#	36, PC:	36
168	#	36, wd:	x
169	#	36, DIVU	
170	#		
171	#	37, PC:	36
172	#	37, wd:	x
173	#	37, DIVU	
174	#		
175	#	38, PC:	36
176	#	38, wd:	x
177	#	38, DIVU	
178	#		
179	#	39, PC:	36
180	#	39, wd:	x
181	#	39, DIVU	
182	#		

```

183 run
184 # 40, PC: 36
185 # 40, wd: x
186 # 40, DIVU
187 #
188 # 41, PC: 36
189 # 41, wd: x
190 # 41, DIVU
191 #
192 # 42, PC: 36
193 # 42, wd: x
194 # 42, DIVU
195 #
196 # 43, PC: 36
197 # 43, wd: x
198 # 43, DIVU
199 #
200 # 44, PC: 36
201 # 44, wd: x
202 # 44, DIVU
203 #
204 # 45, PC: 36
205 # 45, wd: x
206 # 45, DIVU
207 #
208 # 46, reading data: Mem[ 40] => 38834213
209 # 46, PC: 40
210 # 46, wd: x
211 # 46, DIVU
212 #
213 # 47, reading data: Mem[ 44] => 45072
214 # 47, reg_file[16] => 1 (Port 2)
215 # 47, reg_file[18] => 3 (Port 1)
216 # 47, PC: 44
217 # 47, wd: x
218 # 47, OR
219 #
220 # 48, reading data: Mem[ 48] => 43026
221 # 48, reg_file[ 0] => 0 (Port 2)
222 # 48, reg_file[ 0] => 0 (Port 1)
223 # 48, PC: 48
224 # 48, wd: x
225 # 48, MFHI
226 #
227 # 49, reading data: Mem[ 52] => 36735008
228 # 49, PC: 52
229 # 49, wd: x
230 # 49, MFLO
231 #
232 # 50, reading data: Mem[ 56] => 38834210
233 # 50, reg_file[16] => 1 (Port 2)
234 # 50, reg_file[17] => 2 (Port 1)
235 run
236 # 51, reg_file[18] <= 3 (Write)
237 # 50, PC: 56
238 # 50, wd: 3
239 # 50, ADD
240 #
241 # 51, reading data: Mem[ 60] => 911409156
242 # 51, reg_file[18] => 3 (Port 1)
243 # 52, reg_file[22] <= 2 (Write)
244 # 51, PC: 60
245 # 51, wd: 2
246 # 51, SUB
247 #
248 # 52, reading data: Mem[ 64] => 2886860824
249 # 52, reg_file[19] => 1 (Port 2)
250 # 53, reg_file[21] <= 1 (Write)
251 # 52, PC: 64
252 # 52, ORI
253 #
254 # 53, reading data: Mem[ 68] => 1546370
255 # 53, reg_file[ 0] => 0 (Port 1)
256 # 53, reg_file[18] => 3 (Port 2)
257 # 54, reg_file[17] <= 3 (Write)
258 # 53, PC: 68
259 # 53, SW
260 #

```

```

261 # 54, reading data: Mem[ 72] => 305397762
262 # 54, reg_file[23] => 8 (Port 2)
263 # 55, reg_file[18] <= 2 (Write)
264 # 54, PC: 72
265 # 54, wd: 2
266 # 54, SRL
267 #
268 # 55, reading data: Mem[ 76] => 48234504
269 # 55, reg_file[17] => 3 (Port 1)
270 # 55, reg_file[20] => 5 (Port 2)
271 # 56, reg_file[19] <= 7 (Write)
272 # 56, writing data: Mem[ 24] <= 3
273 # 55, PC: 76
274 # 55, BEQ
275 #
276 # 56, reading data: Mem[ 80] => x
277 # 56, reg_file[ 0] => 0 (Port 1)
278 # 56, reg_file[ 0] => 0 (Port 2)
279 # 56, PC: 80
280 # 56, NOP
281 #
282 # 58, reg_file[19] <= 2 (Write)
283 # 57, PC: 84
284 # 57, NOP
285 #
286 # 58, reading data: Mem[ 76] => 48234504
287 # 58, PC: 76
288 # 58, NOP
289 #
290 # 59, reading data: Mem[ 80] => x
291 # 59, reg_file[23] => 8 (Port 1)
292 # 59, PC: 80
293 # 59, wd: x
294 # 59, JR
295 #
296 # 60, reg_file[ 0] => 0 (Port 1)
297 run
298 # 60, PC: 84
299 # 60, NOP
300 #
301 # 61, PC: 88
302 # 61, NOP
303 #
304 # 62, reading data: Mem[ 8] => 305397762
305 # 62, PC: 8
306 # 62, NOP
307 #
308 # 63, reading data: Mem[ 12] => 2385444864
309 # 63, reg_file[20] => 5 (Port 2)
310 # 63, reg_file[17] => 3 (Port 1)
311 # 63, PC: 12
312 # 63, BEQ
313 #
314 # 64, reading data: Mem[ 16] => 305201156
315 # 64, reg_file[ 0] => 0 (Port 2)
316 # 64, reg_file[ 0] => 0 (Port 1)
317 # 64, PC: 16
318 # 64, NOP
319 #

```