VLSID

3D Integrated Circuit

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1. INTRODUCTION

There is a saying in real estate; when land get expensive, multi-storied buildings are the alternative solution. We have a similar situation in the chip industry. For the past thirty years, chip designers have considered whether building integrated circuits multiple layers might create cheaper, more powerful chips.

Performance of deep-sub micrometer very large scale integrated (VLSI) circuits is being increasingly dominated by the interconnects due to increasing wire pitch and increasing die size. Additionally, heterogeneous integration of different technologies on one single chip is becoming increasingly desirable, for which planar (2-D) ICs may not be suitable.

The three dimensional (3-D) chip design strategy exploits the vertical dimension to alleviate the interconnect related problems and to facilitate heterogeneous integration of technologies to realize system on a chip (SoC) design. By simply dividing a planar chip into separate blocks, each occupying a separate physical level interconnected by short and vertical interlayer interconnects (VILICs), significant improvement in performance and reduction in wire-limited chip area can be achieved[1]

In the 3-Ddesign architecture, an entire chip is divided into a number of blocks, and each block is placed on a separate layer of Si that are stacked on top of each other.

2. MOTIVATION FOR 3-D ICs

The unprecedented growth of the computer and the information technology industry is demanding Very Large Scale Integrated (VLSI) circuits with increasing functionality and performance at minimum cost and power dissipation. Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasing interconnect delays. A significant fraction of the total power consumption can be due to the wiring network used for clock distribution, which is usually realized using long global wires[1]

Furthermore, increasing drive for the integration of disparate signals (digital, analog, RF) and technologies (SOI, SiGe, GaAs, and so on) is introducing various SoC design concepts, for which existing planner (2-D) IC design may not be suitable.

➢ INTERCONNECT LIMITED VLSI PERFORMANCE

In single Si layer (2-D) ICs, chip size is continuously increasing despite reductions in feature size made possible by advances in IC technology such as lithography and etching. This is due to the ever growing demand for functionality and high performance, which causes increased complexity of chip design, requiring more and more transistors to be closely packed and connected. Small feature sizes have dramatically improved device performance. The impact of this miniaturization on the performance of interconnect wire, however, has been less positive. Smaller wire cross sections, smaller wire pitch, and longer line to traverse larger chips have increase the resistance and capacitance of these lines, resulting in a significant increase in signal propagation (RC) delay. As interconnect scaling continues, RC delay is increasingly becoming the dominant factor determining the performance of advanced IC's.

➢ PHYSICAL LIMITATIONS OF Cu INTERCONNECTS

At 250 nm technology node, Cu with low-k dielectric was introduced to alleviate the adverse effect of increasing interconnect delay.However,below 130nm technology node, substantial interconnect delays would result in spite of introducing these new materials, which in turn will severely limit the chip performance. Further reduction in interconnect delay is not possible.

This problem is especially acute for global interconnects, which comprise about 10% of total wiring in current architectures. Therefore, it is apparent that material limitations will ultimately limit the performance improvement as technology scales. Also, the problem of long lossy lines cannot be fixed by simply widening the metal lines and by using thicker interlayer dielectric, since this will leas to an increase in the number of metal layers. This will result in an increase in complexity, reliability and cost.

➢ SYSTEM – ON – A – CHIP DESIGN

System – on – a –chip (SoC) is a broad concept that refers to the integration of nearly all aspects of a system design on a single chip. These chips are often mixed-signal and/or mixed-technology designs, including such diverse combinations as embedded DRAM, high – performance and low-power logic, analog, RF, programmable platforms (software, FPGAs, Flash, etc.).

SoC designs are often driven by the ever-growing demand for increased system functionality and compactness at minimum cost, power consumption, and time to market. These designs form the basis for numerous novel electronic applications in the near future, in areas such as wired and wireless multimedia communications including high speed internet applications, medical applications

including remote surgery, automated drug delivery, and non invasive internal scanning and diagnosis, aircraft/automobile control and safety, fully automated industrial control systems, chemical and biological hazard detection, and home security and entertainment systems, to name a few.

There are **several challenges** to effective SoC designs:

1. Large scale integration of functionalities and disparate technologies on a single chip dramatically increases the chip area, which necessitates the use of numerous long global wires. These wires can lead to unacceptable signal transmission delays and increase the power consumption by increasing the total capacitance that needs to be driven by the gates.

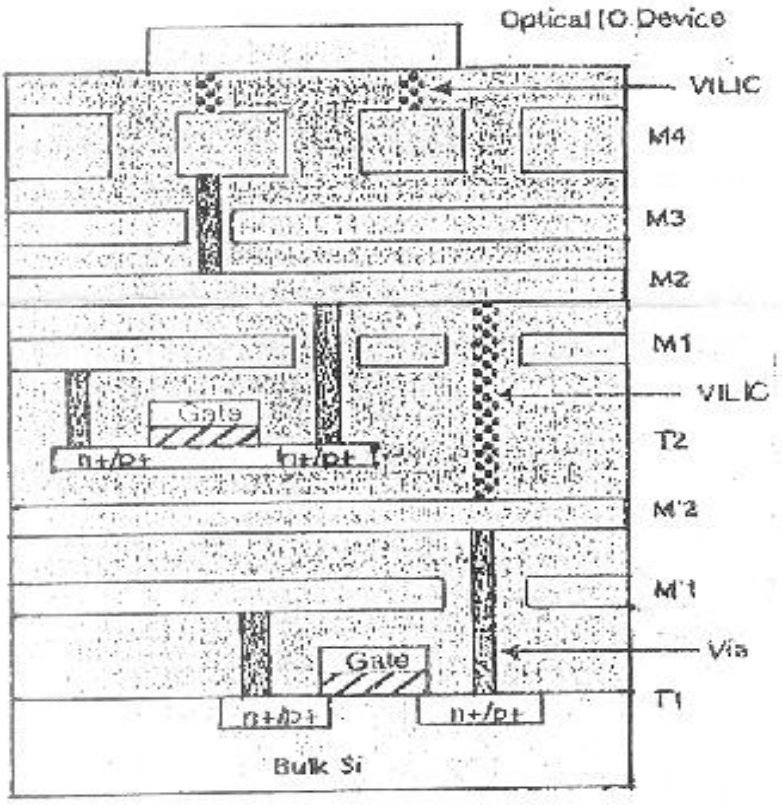
2. Integration of disparate technologies such as embedded DRAM, logic, and passive components in SoC applications introduces significant complexity in materials and process integration.

3. The noise generated by the interference between different embedded circuit blocks containing digital and analog circuits becomes a challenging problem.

4. Although SoC designs typically reduce the number of I/O pins compared to a system assembled on a printed circuit board(PCB), several high performance SoC designs involve very high I/O pin counts , which can increase the cost per chip

5. Integration of mixed technologies on a single die requires novel design methodologies and tools ,with design productivity being a key requirement.

➢ 3D ARCHITECTURE



Three-dimensional integration to create multilayer Si ICs is a concept that can significantly improve interconnect performance ,increase transistor packing density, and reduce chip area and power dissipation. Additionally 3D ICs can be very effective large scale on chip integration of different systems.

In 3D design architecture, and entire(2D) chips is divided into a number of blocks is placed on separate layer of Si that are stacked on top of each other. Each Si layer in the 3D structure can have multiple layer of interconnects(VILICs) and common global interconnects.

➢ ADVANTAGES OF 3D ARCHITECTURE

The 3D architecture offers extra flexibility in system design, placement and routing. For instance, logic gates on a critical path can be placed very close to each other using multiple active layers. This would result in a significant reduction in RC delay and can greatly enhance the performance of logical circuits.

- The 3D chip design technology can be exploited to build SoCs by placing circuits with different voltage and performance requirements in different layers.
- The 3D integration can reduce the wiring ,thereby reducing the capacitance, power dissipation and chip area and therefore improve chip performance.
- Additionally the digital and analog components in the mixed-signal systems can be placed on different Si layers thereby achieving better noise performance due to lower electromagnetic interference between such circuits blocks.
- From an integration point of view, mixed-technology assimilation could be made less complex and more cost effective by fabricating such technologies on separate substrates followed by physical bonding.

3. SCOPE OF THIS STUDY

A 3D solution at first glance seems an obvious answer to the interconnect delay problem. Since chip size directly affects the inter connect delay, therefore by creating a second active layer, the total chip footprint can be reduced, thus shortening critical inter connects and reducing their delay[3]. However, in today's microprocessor, the chip size is not just limited by the cell size ,but also by how much meta is required to connect the cells. The transistors on the Si surface are not actually packed to maximum density, but are spaced apart to allow metal lines above to connect one transistor or one cell to another .The meal required on a chip for inter connections is determined not only by the number of gates ,but also by other factors such as architecture, average fan-out, number of I/O connections, routing complexity, etc Therefore, it is not obvious that using a 3D structure the chip size will be reduced.

4. AREA AND PERFORMANCE ESTIMATION OF 3D ICs

Now we present a methodology that can be used to provide an initial estimate of the area and performance of high speed logic circuits fabricated using multiple silicon layer IC technology. The approach is based on the empirical relationship known as Rent's Rule.

Rent's Rule:

It correlates the number of signal input and output (I/O) pins T, to the number of gates N, in a random logic network and is given by the following expressions :

$$T=kN^{P} \qquad \text{----------(i)}$$

Here k & P denote the average number of fan out per gate and the degree of wiring complexity (with P=1 representing the most complex wiring network), respectively, and are empirically derived as constants for a given generation of ICs.

A) 2-D AND 3-D WIRE-LENGTH DISTRIBUTIONS

The wire-length distribution can be described by i(l),an interconnect density functions (i.d.f), or by I(l), the cumulative interconnect distribution function (c.i.d.f) which gives the total number of interconnects that have length less than or equal to l (measured in gate pitches) and is defined as

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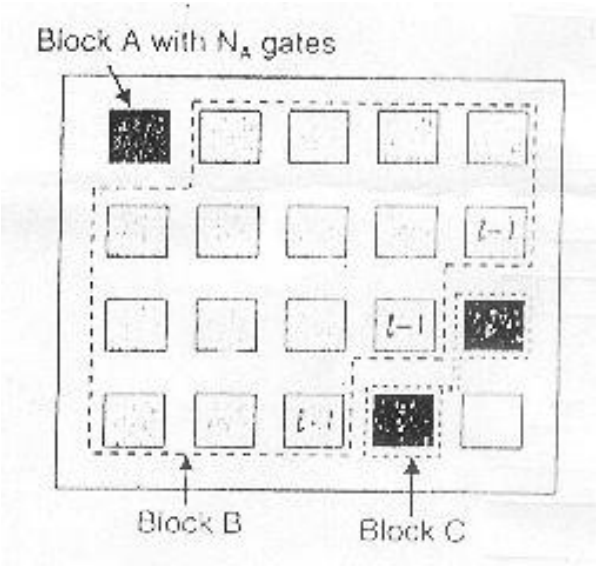
$$I(l)=\int_{1}^{l} i(x)dx \qquad \text{----------(ii)}$$

Where x is a variable of integration representing length and l is the length of the interconnect in gate pitches. The derivation of the wire-length distributed in a Ic

is based on Rent's Rule. To derive the wire length distribution I(l) of an integrated circuit, the latter is divided up into N logic gates, where N is related to the total number of transistor Nt in an integrated circuit by N=Nt/O where O is a function of the average fan-in(f.i0 and fan-out(f.o). The gate pitch is defined as the average separation between the logic gates and is equal to sqt(Ac/N) where Ac is the area of the chip.

In order to derive the complete wire-length distribution for a chip, the stochastic wire-length distribution of a single gate must be calculated.



The number of connections from the single logic gate in Block A to all other gate that are located at a distance of l gate pitches is determined using Rent's Rule. The gates shown in the figure are grouped into three distinct but adjacent blocks(A,B&C), such that a closed single path can encircle one, two or three of these blocks. The number of connections between Block A and Block C is calculated by conserving all I/O terminals for blocks, A, B, and C, which states that terminals for blocks A, B, and C, are either interlock connections or external system connections.

Hence, applying the principle of conservation of I/O pins to this system of three logic blocks, shown gives

$$T_A + T_B + T_C = T_{A\ to\ C} + T_{A\ to\ B} + T_{B\ to\ C} + T_{ABC} \quad \text{.....(iii)}$$

Where T_A, T_B, T_C are the number of I/O blocks A, B, and C respectively. $T_{A\ to\ C}$, $T_{A\ to\ B}$, $T_{B\ to\ C}$ are the number of I/Os between blocks A and C, blocks A and B, and between blocks B and C, respectively. T_{ABC} represents the number of I/Os for the entire system comprising of all three blocks. From conservation of I/Os, the number of I /Os between adjacent blocks A and B, and between adjacent blocks A and B and between adjacent blocks B and C can be expressed as

$$T_{A\ to\ B} = T_A + T_B - T_{AB} \quad \text{.....(iv)}$$

$$T_{B\ to\ C} = T_B + T_C - T_{BC} \quad \text{.....(v)}$$

Substituting (iv) and (v) into (iii) gives

$$T_{A\ to\ C} = T_{AB} + T_{BC} - T_B - T_{ABC} \quad \text{.....(vi)}$$

Now the number of I/O pins for any single block or a group of blocks can be calculated using Rent's Rule. If we assume that N, N, and N are the number of gates in blocks A, B, and C, respectively, then it follows that

$$T_B = k\,(N_B)^P \quad \text{.....(vii)}$$

$$T_{AB} = k(N_A + N_B)^P \quad \text{.....(viii)}$$

$$T_{BC} = k(N_B + N_C)^P \quad \text{.....(ix)}$$

$$T_{ABC} = k(N_A + N_B + N_C)^P \quad \text{.....(x)}$$

Where $N = N_A + N_B + N_C$. Substituting (vii) – (x) into (vi) gives

$$T_{A\ to\ C} = k\,[(N_A + N_B)^P - (N_B)^P + (N_B + N_C)^P - (N_A + N_B + N_C)^P] \quad \text{.....(xi)}$$

The number of interconnects between Block A and Block C ($I_{A\ to\ C}$) is determined using the relation

$$I_{A\ to\ C} = \alpha k\ (T_{A\ to\ C})$$

Where α is related to the average fan out (f.o.) by

$$\alpha = f.o. / (1+f.o.)$$

Applying Rent's Rule to all the layers, we have

$$T=kN^P = (\sum_{i=1}^{n} T_i) - T_{int} = nk(N/n)^P - T_{int}$$

Here, T is the number of I/Os for the entire design, T_i represents the number of I/O ports connecting n layers. Hence it follows that

$$T_{int} = n\ (1- n^{P-1})\ k\ (N/n)^P \quad \text{and}$$

$$T_{ext,i} = T_i - T_{int/n} = kn^{P-1}\ (N/n)^P$$

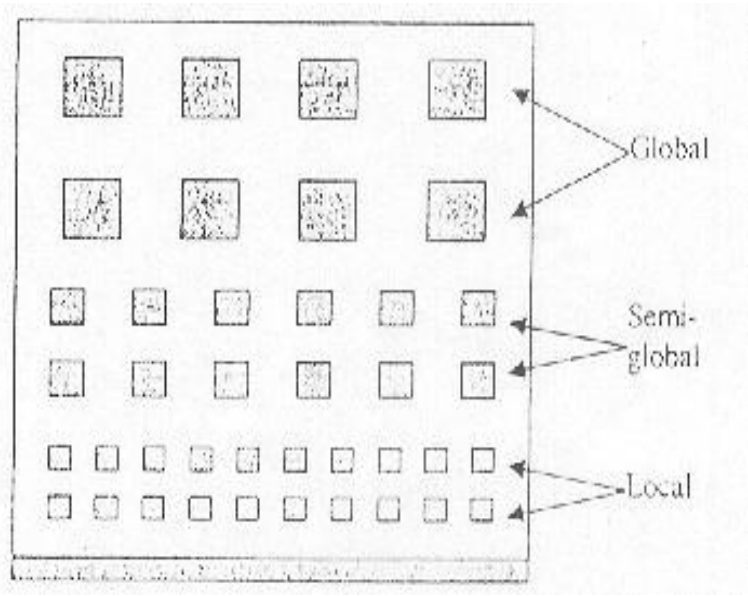
Here, $T_{ext,i}$, is the average of I/O ports per layer.

B) ESTIMATING 2-D AND 3-D CHIP AREA

In integrated circuits that are wire-pitch limited in size, the area require by the wiring network is assumed to be much greater than the area required by the logic gates. For the purpose of minimizing silicon real estate and signal propagation delays, the wiring network is segmented into separate tiers that are physically fabricated in multiple layers.

An interconnect tier is categorized by factors such as metal line pitch and cross-section, maximum allowable signal delay and communication mode (such as intra block, or inter block)[1]. A tier can have more than one layer of metal interconnects if necessary, and each tier or layer is connected to the rest of the wiring network and the logic gates by vertical vias. The tier closest to the logic devices (referred to as the **local tier**) is normally for short distance intra block communications.

Metal lines in this tier will normally be the shortest. They will also normally have the finest pitch. The tier furthest away from the device layer (referred to as **global tier**) is responsible for long distance across chip inter block communications, clocking and power distribution. Since this tier is populated by the longest of wires, the metal pitch is the largest to minimize signal propagation delays[4]. A typical modern IC interconnects architecture will define three wiring tiers: **local, semi-global, and global.** The semi-global tier is normally responsible for inter block communications across intermediate distances.



The area of the chip is determined by the total wiring requirement. IN terms of gate pitch, the total area required by the interconnect wiring can be expressed as

$$A_{required} = \sqrt{A_c}\,(P_{loc}L_{total\_loc}+P_{semi}L_{total\_semi}+P_{glob}L_{total\_glob})/N$$

Where,

A_c	Chip area ;
N	number of gates;
P_{loc}	local pitch;
P_{semi}	semi global pitch;
P_{global}	global pitch;
L_{total_loc}	total lengths of local interconnects;
L_{total_semi}	total length of semi global interconnects;
L_{total_glob}	total length of global interconnects;

The total interconnects length for any tier can be found by integrating the wire-length distribution within the boundaries that define the tier. Hence it follows that

$$L_{total\_loc} = X \int li\,(l)\,dl$$

$$L_{total\_semi} = X \int li\,(l)\,dl$$

$$L_{total\_glob} = X \int li\,(l)\,dl$$

Where X is a correction factor that converts the point –to – point interconnect length to wiring net length (using a linear net model, X=4/(f.o. + 3)

C) TWO ACTIVE LAYER 3-D CIRCUIT PERFORMANCE

This analysis is used to compare area and delay values for 2-D and 3-D ICs. The availability of addition of silicon layers gives the designer extra flexibility in trading off area with delay. A number of different cases are discussed as follows:

1. Chip area minimization with fixed interconnect delay

Here, VILICs are assumed to consume negligible area, interconnect line width is assumed to equal half the metal pitch at all times, and the total number of metal layers for 2-D and 3-D case was conserved. A key assumption for the geometrical construction of each tier of the multilevel interconnect network is that all cross sectional dimensions are equal within that tier.

As P_{semi} increase from its value at the minimum A_c the semi global and global pitches increase resulting in a larger wiring requirement and thus a larger A_c. Furthermore, as P_{semi} increases, even longer wires can now satisfy the maximum delay requirement in the semi global tier. These results in global wires to be rerouted to the semi global tier, which in turn will require greater chip area. Under such circumstances, the semi global tier begins to dominate and determine the chip area[3]. Conversely, as P_{semi} decreases from its value at the minimum A_c, the longer wires in the semi global tier no longer satisfy the maximum delay requirement of that tier and they need to be rerouted to the global tier where they can enjoy a larger pitch. The populations of wires in global tiers increases and since these wires have a large cross section they have a greater area requirement. Under such circumstances the global tier begins to dominate and determine the chip area.

The curve for the 3-D case has a minimum similar to the one obtained for the 2-Dcase.it can be observed that the minimum chip area for the 3-D case is about ≈30% smaller than that of the 2-D case. Moreover, since the total wiring requirement is reduced, the semi global tier pitch is reduced for the 3-Dchip. The significant reductions in chip area demonstrated by the 3-D results are a consequence of the fraction of wires that were converted from horizontal in 2-D to vertical VILICs in 3-D. it is assumed that the area required by VILICs is negligible.

These results demonstrate, with given assumptions, that a 3-D IC can operate at the same performance level, as measured by the longest wire delay, as its 2-D counterpart while using up about 30% less silicon real estate. However, it is possible for 3-D ICs to achieve greater performance than their 2-Dcounterparts by reducing the interconnect impedance at the price of increased chip area as discussed next.

2. Increasing Chip Area and Performance

3-D IC performance can be enhanced to exceed the performance of 2-D ICs by improving interconnect delay. This is achieved by increasing the wire pitch, which causes a reduction in the resistance. The effect of increasing p_{semi} and p_{global} on the operating frequency and A_c.

This illustrates how the optimum semi global pitch (i.e., the p_{semi} associated with the minimum A_c) increases to obtain higher operating frequencies[1]. Also, as the semi global tier pitch increases, chip area and, therefore, interconnect length also increases. However, we can see that the increase in chip area still remains well below the area required for the 2-D case. The figure also helps defines a maximum – performance 3-D chip – a chip with the same area as the corresponding 2-D chip, which can be obtained by increasing the semi global pitch beyond that for the 4-GHz case.

Two scenarios are considered 1) global pitch is increased to match the global pitch for the 2-d case and 2) global pitch is increased to match the chip area (footprint) for the 2-d case. Note that the delay requirements sets a maximum values of interconnect length are given tier. Therefore, as interconnect lengths are increased, lines which exceed this maximum length criterion for that particular tier need to be rerouted on upper ties.

Beyond the maximum performance point for the 3-d chip, the performance gain becomes increasingly smaller in comparison to the decrease in performance resulting from the increase in chip area or reconnect delay. Furthermore, as the semi global wires need to be rerouted on the global tiers, which eventually leads to overcrowding of the global tier . Any further increases in the wiring density in the global tier forces a reduction in the global pitch.

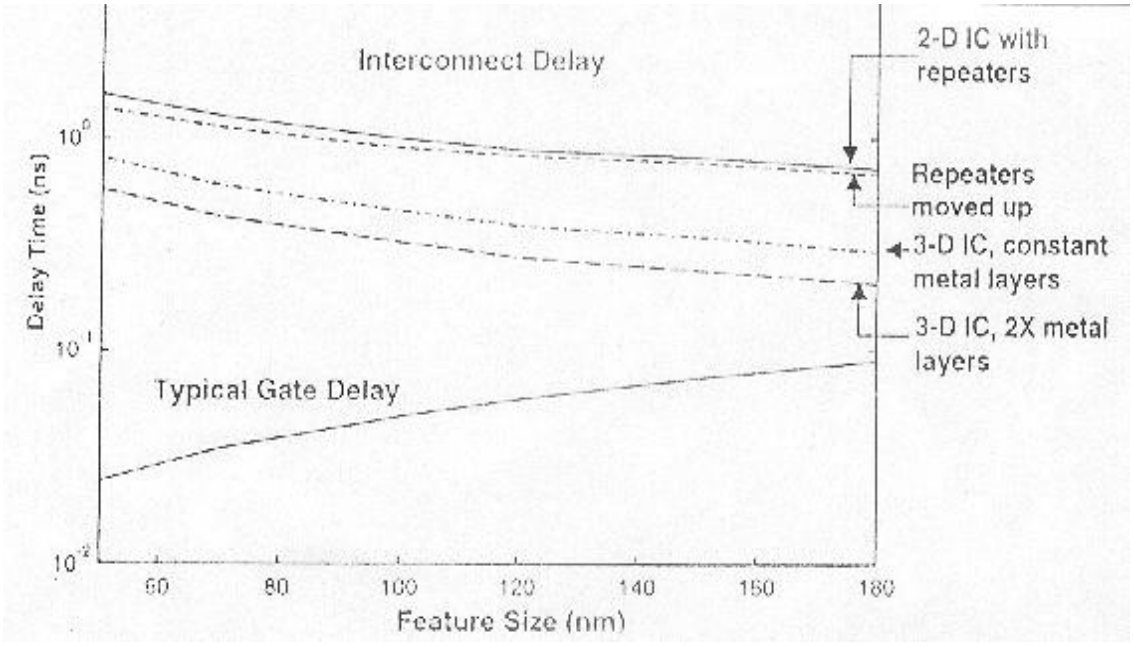
D) EFFECT OF INCREASING NUMBER OF SILICON LAYERS

As the number of silicon layers increases beyond two, the assumption that all interlayer interconnects (ILICs) are vertical and consume negligible area becomes less tenable. The area used up by these horizontal ILICs can be estimated from their total length and pitch.

The decrease in interconnect delay becomes progressively smaller as the numbers of active layers increase. This is due to the fact that the area required by ILICs begins to offset any area saving due to increasing the number of active layers.

E) EFFECT OF INCREASING THE NUMBER OF METAL LAYERS

It is likely that there are local and semi global tiers associated with every active layer, and a common global tier is used . This would result in an increase in the total number of metal layers for the 3-D case.[4] The effect of using 3-D case. The effect of using 3-D ICs with constant metal layers and the effect of employing twice the number of metal layers as in 2-D are summarized in the figure.



It can be observed that by using twice the number of metal layers the performance of the 3-D chip can be increased by an additional amount of 35% as compared to the 3-d chip with the same total number of metal layers as in 2-d . It can be observed that for the more aggressive technologies , the decrease in interconnect delay from 2-D to 3-D case is less impressive. This indicates that more than two active layers are possibly needed for those advanced nodes. The figure also shows the impact of moving only the repeaters to the second layer Si layer . It can also be observed that for more aggressive technologies , the decrease in interconnect delay from 2-D to 3-D case is less impressive This indicates that more than two active layers are possibly needed for those advanced nodes.

F.OPTIMIZATION OF INTERCONNECT DISTRIBUTION

In estimating chip area, the metal requirement is calculated from the obtained wire-length distribution. The total metallization requirement is appropriately divided among the available metal layers in the corresponding

technology . Thus each tier , the local , the semi global and the global has three metal layers . the resulting area of most densely packed tier determines the chip area.

Consequently, higher tier are routed within a larger than required area . An optimization for this scenario is possible by rerouting some of the local wires on the semi global tier and the latter on the global , without violating the maximum allowable Length (or delay) per tier[2]. This is achieved by reducing the maximum allowed interconnect length for the local and semi global tiers. Minimum chip area will achieved when all the tiers are equally congested. The 2-D chip area is seen to reduce by 9% as a result of this optimization is also applied to applied to 3-D ICs .

5.CHALLENGES FOR 3-D INTEGRATION

A) THERMAL ISSUES IN 3-D ICs

An extremely important issue in 3-D ICs is heat dissipation. Thermal effect s are already known to significantly impact interconnected /device reliability and performance in high-performance 2-D ICs. The problem is expected to be exacerbated by the reduction in chip size, assuming that same power generated in a 2-D chip will now be generated in a smaller 3-D chip, resulting in a sharp increase in the power and density Analysis of thermal problems in 3-D circuits is therefore necessary to comprehend the limitations of this technology and also to evaluate the thermal robustness of different 3-D technology and design options[2].

It is well known that most of the heat energy in integrated circuits arises due to transistor switching. This heat energy is typically conducted through the silicon substrate to the package and then to the ambient by a heat sink .With multi layer device designs, devices in the upper layer will also generate a significant fraction of the heat .Furthermore, all the active layers will be insulated from each other by layers of dielectrics (LTO, HSQ, polyamide, etc.) which typically have much lower thermal conductivity than Si .Hence ,the heat dissipation issue can become even more acute for 3-D ICs and can cause degradation in device performance ,and reduction in chip reliability due to increased junction leakage, electro migration failures ,and by accelerating other failure mechanisms.

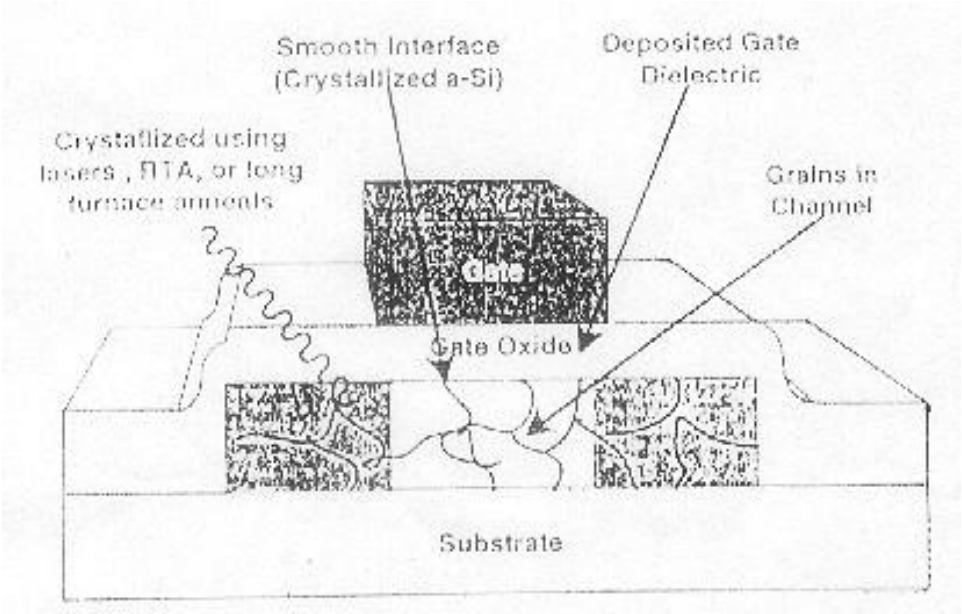
B) RELIABLITY ISSUES IN 3-D ICs

Three dimensional IC s will possibly introduce some new reliability problems. These reliability issues may arise due to the electro thermal and thermo mechanical effects between various active layers and the interfaces between the active layers, which can also influence existing IC reliability hazards such a electro migration and chip performance[1]. Additionally, heterogeneous integration of technologies using 3-d architecture will increase the need to understand mechanical and thermal behavior of new material of new material interfaces and thin film material thermal and mechanical properties.

6. OVERVIEW OF 3-D IC TECHNOLOGY

1) BEAM RECRYSTALIZATION

A very popular method of fabricating a second active layer (Si) on top of an existing substrate (oxidized Si wafer)is to deposit polysilicon and fabricate thin film transistors (TFT). To enhance the performance of such transistors ,an intense laser or electron beam is used to induce recrystalisation of the polysilicon film to reduce or even eliminate most of the grain boundaries.



Advantage

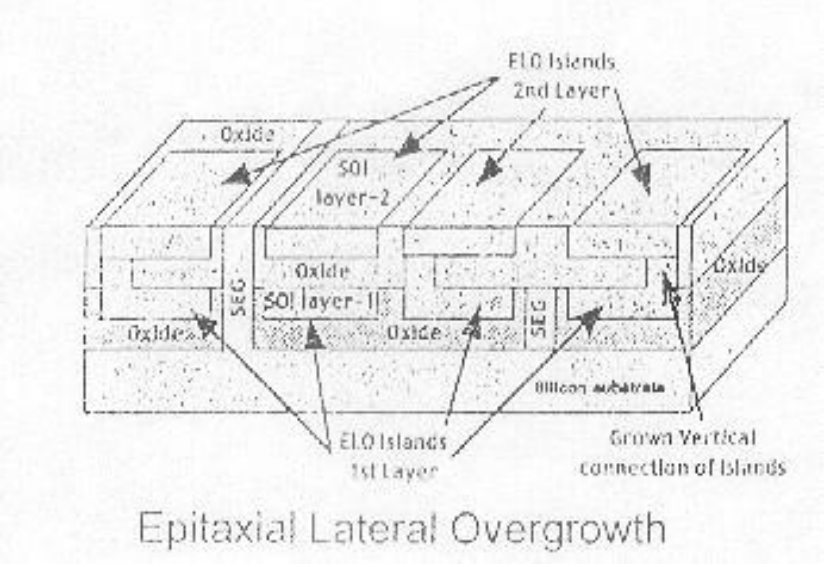
1. MOS on transistors fabricated on polysilicon exhibit very low surface mobility values [of the order of 10 cm/Vs].
2. MOS transistors fabricated on polysilicon have high threshold voltages (several volts) due to the high density of surface states (several 10 cm) present at the grain boundaries.

Disadvantage

1. This technique, however, may not be very practical for 3-D devices because of the high temperature involved during melting of the polysilicon.
2. Difficulty in controlling the grain size variations.

2) SILICON EPITAXIAL GROWTH

Another technique for forming additional Si layers is to etch a hole in a passivated wafer and epitaxially grow a single crystal Si seeded from open window in the ILD. The Si crystal grows vertically and then laterally to cover the ILD.



Epitaxial Lateral Overgrowth

Advantage:

1. The quality of devices fabricated on these epitaxial layer can be as good as those fabricated underneath on the seed wafer surface, since the grown layer is single crystal with few defects.

Disadvantage

1. The high temperatures involved in this process cause significant degradation in the quality of devices on lower layers.

2. PROCESSED WAFER BONDING:

An attractive alternative is to bond two fully processed wafers on which devices are fabricated on the surface ,including some interconnects, such that the wafers completely overlap.Interchip vias are etched to electrically connect both wafers after metallization and prior to the bonding process at 400 degree Celsius. For applications where each chip is required to perform independent processing before communicating with it's neighbor , this technology can prove attractive [3].

Advantage

1. Devices on all active levels have similar electrical properties.
2. Since all chips can be fabricated separately and later bonded ,there is independence of processing temperature.

Disadvantage

1. The lack of precision restricts the interchip communication to global metal lines.

3. SOLID PHASE CRYSTALLIZATION (SPC)

In this technique, a layer of amorphous Si is crystallized on top of the lower active layer devices. The amorphous film is randomly crystallized to form a polysilicon film[1]. Device performance can be enhanced by eliminating the grain boundaries in the polysilicon film. For this purpose ,local crystallization

can be induced using low temperatures processes (<600C) such as using patterned seeding of germanium . In this method, Ge seeds implanted in narrow patterns made on amorphous Si can be used to included lateral crystallization. This results in the formation of small islands, which are nearly single crystal. CMOS transistors can then be fabricated within these islands to give SOI like performance.

Advantages

1. This technique offers flexibility of creating multiple active layers
2. This is a low temperature technique

B) VERTICAL INTERLAYER INTERCONNECT TECHNOLOGY OPTIONS

There is direct relation between improved chip performance and increased utility of VILICs. It is therefore important to understand how to connect different active layers with a reliable and compatible process. Upper layer processing needs to be compatible with metal lines underneath connecting lower layer devices and metal layers. With Cu technologies, this limits the processing temperatures to <450 c for upper layers. Otherwise , Cu diffusion through barrier layers , and the reliability and thermal stability of material interfaces can degrade significantly. Tungsten is a refractory metal that can be used to withstand higher processing temperatures, but it has higher resistivity. Current via technology can also be employed to achieve VILIC functionality. The underlying assumption here requires that interlayer gates are interconnected using regular horizontal metal wires and vias, while interlayer interconnects can be VILICs connecting the wiring network for each layer.

Recently, interlayer (VLIC)metallization schemes for 3-d ICs have been demonstrated using direct wafer bonding. These techniques are based on the bonding of two wafers with their active layers connected through vias ,which serve as VILICs[3] .

One method is based on the bonding of a thinned top wafer to a bottom wafer with a organic adhesive layer of polyamide in between.

Interchip vias are etched through the ILD(inter level dielectric),the thinned top silicon wafer and through the cured adhesive layer ,with an approx depth of 20 μm prior to the bonding process .the interconnect chip via made of chemical wafer depositor (CVD)[3]. Tin liner and CVD-W plug provides a vertical interconnect (VILIC)between the upper most metallization levels of both layers . the bonding between the two wafers is done using a flip-chip bonder with split beam optics at a temperature of 400 degree Celsius

A second technique realizes on the **thermo compression** bonding between the metal parts in each wafer.

In this method, Cu-Ta pads on both wafers save as electrical contacts between the interchips via on the top thinned silicon wafer and the upper most interconnects on the bottom silicon wafer. The Cu-Ta pads can also function as small bond pads for wafer bonding. Additionally, dummy metal patterns can be made to increase the surface area for wafer bonding. The Cu-Ta bilayer pads with a combined thickness of 700 nm are fused together by applying a compressive force at 400 degree Celsius. This technique offers the advantage of a metal –metal interface that will lower the interface thermal resistance between the two wafers (and, hence, provide better conduction) and can be beneficial as a partial ground plane for lowering the electromagnetic effects.

7. PRESENT SCENARIO OF THE 3-D IC INDUSTRY

Many companies are working on the 3-D chips ,including groups at Massachusetts institute of technology (MIT),international business machines(IBM). Rensselar Polytechnic and SUNY Albany are also doing research on techniques for bonding conventional chips together to form multiple layers .whichever approach ultimately wins ,the multilayer chip building technology opens up a whole new world of design .

However ,the Santa Clara, California US based startup company matrix semiconductor will bring the first multilayer chip to the market ,while matrix's techniques will not likely result in more computing power ,they will produce cheaper chips for certain applications, like memory used in digital cameras , personal digital assistants ,cellular phones ,hand held gaming devices ,etc .matrix has adapted the technology developed for making flat –panel liquid crystal displays to build chips with multilayer of circuitry.

The company's first products will be memory chips called 3-Dmemory, for consumer electronics like digital cameras and audio players. current flash memory cards for such devices are rewritable but expensive .however the newly produced chips will cost ten times less, about as much as an audio tape or a roll of film, but will only record information once. The cost is so largely because the stacked chips contain the same amount of circuitry as flash cards but use a much smaller area of the extremely expensive silicon wafers that form the basis for all silicon chips. The chips will also offer a permanent record of the images and sounds users record. The amount of computing power the company can ultimately build in to its chips could be limited .the company hopes to eventually build chips for cell phones, or low performance micro processors like those found in appliances; such chips would be about one tenth as expensive as current ones[4].

The patent technology opens up the ability to build ICs in three dimensions- “up” as well as “out” in the horizontal directions as in the case now with conventional chip designs. The result is a ten fold increase in the potential no of bits on a silicon die, according to the company .moreover, the 3-D circuits can be produced with todays standard semiconductor materials, fab equipments and processors the 3-D memory will be used in memory devices which will be marketed under well known brand names for portable electronics devices, including digital cameras digital audio players, games, PDAs and archival digital storage .the 3-D memory can also be used for pre recorded content such as music, electronics books, digital maps, games, and reference guides.

8. ADVANTAGES OF 3-D MEMORY

Disks are inexpensive, but they requires drives that are expensive bulky ,fragile and consume a lot of battery power . Accidentally dropping a drive or scratching a disk can cause significant damage and the potential loss of valuable pictures and data. Flash and other non volatile memories are much more rugged, battery efficient compact and require no bulky drive technologies . Dropping them is not a problem they are however much more expensive. Both require the use of a pc.

The ideal solution is a 3-D memory that leverages all the benefits of non volatile media, costs as little as a disk, and is as convenient as 35 mm film and audio tape.

9. APPLICATIONS

Portable electronic digital cameras, digital audio players, PDAs, smart cellular phones, and handheld gaming devices are among the fastest growing technology market for both business and consumers. To date, one of the largest constraints to growth has been affordable storage, creating the marketing opportunity for ultra low cost internal and external memory. These applications share characters beyond rapid market growth.

Portable devices all require small form factors ,battery efficiency, robustness, and reliability. Both the devices and consumable media are extremely price sensitive with high volumes coming only with the ability to hit low price points. Device designers often trade application richness to meet tight cost targets. Existing mask ROM and NAND flash non volatile technology force designers and product planners to make the difficult choice between low cost or field programmability and flexibility. Consumers value the convenience and ease of views of readily available low cost storage. The potential to dramatically lower the cost of digital storage weapons many more markets than those listed above. Manufacturers of memory driven devices can now reach price points previously inaccessible and develop richer, easier to use products.

10. FUTURE OF THE 3-D IC INDUSTRY

Matrix is working with partners including Microsoft Corp, Thomas Multimedia, Eastman Kodak and Sony Corp. three product categories are planned: bland memory cards: cards sold preloaded with content, such as software or music ; and standard memory packages, for using embedded applications such as PDAs and set-top boxes .

Thomson electronics, the European electronic giant, will begin to incorporate 3-D memory chips from matrix semiconductor in portable storage cards, a strong endorsement for the chip start –up.

Thomson multimedia will incorporate the 3-D memory in memory cards that cane be used to store digital photos or music. Although the cards plug into cameras Thomson is also working on card readers that will allow consumers to view digital photos on a television. The Thomson /matrix cards price makes the difference from completing flash cards from Sony and Toshiba .the 64 MB Thomson card will cost about as much as camera film does today. to further strengthen the relationship with film ,the cards will be sold under the name Technicolor Digital Memory Card.

Similar flash memory cards from other companies cost around Rs.1900 or more-though consumers can erase and rerecord data on them, unlike the matrix cards. As a result of their price, consumers buy very few of them. Thomson, by contrast , expects to market its write-once cards in retail outlet such as Wal-Mart.

The first Technicolor cards will offer 64 MB of memory; version with 128 MB and 192 MB will appear later. The first 3-D chips will contain 64 MB. Taiwan Semiconductor Manufacturing Co. is producing the chips on behalf of matrix.

11. CONCLUSION

The 3 D memory will just the first of a new generation of dense, inexpensive chips that promise to make digital recording media both cheap and convenient enough to replace the photographic film and audio tape. We can understand that 3-D ICs are an attractive chip architecture, that can alleviate the interconnect related problems such as delay and power dissipation and can also facilitate integration of heterogeneous technologies in one chip. The multilayer chip building technology opens up a whole new world of design like a city skyline transformed by skyscrapers, the world of chips may never look at the same again.

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