Design and Analysis of CMOS Based DADDA Multiplier

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Abstract

Multiplier is an important circuit used in electronic industry especially in digital signal processing operations such as filtering, convolution and analysis of frequency. There are different types of algorithms used in multipliers to achieve better performance. Array multiplier and Wallace tree multiplier are such types of multipliers constructed by using CMOS logic styles such as Swing Restored complementary Pass-transistor Logic (SR-CPL) and Dual Pass-Transistor (DPL). SR-CPL is constructed by using n-MOS transistor that is derived from Complementary Pass Logic (CPL) logic which is traditionally applied to the arithmetic building block and it offers high speed. DPL is constructed by using both n-MOS and p-MOS which has more number of transistors compared to that of SR-CPL. But high robustness is achieved through DPL. However Wallace multiplier offers higher power consumption. Hence, DADDA multiplier is designed by using ripple carry and carry save adder method with the above mentioned two logic styles. The simulation is done by using TANNER EDA tool.

Keywords: *logic family, adder, multiplier*

1. Introduction

Multiplication is one of the arithmetic operations performed by multiplier in the various analog and digital circuits. The speed and power dissipation are the important parameters which should be taken into consideration in digital circuits. In order to achieve energy efficient and low power VLSI (Very Large Scale Integration) circuits, different multiplication algorithm will be used to illustrate methods of designing different cells. Binary multiplication can be achieved by several approaches. A combinational circuits of tree multiplier, with a one-sided reduction tree and a ripple-carry adder as the final stage is called an array multiplier [1]. More number of additions can be performed by chained with previous output but it has worst case delay. Hence speed is reduced. Then, the fastest Wallace tree multiplier has been introduced for minimum propagation delay. However, the Wallace multiplier has complex layout.

Hence an attempt has been made to develop DADDA multiplier which is designed by using 1-bit full adders with Carry Save Adder (CSA). The rest of the paper is organized as follows: Section 2 deals with the design flow of Wallace tree multiplier. In section 3, the algorithm of DADDA multiplier is discussed. Section 4 emphasizes on the simulation results and discussion. Conclusion is drawn in Section 5.

2. Wallace Tree Multiplier

C.S Wallace has suggested the fastest multiplier in 1964. Wallace is a tree of CSA designed for minimum propagation delay. It is implemented by adders [2] using parallel multiplication resulting in less delay. Carry save adder method is used in order to reduce the number of stages. Wallace tree sums up same weight of three bits and produces output which is said to be compressors.
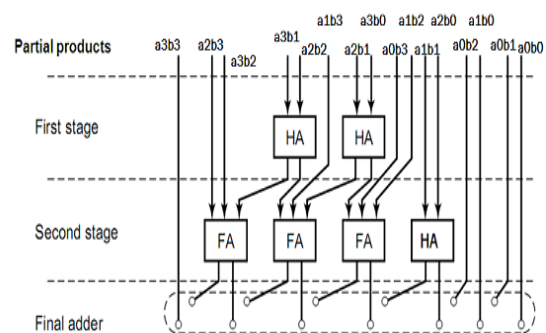

Figure 1: Wallace tree multiplier design flow

In previous researches, the energy efficient multiplier circuits are implemented using various logic styles and for the best results, the half adder is replaced with full order for unique design [3]. The existing model of Wallace tree multiplier is designed by using full adder with SR-CPL and DPL logic styles

The design flow of Wallace Tree multiplier is shown in Fig.1.Wallace method [4] uses three-steps to process the multiplication operation. They are

- Formation of bit products
- Combine all product matrixes to form 2 vectors (carry and sum) outputs in first row using conventional adder.
- The remaining two rows are summed using a fast carry-propagate adder to produce the product.

3. DADDA Multiplier

Luigi Dadda, the computer scientist has invented the DADDA hardware multiplier during 1965. DADDA multiplier is extracted form of parallel multiplier [5]. It is slightly faster and requires fewer gates. Different types of schemes are used in parallel multiplier. The DADDA scheme is one of the parallel multiplier schemes that essentially minimize the number of adder stages required to perform the summation of partial products. This is achieved by using full and half adders to reduce the number of rows in the matrix number of bits at each summation stage. Even though the DADDA multiplication has regular and less complex structure, the process is slower in manner due to serial multiplication process. Further, DADDA multiplier is less expensive compared to that of Wallace tree multiplier. Hence, in this paper, DADDA multiplier is designed and analysed by considering different methods using full adders involving different logic styles.

3.1 Algorithm of DADDA Multiplier

The algorithm of DADDA multiplier is based on the below matrix form shown in Fig.2. The partial product matrix is formed in the first stage by AND stages which is illustrated in Fig. 3.
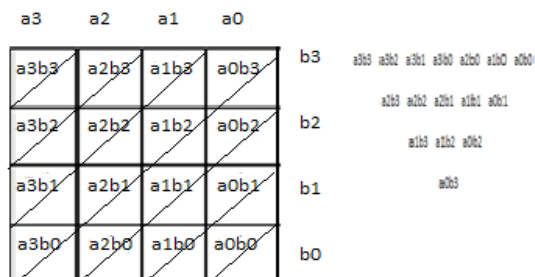

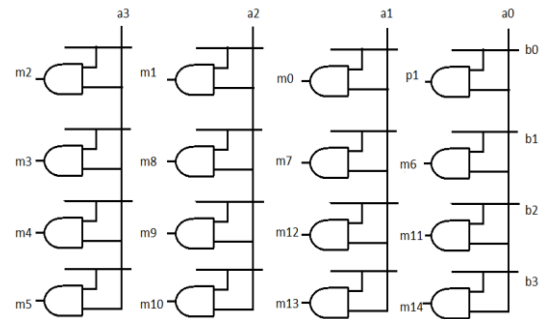
Figure 2: 4x4Dadda Algorithm

Figure 3: Product terms generated by a collection of AND gates

Steps involved in DADDA multipliers Algorithm:

- Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding N results. Depending on position of the multiplied bits, the wires carry different weights.
- Reduce the number of partial products to two layers of full adders.
- Group the wires in two numbers, and add them with a conventional adder.

3.2 Logic Styles

There are different CMOS logic techniques which are implemented in 1-bit full adder [6] for the design of multiplier in order to achieve better performance such as low power [7] and delay with high performance complementary pass transistor logic [8].

3.2.1 SR-CPL

Swing restored complementary pass transistor full adder [9] consists of cross coupled n-MOSFET and restoration circuit in p-MOSFET at the output with full swing operations.
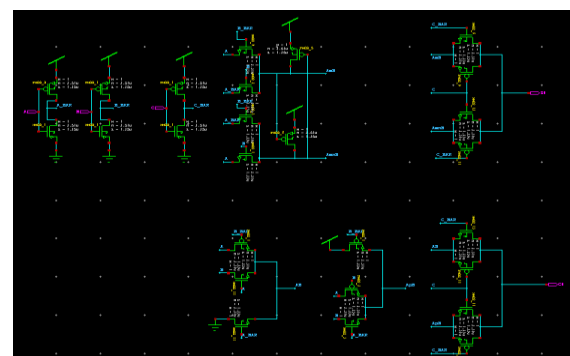

Figure 4: SR-CPL Full adder

Any required Boolean logic function can be implemented by swing restore dual rail form of pass transistor logic [10] using latch. It has less number of transistors. The SR-CPL full adder circuit is shown in Fig.4.

3.2.2. DPL

The full adder using dual pass transistor logic [11] consists of p-MOSFET transistor and n-MOSFET transistors with full swing operations. It is based on dual rail pass transistor logic. No restoration circuit is needed in DPL. And also the speed degradation occurs in SR-CPL due to low supply voltage level which is avoided in DPL.
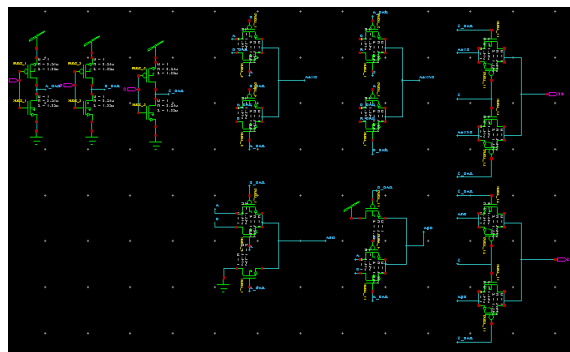

Figure 5: DPL Full adder

3.3 DADDA Multiplier Using Ripple Carry Adder

Ripple Carry Adder is the method used to add more number of additions to be performed with the carry in $_s$ and carry out$_s$ that is to be chained. Thus multiple adders are used in ripple carry adder. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.
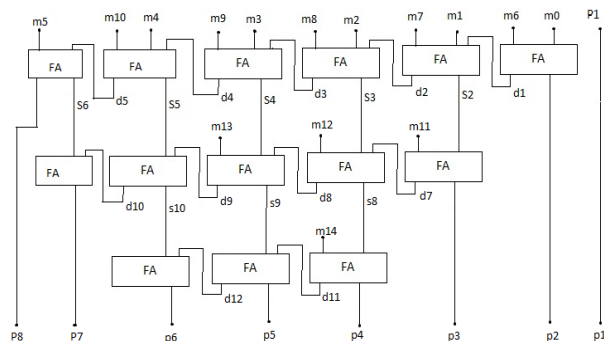

Figure 6: 4x4 DADDA Multiplier using RCA

Full adder in DADDA multiplier is designed using SR-PL and DPL logic family for better performance. The proposed architecture of DADDA multiplier algorithm using RCA is shown in Fig.6. Steps involved in 4x4 DADDA multiplier using RCA are discussed below.

Take any 3 wires with the same weights and give them as input into a full adder. The result will be an output wire of the same weight.

- Partial product obtained after multiplication is taken at the first stage. The data's are taken with 3 wires and added using adders and the carry of each stage is added with next two data's in the same stage.
- Partial products reduced to two layers of full adders with same procedure.
- At the final stage, same method of ripple carry adder method is performed and thus product terms p1 to p8 is obtained.

3.4 DADDA Multiplier using Carry Save Adder

Carry save adder is the technique used to add more number of additions to be performed with the carry in$_s$ and carry out$_s$ parallel after generating the partial products, grouped three rows as stage1 and perform addition using carry save method. The proposed architecture of 4x4 bit DADDA multiplier algorithm using CSA is illustrated in Fig: 7.
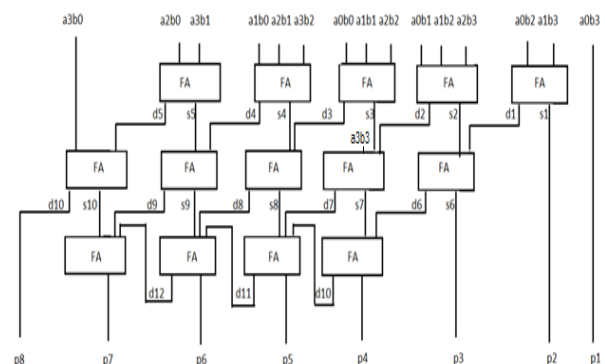

Figure 7: 4x4 DADDA Multiplier using CSA

Steps involved in 4x4 DADDA multiplier using CSA are discussed below

Take any 3 wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each 3 input wires.

- Partial product obtained after multiplication is taken at the first stage. The data's are taken with 3 wires and added using full adders and the carry of each stage is saved and send to the next stage
- In the second step, the partial products are added with previous stage outputs.
- At the final stage, the fast adding method namely ripple carry adder [12] is used to reduce the number of stage thus product terms p1 to p8 is performed.

4. Simulation results and Discussion

Full adder is designed by using DPL and SR-CPL logic style. The performance of the adder is analyzed. Then 4X4 bit Wallace tree and DADDA multiplier are also designed by using CSA and RCA method with the consideration of the DPL and SR-CPL logic style. The performance of above mentioned multipliers is also analyzed. The simulation of adders and multipliers is done by using TANNER EDA Tool.

The timing waveform of full adder designed using DPL and SR-CPL style is shown in Fig. 8. The schematic view of Wallace tree multiplier using Full adder is illustrated in Fig.9.
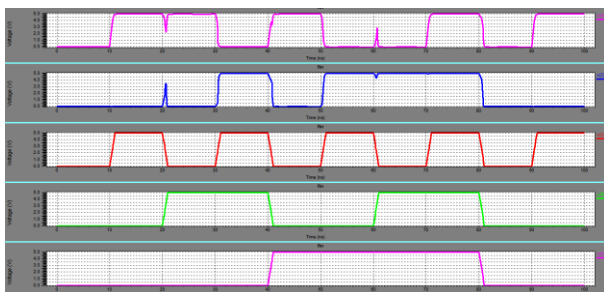

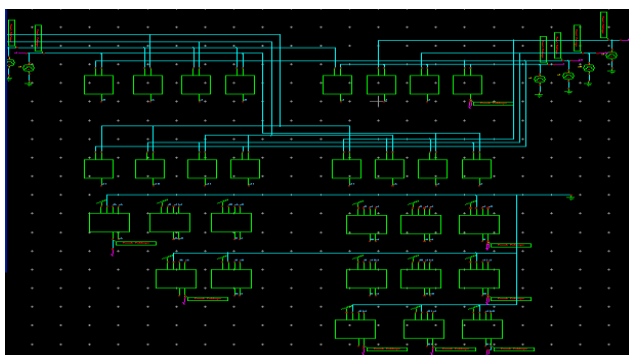Figure 8: Simulation waveform of full adder

Figure 9: Schematic view of Wallace tree multiplier

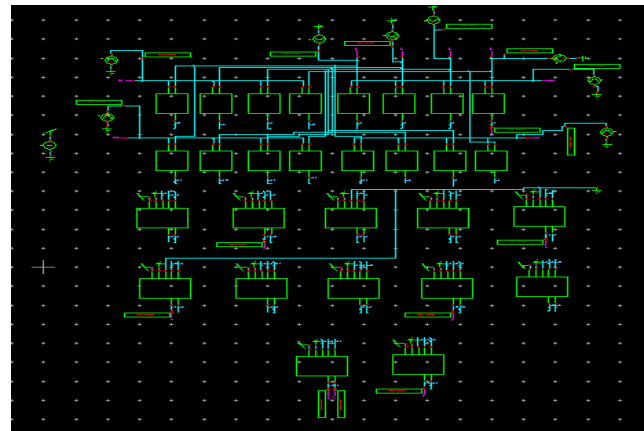DADDA multiplier architecture with SR-CPL logic style is shown in Fig 10

Figure 10: Schematic view of DADDA multiplier with SR-CPL style

DADDA multiplier architecture with DPL logic style is shown in Fig. 11.
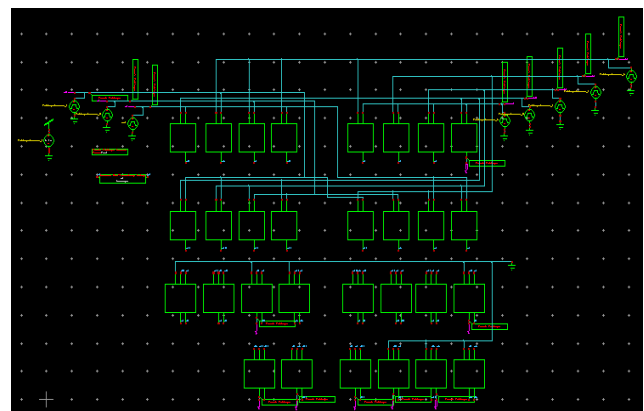

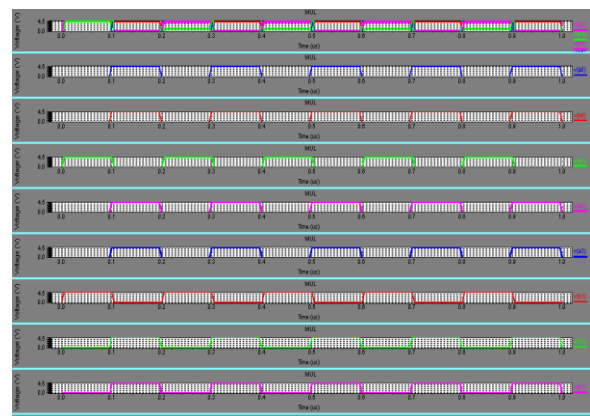Fig 11: Schematic view of DADDA multiplier with DPL style

Fig 12: Simulation waveform of WALLACE and DADDA Multiplier

The timing waveform of Wallace and DADDA multiplier is shown in Fig.12.

Table .1: Comparison Results of Full Adder

Logic family	Transistors	Delay(ns)	Average power(µw)
SR-CPL	26	0.25	321
DPL	28	0.12	361

The performance comparison of full adder circuit using SR-CPL and DPL logical styles are given in Table 1.

Table.2 Comparison Results of Multipliers

PARAM ETERS	WALLACE TREE MULTIPLIER		DADDA MULTIPLIER			
	DPL	SR-CPL	DPL	SR-CPL	DPL	SR-CPL
			CSA		RCA	
DELAY(ns)	0.86	1.12	1.25	1.13	1.85	1.32
POWER(mw)	4.94	5.10	1.85	6.65	2.93	4.67

The comparative performance analysis of Wallace tree and DADDA multiplier is shown in Table 2. It is observed through the Table 2, that the DADDA multiplier achieves better power compared to that of Wallace tree multiplier.

5. Conclusions

In microprocessors, multiplication operation is performed in a variety of forms in hardware and Software using multipliers. Reduction of power in multiplication operation is of great importance in digital signal processors. Hence low power DADDA multiplier is designed by using full adders' circuits involving different logic styles. The DADDA multiplier is simulated by using TANNER EDA tool. Then the performance parameters of multiplier are determined and analysed. It is verified through the parameter analysis that DADDA multiplier using both logical styles has better performance in terms of power than that of Wallace tree multiplier. However optimal delay is achieved through DADDA multiplier.

References

[1] Navdeep Goel and LalitGarg, "Comparative Analysis of 4-bit CMOS Multipliers", *Proceedings of International Conference on VLSI, Communication & Instrumentation*, pp. 33 – 37, 2011.

[2] R.Uma, Vidya Vijayan , M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", *International Journal of VLSI design & Communication Systems*, vol.3, No.1,pp.153-168, February 2012.

[3] C. Jaya Kumar and R. Saravanan "VLSI Design for Low Power Multiplier using Full Adder*", European Journal of Scientific Research,* vol.72, no.1, pp. 5-16, March 2012.

[4] C.S.Wallace, "A suggestion for a fast multiplier", *IEEE Transactions on Electronic Computers, vol.13,* pp.14-17, *February 1964*.

[5] K. C. Bickerstaff, M. Schulte and E. E. Swartzlander Jr., "Parallel reduced area multipliers," *Journal of VLSI Signal Processing Systems*, vol. 9, no. 3, pp. 181–191, April 1995.

[6] A. M. Shams and M. Bayoumi, "Performance evaluation of 1- bit CMOS adder cells," *Proceedings of IEEE International Symposium Circuits and Systems*, Orlando, FL, vol. 1, pp. 27–30, May 1999.

[7] K.Venkata Siva Reddy, C.Venkataiah, " Design of Adder in Multiple Logic Styles for Low Power VLSI", *International Journal of Computer Trends and Technology,* vol. 3, no.3, pp.476-481, 2012.

[8] Lixin Gao," High Performance Complementary Pass Transistor Logic Full Adder", *Proceedings of International Conference on Electronic & Mechanical Engineering and Information Technology*, Harbin, China pp-4306-4309, August 2011.

[9] Mariano Aguirre-Hernandez and Monico Linares-Aranda "CMOS Full-Adders for Energy-Efficient Arithmetic Applications*", IEEE transactions on VLSI systems,* vol. 19, no. 4, pp. 718-721, April 2011.

[10] C. Senthilpari ,K. Diwakar, A.Arokiaswamy, S.Kavitha, Ajay Kumar Singh, "An Efficient 16-bit Non-Clocked Pass Gates Adder Circuit with Improved Performance on Power Constraint", *European Journal of Scientific Research*, vol.28, no.3, pp.451-461, 2009.
.

[11] Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic

Applications", *IEEE transactions on VLSI systems*, vol. 19, no. 4, April 2011.

[12] Parhami, B., "Computer Arithmetic – Algorithms and Hardware Designs", Oxford University Press, 2000.

[13] Dilip I. Thakor, Pankaj P. Prajapati, "A 11.8MW Low Noise Amplifiler for 3-8 GHz Wideband application", IJCEM, vol. 15 issue 2, March 2012.

Biography

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