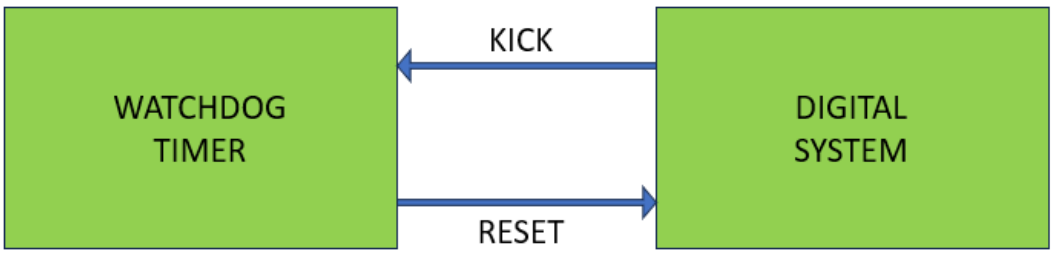
DESIGN AND SIMULATION OF A SIMPLE WATCHDOG TIMER USING VERILOG

A Verilog-Based Implementation of a Simple Watchdog Timer for Fault Detection, System Recovery, and Robust Digital Design



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WATCHDOG TIMER

A Watchdog Timer (WDT) is a safety feature used in digital and embedded systems to improve reliability. It works like a guardian for the system. The system must regularly send a signal, called a kick or refresh, to the WDT. If this signal is missed within the set time limit, the WDT assumes the system is stuck or has failed. In response, it forces a reset, bringing the system back to a safe, working state.

Watchdog Timers are important because digital systems can sometimes freeze due to software bugs, hardware faults, or unexpected external conditions. Without a WDT, such systems may remain locked until someone manually restarts them. With a WDT, the recovery is automatic, ensuring the system is always available.

APPLICATIONS

Home Appliances – In washing machines and microwave ovens, a WDT ensures the program doesn't get stuck in the middle of a cycle.

Printers & Scanners – Makes sure a print job doesn't lock up the device; if it does, the WDT resets the controller.

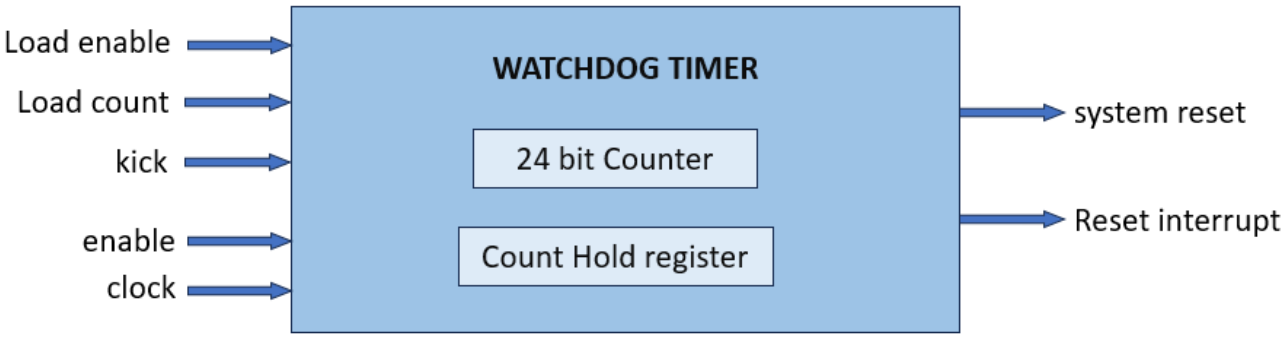
Security Systems (CCTV) – Resets the system automatically if the recording or monitoring software hangs.

Consumer Electronics - Used in devices like TVs, set-top boxes, and smart appliances to recover from software crashes automatically.

Communication Equipment - Maintains network routers, modems, and IoT devices in operational condition by resetting them when they stop responding.

Vehicles - Used in dashboard systems and infotainment units to ensure they remain responsive.

SCHEMATIC



SIGNALS

INPUTS:

Signal	Width	Purpose
clk	1-bit	System clock. The counter updates on every rising edge.
en	1-bit	Enable signal for the WDT. If low, the WDT does not count.
kick	1-bit	Refresh signal. When high, it reloads the counter to prevent system reset.
ld_en	1-bit	Load enable. When high, it loads a new counter value from ld_cnt.
ld_cnt	24-bit	Load value for the counter. Sets the timeout duration for the WDT.

OUTPUTS:

Signal	Width	Purpose
rst_sys	1-bit	System reset signal. Asserted when the WDT times out (counter reaches zero).
rst_int	1-bit	Interrupt signal. Asserted shortly before the system reset (when counter = 3).

INTERNAL REGISTERS

Register	Width	Purpose
counter	24-bit	Main countdown counter of the WDT. Counts down every clock cycle when enabled.
cnt_hld	24-bit	Holds the reload value of the counter. Used when kick or ld_en occurs to reset the counter.

VERILOG CODE

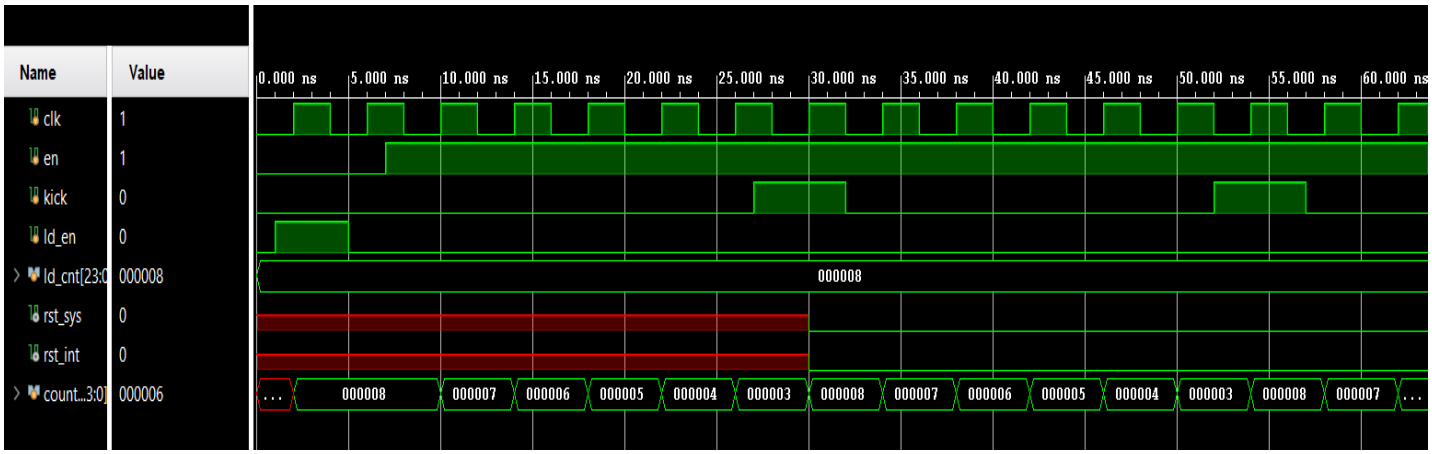
```
`timescale 1ns / 1ps

module WDT(clk,en,kick,rst_sys,ld_cnt,ld_en,rst_int);
input clk,en,kick,ld_en;
input [23:0]ld_cnt;
output reg rst_sys,rst_int;

reg [23:0]counter,cnt_hld;

always@(posedge clk)
begin
    if(en) begin

        if(kick) begin
            counter <= cnt_hld;
            rst_sys <= 0;
            rst_int <= 0;
        end
        else if(counter==3) begin
            rst_int <= 1;
            counter <= counter-1;

        end
        else if(counter==0) begin
            rst_sys <= 1;
            counter <= cnt_hld;
        end
        else begin
            counter <= (counter>0) ? (counter-1) : 0 ;
        end
     end
     if(rst_sys || rst_int) begin
            rst_sys <= 0;
            rst_int <= 0;
        end
     if (ld_en) begin
        cnt_hld <= ld_cnt;
        counter <= ld_cnt;
    end

end
endmodule
```

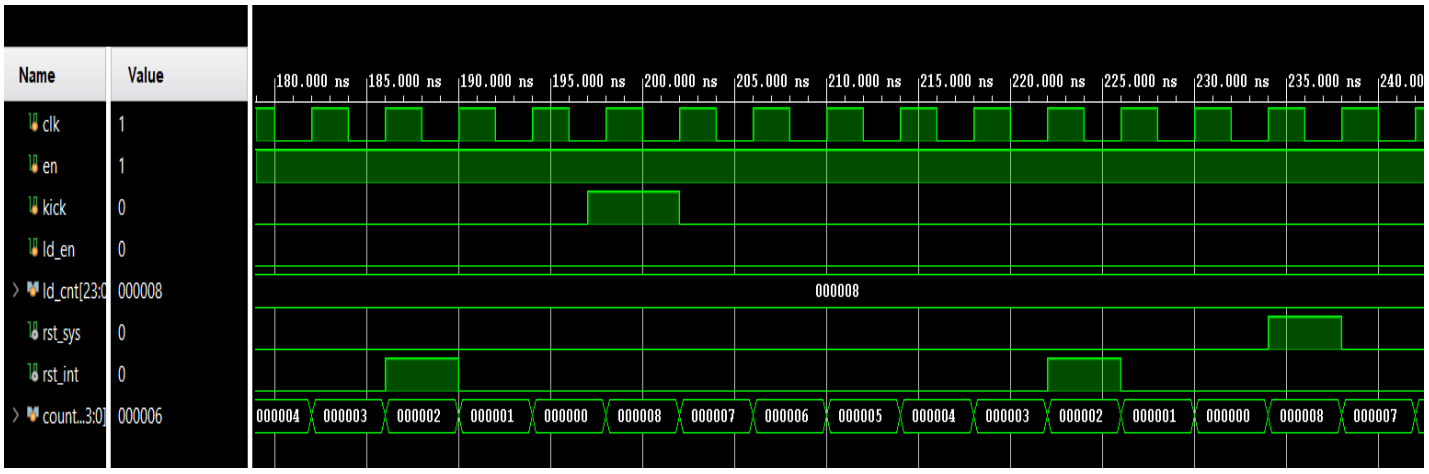
VERILOG TESTBENCH

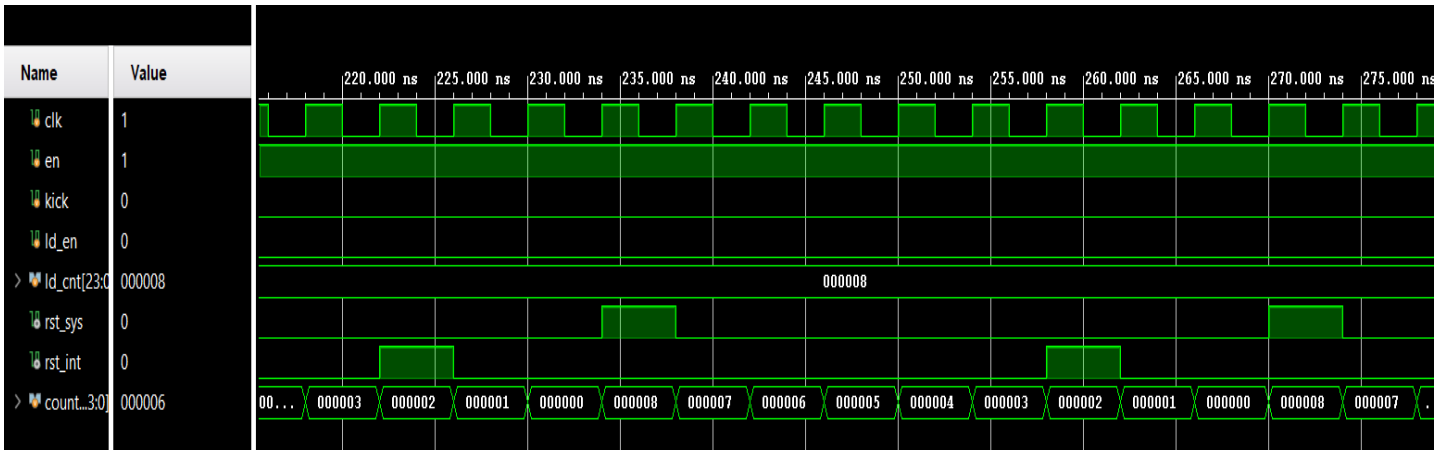
```
`timescale 1ns / 1ps
module tb_WDT;
reg clk;
reg en;
reg kick;
reg ld_en;
reg [23:0] ld_cnt;
wire rst_sys;
wire rst_int;
WDT uut (.clk(clk),.en(en),.kick(kick),.ld_cnt(ld_cnt), .ld_en(ld_en),.rst_sys(rst_sys),.rst_int(rst_int) );
always #2 clk = ~clk;
initial begin
    clk = 0;
    en = 0;
    kick = 0;
    ld_en = 0;
    ld_cnt = 24'd8;
    #1 ld_en = 1;
    #4 ld_en = 0;
    #2 en = 1;
    #20;
    kick = 1;
    #5 kick = 0;
    #20;
    kick = 1;
    #5 kick = 0;
    #140 kick =1;
    #5 kick=0;
    #150 $finish;
end
endmodule
```

SIMULATION RESULTS

- Counter loaded for 8 counts.
- Tested by providing Kick signal.
- Tested without input Kick signal.







RTL SCHEMATIC

- Tool used: Vivado