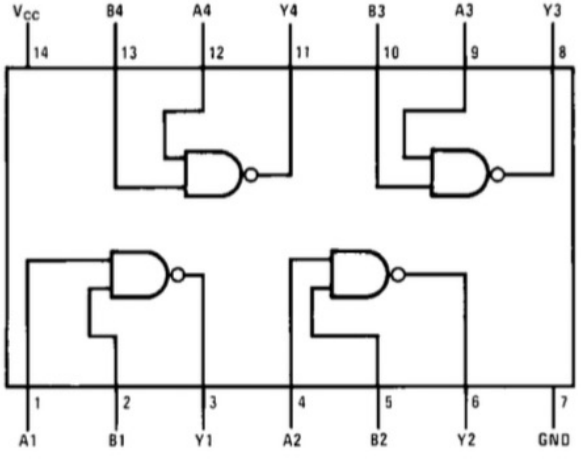
DM74LS03
Quad 2-Input NAND Gates with Open-Collector Outputs

Connection Diagram



Function Table

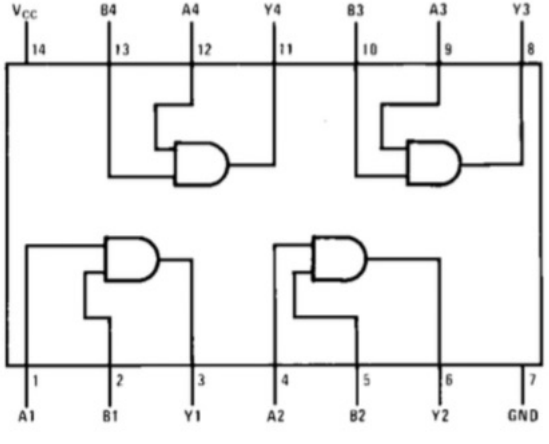
$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

DM74LS09
Quad 2-Input AND Gates with Open-Collector Outputs

Connection Diagram



Function Table

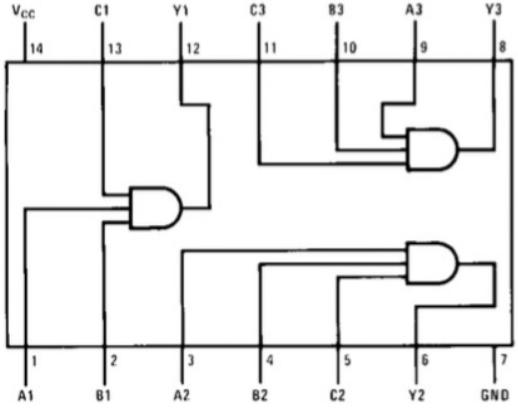
$$Y = AB$$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

DM74LS11
Triple 3-Input AND Gate

Connection Diagram



Function Table

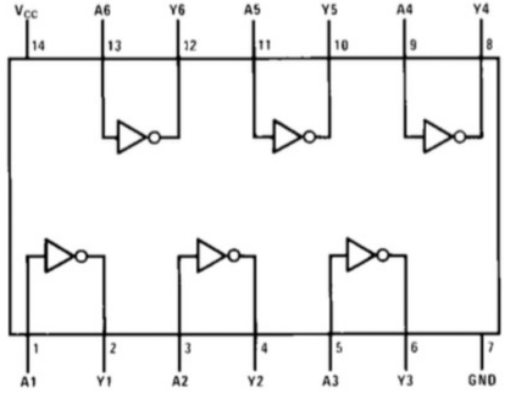
$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

DM74LS05
Hex Inverters with Open-Collector Outputs

Connection Diagram



Function Table

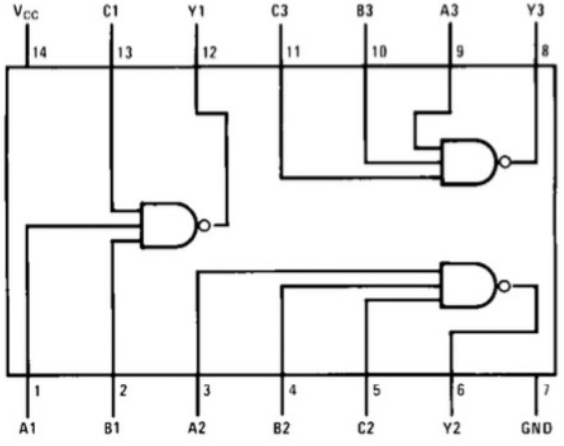
$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

DM74LS10
Triple 3-Input NAND Gate

Connection Diagram



Function Table

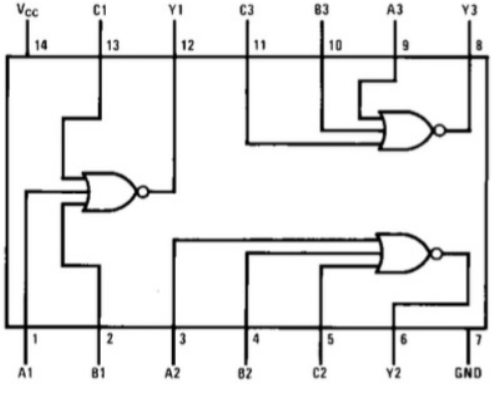
$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

DM74LS27
Triple 3-Input NOR Gate

Connection Diagram



Function Table

$$Y = \overline{A + B + C}$$

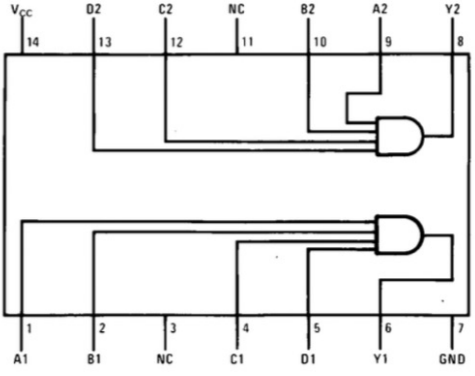
Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

54LS21/DM54LS21/DM74LS21 Dual 4-Input AND Gates

Connection Diagram

Dual-In-Line Package



TL/F/6356–1

Order Number 54LS21DMQB, 54LS21FMQB, 54LS21LMQB, DM54LS21J, DM54LS21W, DM74LS21M or DM74LS21N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

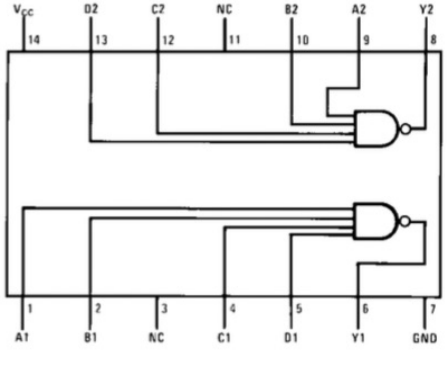
$Y = ABCD$

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

DM74LS20
Dual 4-Input NAND Gate

Connection Diagram



Function Table

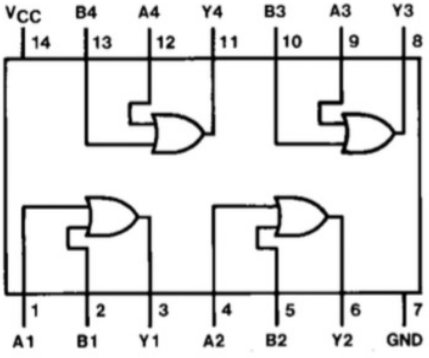
$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

DM74LS32
Quad 2-Input OR Gate

Connection Diagram



Function Table

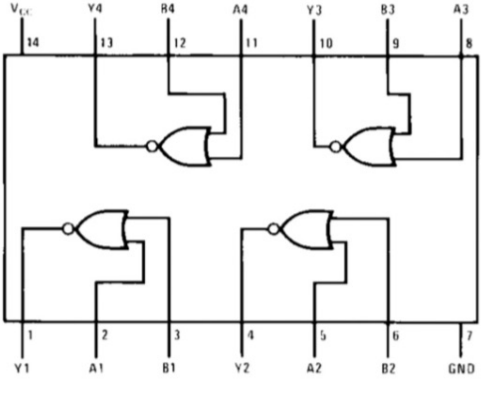
$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

DM74LS02 - 4 x NOR2

Connection Diagram



Function Table

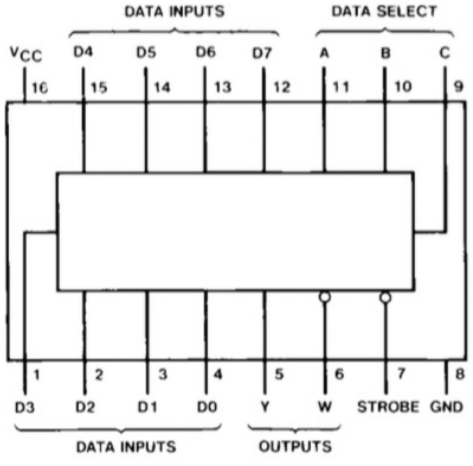
$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

DM74LS151
1-of-8 Line Data Selector/Multiplexer

Connection Diagram



Truth Table

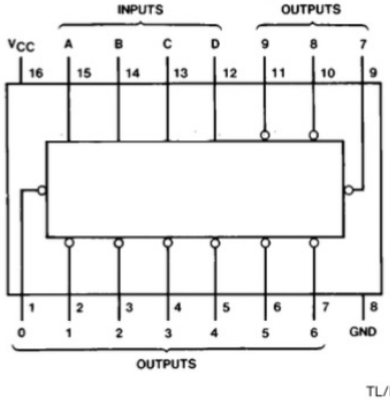
Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = HIGH Level
L = LOW Level
X = Don't Care
D0, D1...D7 = the level of the respective D input

54LS42/DM54LS42/DM74LS42 BCD/Decimal Decoders

Connection Diagram

Dual-In-Line Package



TL/F/6365–1

Order Number 54LS42DMQB, 54LS42FMQB, DM54LS42J, DM54LS42W, DM74LS42M or DM74LS42N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

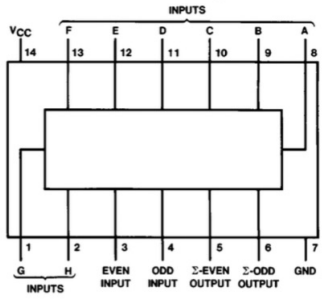
No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

DM54180/DM74180 9-Bit Parity Generators/Checkers

Connection Diagram

Dual-In-Line Package



TL/F/6559–1

Order Number DM54180J, DM54180W or DM74180N
See NS Package Number J14A, N14A or W14B

Function Table

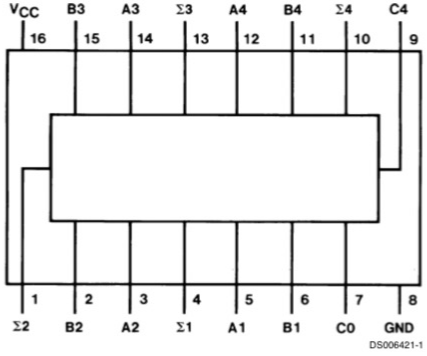
Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

DM74LS283
4-Bit Binary Adders with Fast Carry

Connection Diagram

Dual-In-Line Package



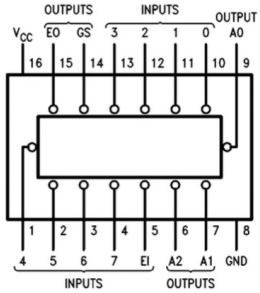
DS006421-1

Order Number 54LS283DMQB, 54LS283FMQB, 54LS283LMQB,
DM54LS283J, DM54LS283W, DM74LS283M or DM74LS283N
See Package Number E20A, J16A, M16A, N16E or W16A

DM54148 Priority Encoder

Connection Diagram

Dual-In-Line Package



TL/F/6545–1

Order Number DM54148J or DM54148W
See NS Package Number J16A or W16A

Function Table

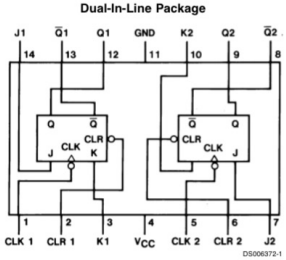
DM54148

Inputs									Outputs				
E1	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**E0**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

DM74LS73A
Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

Connection Diagram

Dual-In-Line Package



Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See Package Number J14A, M14A, N14A or W14B

Function Table

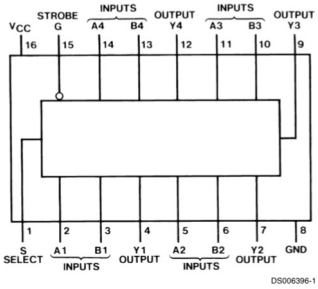
Inputs				Outputs	
CLR	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

DM74LS157/DM74LS158
Quad 2-Line to 1-Line Data Selectors/Multiplexers

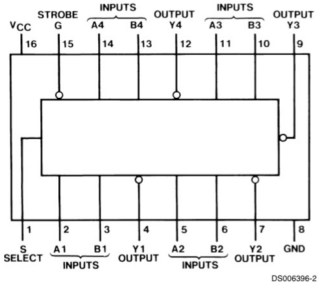
Connection Diagrams

Dual-In-Line Package



Order Number 54LS157DMQB, 54LS157FMQB, 54LS157LMQB, DM54LS157J, DM54LS157W, DM74LS157M or DM74LS157N
See Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



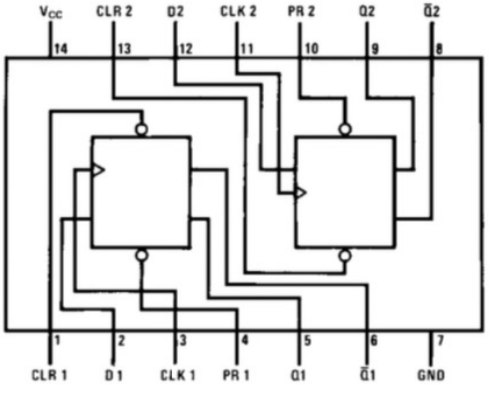
Order Number 54LS158DMQB, 54LS158FMQB, 54LS158LMQB, DM54LS158J, DM54LS158W, DM74LS158M or DM74LS158N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

DM74LS74A
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

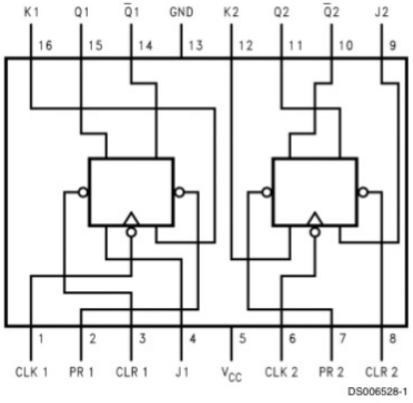
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

DM7476
Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

Connection Diagram

Dual-In-Line Package



Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N
See Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

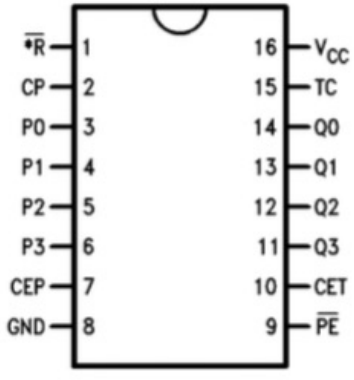
H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

54LS160A/DM74LS160A, 54LS162A/DM74LS162A
Synchronous Presettable BCD Decade Counters

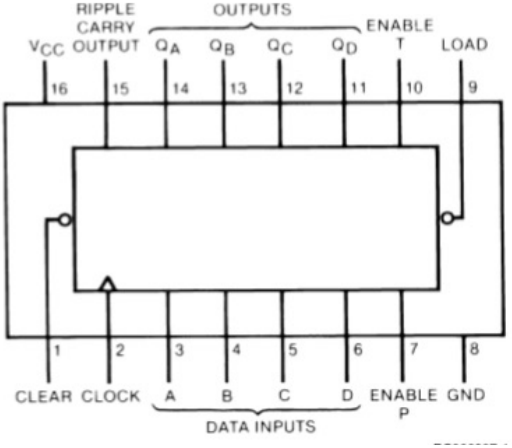
Connection Diagram

Dual-In-Line Package



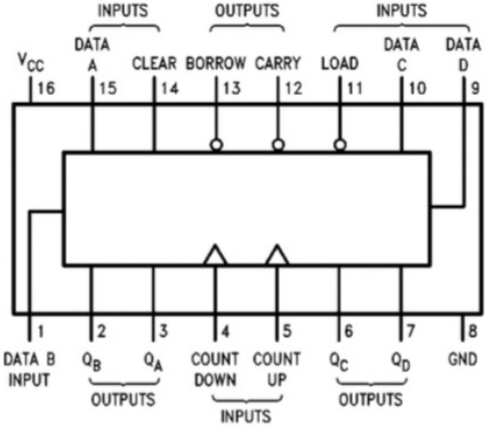
DM74LS161A/DM74LS163A
Synchronous 4-Bit Binary Counters
Connection Diagram

Dual-In-Line Package



DM74LS193
Synchronous 4-Bit Binary Counter with Dual Clock

Connection Diagram



DM74LS194A

4-Bit Bidirectional Universal Shift Register

Connection Diagram