

SF-1P
(Rev 0.7)

Version 07	Changes Description
07.05.2023 J61 pins 1 & 1A net change	1. To disconnect J61 pins 1 &1A from net PS_3V3 and connect it to 3V3 plane
07.05.2023 Net SPI2UART_IRQn moving to R787	2.To disconnect the net SPI2UART_IRQn (U603/14) from R785. To remove R785 from design. To disconnect net IO_EXP2_INTn from R787. To connect net SPI2UART_IRQn (U603/14) to R787. This net is also connected to R790.
07.05.2023 Pullup of 1K on net SPI2UART_MISO.	3.To add Pullup of 1K on net SPI2UART_MISO.


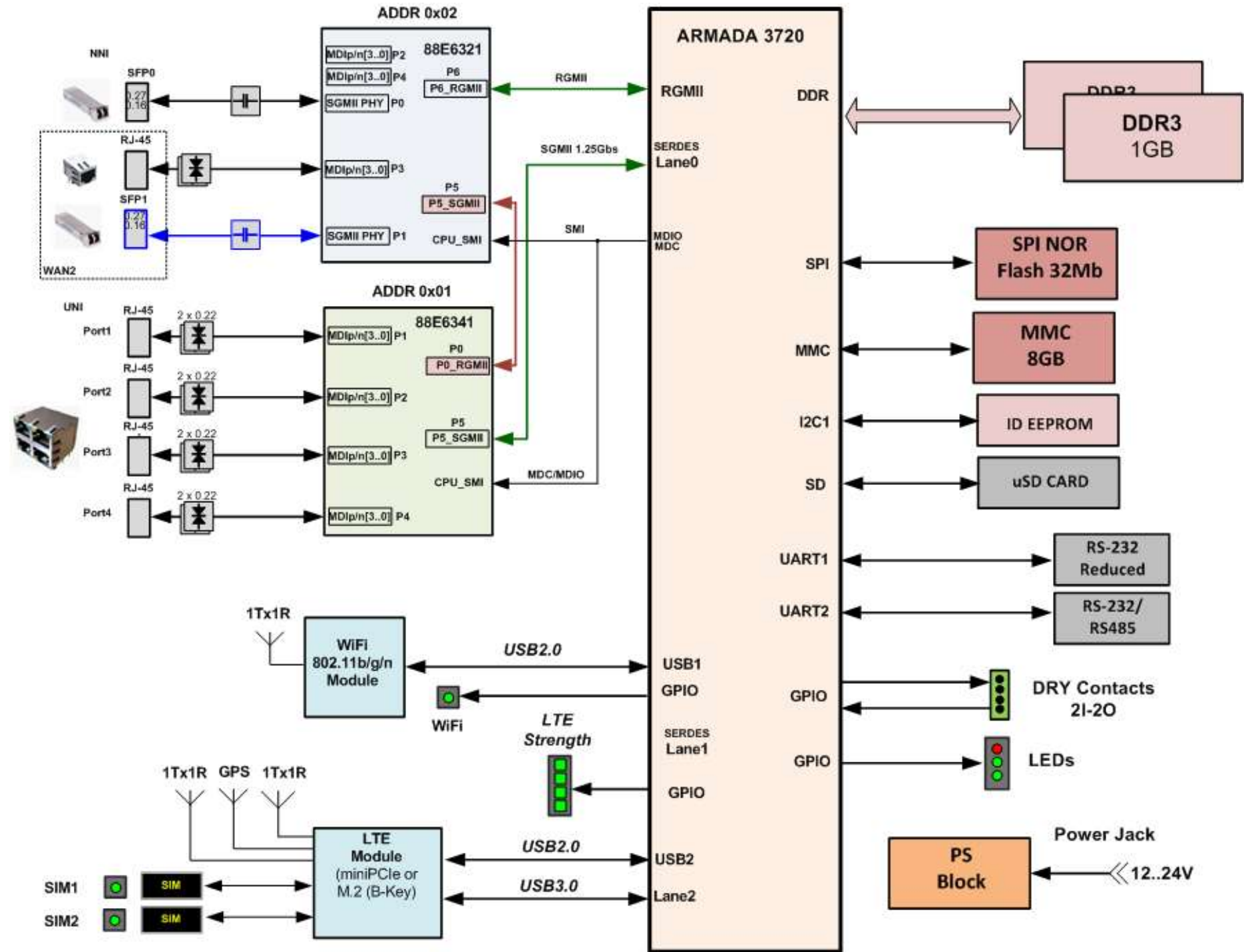
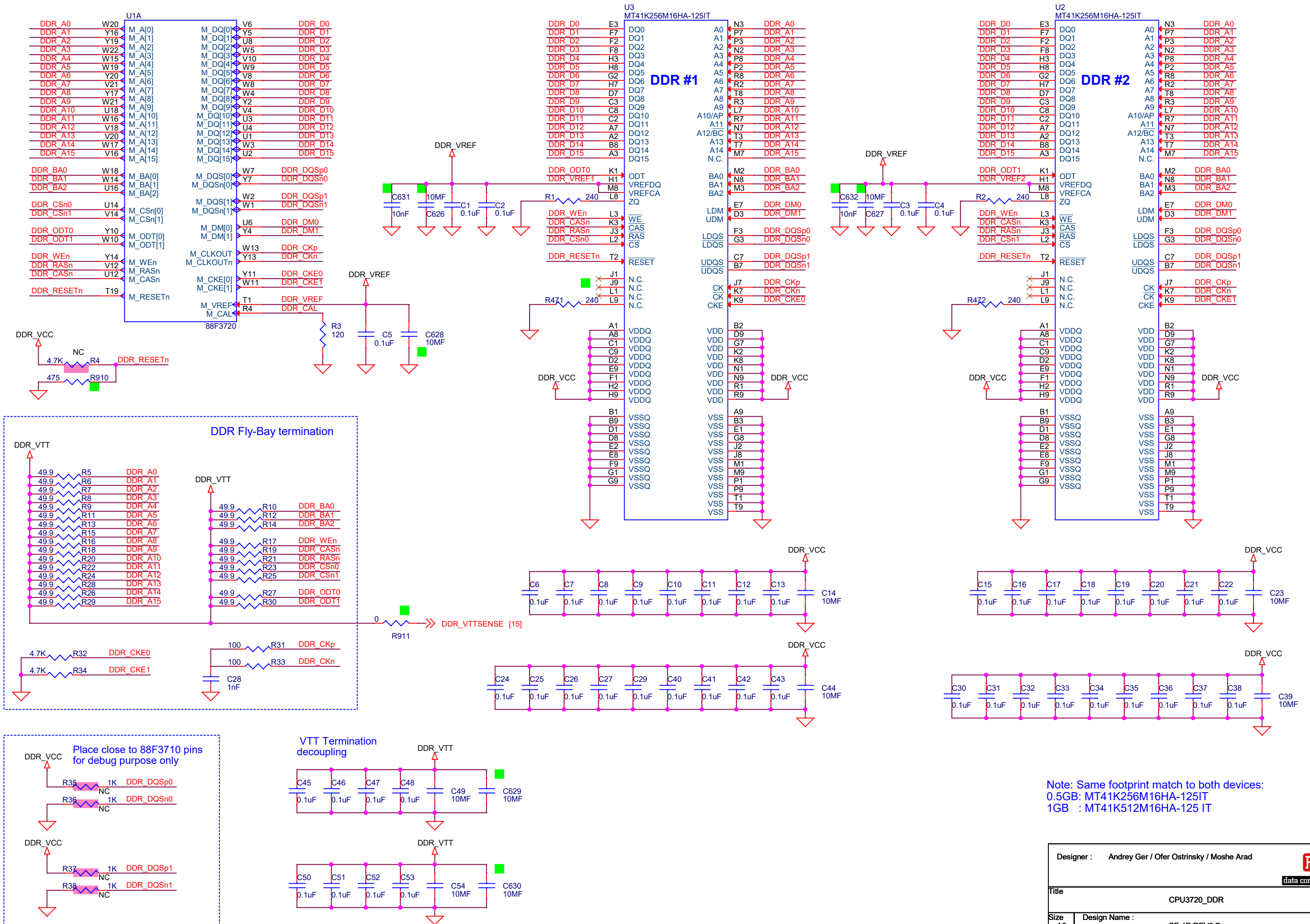
Designer : Andrey Ger / Ofer Ostrinsky / Moshe Arad		 data communications
Title COVER PAGE		
Size B	Design Name : SF-1P.REV0.7	Rev 07
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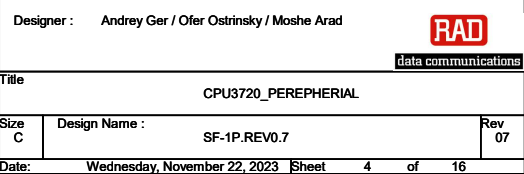
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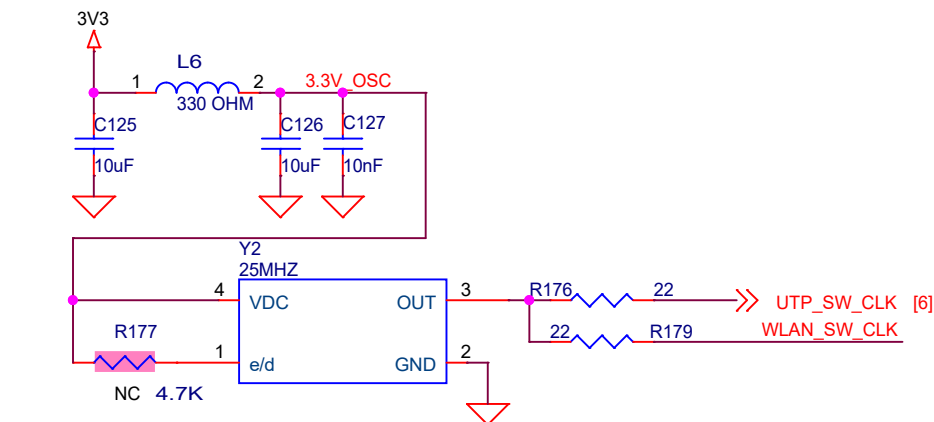
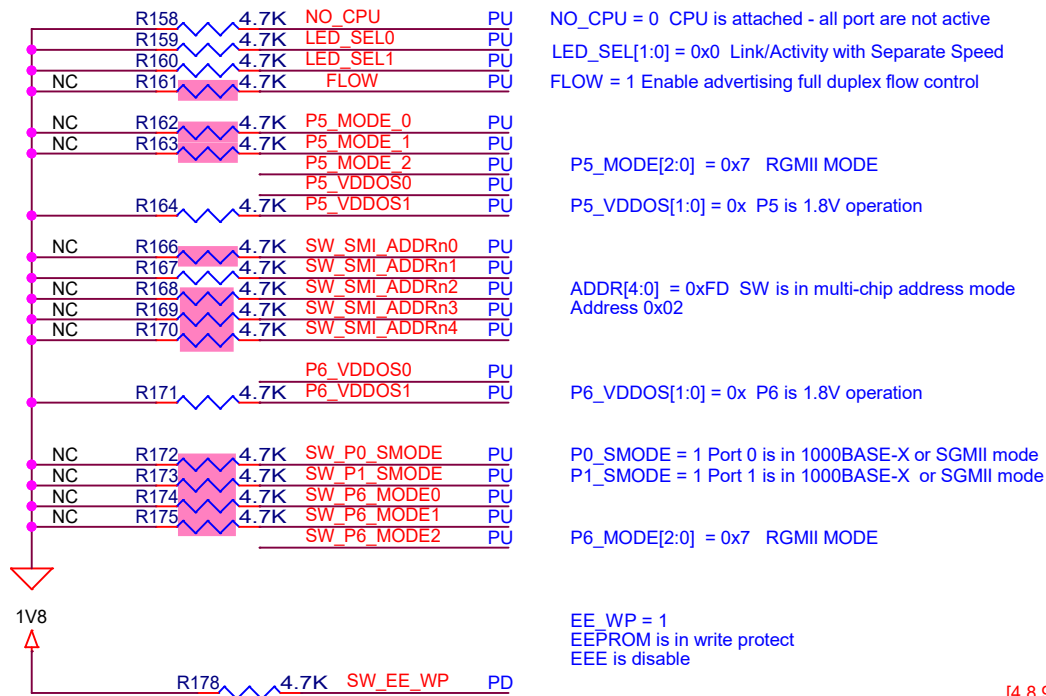
ARMADA3720_DDR



Note: Same footprint match to both devices:
 0.5GB: MT41K256M16HA-125IT
 1GB: MT41K512M16HA-125IT



WLAN GETH SWITCH



[4,8,9,10,15] 3V3_RESETn

[8] R2_LED
 [14] R1_LED
 [8,14] R0_LED
 [8,14] C1_LED
 [8,14] C0_LED

[6] P5_RGMII_RXCLK
 [6] P5_RGMII_RXD3
 [6] P5_RGMII_RXD2
 [6] P5_RGMII_RXD1
 [6] P5_RGMII_RXD0
 [6] P5_RGMII_RXDV

[6] P5_RGMII_TXEN
 [6] P5_RGMII_TXCLK
 [6] P5_RGMII_TXD3
 [6] P5_RGMII_TXD2
 [6] P5_RGMII_TXD1
 [6] P5_RGMII_TXD0

[8] WAN_P3_MDI0n
 [8] WAN_P3_MDI0p
 [8] WAN_P3_MDI1n
 [8] WAN_P3_MDI1p
 [8] WAN_P3_MDI2n
 [8] WAN_P3_MDI2p
 [8] WAN_P3_MDI3n
 [8] WAN_P3_MDI3p
 [8] SW_P1_S_RXP
 [8] SW_P1_S_RXN
 [8] SW_P0_S_RXP
 [8] SW_P0_S_RXN
 [8] SW_P1_S_TXP
 [8] SW_P1_S_TXN
 [8] SW_P0_S_TXP
 [8] SW_P0_S_TXN

R128 4.99K
 WLAN_SW_CLK

R134 300 NO_CPU
 R135 300 LED_SEL1
 R137 300 LED_SEL0
 R139 0
 R141 0 FLOW

TP30 1
 TP31 1
 R144 33 P5_VDDOS0
 R146 22 P5_RGMII_TXCLK R
 R147 33 P5_VDDOS1
 R148 33 P5_MODE_2
 R150 33 P5_MODE_1
 R152 33 P5_MODE_0

TP30 1
 TP31 1
 R144 33 P5_VDDOS0
 R146 22 P5_RGMII_TXCLK R
 R147 33 P5_VDDOS1
 R148 33 P5_MODE_2
 R150 33 P5_MODE_1
 R152 33 P5_MODE_0

P5_INCLK/GPIO1
 P5_IND3/GPIO6
 P5_IND2/GPIO5
 P5_IND1
 P5_IND0
 P5_INDV/GPIO2
 P5_CRS/MDC_PHY/GPIO8
 P5_MDIO_PHY/GPIO7
 P5_OUTEN/P5_VDDOS0
 P5_OUTCLK/P5_TXC/GPIO0
 P5_OUTD3/P5_VDDOS1
 P5_OUTD2/P5_MODE2
 P5_OUTD1/P5_MODE1
 P5_OUTD0/P5_MODE0

N.C.
 N.C.
 N.C.
 VSS
 VSS

U4 88E6321-A0-NAZ

P4_MDIN_0
 P4_MDIP_0
 P4_MDIN_1
 P4_MDIP_1
 P4_MDIN_2
 P4_MDIP_2
 P4_MDIN_3
 P4_MDIP_3

P3_MDIN_0
 P3_MDIP_0
 P3_MDIN_1
 P3_MDIP_1
 P3_MDIN_2
 P3_MDIP_2
 P3_MDIN_3
 P3_MDIP_3

P1_S_RXP
 P1_S_RXN
 P0_S_RXP
 P0_S_RXN
 P1_S_TXP
 P1_S_TXN
 P0_S_TXP
 P0_S_TXN

RSET
 XTAL_IN
 XTAL_OUT
 XTAL_GND
 RESERT_n
 SE_SCLK

R2_LED/P3_LED0/NO_CPU
 R1_LED/P1_LED0/LED_SEL0
 R0_LED/P0_LED0/LED_SEL0
 EE_DOUT/C1_LED/P4_LED0

EE_CLK/C0_LED/FLOW
 P5_INCLK/GPIO1
 P5_IND3/GPIO6
 P5_IND2/GPIO5
 P5_IND1
 P5_IND0

P5_INDV/GPIO2
 P5_CRS/MDC_PHY/GPIO8
 P5_MDIO_PHY/GPIO7
 P5_OUTEN/P5_VDDOS0
 P5_OUTCLK/P5_TXC/GPIO0
 P5_OUTD3/P5_VDDOS1
 P5_OUTD2/P5_MODE2
 P5_OUTD1/P5_MODE1
 P5_OUTD0/P5_MODE0

N.C.
 N.C.
 N.C.
 VSS
 VSS

P6_MDIN_0
 P6_MDIP_0
 P6_MDIN_1
 P6_MDIP_1
 P6_MDIN_2
 P6_MDIP_2
 P6_MDIN_3
 P6_MDIP_3

P5_VDDO
 P5_VDDO
 P6_VDDO
 P6_VDDO
 EE_VDDO
 P4_AVDD33
 P3_AVDD33
 VDD33
 VDD33_PLL
 CTOP
 CBOT
 VOUT15
 P4_AVDD15
 P3_AVDD15
 AVDD15
 AVDD15
 P1_AVDD15
 P0_AVDD15
 VOUT11
 VOUY11_SEN
 VDD_CORE
 VDD_CORE

P5_VDDO = 1V8
 P6_VDDO = 1V8
 EE_VDDO = 3V3
 (RESETn LEDs (pin 97..103))
 P3_AVDDO = 3V3
 P4_AVDDO = 3V3
 VDD33 = 3V3 (Internal VReg)
 VDD33_PLL = 3V3

SW_P34_AVDD33
 SW_VDD33_PLL
 SW_VDD33_PLL

SW_VDD15
 SW_CORE_1V1
 Embedded PS
 Normal Operation

R130 4.7K
 R131 0
 R136 33
 R138 33
 R140 33
 R142 33
 TP28
 TP29
 TP32
 TP33

P6_RGMII_TXD0 [4]
 P6_RGMII_TXD1 [4]
 P6_RGMII_TXD2 [4]
 P6_RGMII_TXD3 [4]
 P6_RGMII_TXCLK [4]
 P6_RGMII_TXEN [4]
 P6_RGMII_RXD0 [4]
 P6_RGMII_RXD1 [4]
 P6_RGMII_RXD2 [4]
 P6_RGMII_RXD3 [4]
 P6_RGMII_RXCLK [4]

P6_IND4/P2_IND0/GPIO11
 P6_IND5/P2_IND1/GPIO12
 P6_IND6/P2_IND2/GPIO13
 P6_IND7/P2_IND3/GPIO14
 P6_INCLK

C128 10nF
 C129 1nF
 C130 0.1uF
 C131 0.1uF
 C132 0.1uF
 C133 10uF

C118 0.1uF
 C119 0.1uF
 C120 10uF

C121 0.1uF
 C122 0.1uF
 C123 0.1uF
 C124 10uF

C114 0.1uF
 C115 0.1uF
 C116 10uF
 C117 10uF

C109 0.1uF
 C110 0.1uF
 C111 10uF
 C112 10uF

L5 300MA
 L4 300MA

SW_VDD33_PLL
 SW_P34_AVDD33

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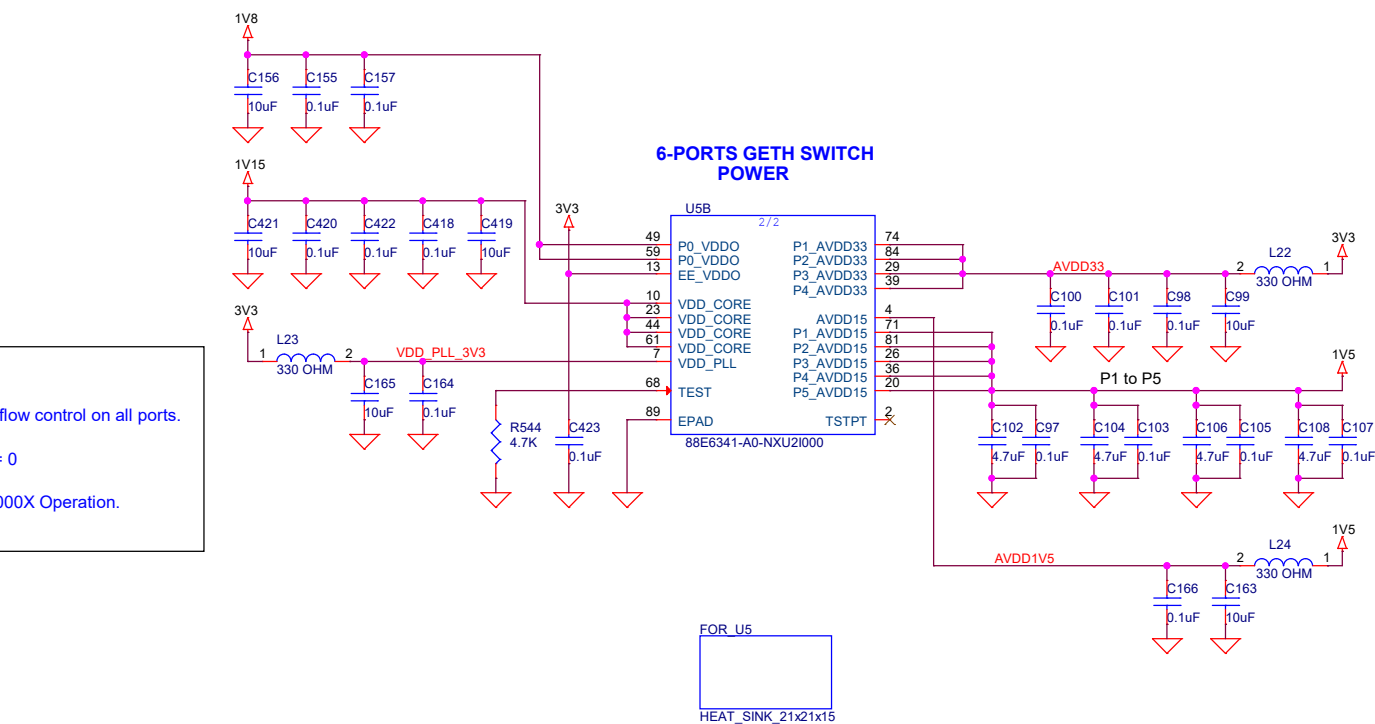
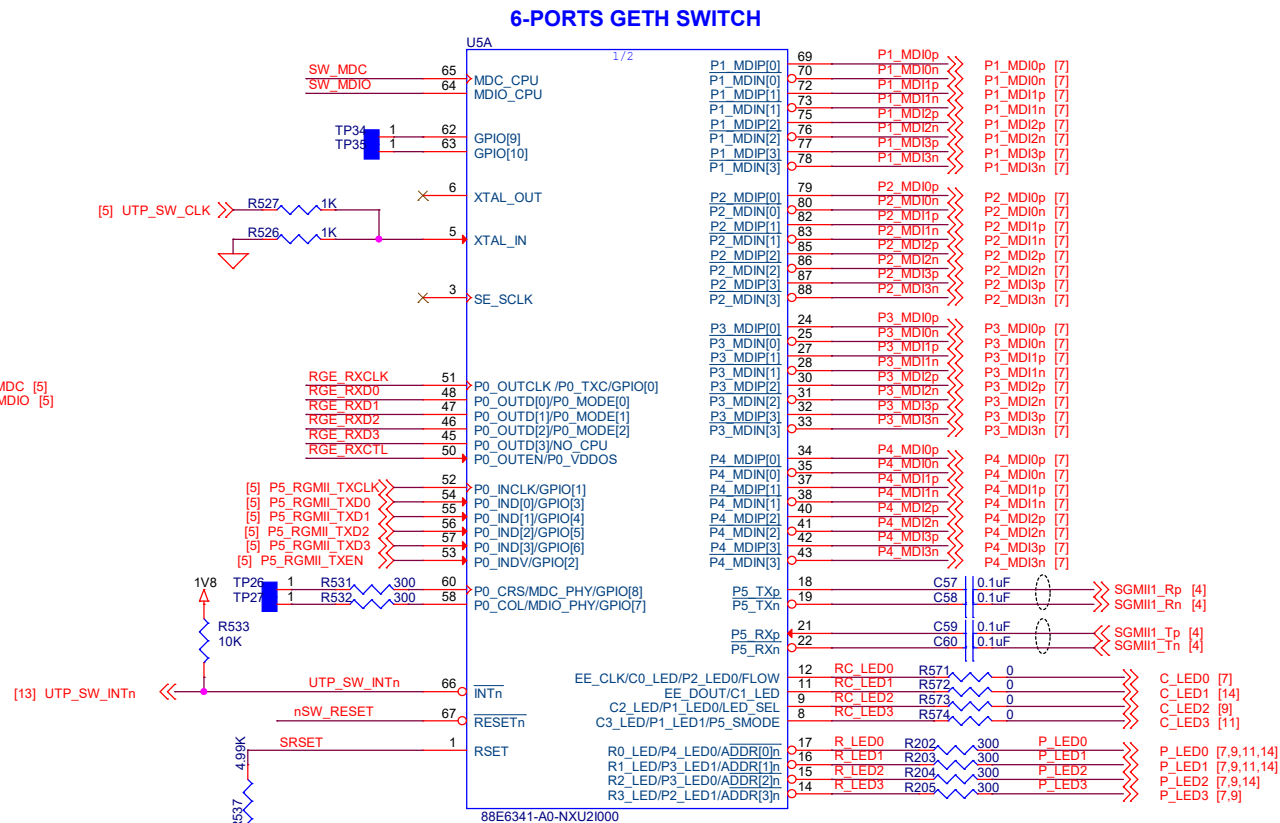
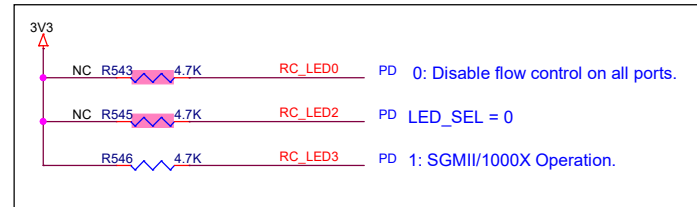
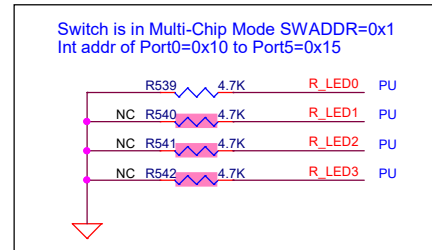
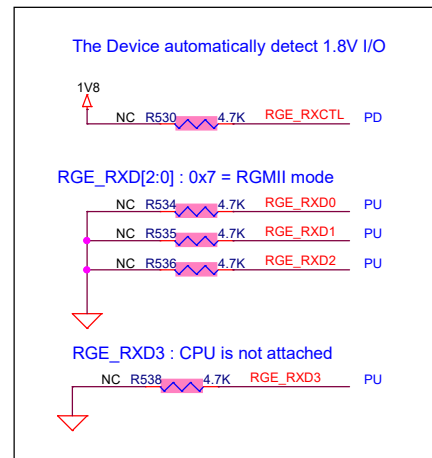
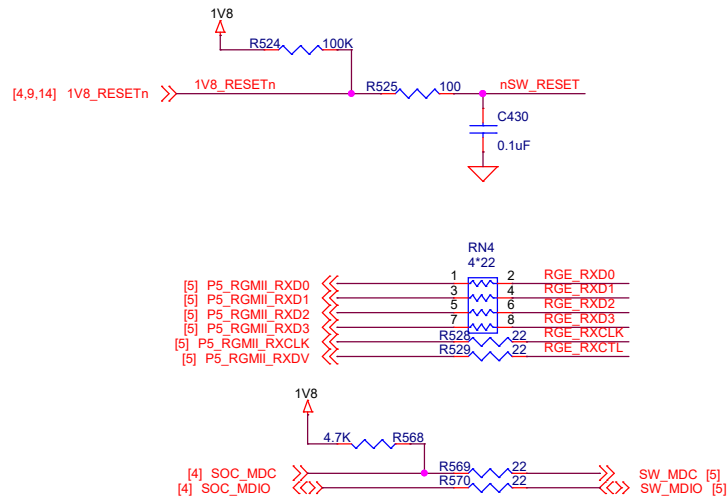
SW_VDD33_PLL
 SW_P34_AVDD33

SW_VDD33_PLL
 SW_P34_AVDD33

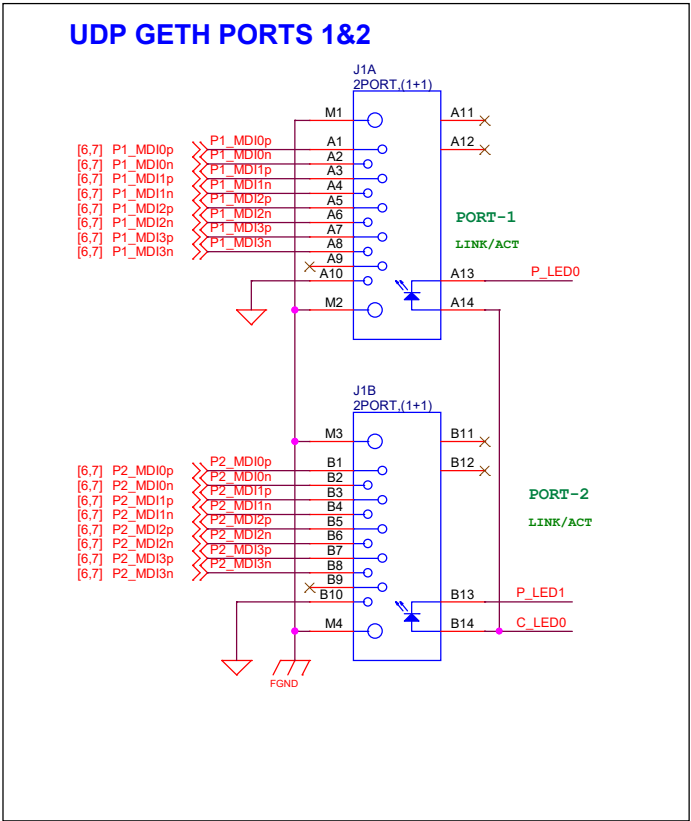
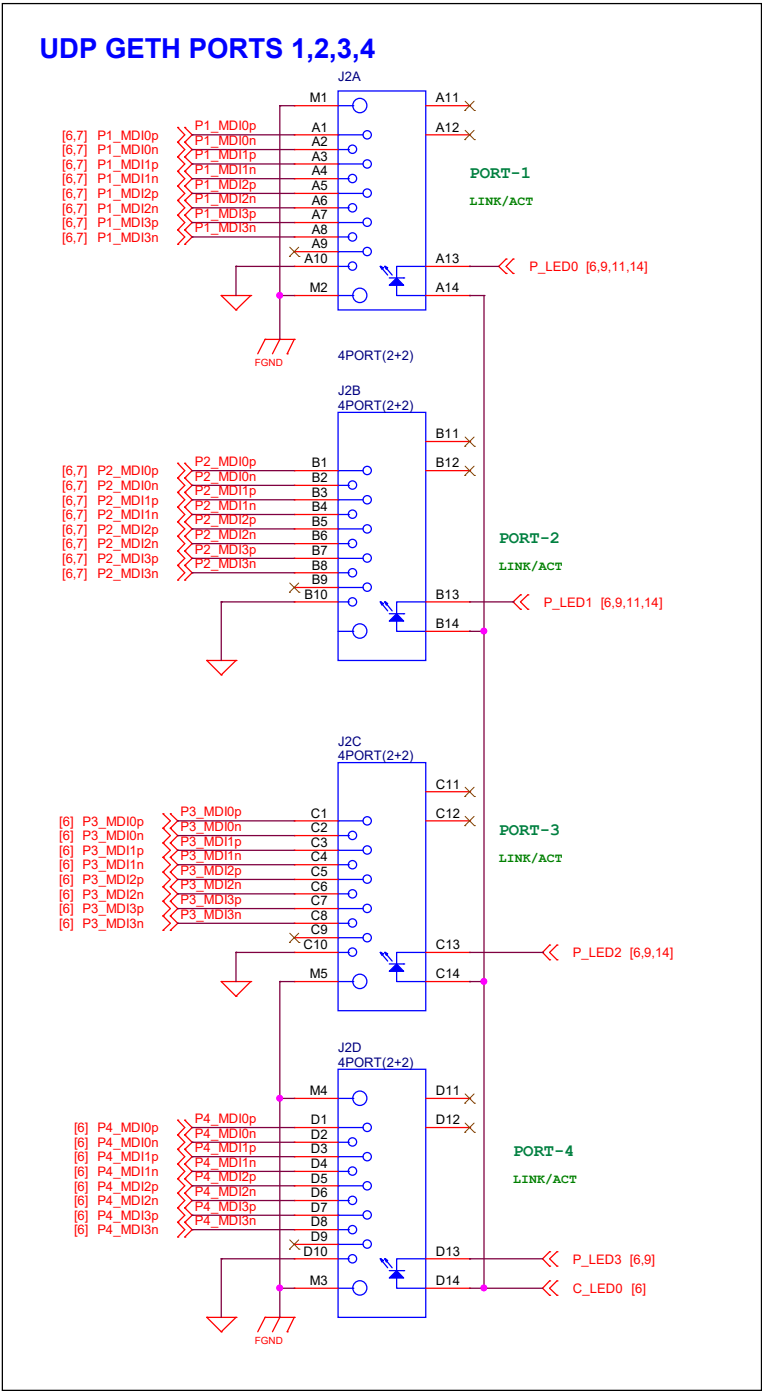
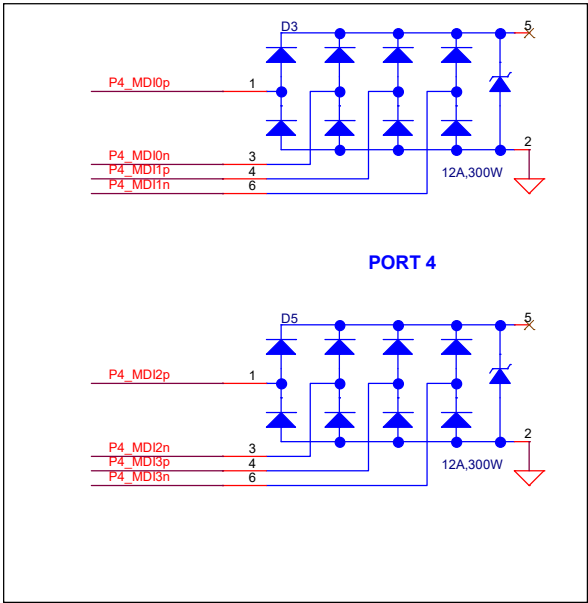
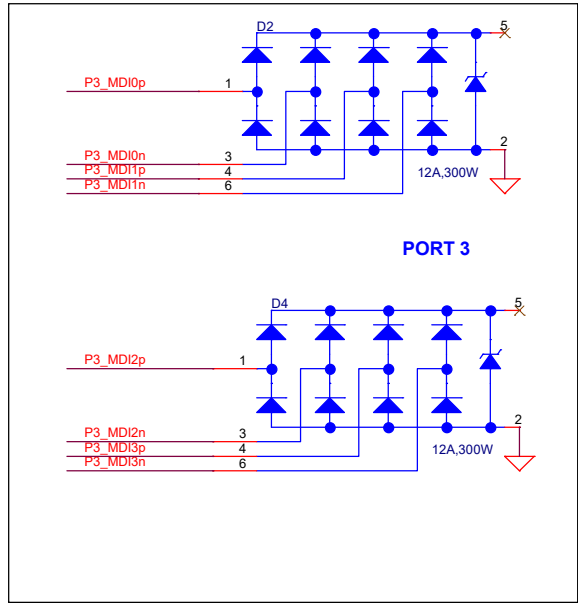
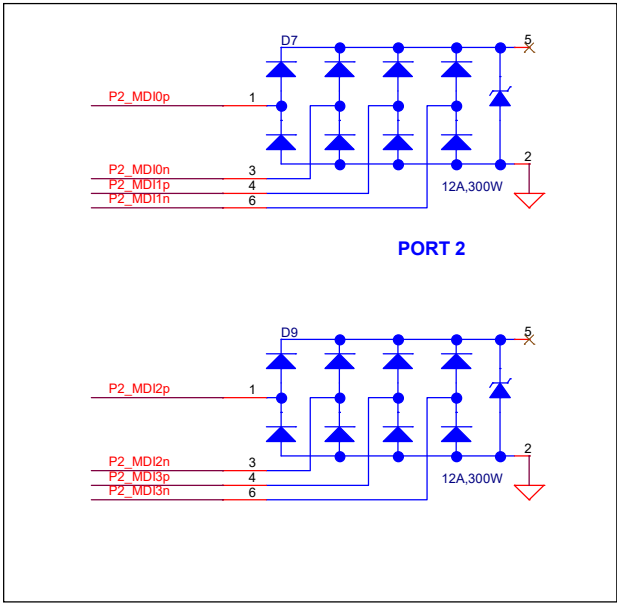
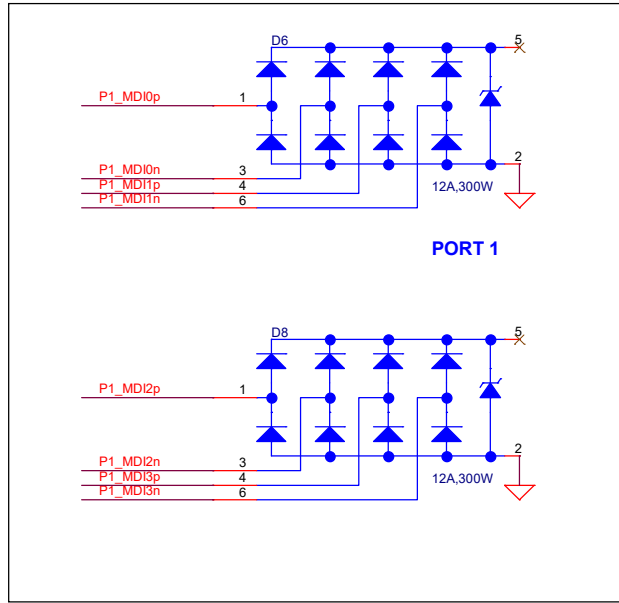
SW_VDD33_PLL
 SW_P34_AVDD33

SW_VDD33_PLL
 SW_P34_AVDD33

UTP GETH SWITCH



FOR U5
HEAT_SINK_21x21x15



Designer : Andrey Ger / Ofer Ostrinsky



data communications

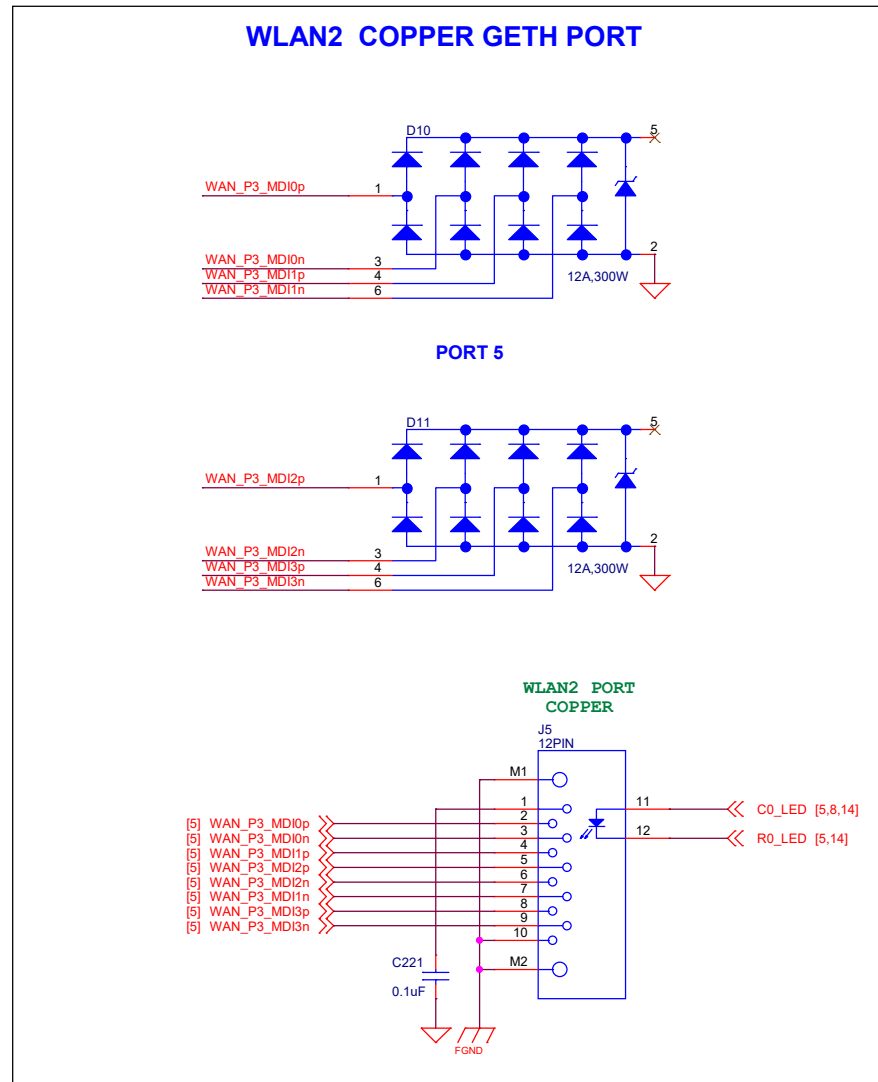
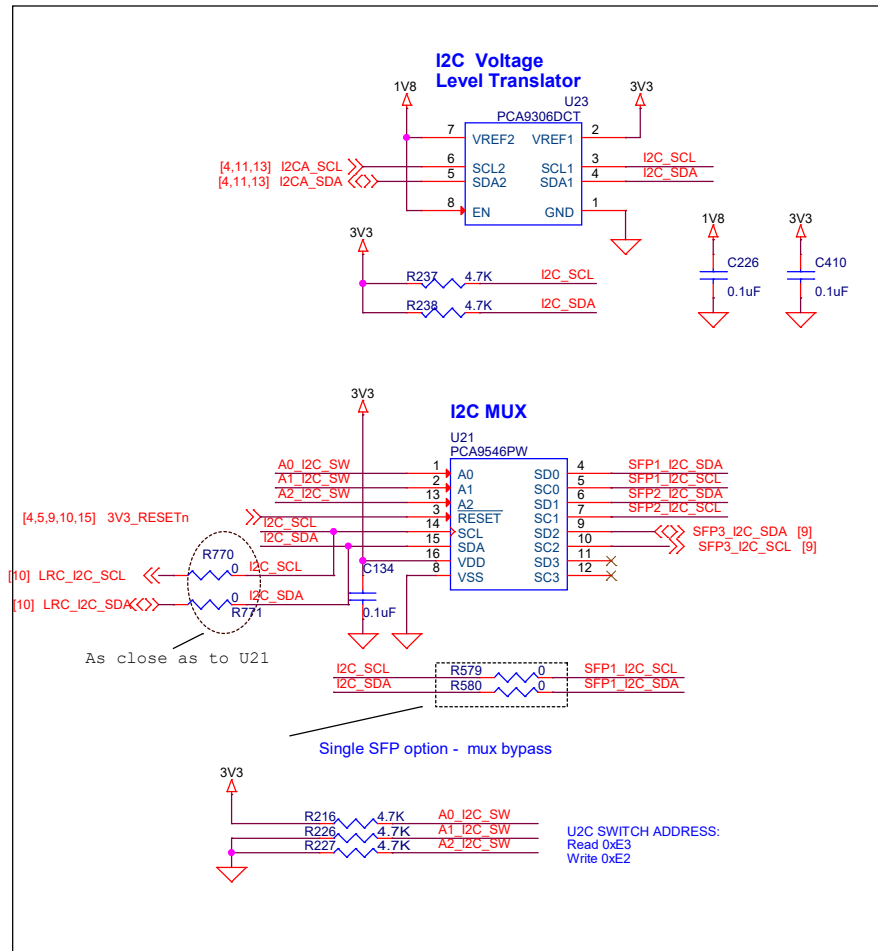
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Design Name : SF-1P.REV0.7

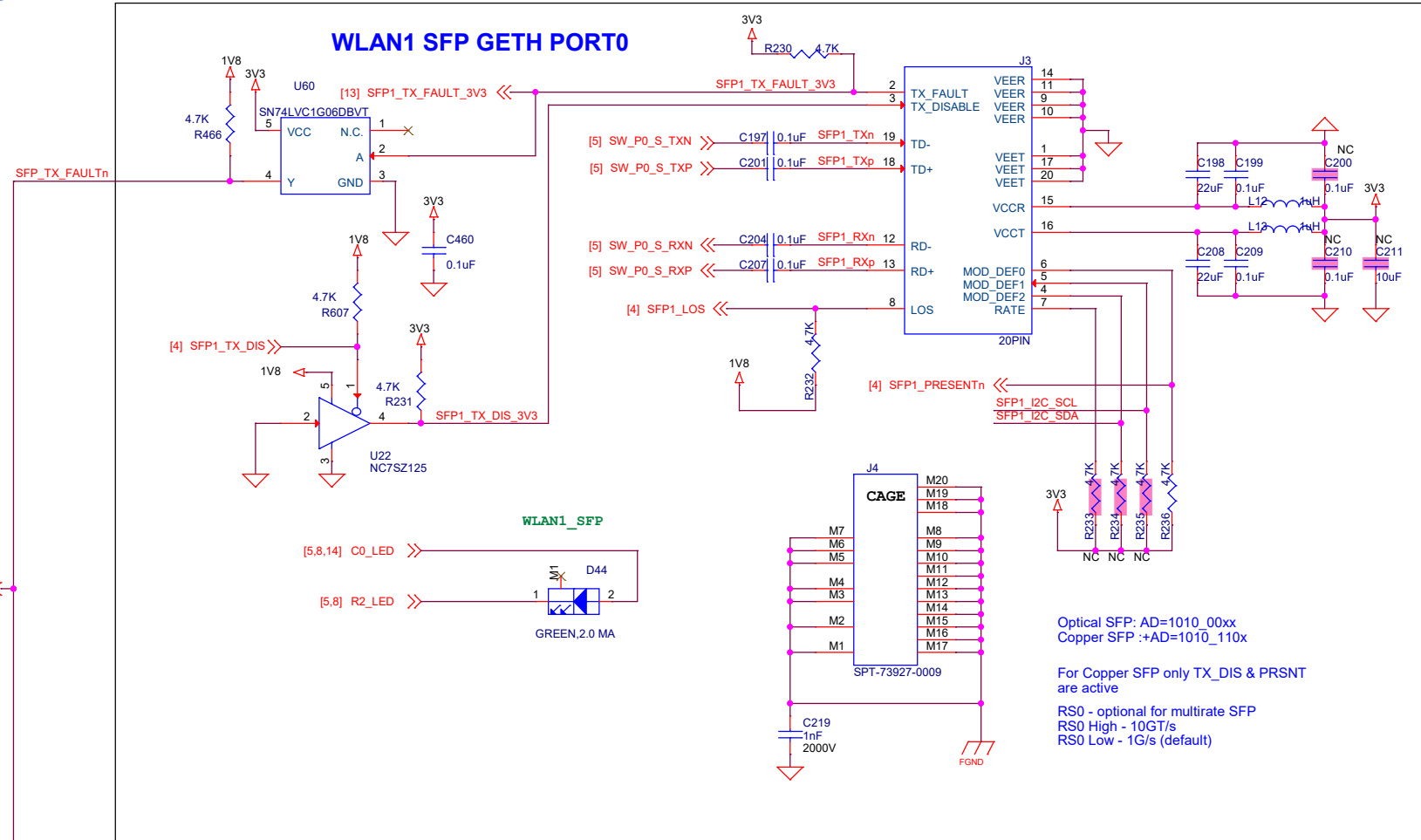
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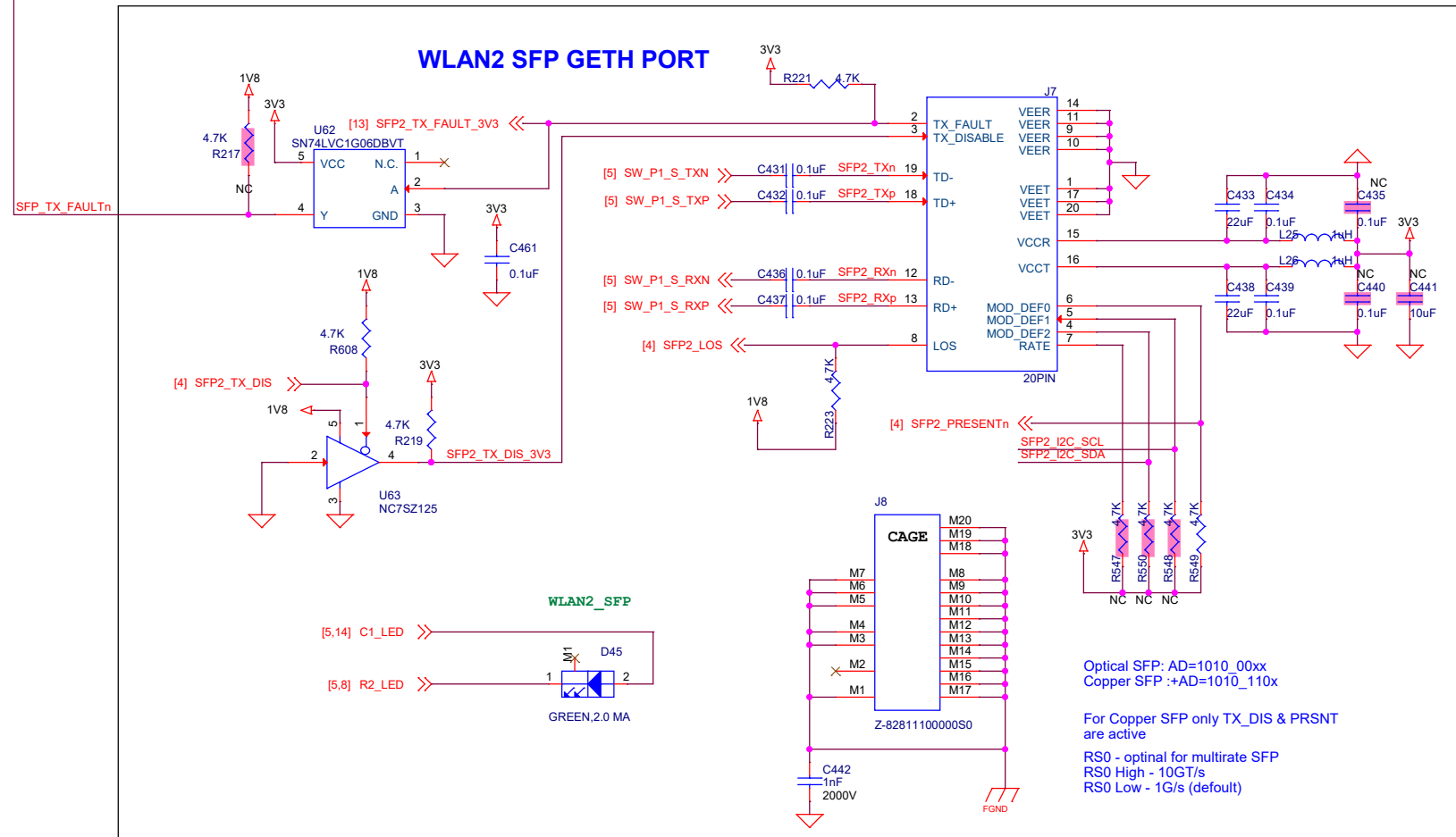
WLAN PORTS



WLAN1 SFP GETH PORT0



WLAN2 SFP GETH PORT



Designer : Andrey Ger / Ofer Ostrinsky

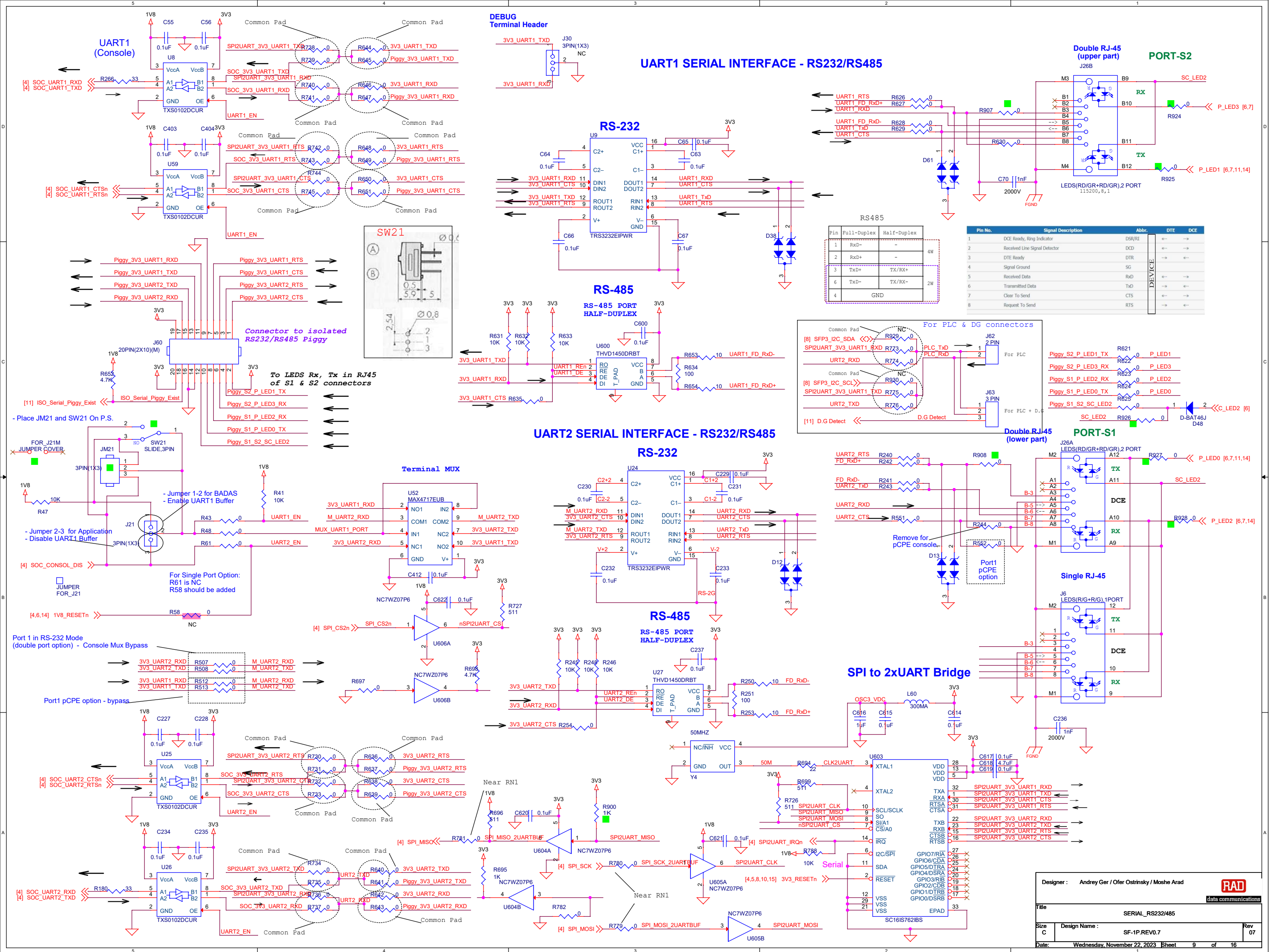


data communications

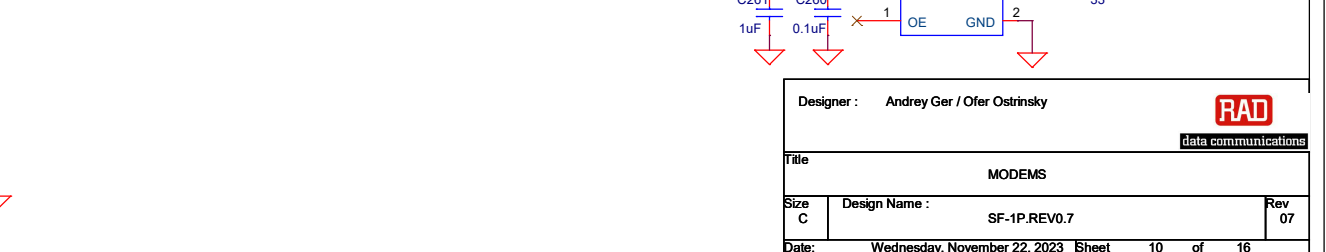
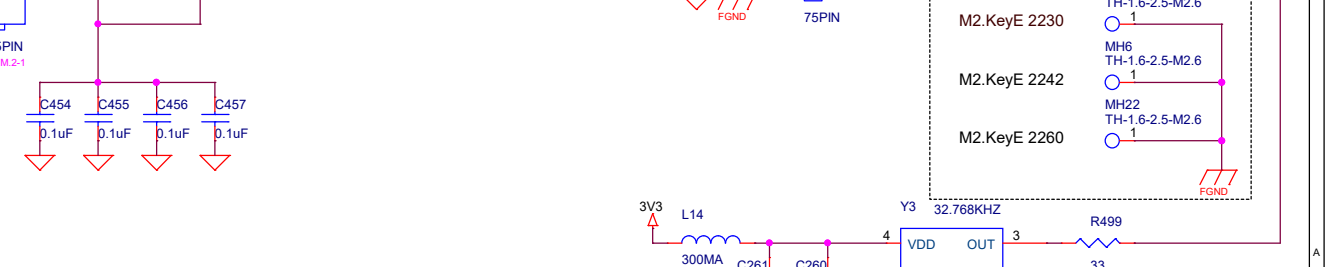
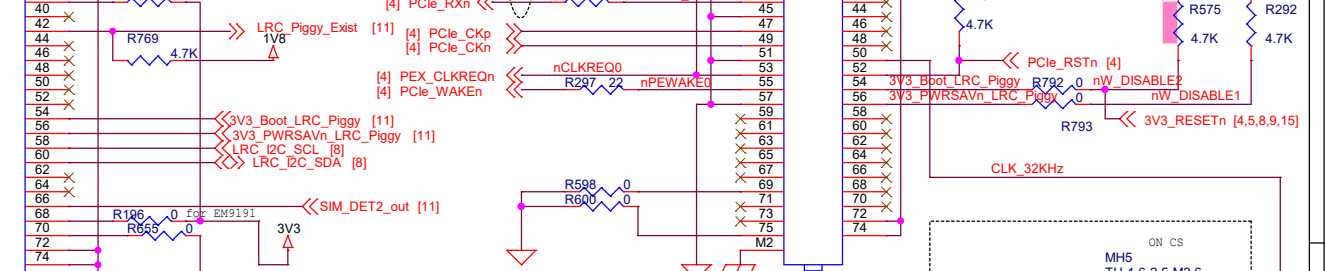
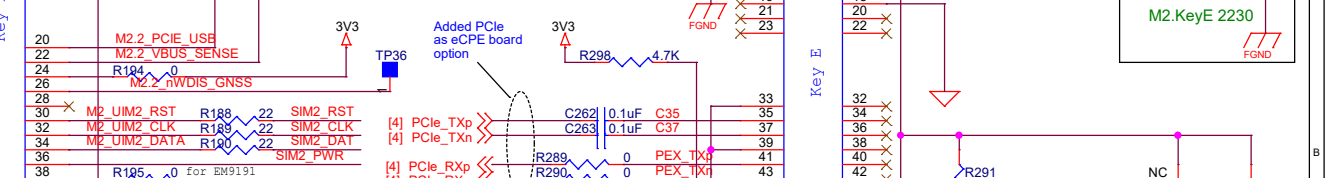
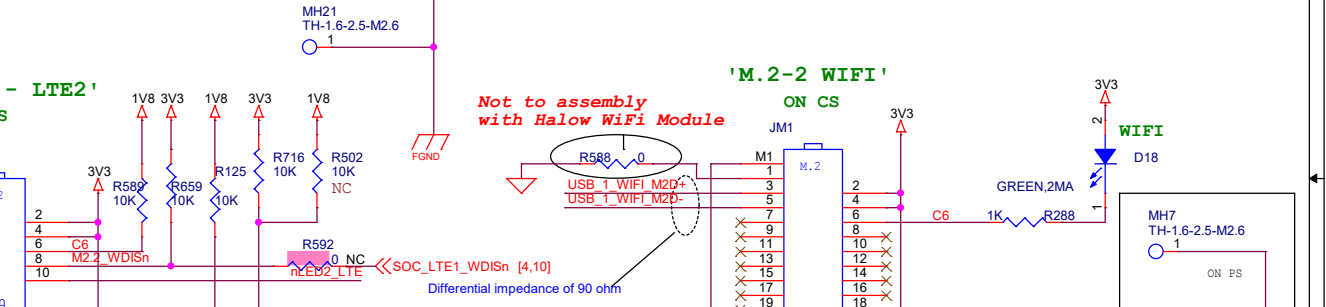
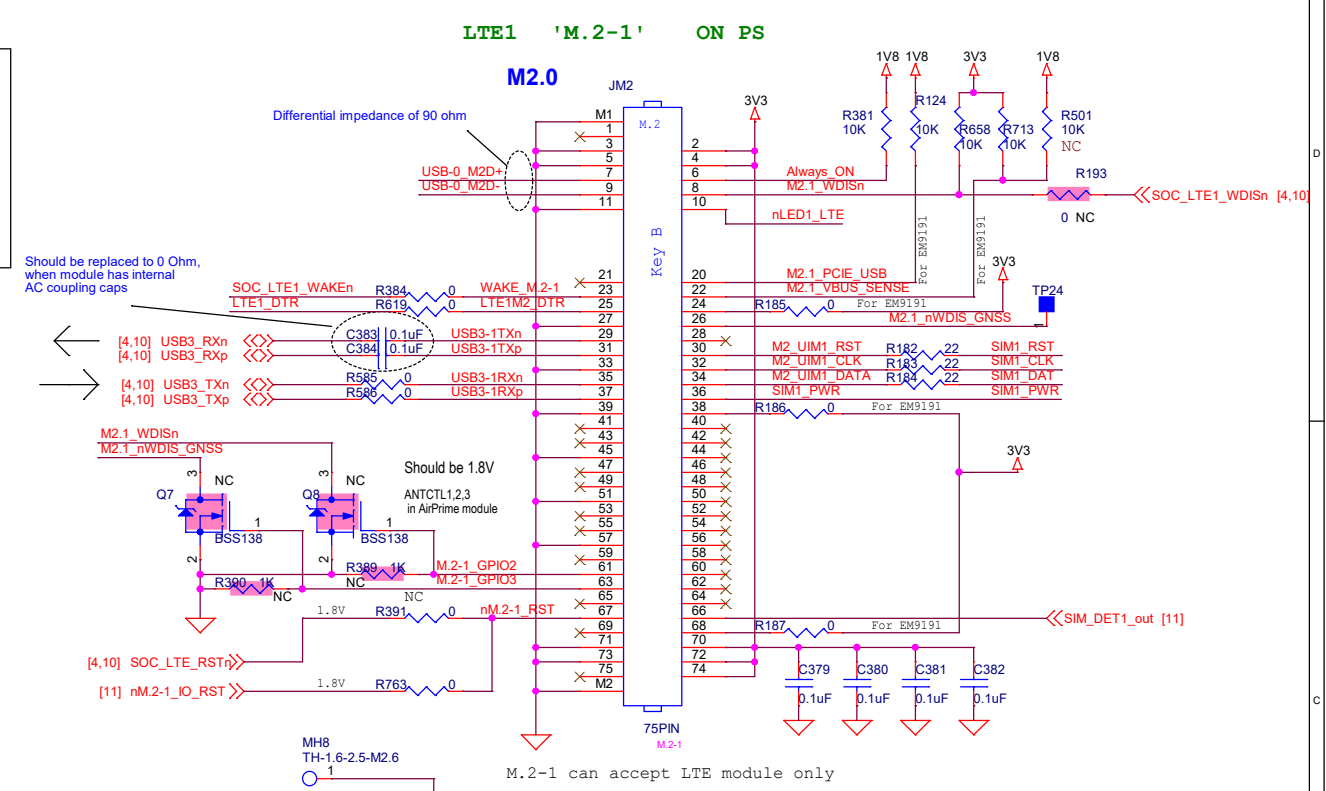
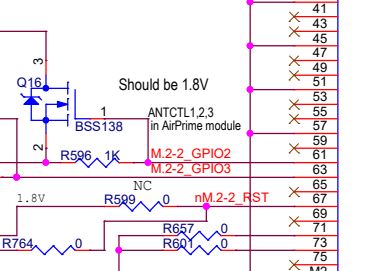
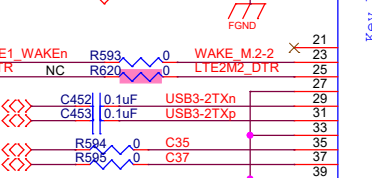
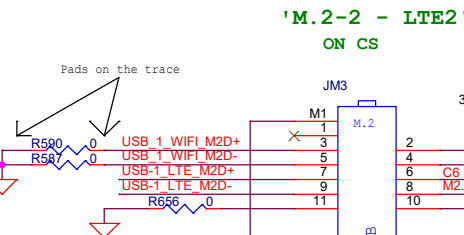
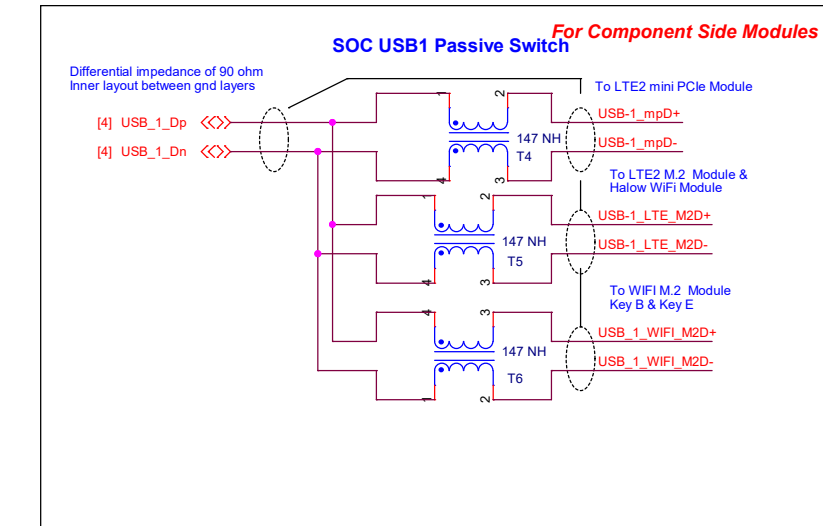
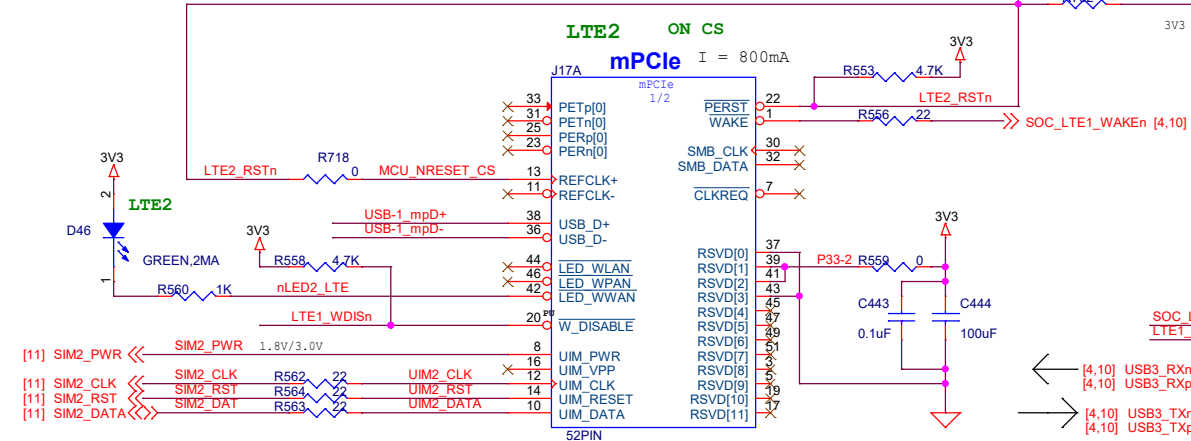
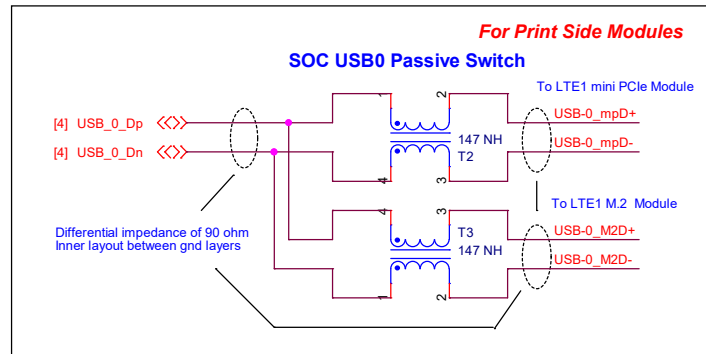
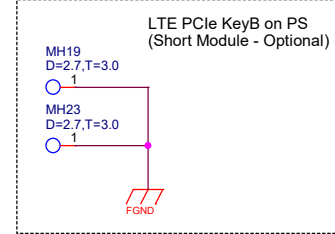
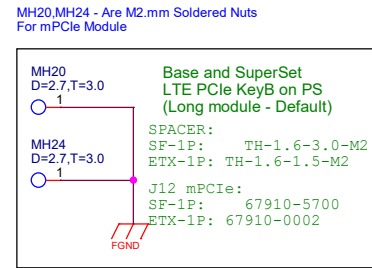
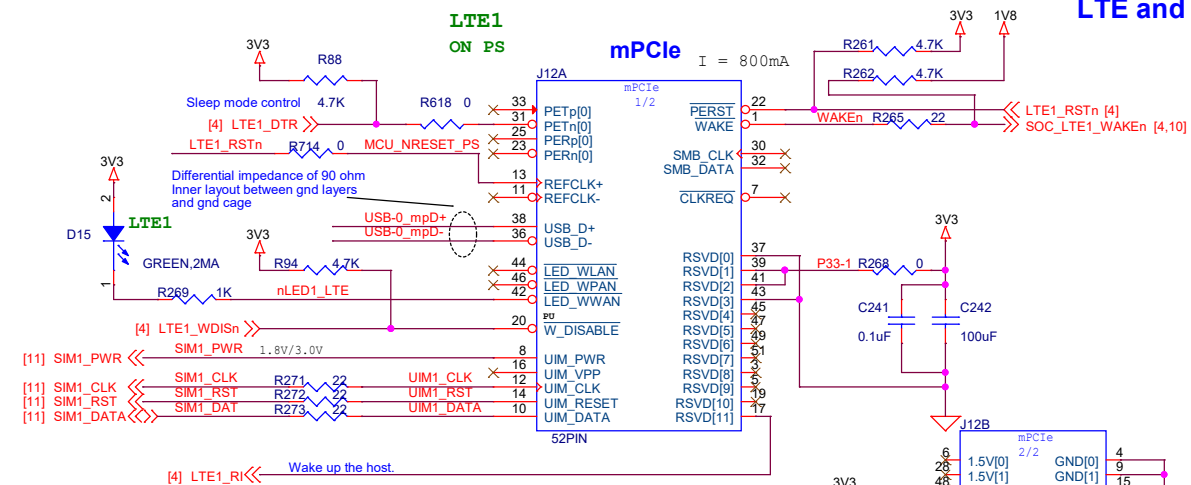
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Size	Design Name :	05 1B BEV/0.3
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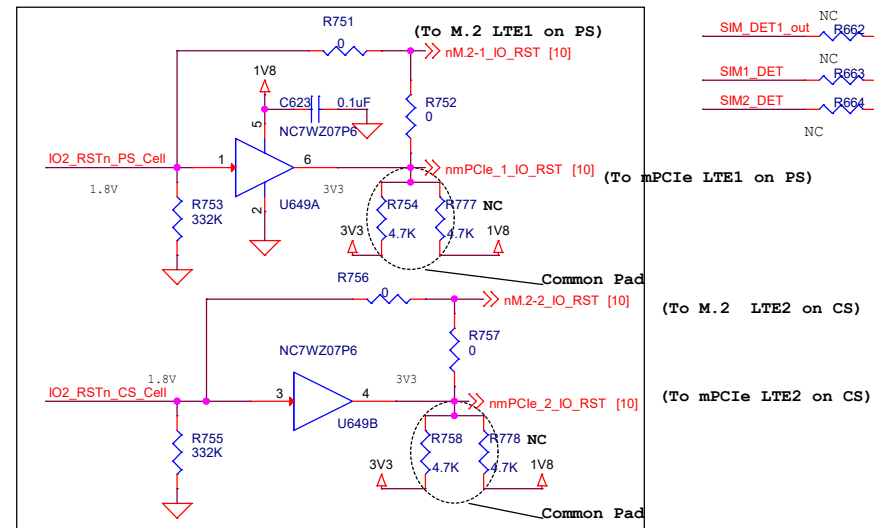
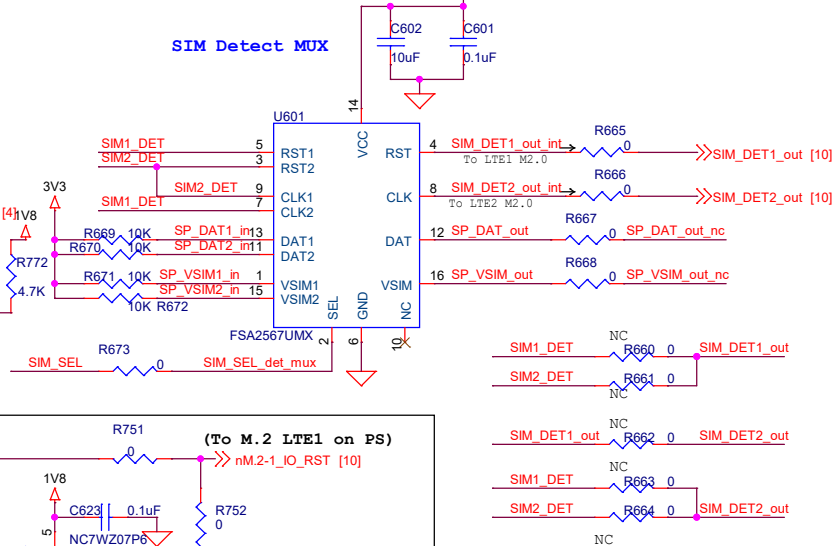
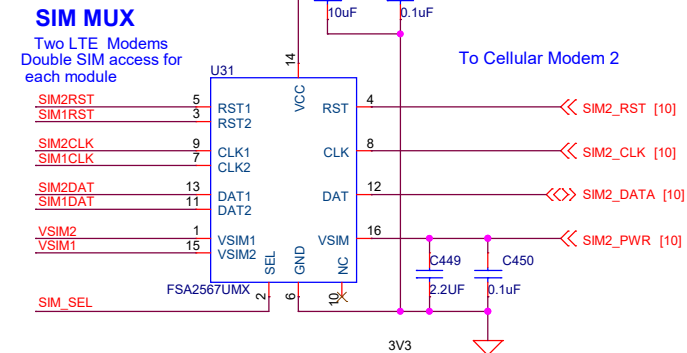
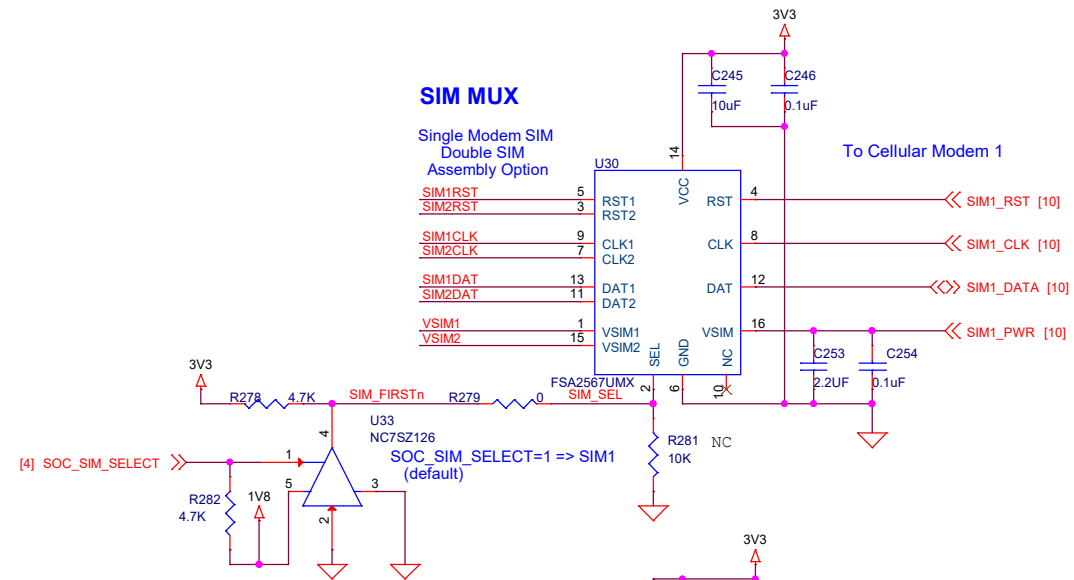
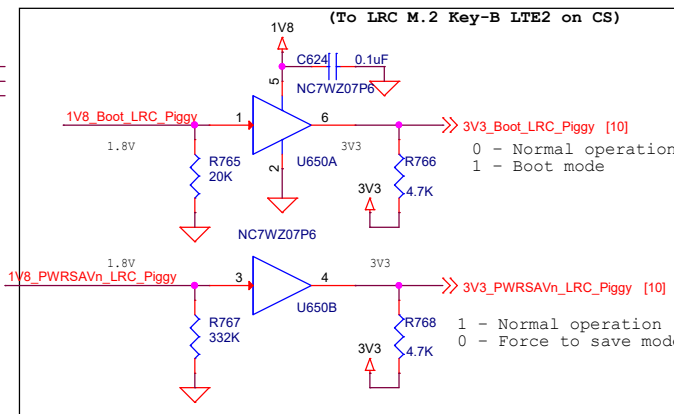
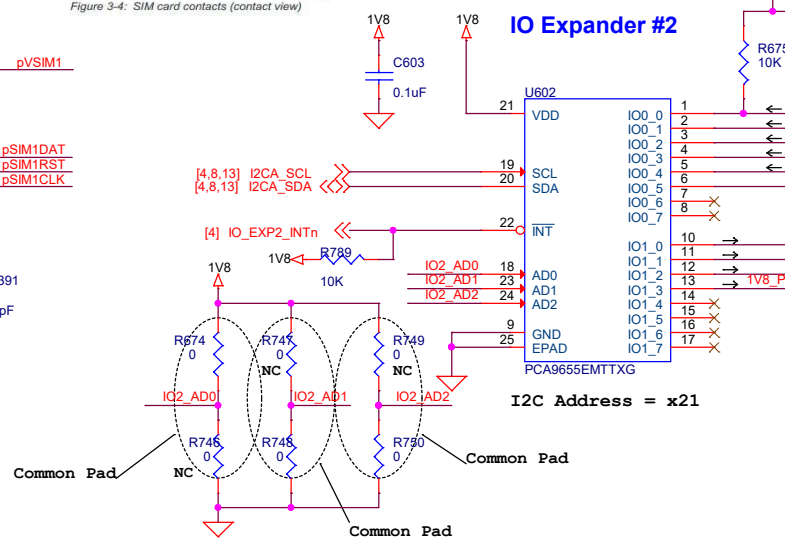
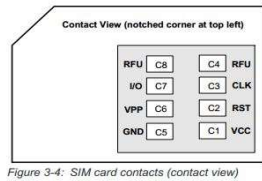
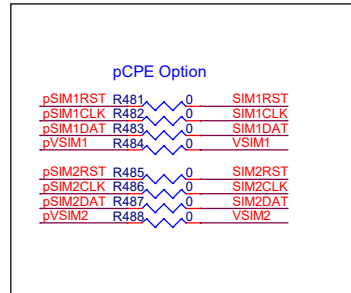
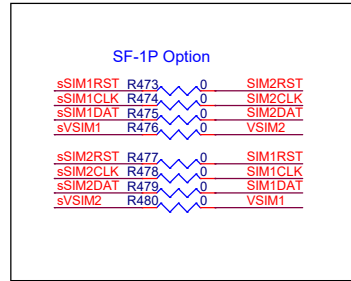
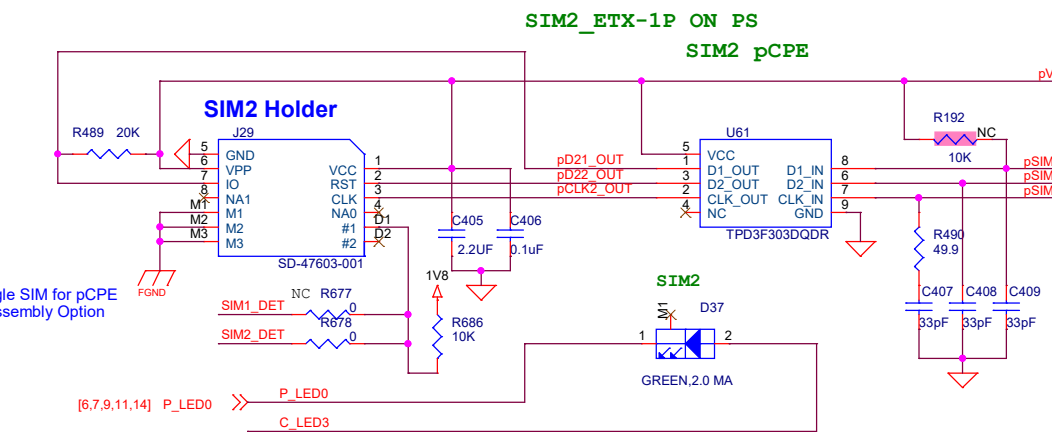
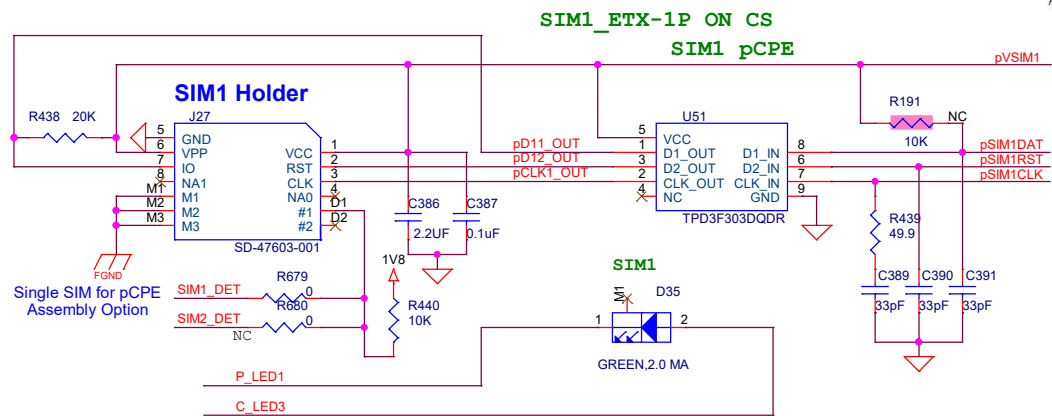
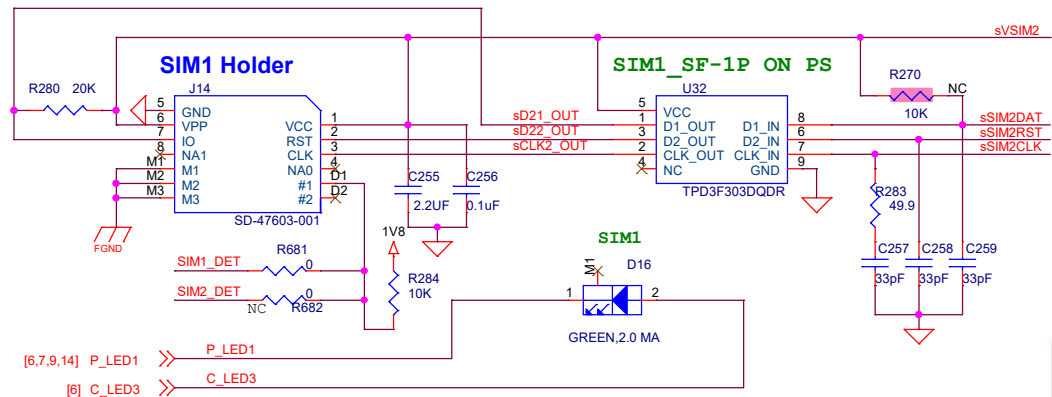
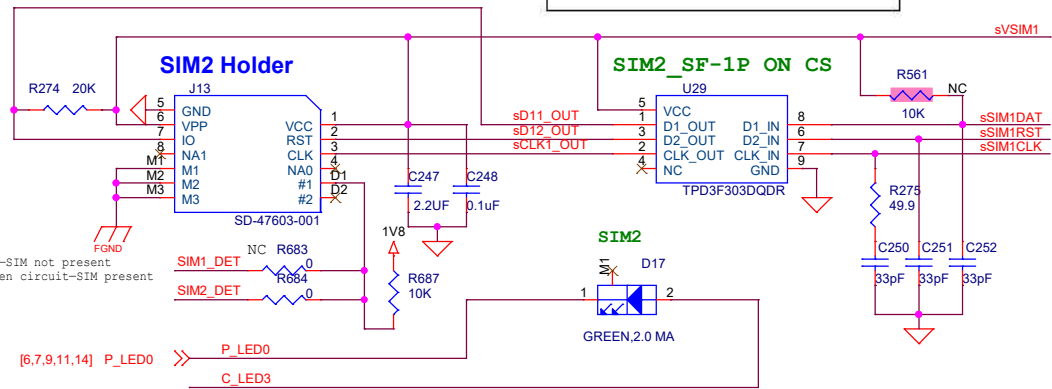
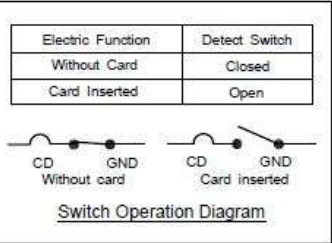


LTE and WIFI Modems



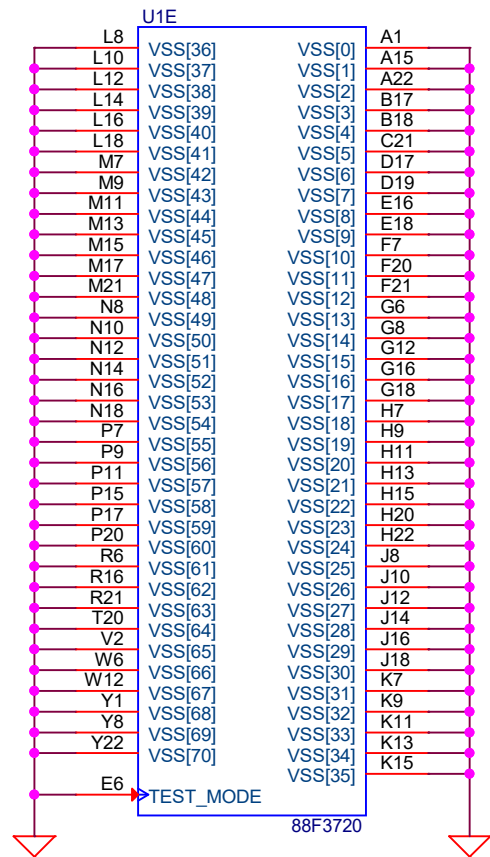
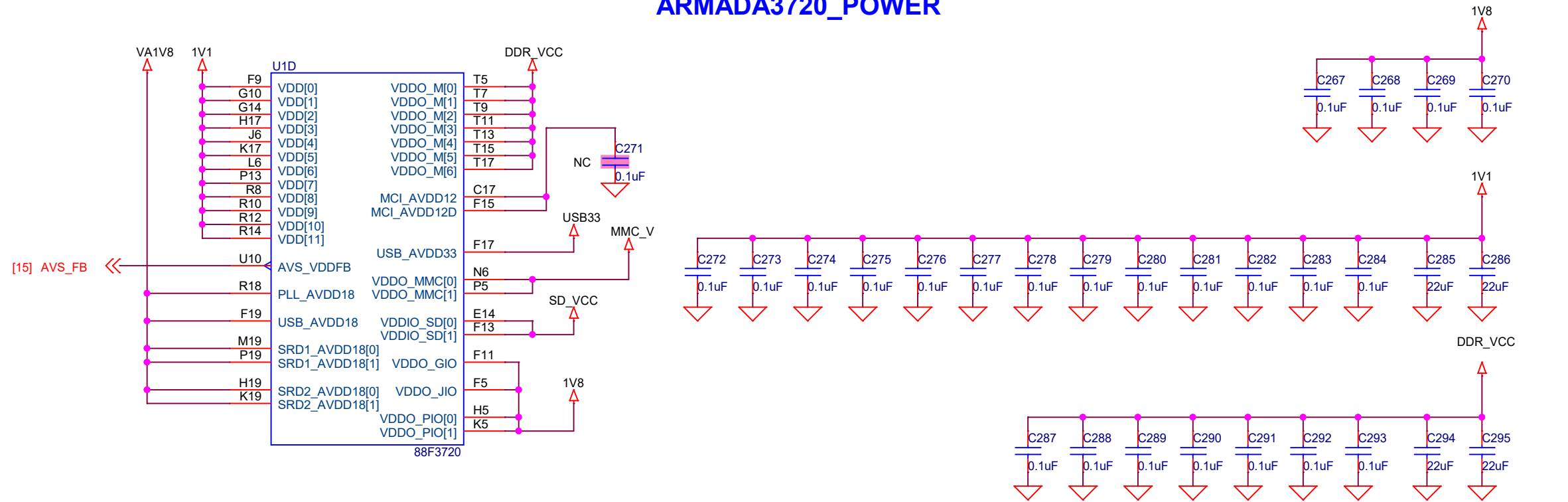
Designer : Andrey Ger / Ofer Ostrinsky	
Title MODEMS	
Design Name : SF-1P.REV0.7	Rev 07
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LTE SIM CARDS

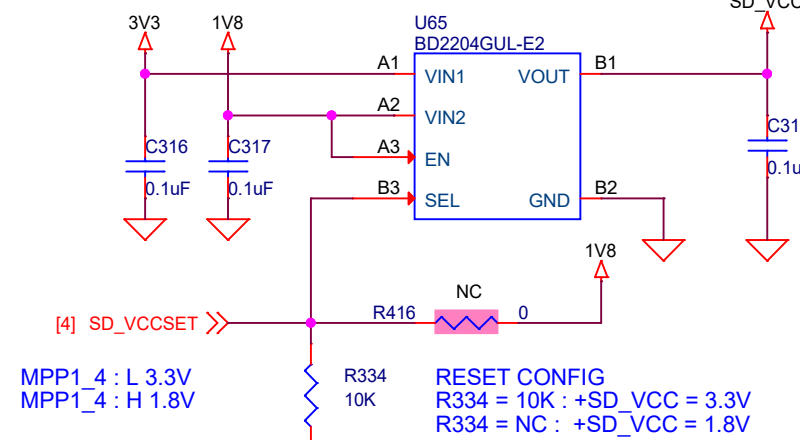
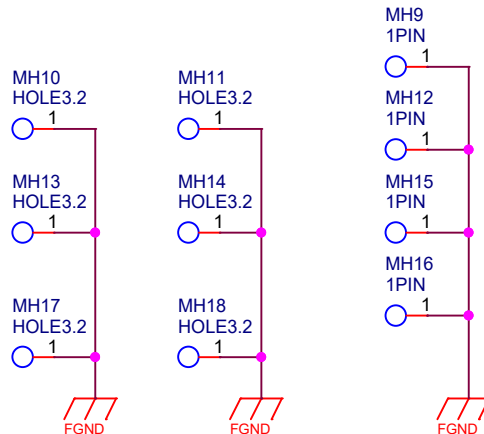


ARMADA3720_POWER

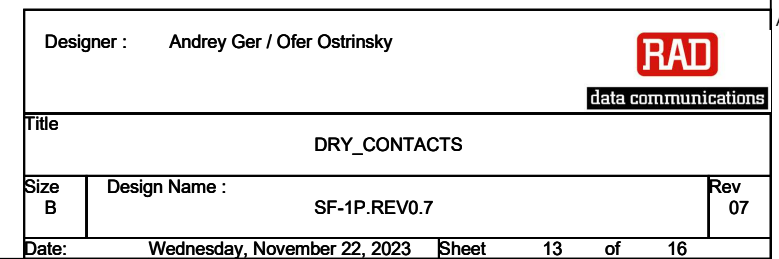
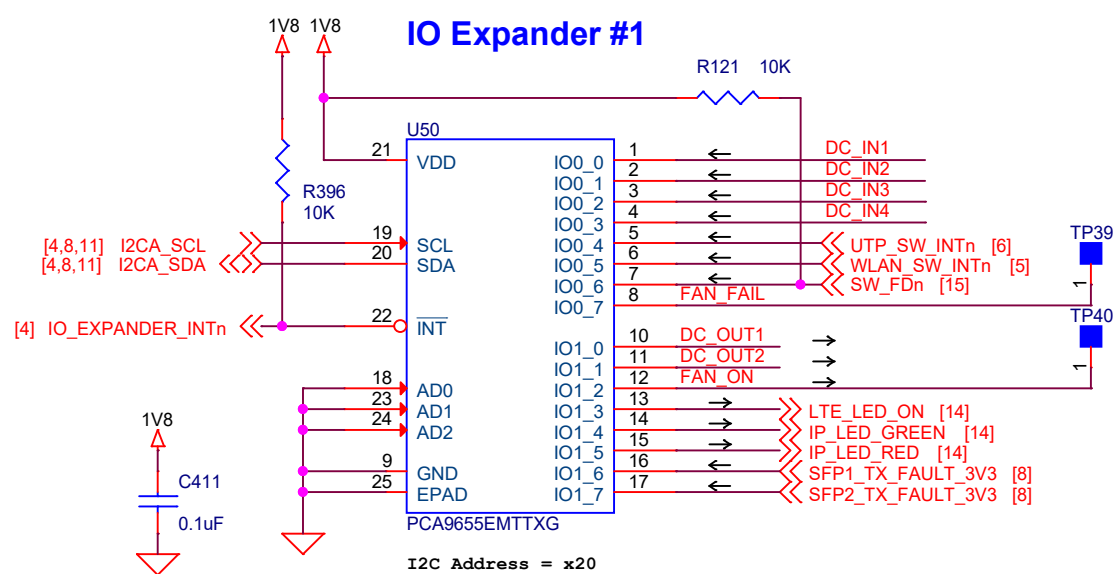
VDD: 1.1V
MCI_AVDD12D: NC
PLL_AVDD18: 1.8V
MCI_AVDD12D: 1.2V
SRD1_AVDD18: 1.8V
SRD2_AVDD18: 1.8V
USB_AVDD18: 1.8V
USB_AVDD33: 3.3V
VDDO_GIO: 1.8V
VDDO_JIO: 1.8V
VDDO_PIO: 1.8V
VDDO_MMC: 1.8V
VDDO_SD: 1.8V
USB_AVDD33: 3.3V
VDDO_M: 1.35V



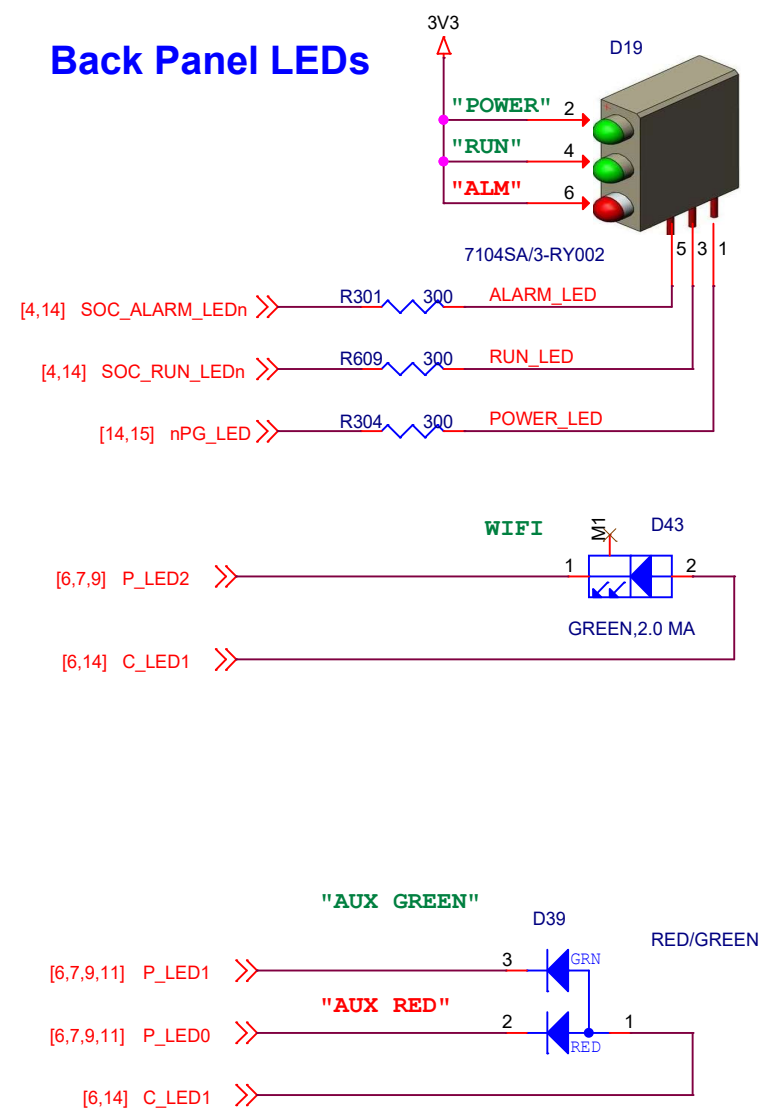
FOR U1
HEAT_SINK_31x31x14



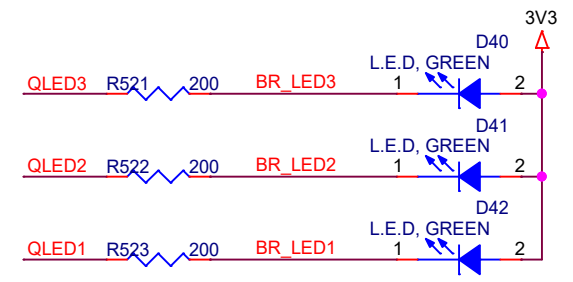
Designer : Andrey Ger / Ofer Ostrinsky		
Title CPU3720_POWER		
Size B	Design Name : SF-1P.REV0.7	Rev 07
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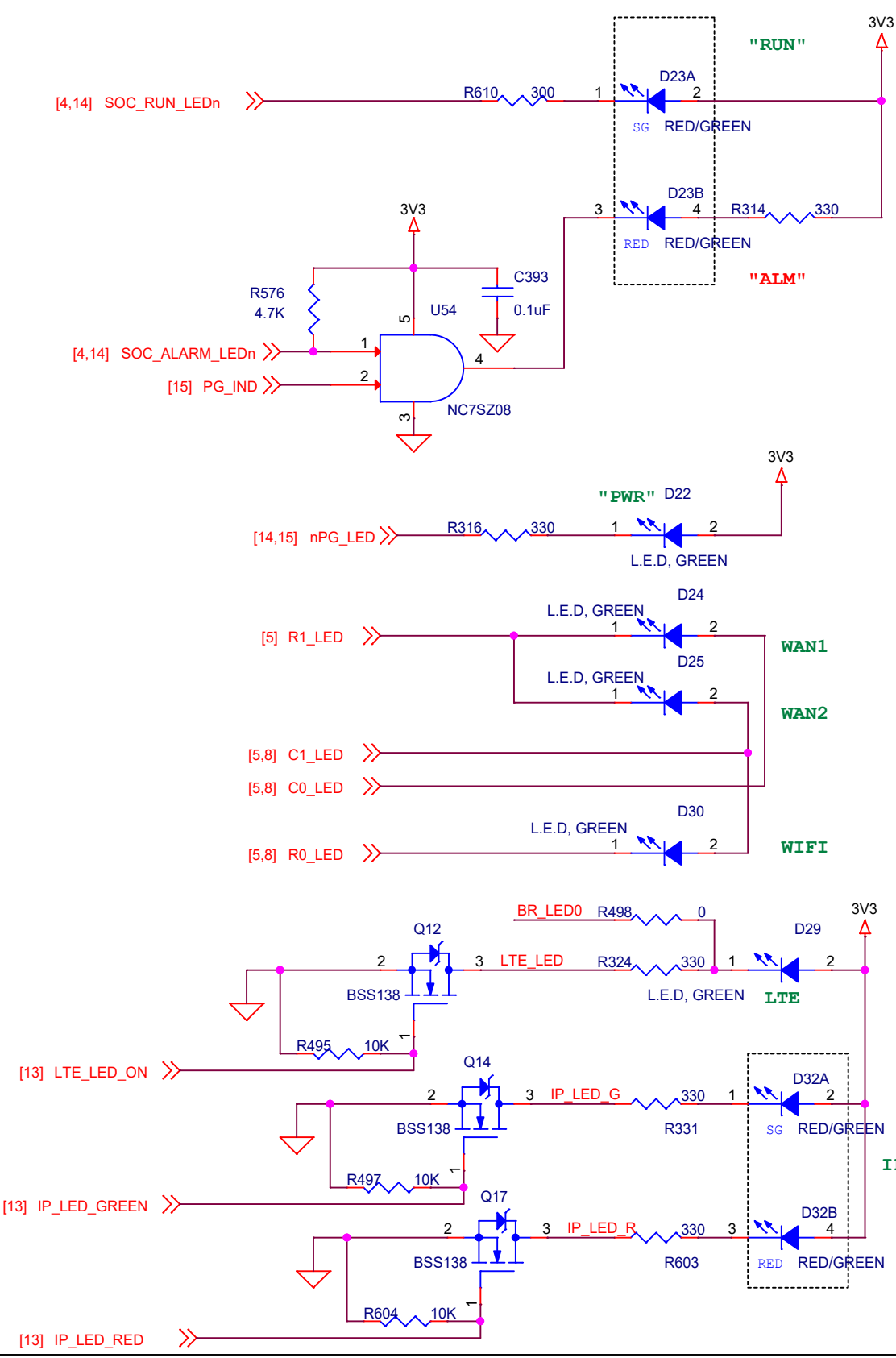
Back Panel LEDs



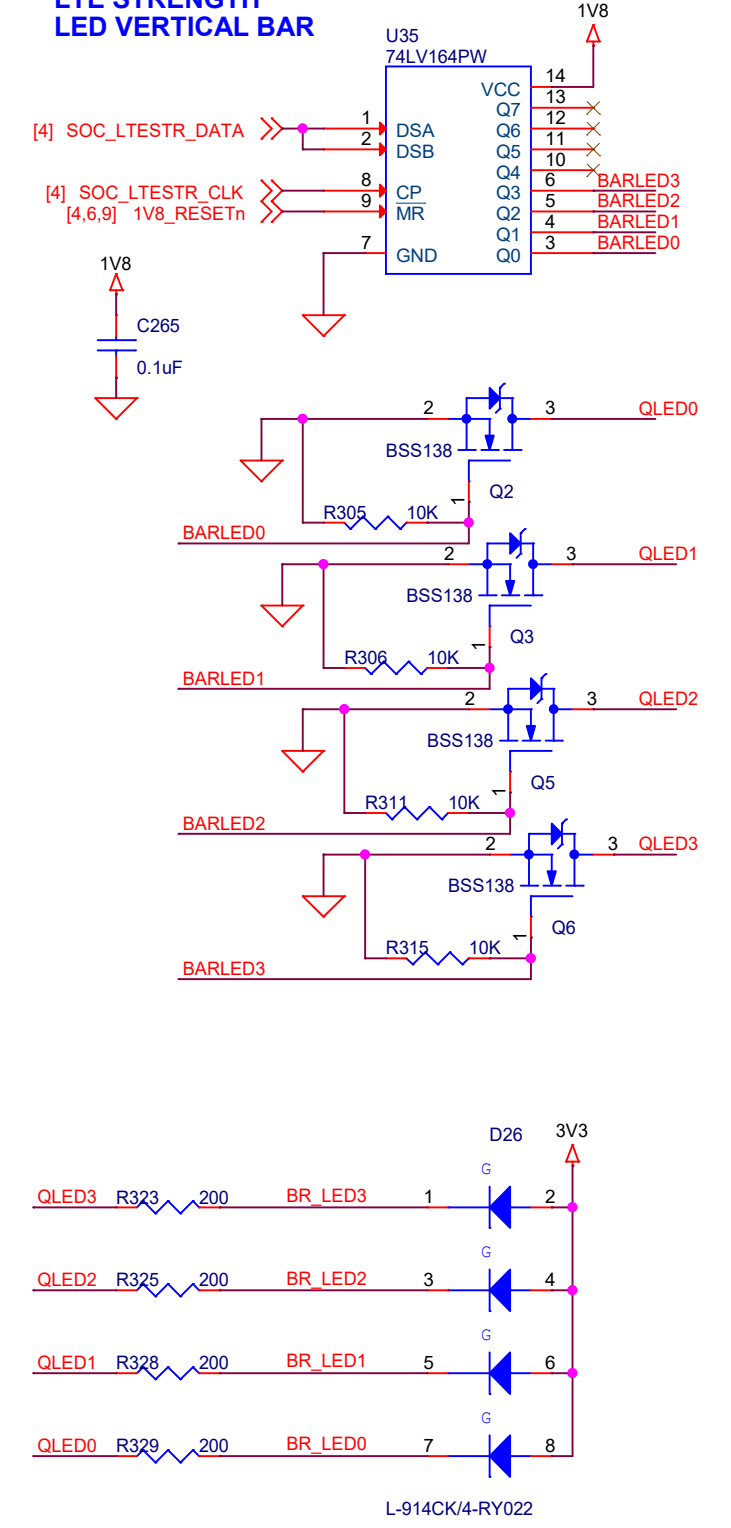
pCPE_TYPE 4 PANEL BAR




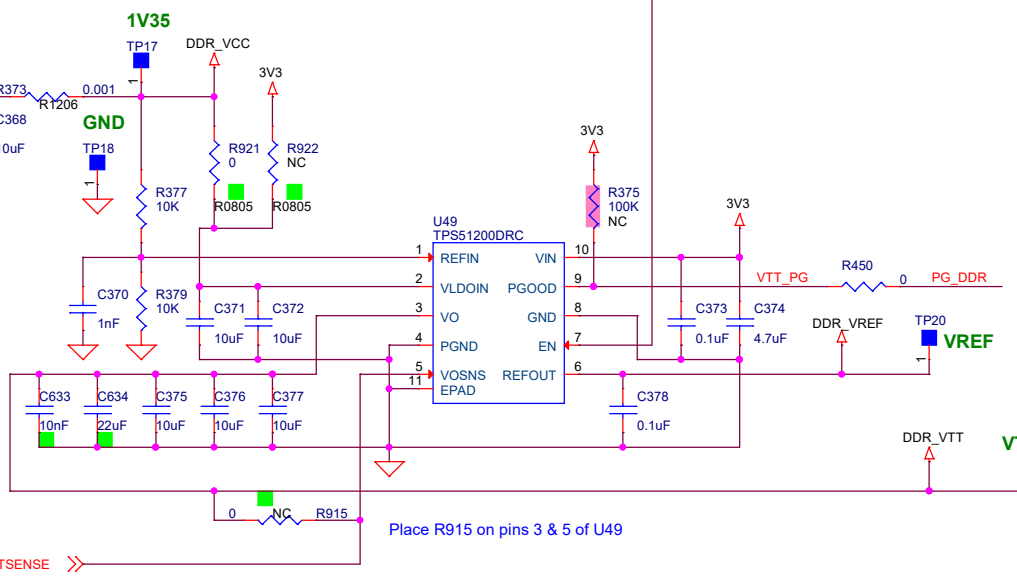
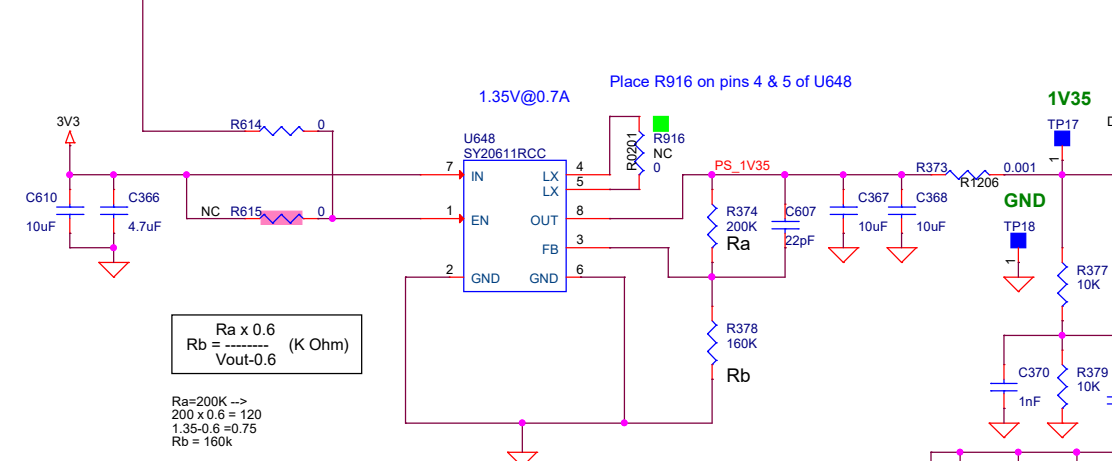
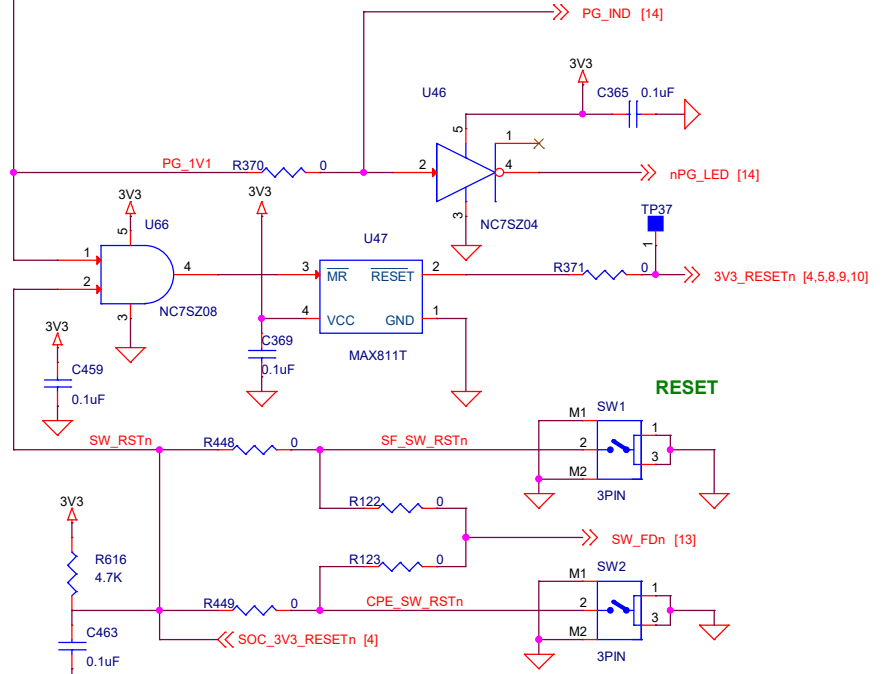
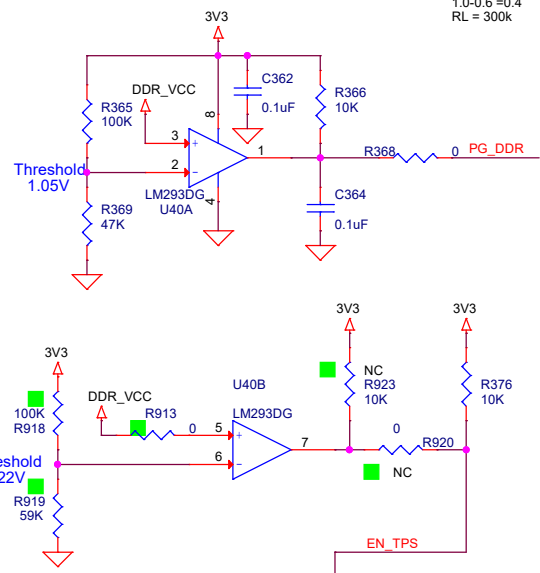
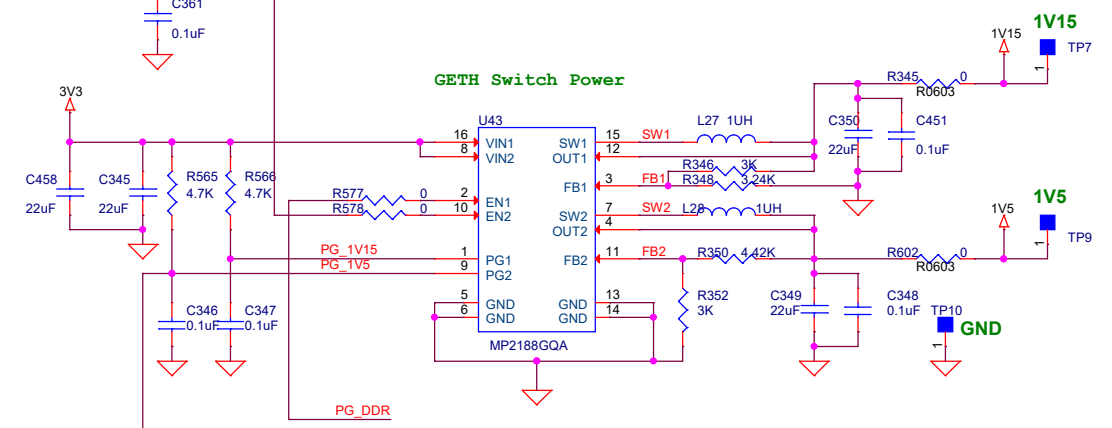
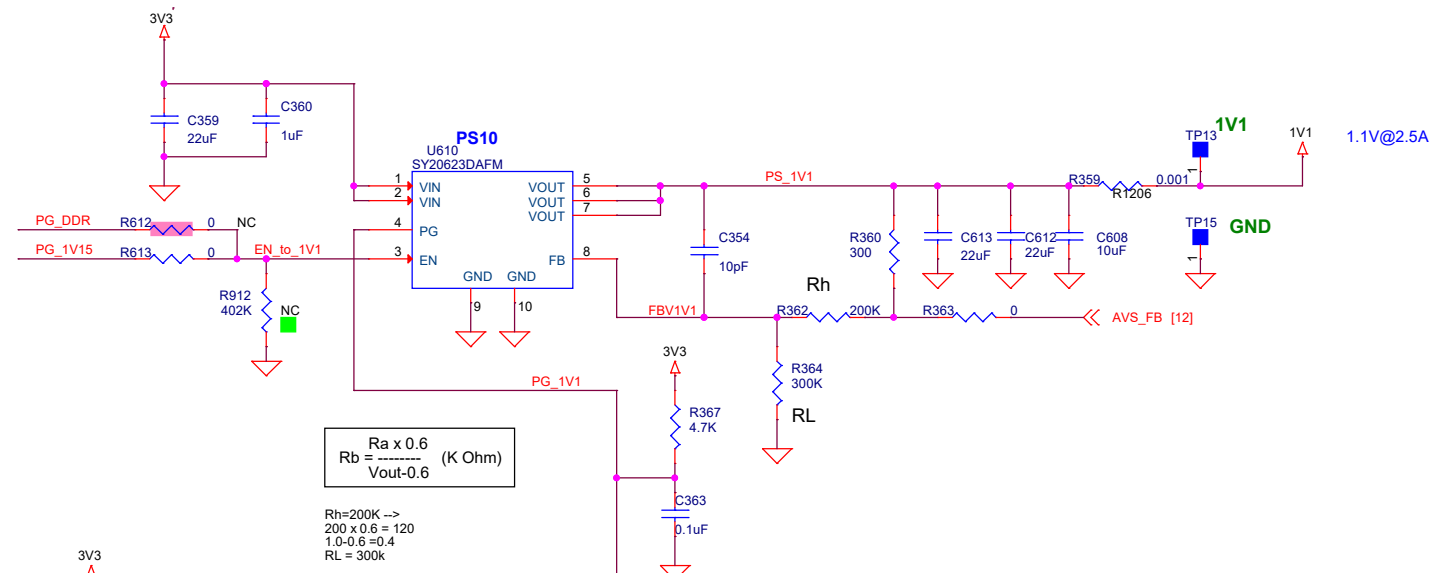
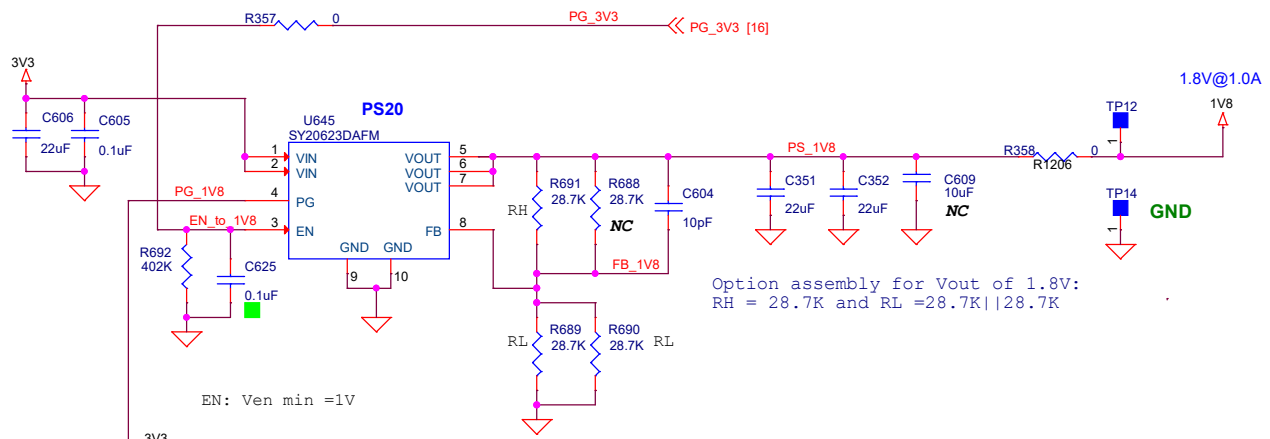
ETX-1p Front Panel LEDs




LTE STRENGTH LED VERTICAL BAR



Designer : Andrey Ger / Ofer Ostrinsky		 data communications	
Title LEDs			
Size B	Design Name : SF-1P.REV0.7		Rev 07
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Designer : Andrey Ger / Ofer Ostrinsky / Moshe Arad			data communications
Title			
Power Distribution System			
Size	Design Name :		Rev
C	SF-1P.REV0.7		07
Date:		Wednesday, November 22, 2023	
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Power Distribution System

