

# Nikhil Ganpat Navghade

Munich, Germany

Phone: +49 176 58609849 | Email: nikhil.nawaghadej@gmail.com

LinkedIn: <https://www.linkedin.com/in/nikhil-navghade/>

## Senior Radar Algorithm Engineer – FMCW, DSP & Radar Systems R&D

### Professional Summary

T-shaped Senior Radar R&D Engineer with 10+ years of deep specialization in FMCW radar algorithms, 1D–4D FFT pipelines, MIMO/DOA processing, antenna modeling, and embedded DSP optimization. Strong system-level engineering foundation complemented by FAE experience, enabling cross-functional collaboration, full-pipeline debugging (ADC → detection → angle), and practical end-to-end radar problem solving. Proven track record in developing radar processing chains, designing multi-core DSP architectures, and delivering high-performance ADAS radar solutions.

### Core competencies

- **Radar Signal Processing:** FMCW, Pulse Radar, range–Doppler–angle estimation
- **Radar Algorithms:** CFAR, noise estimation, Doppler artifact removal, sidelobe suppression, clustering, ambiguity resolution
- **MIMO & Beamforming:** azimuth/elevation, HRT-based elevation, antenna performance evaluation
- **ADAS Radar Systems:** Gen5/Gen6 automotive radar platforms, 4x4 corner radar
- **System & Software Architecture:** radar processing chain design, dataflow, I/O structures
- **Programming:** MATLAB/Simulink, Embedded C, C (MISRA), C++ (basic), Python (basic)
- **DSP & Embedded:** ARM Cortex-M, TI AWR2944, Calterah Alps-Pro, TS201, BF561, multi-core optimization
- **Tools:** Trace32, Visual Studio/VS Code, VDSP++, Jira, Confluence, Git, CI/CD
- **Development Methods:** Agile, unit & dynamic testing, coverage improvement
- **Architecture Tools:** HP DOORS, Enterprise Architecture tools, Draw.io
- **Soft Skills:** technical leadership, module ownership, training & mentoring

### Experience

Calterah GmbH — Radar System Engineer (Sept 2024 – Present)

- Performed system-level debugging and validation of the complete automotive radar signal processing chain (ADC sampling, calibration, detection, algorithm behavior verification, and angle estimation) using real-world radar captures, corner cases, and stress scenarios across multiple radar platform variants.
- Led root-cause analysis and resolution of 5+ critical system blockers related to OTP programming, Secure Boot enablement, Functional Safety (FuSa), and Ethernet interfaces during SoC bring-up.

- Reduced radar bring-up and issue resolution cycles by establishing structured debug workflows across signal processing algorithms, firmware, and SoC layers.
- Contributed to radar SoC feature enablement and validation by collaborating with internal R&D teams on detection and angle-estimation algorithm requirements, security, safety, and system architecture topics.
- Supported radar platform maturity through system characterization, internal knowledge transfer, and cross-team technical alignment.

#### Fusionride GmbH — Senior Radar Signal Processing Engineer (Feb 2022 – Sept 2024)

- Architected complete radar processing chain (1D–4D FFT, MIMO, beamforming) in MATLAB.
- Designed multi-core system architecture with optimized memory/runtime performance.
- Built antenna performance evaluation tools (beam patterns, sidelobes, virtual array checks), reducing analysis time from 1 week to 1 day
- Delivered first 4×4 corner radar prototype within 1 year and contributed to 6×8 front radar design.
- Led technical decisions for algorithms, architecture, and module integration.

#### Continental Automotive — Technical Specialist Radar (Jul 2018 – Feb 2022)

- Achieved 99.92% functional coverage for Gen5 radar validation.
- Implemented CFAR, elevation MIMO modules, and sidelobe suppression, noise estimation.
- Developed RPD/RSP modules on ARM M4, DSP, and MATLAB with significant runtime/memory improvements. Supported root cause analysis across DSP/M4 modules

#### Wavelet Technologies — Project Engineer (Jul 2015 – Jul 2018)

- Developed firmware for pulse wind profile radar and participated in full lifecycle development.

#### **Education**

- Masters in Embedded Systems & VLSI — Pune University, 2016 — CGPA 8.54/10
- Bachelor of Electronics & Telecommunication — Pune University, 2013 — CGPA 8.43/10

#### **Publications & Achievements**

- IEEE Conference Paper: "[Comparative study and implementation .... wind profiler radar](#)", 2017.
- Key Achievement: Pioneered introduction of first 4x4 corner radar product with real-time detections within one year at Fusionride | Received monetary award for developing a tool that significantly accelerated initial RSP bring-up and reduced engineering time

#### **Languages**

English, Hindi, Marathi, German (A1)