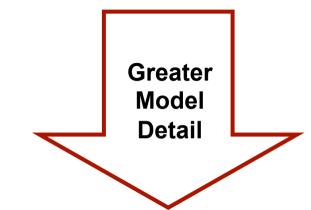


Modeling Towards Layout



Functional Level

Algorithm and ISA Development

Cycle Level

Design Space Exploration

Register Transfer Level

Area/Energy/Timing Validation and Prototype Development