16 words bit each) main mem 1024 blocks 2 Cacho Hage porty & valid (per block in cache) 1 por block 126 in main mem -> Lincohe
Tago > Which of those
126 it is mapped
to. Joys Toy Set/line offset Contrags extra 1024×16=> 214 14 -> @ fora word. Processor sends address of word in

F DATE: / /

PAGE: DATE: // cache controller a) is the word in the cake? the block contains the word addy 14 -> last 4 bits are offset a Re remove offset Softe nous velhaus 10 bits of these 10 last 3 are set no got to line in to by the 3 / bits. K rem 3 bits 7hits -> comp with tay chak nothing valid Edirty maching and valid. 1=1 readfull using lobit read/usite using the ering corret last 4 bits of block. Modale mem adress dirty data so block