DATA SHEET

LG5QxxxA Series *(OTP)*

Single-Chip 4-bit MCU & 4-ch Speech/Midi

Version 1.0

Jul. 29, 2021

Revision History

Version	Date	Description	Modified Page
1.0	2021/07/29	Formal release.	-
2.0	2022/04/26	Add NY35QXXXAS8,NY5Q342AS8	-

1. 概述

LG5Q 系列產品爲多功能單晶片CMOS語音合成4位元微控制器，是爲了支援新 LG5 (LG5+) 系列所專門開發的嵌入式EPROM架構的OTP IC (One Time Programmable)。提供4通道的語音/Midi合成功能，語音合成方式採用先進的高音質ADPCM演算法，最高採樣率可達CD音質44.1KHz，且硬體有音量控制。提供兩種聲音輸出方式可供選擇，一種PWM輸出和一種DAC輸出。PWM 模式內建增強降低底噪輸出。MCU 使用RISC精簡指令集架構，共有43條指令，除了少數指令需要2個時序，大多數指令都是1個時序即可完成，可以很方便的以程式控制來完成不同的應用。利用精準的+/- 0.5%內阻震盪，客戶可以不需外加震盪電阻。提供待機模式(Halt mode)，可大幅度的節省功耗；另外還提供慢速模式(Slow mode)，可以降低功耗。

2. 功能

- 寬廣的工作電壓：2.0V ~ 5.5V。
- 4-bit RISC 精簡指令集架構的微控制器，共有43條指令。
- 共有9個OTP母體，最大母體的ROM容量為 832Kx10-bit，程式和資料共用同一塊ROM。ROM容量，秒數和I/O腳數如下：

IC Type	Time* (sec)	ROM (bits)	RAM (bits)	I/O	PWM-IO	Ch.	DAC
LG5Q020A	18.3	48K x 10	248 x 4	8	-	4	Y
LG5Q040A	38.3	96K x 10	248 x 4	8	-	4	Y
LG5Q060A	58.3	144K x 10	248 x 4	16	8	4	Y
LG5Q092A	91.6	224K x10	248 x 4	16	8	4	Y
LG5Q172A	171.6	416K x 10	248 x 4	16	8	4	Y
LG5Q342A	345	832K x 10	248 x 4	20	8	4	Y

* 聲音秒數以 6 KHz 4-bit ADPCM 計算.

- 248x4-bit RAM，支援間接定址模式。
- 1MHz 或 2MHz指令頻率。(使用兩通道以上需選擇 2MHz)
- 提供慢速模式(Slow mode)，可降低功耗。*(注意：由於慢速模式的時間誤差較大，不建議使用在計時的應用)*
- 提供待機模式(Halt mode)，可節省功耗，靜態電流 3V 時(Isb)小於1uA。
- 精準的+/- 0.5% 內阻震盪。
- 提供低壓復位(LVR=1.8V)，看門狗計時(WDT)，I/O復位功能(External Reset)。
- 一個中斷輸入可連結到一組獨立的堆棧(Stack)，並有多種中斷來源可以使用。
- 最多 20 根彈性的雙向 I/O，每根 I/O 功能皆可由單獨暫存器控制。
- IR紅外線輸出: 提供31KHz~58KHz可選擇的紅外線頻率輸出，並可選擇高電平/低電平編碼。
- 多組 PWM-IO 分時多工，每通道 8-bit 解析度。

- 提供4通道的語音/Midi合成功能，可以單獨設定每個通道爲語音或Midi輸出。
- 更先進的高音質ADPCM語音合成演算法，可以經由簡單的調整採樣位數來提升音質。
- 新高音質合成演算法可混合 ADPCM 或 PCM，ADSR 段內建 256 階 Midi 包絡 (Envelope) 合成。
- 一組12-bit PWM純硬體輸出，可以直接驅動喇叭或蜂鳴片；一組12-bit DAC純硬體輸出，可以外加放大線路來放大音量 (通常用於多通道輸出)。
- 提供三階音量PWM輸出 (Normal/ Large/ Ultra)，輸出語音不需外加三極管放大。
- 內建16階硬體音量控制(Volume Control)，用於進行整體音量的控制。
- 支援 Quick-IO 訊號控制。
- 內建低電壓偵測 (LVD) 可用來監控當前電壓狀態，避免電壓不穩定導致系統出錯。
- 提供特殊的快速燒錄模式，以加快OTP燒錄時間。
- 支援特殊的ICP (In Circuit Programming) 燒錄功能，以方便客戶先組裝PCBA模組再進行燒錄。
- 提供可程式的Code資料保護模式。*(當Security-Bit 被燒斷後，資料將無法讀取。)*
- 提供多種出貨型態，以滿足客戶不同的應用需求。

1. GENERAL DESCRIPTION

The LG5Q series IC is a powerful 4-bit micro-controller based sound processor with embedded OTP (One Time Programmable) from New LG5 series (LG5+). There are 4 channels that are configured as speech or MIDI, and all of them can be auto-played back simultaneously. By using the high fidelity ADPCM speech synthesis algorithm, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz and different volume level are supported. It is also equipped two kinds of audio outputs with fine resolution, including a current D/A converter and a PWM direct-drive. PWM mode also enhanced with noise-shaping function. The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 43 instructions, and most of them are executed in single cycle. Furthermore, in addition to the HALT mode (sleep mode), it offers the SLOW mode to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 2.0V to 5.5V.
- 4-bit RISC type micro-controller with 43 instructions.
- There are 6 OTP bodies. 832Kx10-bit ROM is the maximum. Program and voice data share the same ROM space. The voice duration, ROM size and I/O counts are shown below.

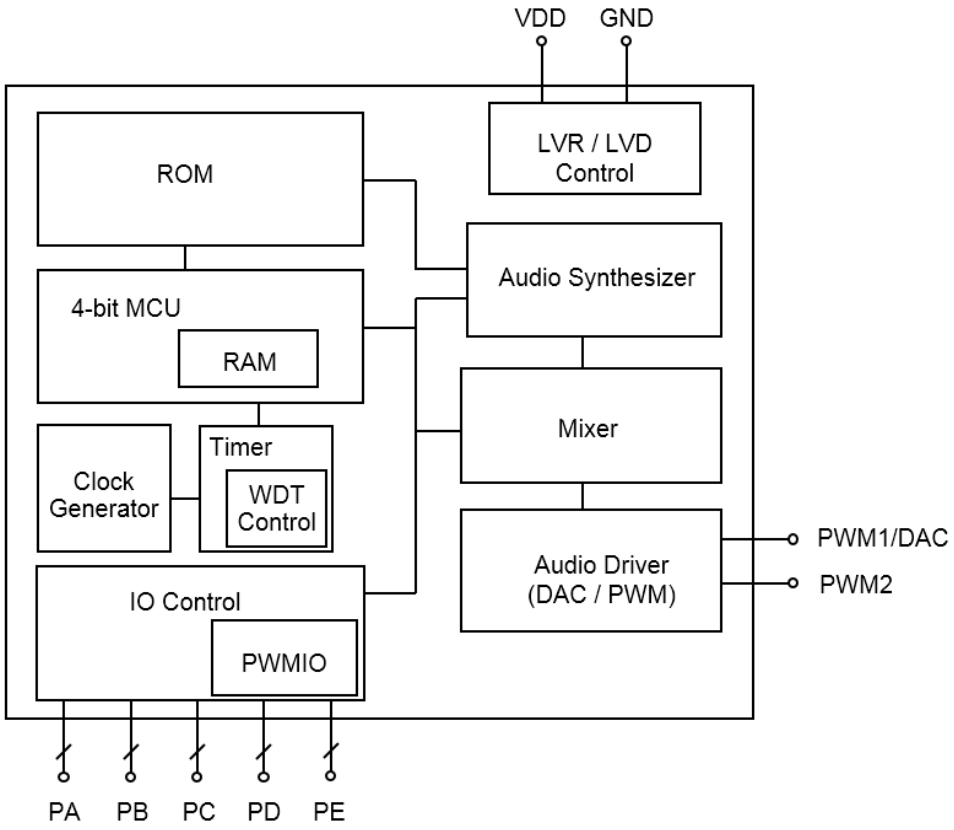
IC Type	Time* (sec)	ROM (bits)	RAM (bits)	I/O	PWM-IO	Ch.	DAC
LG5Q020A	18.3	48K x 10	248 x 4	8	-	4	Y
LG5Q040A	38.3	96K x 10	248 x 4	8	-	4	Y
LG5Q060A	58.3	144K x 10	248 x 4	16	8	4	Y
LG5Q092A	91.6	224K x10	248 x 4	16	8	4	Y
LG5Q172A	171.6	416K x 10	248 x 4	16	8	4	Y
LG5Q342A	345	832K x 10	248 x 4	20	8	4	Y

* The voice duration is calculated at 6 KHz by 4-bit ADPCM algorithm.

- 248x4-bit RAM maximum, indirect RAM addressing mode is supported.
- 1MHz or 2MHz instruction frequency (2MHz is required for over 2-ch speech or MIDI).
- SLOW mode to operate at low power consumption.
- HALT mode to save power, less than 1uA@3V standby current.
- Built-in RC oscillation is accurate with +/- 0.5% frequency deviation.
- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.
- Single interrupt entrance with an independent stack, multiple interrupt sources.
- Up to 20 flexible Bi-direction I/Os. Each I/O direction is independently controlled by individual register bit.
- Shared pins to provide IR carrier and external reset feature. (Mask option)
- Selection of IR carrier frequency and data high/low IR output is supported.
- Multiple groups of PWM-IO share a group of time, each channel has 8-bit resolution.

- LG5Q series are all 4 channels and can play simultaneously; each channel can be arbitrarily assigned as speech or MIDI channel based on the product spec.
- New high fidelity ADPCM speech synthesis algorithm.
- New high fidelity mixed ADPCM or PCM speech synthesis algorithm and ADSR with 256-step envelope for MIDI synthesis.
- High quality 12-bit D/A converter or 12-bit PWM driver.
- Support 3 levels Normal, Large, Ultra PWM current output.
- 16-level digital volume control for synthetic Speech/MIDI.
- Quick-IO control supported.
- Low Voltage Detector (LVD) is built-in for monitoring the status of power and protect malfunction if unstable power is given.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP *(In Circuit Programming)* writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*
- Various shipping type for different application requirement.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

Pin	ATTR.	Description
VDD#	Power	Positive power
GND#	Power	Negative power
PWM1/DAC	O	PWM1 output or DAC output
PWM2	O	PWM2 output
PA0~3	I/O	Bit 0~3 for Port A
PB0~3	I/O	Bit 0~3 for Port B
PC0~3	I/O	Bit 0~3 for Port C
PD0~3	I/O	Bit 0~3 for Port D
PE0~3	I/O	Bit 0~3 for Port E

* LG5Q020A、LG5Q040A : PA0~PB3

* LG5Q060A、LG5Q092A、LG5Q172A : PA0~PD3

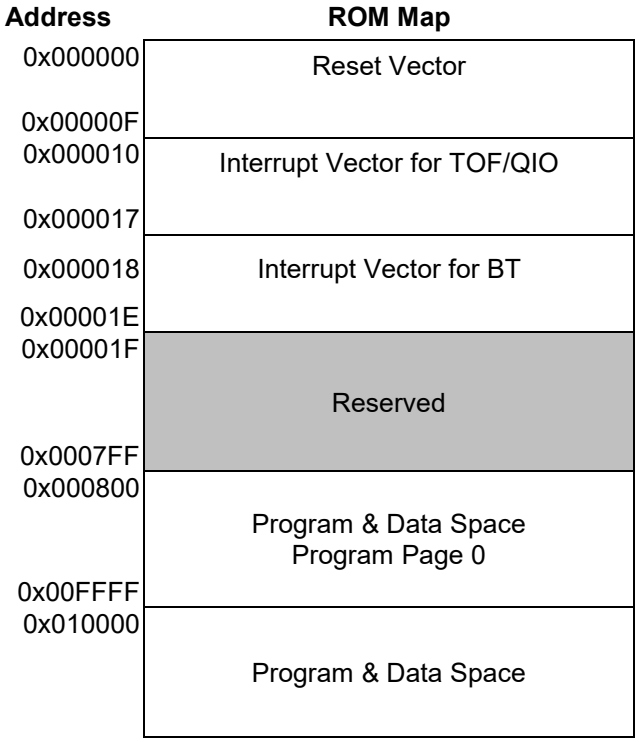
* LG5Q342A : PA0~PE3

5. MEMORY ORGANIZATION

There are maximum 832K words ROM, 248 nibbles of RAM and some dedicated system control register. The registers are divided into normal system registers and 8 nibbles of Multi-function registers.

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 16-bit length address of ROM, the program page size is 64K words.



5.2 RAM

LG5Q provide 248 nibbles RAM space. The address for RAM is 0x008~0x0FF. The first space from 0x08 to 0x3F is function RAM space, it only needs one-word instruction operation. And the second space from 0x040 to 0x0FF is data RAM space; the related operation is two-word instruction.

In addition to the immediate addressing mode, the indexed addressing mode is also supported. The page and address of the indexed RAM should be stored into RPT3 and RPT2 first, and users can read from or write in the XMD memory register to realize the indexed ROM access.

Address	RAM map
0x000 0x007	Memory Register
0x008 0x03F	56 nibble Function RAM
0x040 0x0FF	192 nibble Function RAM
0x100 0x1X7	Reserved
0x1C8 0x1CF	System registers
0x1D0 0x1DF	Reserved
0x1E0 0x1EF	System registers
0x1F0 0x1F3	Reserved
0x1F4 0x1FF	System registers

6. CLOCK GENERATOR

The clock generator is a Ring oscillator, and users can only select the internal resistor oscillation (INT-R). The INT-R oscillator accuracy is up to ± 0.5%.

7. INTERRUPT GENERATOR

There is one hardware interrupt and it has 3 different sources in LG5+. The interrupt event can be a fixed interval of the system base timer (BT), the timer overflow flag (TOF), or the quick-IO flag (QIOF). The TOF can be selected as one of the sample rate timer overflow by the register INT, and the QIOF arises as a QIO control code of any channel coming up. There is a system base timer in the LG5+ IC, which functions as long as the IC isn't in the halt mode. We provide 4 fixed intervals from the system base timer for interrupt source: 0.128, 0.256, 0.512 and 1.024ms.

As an interrupt occurs, LG5+ stores the accumulator (ACC), carry flag (C), zero flag (Z) and RAM page (PG) automatically. Then move PC to STK, and jump to the interrupt vector (0x000010 or 0x000018). An interrupt routine finishes with an IRET instruction. The IC draws the ACC, C, Z and PG back, and moves STK to PC back to jump back the main program.

The interrupt event of BT will be automatically cleared after entering the interrupt routine, but the TOF and QIOF have to be cleared by users.

8. IO PORTS

There are at most 20 I/O pins, designated as PAx through PEx, and x=0~3. All the I/O pins are bi-directional. An individual and independent register bit can determine the direction of each I/O pin. These register bits are PAIO ($1E1), PBIO ($1E3), PCIO ($1E5), PDIO ($1E7), and PEIO ($1E9).

Using as input pin of each I/O, there are 3 kinds of mask option. Users can select input with pull-high resistor, input without pull-high resistor, or input with register-controlled pull-high resistor (high-to-low wakeup only). If users want to enable/disable pull-high resistor by register during program execution, only high-to-low level change on this pin can wakeup LG5Q. On the other hand, if the pull-high resistor is fixed by option, either high-to-low or low-to-high level change on this pin can wakeup LG5Q. Users can refer user manual for details. The pull-high resistor of all the I/O pins has two kinds of option: weak and strong. The weak one is about 1.2MΩ@3V for normal application and the strong one is about 100KΩ@3V usually for key matrix function. When users decide this option, the same strength of pull-high resistor will be applied to all I/O pin.

Using as output pin of each I/O, there are 3 kinds of mask option. Users can select output with normal drive current and normal sink current or normal drive current and large sink current.

The PX0 port means the PA0, PB0, PC0, PD0, or PE0 port can also be optioned as an external reset pin or an infrared (IR) output pin. A reset port can possess a pull-high resister or not, and an IR port can be initial low or high and also large sink current or not.

9 LOW VOLTAGE DETECTOR (LVD)

There is one hardware voltage detector in LG5Q. It offers four levels for various application, 2.0v, 2.2v, 2.4v, 2.8v, 3.0v, 3.3v and 3.6v controlled by register $LVD. The voltage detection function has to be enabled first, then select specific level for application, the flag will go to high while VDD is lower than selected level. User can check power status by setting different level and monitoring the flag.

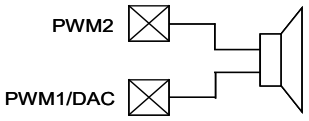
10. AUDIO SYNTHESIZER STRUCTURE

There are 4-ch speech or MIDI audio output, and all modes are auto-played back by hardware. Different channel mode possesses different hardware structure. It provides a hardware mixer to mix the channel data. Two audio output stages: DAC and PWM are supported. Please noticed that 2MHz is required for over 2-ch speech or MIDI.

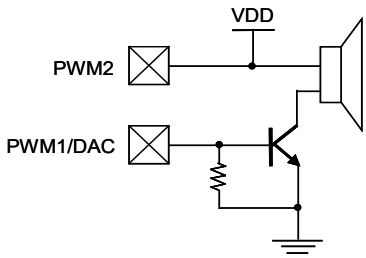
10.1 Audio Output

By set the AUD register, PWM or DAC can be easily chosen as the audio output stage. Besides, it provides a pad detecting mechanism. The pad detecting mechanism detects the PWM2 pad during the reset initialization period, and sets the initial value of the audio output register as PWM if the PWM2 connection is floating, or sets the initial value of the audio output register as DAC if the PWM2 connection is high. In conclusion, connect the speaker to PWM1 and PWM2 only if using PWM, otherwise connect PWM2 to VDD if using DAC. Since the mechanism sets only the initial value of AUD, don't change the value of the AUD register if the pad detecting mechanism is adopted.

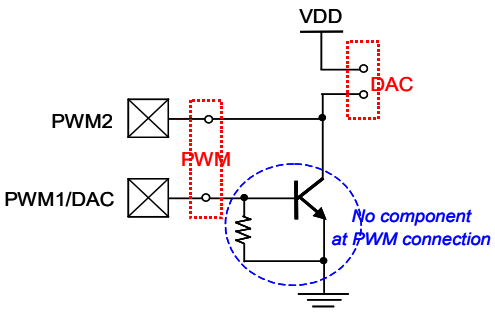
PWM2 Pad	Audio Output Initialization
Speaker (Floating)	PWM
VDD	DAC



PWM Output Connection



DAC Output Connection



PWM/DAC Connection Together

When using the PWM output, we provide an option of normal PWM current, large PWM current or ultra PWM current for different customer demand. The ultra PWM current consumes more current and makes sound louder.

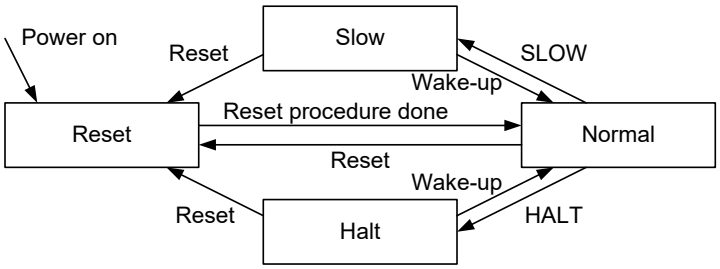
10.2 Volume Control

Both PWM and DAC supports 16 steps hardware volume control by the VOL register, 0x0~0xF.

11 WATCH-DOG TIMER (WDT)

To recover from program malfunction, the LG5+ IC supports an embedded watch-dog timer reset. The WDTR function always works with the program executing. Users have clear the WDT periodically to prevent from timing up with a reset generation. Typically, the minimum time-up period of the WDT is about 15ms. Users can move a 0x5 value to the 0x1CA BTF system register to clear WDT.

12. Power Saving Mode



Power Saving Mode Flow Chart

12.1 Halt Mode

The system enters the halt mode if the HALT command executed. The halt mode is also known as the sleep mode. As implied by the name, the IC falls asleep and the system clock is completely turned off, so all the IC functions are halted and it minimizes the power consumption.

The only way to wake-up the sleeping system is an input port wake-up. The IC keeps monitoring the input pads during the halt mode. If the input status of any input pad differs from the corresponding port register, the system will be waked-up. Then the succeeding instructions after the HALT instruction will be executed after the wake-up stable time (about 48us). So before executing the HALT instruction, users have to keep in mind to store the current input port statuses into port registers.

If the IC is waked-up from the halt mode by a reset port, it goes into the reset procedure.

12.2 Slow Mode

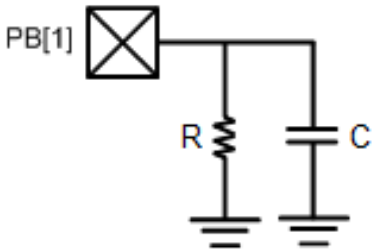
The system enters the slow mode if the SLOW command executed. The system clock in the slow mode slows down about 32 times slower than in the normal mode. The difference between the halt mode and the slow is only the system clock. So the IC can be waked-up from the slow mode by the interrupt in addition to the input port. Since the sample rate timer and the audio engine are suspended during the slow mode, interrupt from TOF and QIOF in the slow mode can't operate, of course can't wake-up the system.

The input wake-up manner is the same as the halt mode. So before executing the SLOW instruction, users have to keep in mind to store the current input port statuses into port registers. If the IC is waked-up from the slow mode by a reset port, it goes into the reset procedure. After the IC is waked-up by the input port or an INT of BT, the succeeding instructions after the SLOW instruction will be executed after the wake-up stable time (128us maximum).

Remember to turn off the audio output before entering to the slow mode.

12.3 RC Slow Mode

Another power saving mode is RC Slow mode, using external components with PB[1] and HALT commands, an application example is shown below.



There are three differences between using RC slow mode and slow mode. The first is that the user can adjust the value of R and C to determine the wake-up interval, instead of using the fixed BT interrupt. The second is that under the same interval time, the value of R can be increased, which saves more power during work. Third, the interval time of slow mode between different ICs will be slightly different and cannot be corrected. In RC slow mode, all products can get closer results by adjusting the value of RC. And it should be noted that the RC slow mode requires a resistor and a capacitor for charging and discharging, and the charging and discharging time will vary slightly with the voltage.

14. ELECTRICAL CHARACTERISTICS

14.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	-20 ~ +70 (*)	°C
Tst	Storage Temperature	-40 ~ +125 (**)	°C

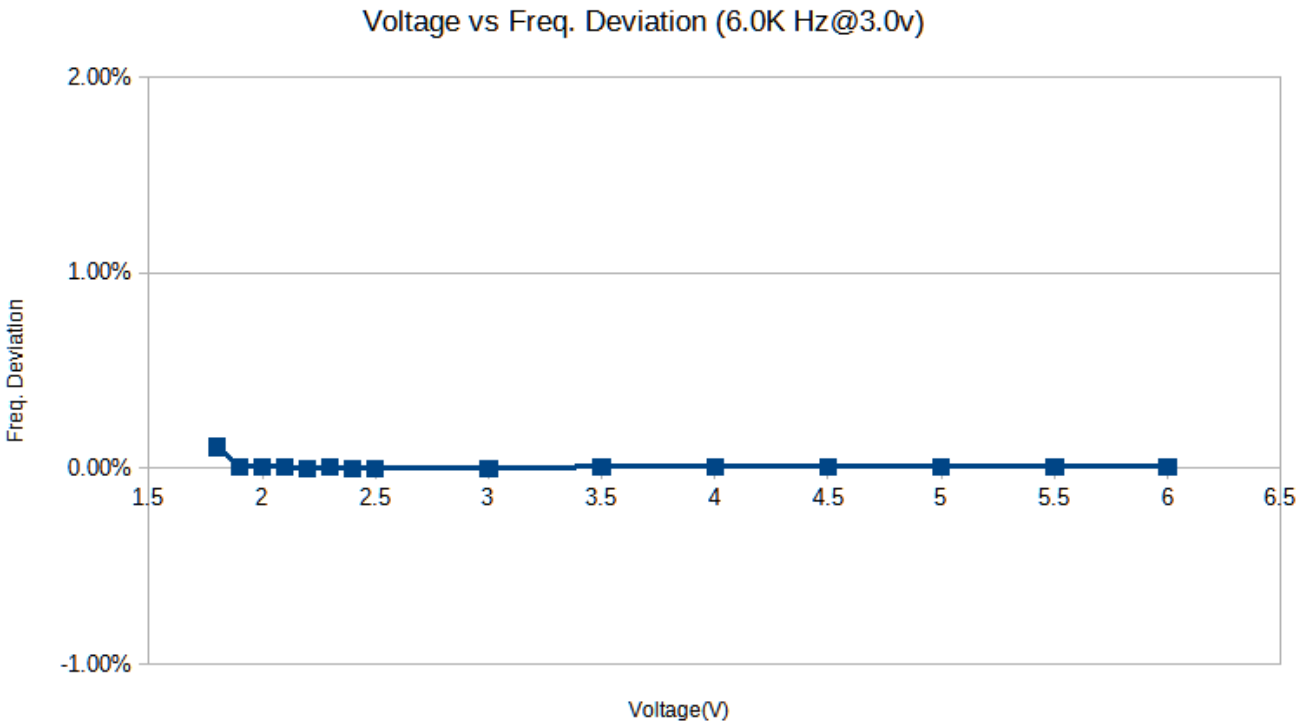
(*) Please make sure all other components can meet temperature range.

(**) SOP package only.

14.2 DC Characteristics

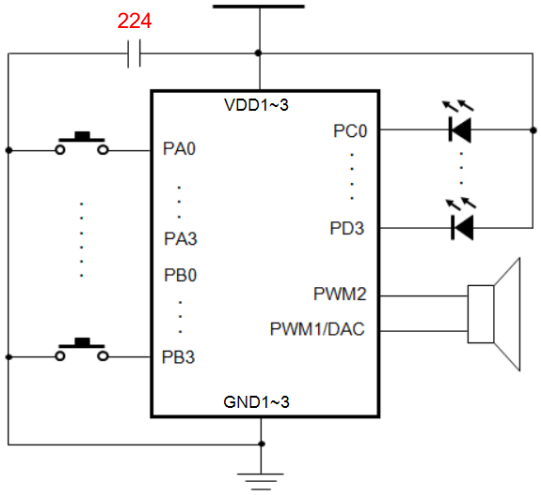
Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	2MHz
I_{SB}	Supply current	Halt mode	3		1		uA	Sleep, no load
			4.5		1			
I_{SL}		Slow mode	3		30		uA	BT=1ms, no load
			4.5		35			
Iop		Operating mode	3		0.9		mA	2MHz, no loading
			4.5		1			
I_{IL}	Input current (Internal pull-high)	Weak (1.2M ohms)	3		2.5		uA	V_{IL}=0V
			4.5		7.4			
		Strong (100K ohms)	3		35		uA	
			4.5		70			
I_{OH}	Output high current		3		-7		mA	V_{OH}=2.0V
			4.5		-11			V_{OH}=3.5V
I_{OL}	Output low current (Normal current)		3		11		mA	V_{OL}=1.0V
			4.5		19		mA	
	Output low current (Large current)		3		23		mA	
			4.5		36		mA	
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
	PWM output current (Ultra)		3		80		mA	
			4.5		125			
I_{DAC}	DAC output current		3		1.4		mA	Half scale
			4.5		1.6			
△F/F	Frequency deviation by voltage drop		3		-0.5		%	Fosc(3.0v)-Fosc(2.4v) / Fosc(3v)
			4.5		0.5			Fosc(4.5v)-Fosc(3.0v) / Fosc(4.5v)
△F/F	Frequency lot deviation		3	-0.5		0.5	%	Fmax(3.0v)-Fmin(3.0v) / Fmax(3.0v)
Fosc	Oscillation Frequency		-	1.90	2	2.05	MHz	VDD=2.0~5.5V

14.3 Voltage vs. Frequency

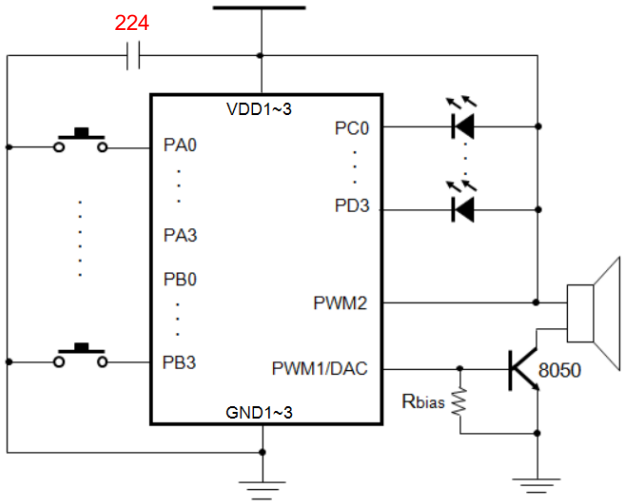


15. APPLICATION

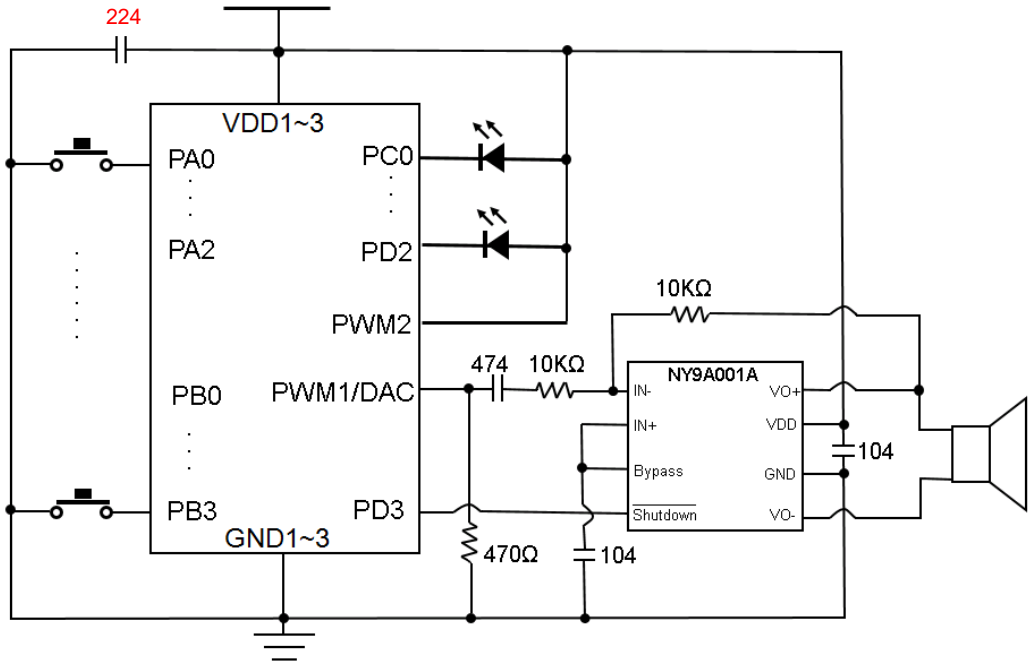
(1) PWM Direct-Drive



(2) DAC Output with BJT

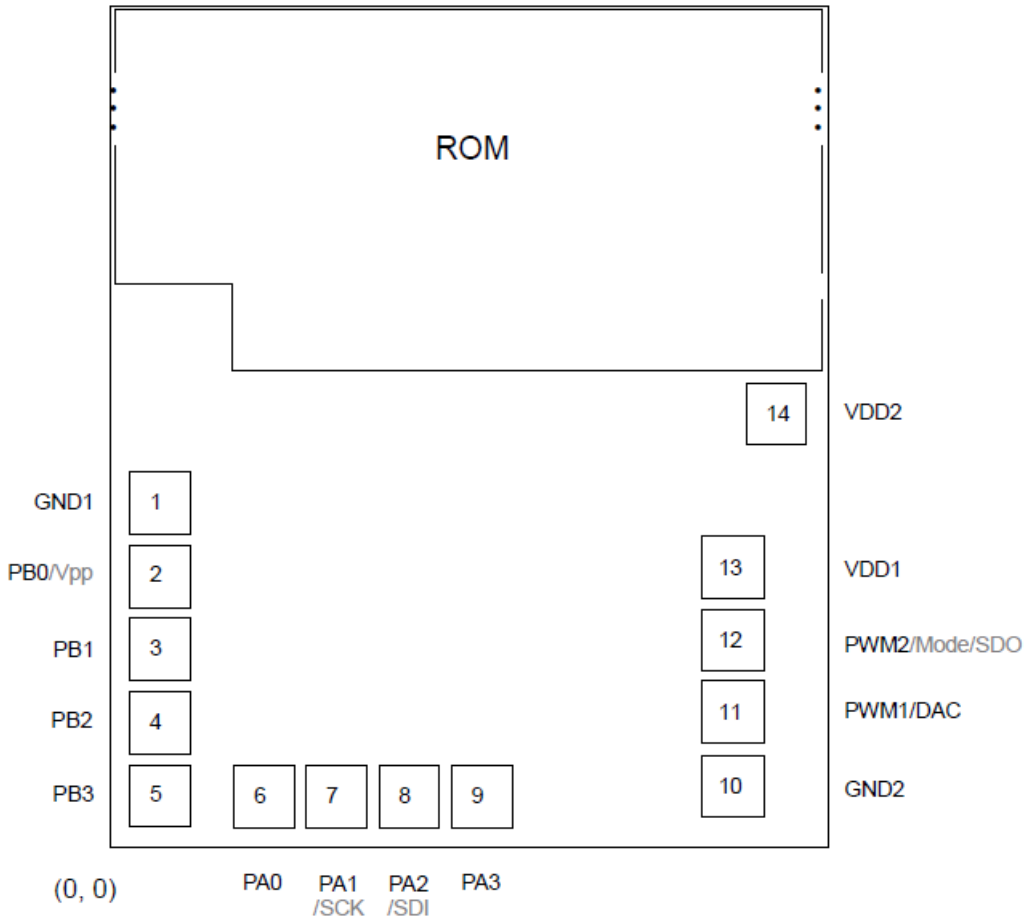


(3)DAC Output with Amplifier

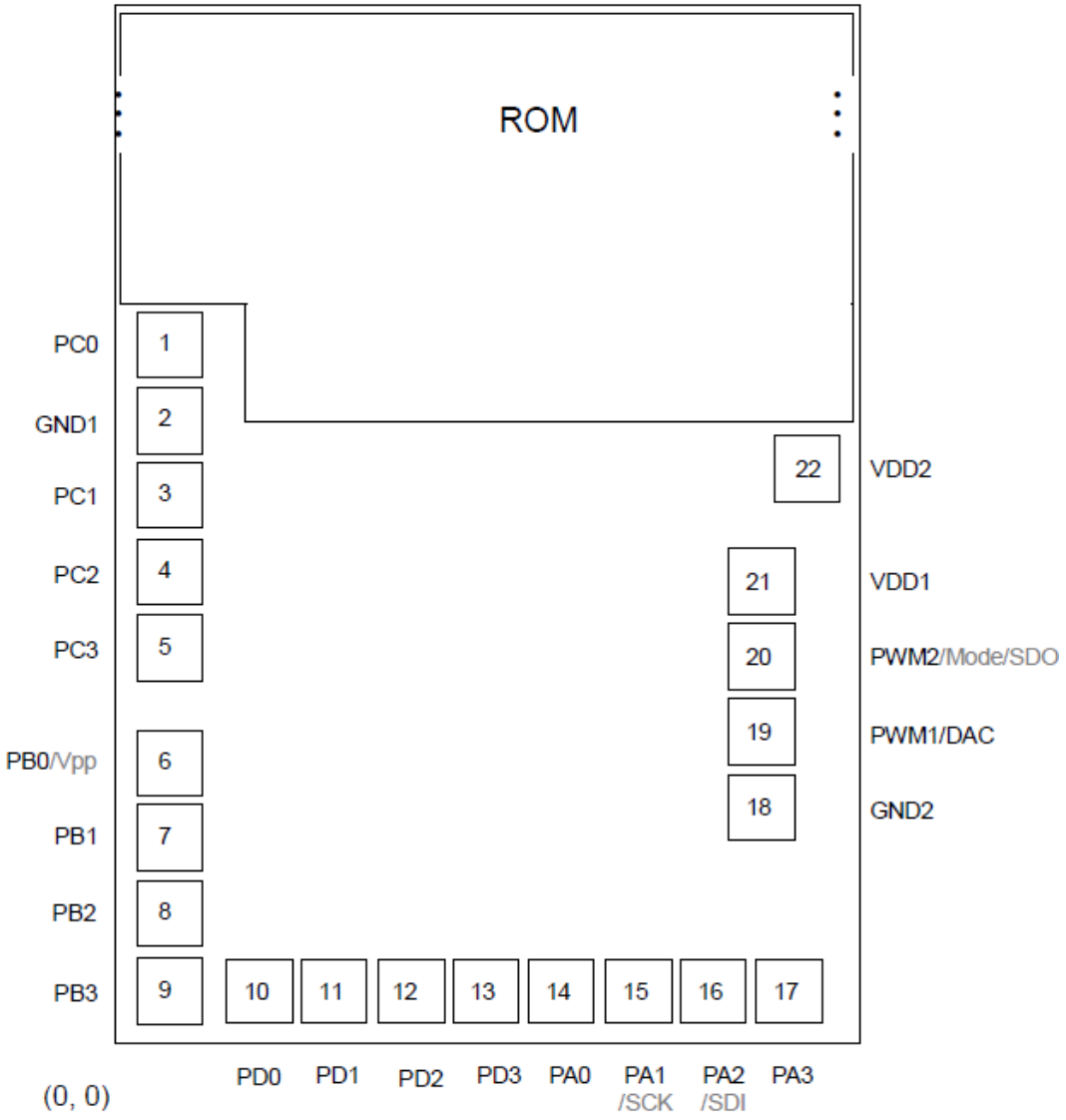


15. DIE PAD DIAGRAM

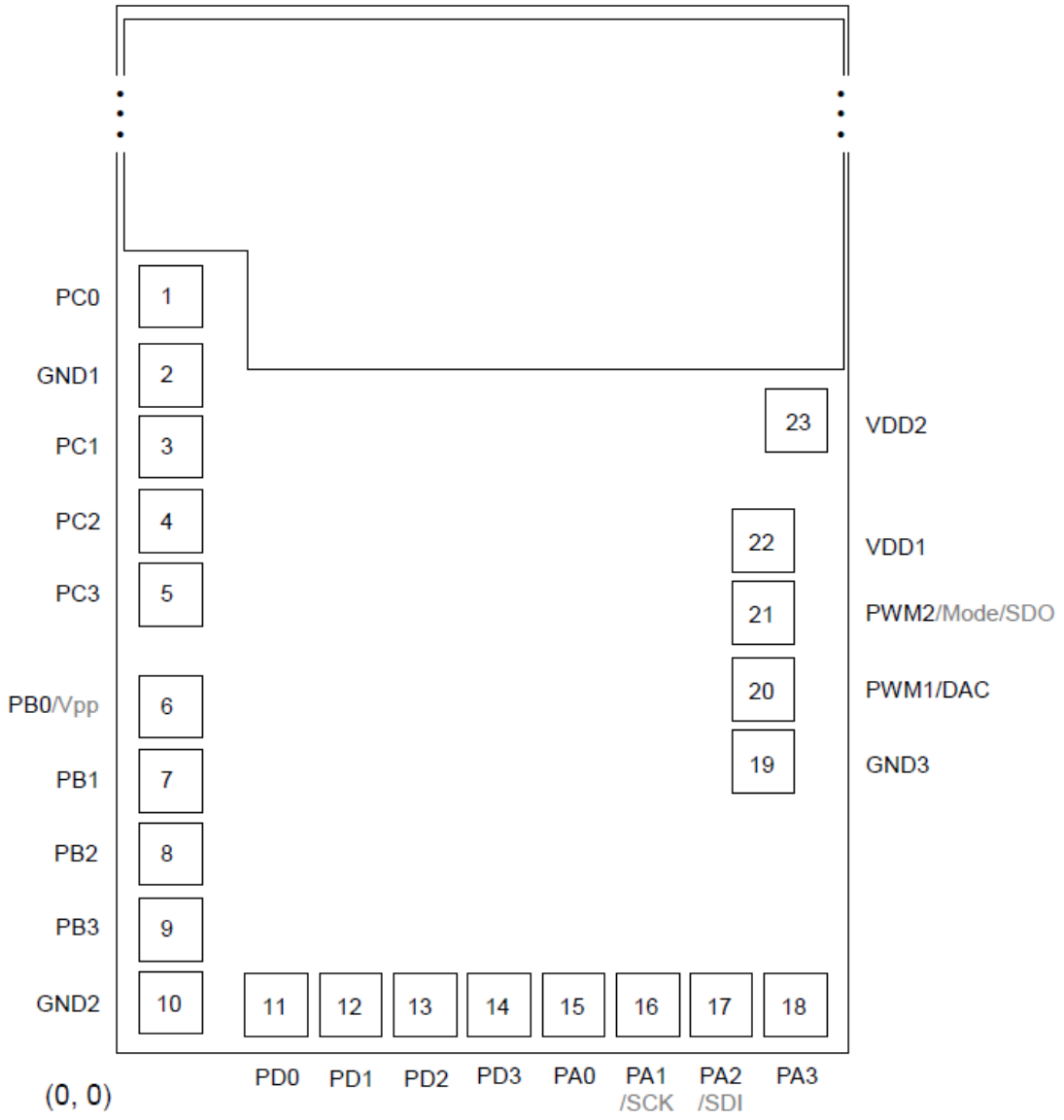
15.1 LG5Q020A, LG5Q040A



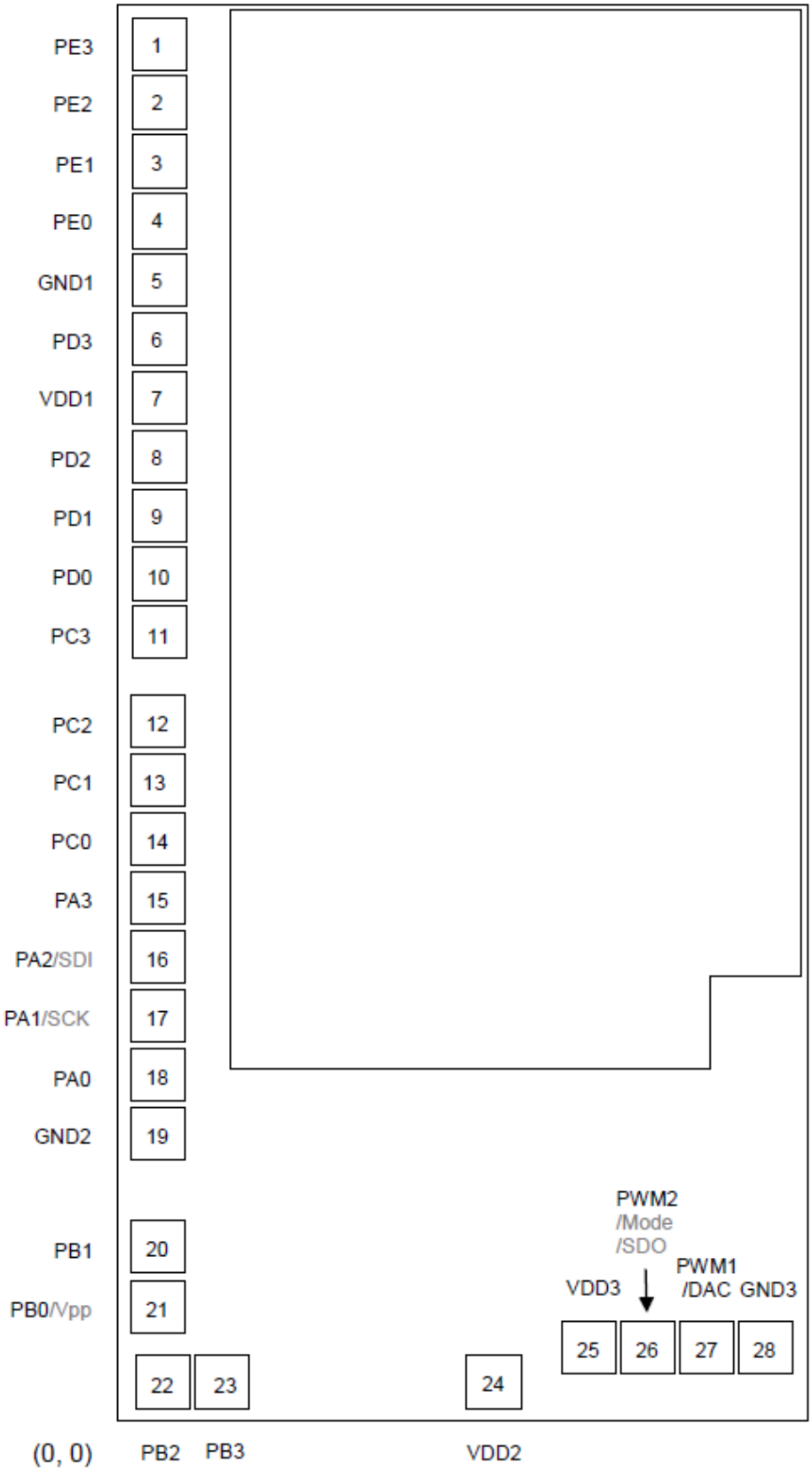
15.2 LG5Q060A, LG5Q092A



15.3 LG5Q172A

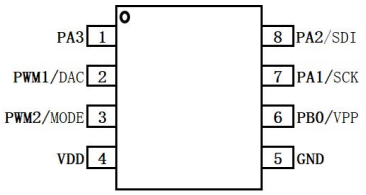


15.4 LG5Q342A



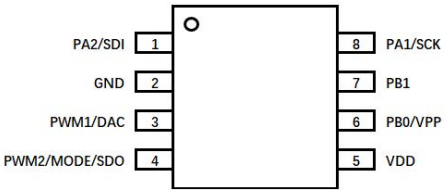
16 PACKAGE PIN ASSIGNMENT

8-pin SOP (150mil)



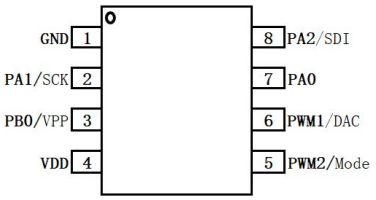
LG35Q020AS8
LG35Q040AS8
LG35Q060AS8
LG35Q092AS8

8-pin SOP (150mil)



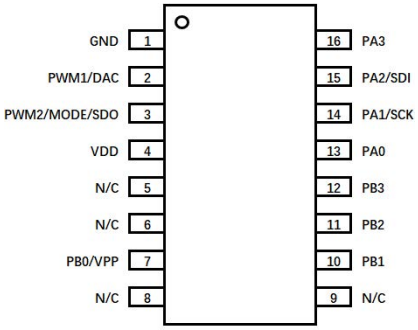
LG5Q060AS8
LG5Q092AS8
LG5Q172AS8

8-pin SOP (150mil)



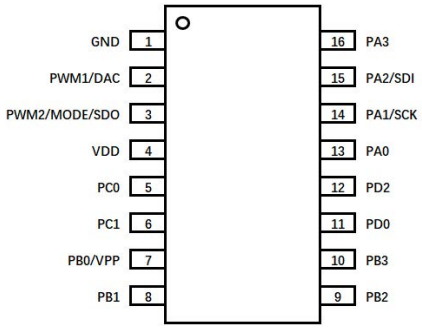
LG5Q342AS8

16-pin SOP (150mil)



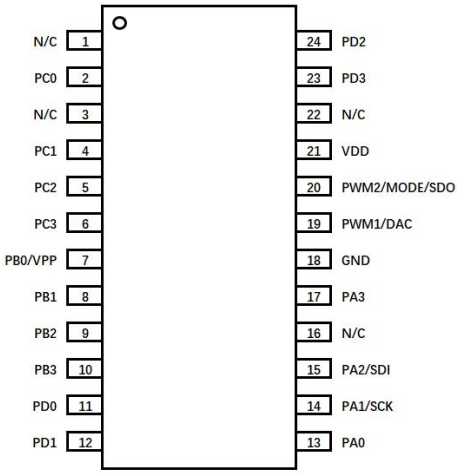
LG5Q020AS16
LG5Q040AS16

16-pin SOP (150mil)



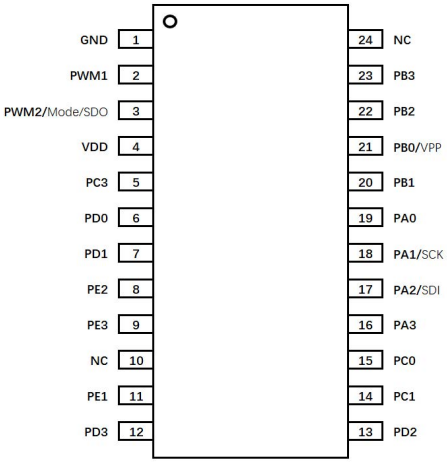
LG5Q060AS16
LG5Q092AS16
LG5Q172AS16

24-pin SSOP (150mil)



LG5Q060AU24
LG5Q092AU24
LG5Q172AU24

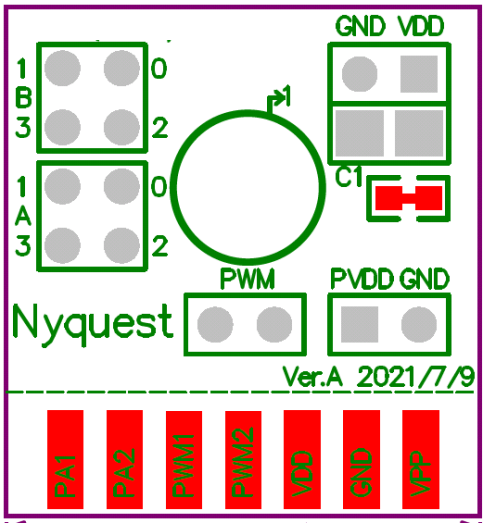
24-pin SOP (150mil)



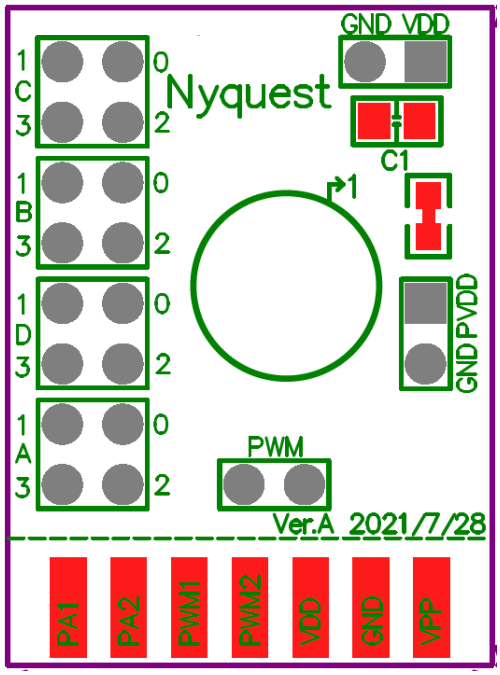
LG5Q342AU24

17 COB PIN ASSIGNMENT

LG5Q020AB, LG5Q040AB *(8 I/O)*

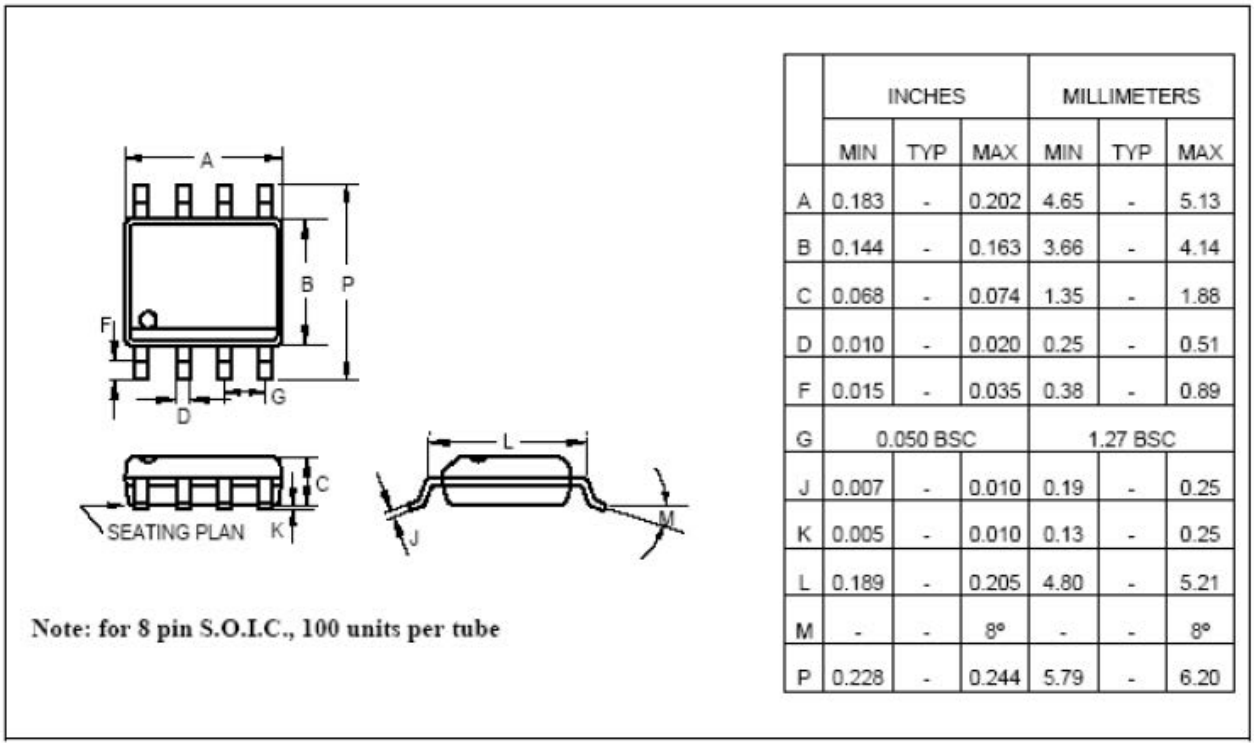


LG5Q060AB, LG5Q092AB, LG5Q172AB *(16 I/O)*



18. PACKAGE DIMENSION

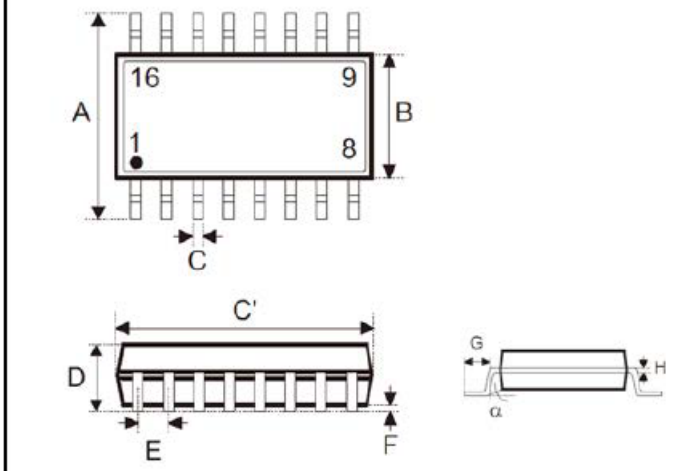
18.1 8-Pin Plastic SOP (150 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.183	-	0.202	4.65	-	5.13
B	0.144	-	0.163	3.66	-	4.14
C	0.068	-	0.074	1.35	-	1.88
D	0.010	-	0.020	0.25	-	0.51
F	0.015	-	0.035	0.38	-	0.89
G	0.050 BSC			1.27 BSC		
J	0.007	-	0.010	0.19	-	0.25
K	0.005	-	0.010	0.13	-	0.25
L	0.189	-	0.205	4.80	-	5.21
M	-	-	8°	-	-	8°
P	0.228	-	0.244	5.79	-	6.20

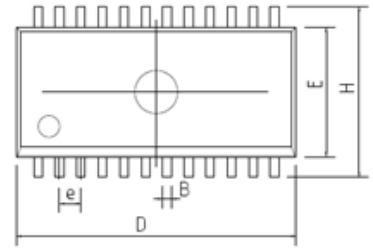
Note: for 8 pin S.O.I.C., 100 units per tube

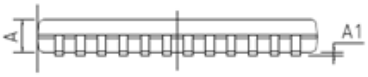
18.2 16-Pin Plastic SOP (150 mil)

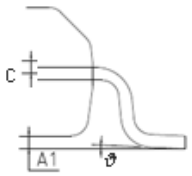


	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.236 BSC			6.00 BSC		
B	0.154 BSC			3.90 BSC		
C	0.012	-	0.020	0.31	-	0.51
C'	0.390 BSC			9.90 BSC		
D	0.065	-	0.069	1.64	-	1.75
E	0.050 BSC			1.27 BSC		
F	0.004	-	0.010	0.10	-	0.25
G	0.016	-	0.050	0.40	-	1.27
H	0.004	-	0.010	0.10	-	0.25
α	-	-	8°	-	-	8°

18.3 SSOP-24 (150mil, 0.635mm pin pitch)







	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.049	-	0.061	1.25	-	1.55
A1	0.002	-	0.010	0.05	-	0.25
B	0.008	-	0.012	0.19	-	0.31
C	0.006	-	0.010	0.15	-	0.25
D	0.337	-	0.344	8.55	-	8.75
e	0.025 BSC			0.635 BSC		
E	0.150	-	0.157	3.80	-	4.00
H	0.224	-	0.248	5.70	-	6.30
L	0.012	-	0.035	0.30	-	0.90
θ	0°	-	7°	0°	-	7°

Note: For 24-pin SSOP, 50 units per tube.