Design and Implementation of Costas Loop Based on FPGA

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***Abstract*-On the basis of analyzing the mathematical models of Costas loop, a method to model and simulate it by Simulink is put forward. In order to reduce the complexity of translating model to HDL (hardware description language), the model is realized by MATLAB code; the digital design of LPF (low-pass filter), LF (loop filter) and VCO (voltage-controlled oscillator) are mainly researched. At last, we accomplish the functional simulation by Verilog HDL code on Modlesim platform, finish the logic synthesis by synplify, and implement the hardware verification on the Cyclone series FPGA device EP1C6Q240C8 of Altera company. The final results are applied to the ASIC(application specific integrated circuit) design of BPSK（Binary Phase Shift Keying）signal's demodulation. Results show that the Costas loop could correctly realize BPSK signal's carrier recovery and data demodulation. Results of theoretical simulation and practical engineering experiments are the same. The method is proved simple, convenient and hardware resource saving.**

I. INTRODUCTION

Costas loop is a kind of closed-loop and auto-tracking system that can be applied in tracking the input signal's phase [1]. The Costas loop performs both phase-coherent suppressed carrier reconstruction and synchronous data detection within the loop. It is widely used in fields of radio-technology and has become an indispensable part of communication, radar, navigation, electronic equipment and other devices. Phase-Locked-Loop (PLL) has wide application just because of its unique narrowband tracking performance [2]-[4]. The merits of its performance in electronic design have great significance.

The performances of traditional analogy Costas loop are affected because of the imbalance between in-phase branch and quadrature branch, and there are also some disadvantages such as direct current zero excursion and difficulty to debug [5]. But these problems can be avoided by using all-digital Costas loop [6] .

In recent years, processing digital signals on FPGA gives more and more dominance because of FPGA's high flexible in-system programmability. While the key of accomplishing all-digital Costas loop is its effect of limited bit length, digitalizing of loop parameters and clock design of each loop component. Detail analysis on VLSI (very large scaled integrated) design of digital Costas loop are given in [7], and how to get loop parameters are illustrated too. But when FPGA design is accomplished concretely, the practical value of loop parameters have more different with that of calculated by formula given by [7]. It is bound to bring a certain degree of difficulty of adjusting loop parameters on period of practical engineering; On the basis of [7], [8] readjusts the formula of calculating the loop parameters and mends the structure of the loop, finally, the RTL (register transfer level) circuit and simulation results are provided combining the application of their project. The implementation method of discrete Costas loop was researched in [9], loop filter was discussed in discrete time domain, the discrete time domain implementation method of DCO was discussed, and logical circuit of the digital second order Costas loop was implemented in FPGA chip with VHDL.

In [8]-[9], loop parameters are calculated by formula, it is bound to lead difference between theory and practice, and theoretical simulation could not be obtained to compare with practical simulation. These methods are not simple and convenient. In [10], Costas loop is designed as dynamic systems in a block diagram format with SIMULINK, and their future work is that they will continue writing MATLAB code to achieve the processing of demodulation. Furthermore, the key of FPGA design is how to make the most of smaller logic elements to finish the same design.

In our paper, the SIMULINK model of Costas loop is established, theoretical simulation are obtained, and loop parameters can be mended easily according to the model. At the same time, the model is realized by MATLAB code to achieve the processing of demodulation. Then, we accomplish the functional simulation by Verilog HDL code on Modlesim platform, finish the logic synthesis by synplify, and implement the hardware verification on FPGA. Furthermore, when we write HDL code, we avoid using the IP core provided by explore environment as possible as we can. All modules are designed according to the practical requirements by ourselves, so the design effect of area optimism can be achieved. The implementation is quite simple and the structure is very powerful and useful in many situations.

II. THE MATHEMATICAL MODEL OF COSTAS LOOP

Costas loop is also known as the in-phase and quadrature loop, its principle [11] is shown in Fig.1. Costas loop basically consists of three multipliers called mixers, two low-pass filters (LPF), a loop filter (LF), a voltage-controlled oscillator (VCO) and a 90 degree phase shift.

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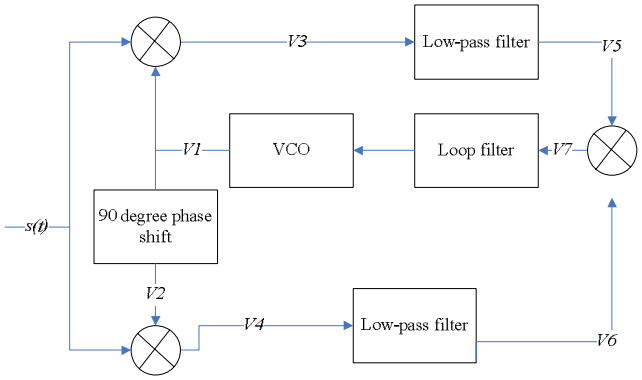


Fig.1. Block diagram of Costas loop

The external PSK signals are sent to two multipliers of the upper called in-phase branch and the lower called quadrature branch respectively, the in-phase branch multiply input by VCO's output, but the quadrature branch multiply input by VCO's output after 90 degree phase shift. The multiplier output of the in-phase branch and quadrature branch are passed through the low-pass filter, then multiply together to get the error signal. Finally, the error signal is filtered by the loop filter (LF), whose output is control voltage that can control VCO's phase and frequency.

In Fig.1, it is assumed that the loop is locked and noise signal is not considered. To be specific, suppose we have an amplitude signal of the form

$$s(t) = A(t)\cos(2\pi f_c t + \phi) \tag{1}$$

If we demodulate the signal by multiplying $s(t)$ with the carrier reference

$$V1 = \cos(2\pi f_c t + \hat{\phi}) \tag{2}$$

We obtain

$$\begin{aligned} V3 &= s(t)V1 \\ &= \frac{1}{2}A(t)\cos(\phi - \hat{\phi}) + \frac{1}{2}A(t)\cos(4\pi f_c t + \phi + \hat{\phi}) \end{aligned} \tag{3}$$

The double-frequency component may be removed by passing the product signal $V3$ through a low-pass filter. This filtering yields the in-phase component

$$V5 = \frac{1}{2}A(t)\cos(\phi - \hat{\phi}) \tag{4}$$

where $\Delta\phi = \phi - \hat{\phi}$ is the phase error.

Similarly, If we demodulate the signal by multiplying $s(t)$ with the quadrature carrier reference

$$V2 = \sin(2\pi f_c t + \hat{\phi}) \tag{5}$$

We obtain

$$\begin{aligned} V4 &= s(t)V2 \\ &= \frac{1}{2}A(t)\sin(\phi - \hat{\phi}) + \frac{1}{2}A(t)\sin(4\pi f_c t + \phi + \hat{\phi}) \end{aligned} \tag{6}$$

multiplication of $s(t)$ with $V2$ followed by low-pass filtering yields the quadrature component

$$V6 = \frac{1}{2}A(t)\sin(\phi - \hat{\phi}) \tag{7}$$

Multiply *V5* by *V6,* then we can get

$$\begin{aligned} V7 &= V5 \times V6 = \frac{1}{4}A(t)^2 \sin(\phi - \hat{\phi})\cos(\phi - \hat{\phi}) \\ &= \frac{1}{8}A(t)^2 \sin 2(\phi - \hat{\phi}) \approx \frac{1}{8}A(t)^2(\phi - \hat{\phi}) = \frac{1}{8}A(t)^2\Delta\phi \end{aligned} \tag{8}$$

This voltage controls VCO to the same frequency with f_c and a small phase error $\Delta\phi$ after passing through a loop filter. At this time, *V1* is the synchronous carrier that we want to extract and *V5* is the demodulation output signal.

From the processing of mathematical analysis, we can see that Costas loop works in the f_c frequency which is lower than the square loop's working frequency and don't need the squarer and frequency divider. While the loop locks normally, the output of in-phase branch is the original digital sequence which we need to demodulate. Therefore, this circuit has dual function of extract coherent and demodulation carrier [12]-[14]. However, the disadvantage of Costas loop is its complex circuit and difficulty to achieve.

III. SIMULINK MODEL AND SIMULATION OF COSTAS LOOP

In the engineering project which the author engaged in, the data rate is 1200bit/s, carrier frequency is 120KHz, sampling bit is 1bit, sampling rate is 9.6MHz, FPGA chip is EP1C6Q240C8，the explore platform is Quartus II 6.0, and the HDL simulation tool is Modelsim6.1f, the system simulation tool is MATLAB/SIMULINK [15]-[18], the HDL synthesis tool is Synplify8.1.

According to the Costas loop's mathematical model, simulink model of Costas loop that we are established is shown in Fig. 2.

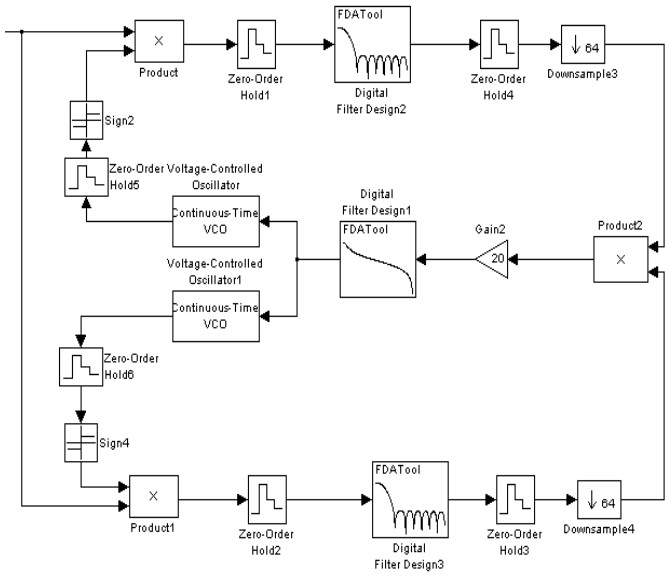


Fig.2. Simulink model of Costas loop

In Fig. 2, Zero-Order Holders are used to make the signal discrete, Sign2 and Sign4 are used to get sign in order to transform the VCO's output from sinusoidal signal to square signal, Product and Product2 named mixer are used to

complete the mixing of BPSK's signal with local carrier signal, Digital Filter Design2 and Digital Filter Design3 are low-pass filters whose function are to remove the double-frequency component, Digital Filter Design1 is loop filter whose function is same as low-pass filter, Down samples are used to make the signals after filtering by low-pass filter sampling 64 times down, and VCO is basically a sinusoidal signal generator.

The low-pass filter used in the model is FIR(finite-impulse response) filter of Hamming windows, whose sampling frequency is 9.6e6，central frequency is 60e3，order is 61.The Loop filter used in the model is IIR(infinite impulse response) filter of Butterworth I, whose sampling frequency is 1.5e3，central frequency is 2k.The VCO Gain is 500 and the warp is 1000.

Costas loop is simulated according to our simulink model, and the voltage-controlled signal which can lock the process is achieved and shown in Fig. 3. From which we can see that Costas loop is stabilized to 1000 after a short adjustment and the frequency is locked quickly.

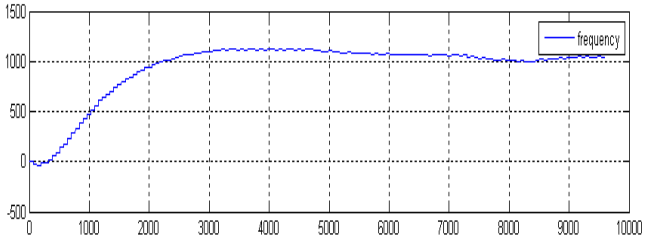


Fig.3. Tracking and locking process of Costas loop

In this model, the system performance can be continuously improved by adjusting parameters of low-pass filter, loop filter and VCO repeatedly. That is just Simulink's one feature of flexibility, and the design efficiency has been increased greatly.

IV. THE IMPLEMENTATION OF COSTAS LOOP BY MATLAB CODE

A. The implementation of FIR and IIR filter

From the Simulink model of Costas loop, we can see that simulation model of this system is a continuous system. However, it must be a discrete system when we use MATLAB code and Verilog HDL to implement it. The FIR filter and the IIR filter of this model are realized by using MATLAB code in this paper.

Because Costas Loop is a closed-loop feedback auto-control system, we cannot use the filter function which is provided by the MATLAB's Toolbox directly[11-12]. The filter of this model is designed as follows:

1. FIR filter:

```
for j= 1:length(lpf_num)
   lpfI(k + lpf_order) = lpfI(k + lpf_order) +
   lpf_num(j)*dI(k + lpf_order - (j - 1));
   lpfQ(k + lpf_order) = lpfQ(k + lpf_order) +
   lpf_num(j)*dQ(k + lpf_order - (j - 1));
  end
```

Where, j is suffix of the signals after filtering by low-pass filter, Length is the function of getting array's length in Matlab, Lpf_num is coefficient of LPF's numerator, LpfI and lpfQ are signals of I channel and Q channel after filtering by low-pass filter, K is the extend length ahead of LPF equal to order of filter, Lpf_order is order of LPF, dI and dQ are signals after mixing.

The FIR filter's amplitude-frequency response is shown in Fig. 4.

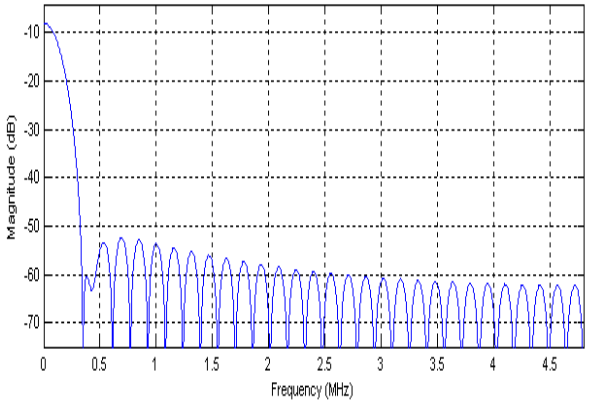


Fig.4. FIR low-pass filter's amplitude-frequency response

2. IIR filter:

```
for j= 1:length(L_num)
   vco_o(n+ L_order) = vco_o (n + L_order) +
   L_num(j)*down(n + L_order - (j-1));
 end
 for j= 2:length(L_den)
    vco_o (n + L_order) = vco_o (n + L_order) -
    L_den(j)* vco_o (n + L_order - (j-1));
  end
```

where, j is suffix of the signals after filtering by low-pass filter, Length is the function of getting array's length in Matlab, L_num is coefficient of LF's numerator, L_den is coefficient of LF's denominator, *vco_o* is signal after filtering by loop filter, N is the extend length ahead of LF equal to order of filter, L_order is order of LF, Down is signal which is LP's input after sampling down.

The IIR filter's amplitude-frequency response is shown in Fig. 5.

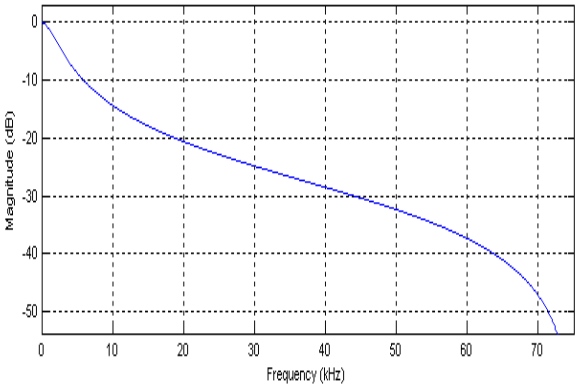


Fig.5. IIR loop filter's amplitude-frequency response

B. *Digital implementation of VCO*

VCO's digital implementation is *DCO*（digital-controlled oscillator）, so *DCO*'s position in digital PLL is equal to that of *VCO* [13-14]. *DCO*'s output is a local carrier wave which is controlled by a regulation signal transmitted from the loop filter. Costas Loop is a closed-loop feedback auto-control system, its control features is that the regulation signal gotten at previous sampling period will change the phase of signal gotten at the next sampling period. It means that there is a delay in the system. *DCO*'s structure is shown in Fig. 6.

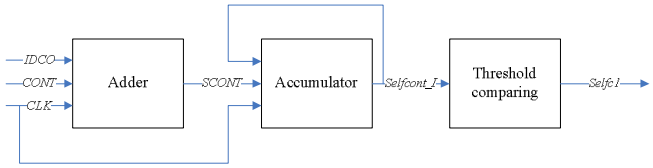


Fig.6. Structure of *DCO*

In Fig. 6, *IDCO* is a regulation signal which is transmitted from loop filter, *CONT* is a constant decided by *DCO*'s inherence frequency, *CLK* is *DCO*'s clock signal, whose frequency is f_b, *SCONT* is the output of the adder, *selfcont_I* is the output of a 32bit accumulator, and threshold comparing is a comparing. When the result is greater than the threshold value, the output is a reversal of the local carrier wave signal *selfc1*. (Note: In our design, the local carrier wave signal which is the output of *DCO* is a square wave signal.)

The system works as follows: *CONT* is a constant, and it decides the *DCO*'s inherence frequency

$$f_c = f_b \times \frac{CONT}{2^N} \tag{9}$$

Where f_b is the clock frequency of the system, N is the data's width of the accumulator.

Hence, *DCO*'s output frequency is

$$f_o = f_b \times \frac{SCONT}{2^N} \tag{10}$$

Where

$$SCONT = CONT + IDCO \tag{11}$$

In this condition, we can change the value of *SCONT* in order to control the output frequency, whose minimum changing step is

$$\Delta f = \frac{f_b}{2^N} \tag{12}$$

From (12), we can see that Δf is decided by *N*. *N* is bigger, and Δf is smaller. So we can set *CONT* to ensure the *DCO*'s inherence frequency, and change *IDCO* signal to adjust the *DCO*'s output. The smaller *IDCO* signal and the bigger *N* is, the more exact adjustment is. However, because of the limit of the hardware, *IDCO* and *N* cannot be so big, we set *N* is 32 in this design.

In this paper, the local carrier wave signal which we generate is a square wave signal, so *DCO* should contain a module of threshold comparing. When the accumulator overflows, we can turn over the output carrier signal *selfc1*. We can generate orthogonal carrier signal by the same method, it just need to initialize the accumulator in different value. We do not talk about this more.

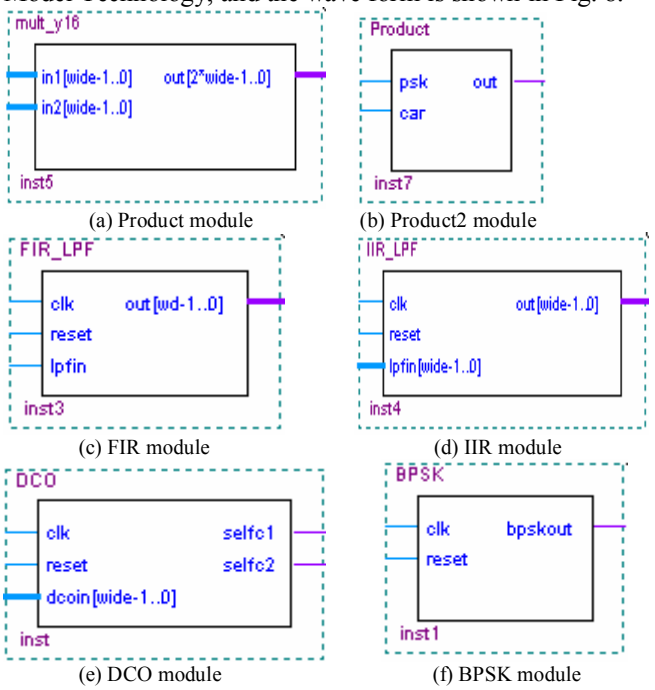
V. FPGA REALIZATION OF COSTAS LOOP

A. *Verilog HDL realization*

According to the structure shown in Fig. 2, the system is separated into 5 modules: multiplier module shown in Fig. 7(a) and Fig. 7 (b), FIR filter module shown in Fig. 7(c), IIR filter module shown in Fig. 7(d) and DCO module shown in Fig. 7(e). Function of these modules can refer to IV*(A)*. In our project, the data rate is 1200bit/s, carrier frequency is 120KHz, sampling bit is 1bit, sampling rate is 9.6MHz, data's width of the accumulator in DCO is 32 bit. Based on these parameters, all modules are programmed by Verilog HDL code and completed compilation on the explore platform of Quartus II 6.0, who is a popular FPGA design tool of Altera company. Altera's Quartus II software leads the industry as the most comprehensive environment available for FPGA designs, delivering unmatched performance, efficiency, and ease-of-use. Altera's Quartus II software is the first design environment that supports intellectual property (IP)-based system design—including complete and automated system definition and implementation—without requiring lower-level hardware description language (HDL) or schematics.

In addition, BPSK demodulation module are designed and added, whose symbol is shown in Fig. 7(f), so the Costas loop can be tested. In our model, all parameters can be changed anytime, only if HDL programs are reworked. The design is very flexible.

The system is simulated by Modelsim6.1f, who is a Verilog /VHDL mixed simulation tool based on single IP core of Model Technology, and the wave form is shown in Fig. 8.



(a) Product module (b) Product2 module

(c) FIR module (d) IIR module

(e) DCO module (f) BPSK module

Fig.7. Verilog modules of Costas Loop

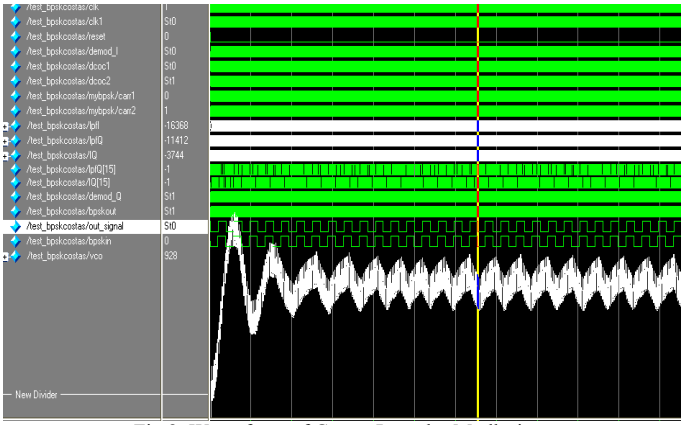


Fig.8. Wave form of Costas Loop by Modlesim

Costas loop's tracking and locking time is decided by loop filter's parameters and VCO's gain. The narrower the filter's frequency bandwidth and the smaller the gain is, the longer the locking time is, but the smaller the steady-state error is. In contrast, the locking time is shorter, but steady-state error is bigger. In sum, locking time and steady-state error is opposite. We could only choose the frequency bandwidth and VCO's gain eclectically according to our require performance. From the wave form of Costas loop's Modlesim simulation, we can know that VCO signal can stay at a steady value after about 6 carrier wave periods and recovery the local carrier wave correctly.

B. Result of hardware verification

On the *Altera*'s *Cyclone* series FPGA chip EP1C6Q240C8, we download the program, and the result of the whole design running on the hardware is observed through oscillograph. When we write HDL code, we avoid using the IP core provided by explore environment as possible as we can. All modules are designed according to the practical requirements by ourselves, so the design effect of area optimism can be achieved. The hardware resource used in this design is 2490 logic elements, and the RTL circuit synthesized by Synplify8.1, who is a HDL synthesis tool of Synplicity company, is shown in Fig. 9.

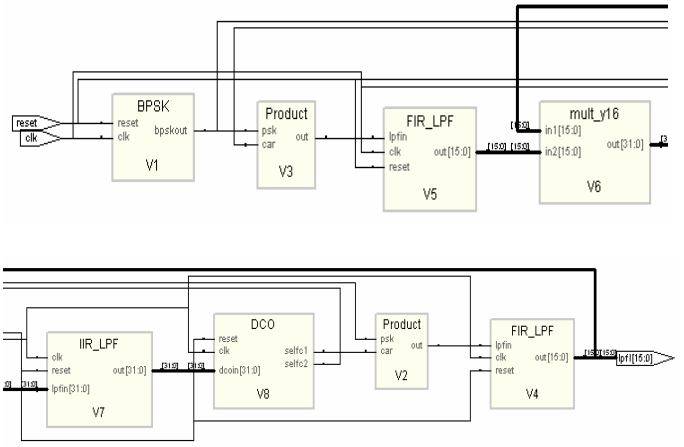


Fig.9. RTL circuit

Fig.10 is the wave forms shown on the screen of oscillograph in condition of closed-loop locked, when the transmitted carrier wave and local carrier have warp (In the picture, the upper wave is the local carrier wave signal and the lower wave is the data of demodulated output. The data is four "1" and one "0").

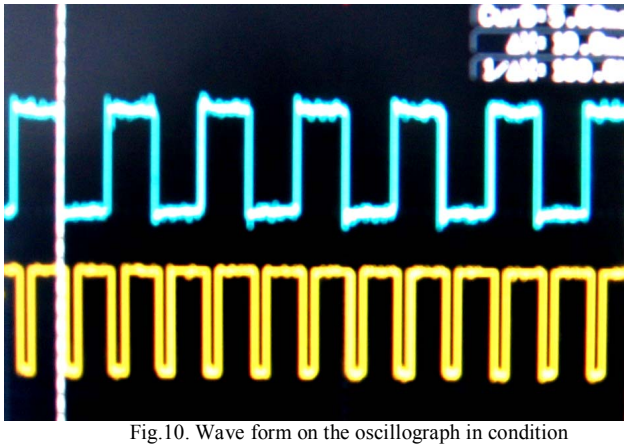


Fig.10. Wave form on the oscillograph in condition of closed-loop locked

Fig.11 is the wave forms shown on the screen of oscillograph in condition of open loop, when the transmitted carrier wave and local carrier have warp. (In the picture, the upper wave is the local carrier wave signal and the lower wave is the data of demodulated output).

Compared with the wave forms on the oscillograph, we can know that we are able to recover the local carrier wave exactly and demodulate the data correctly by using Costas loop in condition of closed-loop locked.

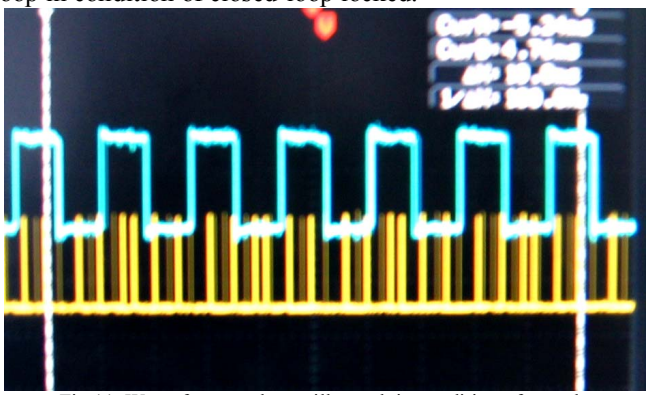


Fig.11. Wave form on the oscillograph in condition of open loop

VI. CONCLUSIONS

On the basis of analyzing the Costas loop's mathematical model, a Butterworth loop filter and a low-pass FIR filter in the Costas loop are designed, and a simulation model of Costas loop is build by Simulink in this paper. In order to reduce the complexity of HDL implementation, we use the MATLAB code to realize the Costas Loop. The advantages of using HDL language to design PLL is that it is flexible to design, convenient to rework and easy to implement. So PLL

can be designed most easily and flexibly according to various conditions.As the result, the Costas Loop achieves the BPSK signals' recovery of local carrier wave and data's demodulation output. Theoretical simulation and practical engineering basically get the same result.

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