**Slide #1**

6 months ago in Seminar, our team set out to design a communications device using FPGA technology. Our advisor presented us with a paper written by Amateur Radio community member, John A. Magliacane (call-sign, KD2BD) that outlines the design of a 1200 b/sec BPSK modem used for communication with Low Earth Orbiting Amateur Satellites.

6 months later on October 4th, our Team leader introduced our design proposal for an FPGA implementation of a 1200 b/sec BPSK modem in our first webEX project review. In our second webEX review, submitted on October 18th, we proposed the Costas loop demodulator as an alternative to the squaring loop demodulator presented in KD2BD’s design.

However, while developing the draft design document that was due on the same date as the second WebEX review, we realized that our BPSK modem lacked an overall motivation for design. As a result, design and simulation of the BPSK modem was temporarily put on hold because as a team, we decided it was irresponsible to continue design without having a clear, concise, and thorough understanding of the projects overall objective and motivation. Thus the majority of the last two weeks were spent refining the Problem statement in the Design Document to avoid any further delays.

**Slide #2**

Our research during this time period led us to the conclusion that the Amateur Radio community as a whole, is not progressing towards the modernization of technology that should be used in future Amateur Satellites. This is evident in the fact that the majority of satellites currently being operated are still using legacy technology like Audio Frequency Shift Keying found in the original Bell 202 modem. This is illustrated with the list of satellites displayed on your screen.

**Slide #3**

However, recent efforts from active community members like Phil Karn of KA9Q, are advocating for the inclusion of forward error correction that improves Bit Error Rate Performance and the reliability of packet radio transmission. His work on forward error correction was also recently published at the 2010 AMSAT Symposium.

**Slide #4**

Thus our work in the past two weeks culminated in the following formal Problem statement upon which the rest of our design will be based off:

*The objective of the Programmable Communications Group is to demonstrate that a forward thinking BPSK Key modem using Interleaving FEC will outperform traditional FSK and PSK modems. Our motivation is to encourage the Amateur Radio community to progress towards more reliable and robust technology.*

We will then compare the BER performance from our results to traditional methods like FSK found in TAPR’s modem as well as KD2BD’s BPSK modem.

**Slide #5**

Completing this objective will require the design of a PSK modem, an FSK modem, and design of a convolutional encoder for the interleaving FEC. Each team member is currently responsible for one of the required components. Our team leader Brandon is providing the interleaving forward error correction, Cedric is designing the FSK modem that will be based off the bell 202, and I am continuing design of the PSK modem.

Since Tuesday October 29th, the Programmable Communications Group has resumed design and simulation of the PSK and FSK modems. On Friday Nov 1st our team will have submitted a revised design document with that describes in more detail, the problem statement and design requirements that are mentioned in this project review.

**Slide #6**

Like most product design life cycles, our progression from Design to Delivery will take place in three phases:

1. Design and Simulation
2. Hardware Implementation
3. Test and Verification

Each of the components listed on the previous slide will be designed in Matlab/Simulink and then realized in hardware using Xilinx’s System Generator. Following successful simulation, the modems and forward error correction module will be programmed in Verilog followed by synthesis onto a Xilinx Spartan 6 FPGA. Lastly, using a suite of Verilog test benches, software, and hardware, we will test and verify that our modems meet the desired specifications required for our performance assessment. Only after test and verification is complete and design meets specifications, will we begin to compare the results of our BPSK modem with FEC to TAPR’s and KD2BD’s.

**Slide #7**

Look ahead at the remaining schedule for SD1, you can expect to see a nearly completed Matlab/Simulink demonstration of ALL required components in the next WebEX project that is duetwo weeks from now on Nov 15th. Then a week later on Nov 22nd, we will deliver a completed Matlab/Simulink simulation of the required components. Finally, on Saturday Dec 7th we will presents our preliminary prototype to the board of coordinators and conclude Phase I of the design life cycle. Phases two and three will be completed during winter break and spring 2014. Our final results will be presented in April 2014.