Micropower Three-Axis ±2*g*/±4*g*/±8*g* Digital-Output MEMS Accelerometer

Preliminary Technical Data

ADXL362

FEATURES

Ultra low power
- **Power can be derived from coin cell battery**
- **1.8 µA @ 100 Hz ODR, 2.0V supply**
- **3.0 µA @ 400 Hz ODR, 2.0V supply**
- **300 nA motion-activated Wake-up Mode**
- **10nA Standby Current**

Built-in features for system-level power savings:
- **Adjustable-threshold sleep/wake modes for motion activation**
- **Autonomous interrupt processing without need for microcontroller intervention, so the rest of the system can be turned off completely**
- **Deep embedded FIFO minimizes host processor load**
- **Awake state output enables implementation of standalone motion-activated switch**

High resolution of 1 m*g*/LSB
Low noise down to 175 µ*g*/√Hz
Wide supply and I/O voltage ranges: 1.6 V to 3.6 V
- **Operates off 1.8V to 3.3V rails**

Acceleration sample synchronization via external trigger
On-chip temperature sensor
SPI digital interface
Measurement ranges selectable via SPI command
Small and thin 3 mm × 3.25 mm × 1.06 mm package

APPLICATIONS

Hearing aids
Home healthcare devices
Motion-enabled power save switch
Wireless sensors
Motion-enabled metering devices

GENERAL DESCRIPTION

The ADXL362 is an ultra-low power 3-axis MEMS accelerometer that consumes less than 2 µA at a 100 Hz output data rate, and 300 nA in motion-triggered Wake-Up Mode. Unlike accelerometers that use power duty cycling to achieve low power consumption, the ADXL362 does not alias input signals by undersampling; it samples the sensor's full bandwidth at all data rates.

The ADXL362 always provides 12-bit output resolution; 8-bit formatted data is also provided for more efficient single-byte transfers when a lower resolution is sufficient. Measurement ranges of ±2 *g*, ±4 *g*, and ±8 *g* are available, with a resolution of 1 m*g*/LSB on the ±2 *g* range. For applications where a noise level lower than the ADXL362's normal 550 µg/√Hz is desired, either of two lower noise modes (down to 175 µg/√Hz typ) may be selected at minimal increase in supply current.

In addition to its ultra-low power consumption, the ADXL362 has many features to enable true system-level power reduction. It includes a deep multimode output FIFO, a built-in micropower temperature sensor, and several activity detection modes including adjustable-threshold sleep and wakeup operation that can run as low as 300 nA at a 6 Hz (approximate) measurement rate. A pin output is provided to directly control an external switch when activity is detected if desired. In addition, the ADXL362 has provisions for external control of sampling time and/or an external clock.

The ADXL362 operates on a wide 1.6 V to 3.6 V supply range, and can interface, if necessary, to a host operating on a separate, lower supply voltage. The ADXL362 is available in a 3 mm × 3.25 mm × 1.06 mm package.

FUNCTIONAL BLOCK DIAGRAM

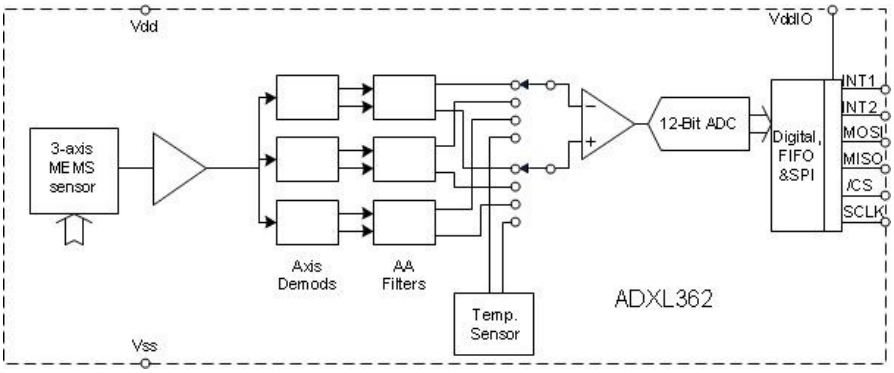

Figure 1.

Rev. PrB

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SPECIFICATIONS

T_A = 25°C, V_S = 2.0 V, $V_{DD\ I/O}$ = 2.0 V, 100 Hz ODR, Acceleration = 0 *g*, default register settings, unless otherwise noted.

Table 1. Specifications[1]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User Selectable		±2, 4, 8		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Sensor Resonant Frequency			3500		Hz
Cross-Axis Sensitivity[2]			±1.5		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges			12		Bits
SENSITIVITY	Each axis				
Sensitivity Calibration Error				±10	%
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	2 *g* range		1		mg/LSB
	4 *g* range		2		mg/LSB
	8 g range		4		mg/LSB
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	2 *g* range		1000		LSB/*g*
	4 *g* range		500		LSB/*g*
	8 g range		250		LSB/*g*
Sensitivity Change due to temperature[3]	−40°C to +85°C		0.01		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output	X_{OUT}, Y_{OUT}	-150	±35	+150	m*g*
	Z_{OUT}	-250	±50	+250	m*g*
0 *g* Offset vs. Temperature[3]	X_{OUT}, Y_{OUT}		±0.5		mg/°C
	Z_{OUT}		TBD		mg/°C
NOISE PERFORMANCE					
Noise Density					
Normal Operation	X_{OUT}, Y_{OUT}		550		µg/√Hz
	Z_{OUT}		920		µg/√Hz
Low Noise Mode	X_{OUT}, Y_{OUT}		400		µg/√Hz
	Z_{OUT}		550		µg/√Hz
Ultra-Low Noise Mode	X_{OUT}, Y_{OUT}		250		µg/√Hz
	Z_{OUT}		350		µg/√Hz
	V_S = 3.5V; X_{OUT}, Y_{OUT}		175		µg/√Hz
	V_S = 3.5V; Z_{OUT}		250		µg/√Hz
BANDWIDTH					
Low Pass (Anti-Aliasing) Filter −3 dB corner	HALF_BW = 0 (Bandwidth = ODR / 2)	6.25		200	Hz
	HALF_BW = 1 (Bandwidth = ODR / 4)	6.25		100	Hz
Output Data Rate (ODR)	User Selectable in 8 steps	12.5		400	Hz
SELF TEST					
Output Change[4]	X_{OUT}, Y_{out}, Z_{out}		TBD		m*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		1.6	2.0	3.6	V
I/O Voltage Range ($V_{DD\ I/O}$)		1.6	2.0	3.6	V
Supply Current					
Measurement Mode	100 Hz ODR (50 Hz bandwidth)[5]				
Normal Operation			1.8		µA
Low Noise Mode			3		µA
Ultra-Low Noise Mode			10		µA
Wake-up Mode			0.30		µA
Standby			0.01		µA
Turn-On Time	100 Hz ODR (50 Hz bandwidth)		TBD		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Bias	@25°C		TBD		LSB
Accuracy	@25°C		±0.5		°C
Sensitivity	@25°C		0.05		°C/LSB
Resolution			12		Bits
ENVIRONMENTAL					
Operating Temperature Range		−40		+85	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications may not be guaranteed.
[2] Cross-axis sensitivity is defined as coupling between any two axes.
[3] −40°C to +25°C or +25°C to +85°C.
[4] Self-test change is defined as the output change in *g* when self-test is asserted.
[5] Refer to Figure 4 for current consumption at other bandwidth settings.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	5,000 *g*
Acceleration (Any Axis, Powered)	5,000 *g*
V_S	−0.3 V to 3.6 V
$V_{DD\ I/O}$	−0.3 V to 3.6 V
All Other Pins	−0.3 V to V_S
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
ESD	2000V (HBM)
Short Term Maximum Temperature	
Four Hours	150°C
One Minute	260°C
Temperature Range (Powered)	−50°C to +150°C
Temperature Range (Storage)	−50°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	150°C/W	85°C/W	18 mg

PACKAGE INFORMATION

Figure 2 and Table 4 provide details about the package branding for the ADXL362. For a complete listing of product availability, see the Ordering Guide section.

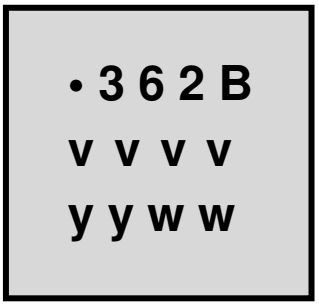

Figure 2. Product Information on Package (Top View)

Table 4. Package Branding Information

Branding Key	Field Description
• 362B	Pin 1 indicator and part identifier
vvvv	Factory lot code
yyww	Date code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

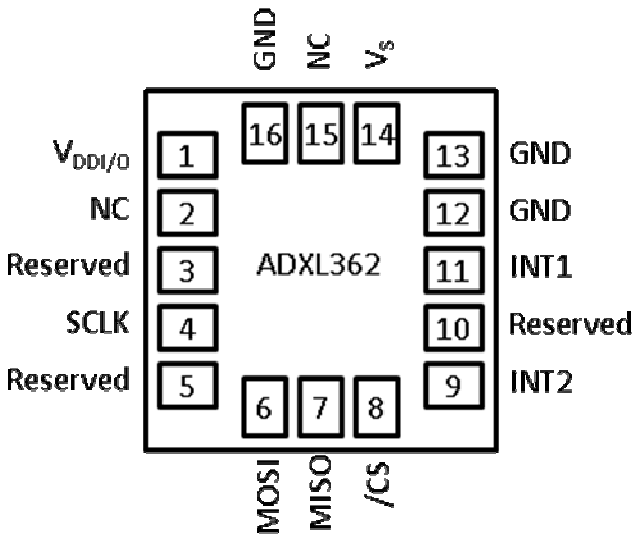

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Supply Voltage for Digital I/O.
2	NC	Not Internally Connected.
3	Reserved	Reserved. May be left unconnected, or connected to GND.
4	SCLK	SPI Communications Clock.
5	Reserved	Reserved. May be left unconnected, or connected to GND.
6	MOSI	SPI Serial Data Input.
7	MISO	SPI Serial Data Output.
8	$\overline{CS}$	SPI Chip Select, Active Low. Must be low during SPI communications.
9	INT2	Interrupt 2 Output. Also serves as input for synchronized sampling.
10	Reserved	Reserved. May be left unconnected, or connected to GND.
11	INT1	Interrupt 1 Output. Also serves as input for external clocking.
12	GND	Must be connected to ground.
13	GND	Must be connected to ground.
14	V_S	Supply Voltage.
15	NC	Not Internally Connected.
16	GND	Must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

FUNCTIONAL DESCRIPTION

The ADXL362 is a complete three-axis acceleration measurement system that operates at extremely low power consumption levels and enables system-level power savings. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as tilt. Acceleration is reported digitally and the device communicates via the SPI protocol.

MECHANICAL DEVICE OPERATION

The moving component of the sensor is a polysilicon surface-micromachined structure, also referred to as a beam, built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the beam and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase-sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

OPERATING MODES

The ADXL362 has two operating modes: Measurement Mode for continuous, wide-bandwidth sensing, and Wake-up Mode for limited-bandwidth activity detection. Measurement can be suspended altogether by placing the device in Standby.

Measurement Mode

Measurement Mode is the normal operating mode of the ADXL362. In this mode, acceleration data is read continuously and the accelerometer consumes less than 3 μA (typical) across its entire range of output data rates up to 400 Hz, with a 2.0V supply. All features described in this datasheet are available when operating in this mode.

The ability to continuously output data from the minimum 12.5Hz to the maximum 400Hz data rate without aliasing any input signal while also still delivering less than 3 μA (typical) of current consumption is what makes the ADXL362 truly a breakthrough ultra-low power accelerometer. Other accelerometers derive low current by using a specific low power mode that power cycles acceleration sensing. This leads to a small effective bandwidth in the low-power modes and undersampling of input data and thus unwanted aliasing can occur. Undersampling and aliasing will not happen with the ADXL362 since it continuously samples the full bandwidth of its sensor at all data rates.

Wake-up Mode

Wake-Up Mode is ideal for simple detection of the presence or absence of motion, at extremely low power consumption (300 nA at a 2.0V supply voltage). This mode is useful particularly for implementation of a motion-activated on/off switch, allowing the rest of the system to be powered down until activity is detected.

Wake-up Mode reduces current consumption to a very low level by measuring acceleration only about six times per second to determine whether motion is present. If motion is detected, the accelerometer can respond autonomously in several ways: it can switch into full-bandwidth measurement mode, signal an interrupt to a microcontroller, and/or wake up downstream circuitry, depending on configuration.

Standby

Placing the ADXL362 in Standby suspends measurement and reduces current consumption to merely 10nA (typical). Pending interrupts and data are preserved. No new interrupts are generated.

The ADXL362 powers up in Standby with all sensor functions off.

POWER/NOISE TRADEOFF

The ADXL362 offers a few options for decreasing noise at the expense of only a small increase in current consumption.

The noise performance of the ADXL362 in normal operation, typically 7 LSB RMS at 100 Hz bandwidth, will be adequate for most applications, depending upon bandwidth and the desired resolution. For cases where lower noise is needed, the ADXL362 provides two lower-noise operating modes that trade reduced noise for somewhat higher supply current.

Table 6 shows the supply current values and noise densities obtained for normal operation and the two lower-noise modes, at a typical 2.0V supply.

Operating the ADXL362 at a higher supply voltage also decreases noise. Table 7 shows the supply current values and noise densities obtained for normal operation and the two lower-noise modes the highest recommended supply, 3.3V.

Table 6. Noise and current consumption in normal operation, Low Noise Mode, and Ultra-Low Noise Mode @ V_S = 2.0 V

Mode	Noise [µg/√Hz] (Typical)	Current Consumption [µA] (Typical)
Normal Operation	550	1.8
Low Noise	400	3.0
Ultra-Low Noise	250	10

Table 7. Noise and current consumption in normal operation, Low Noise Mode, and Ultra-Low Noise Mode @ V_S = 3.3 V

Mode	Noise [µg/√Hz] (Typical)	Current Consumption [µA] (Typical)
Normal Operation	380	2.7
Low Noise	280	4.5
Ultra-Low Noise	175	15

Anti-Aliasing

The ADXL362's analog-to-digital converter (ADC) samples at the (user-selected) output data rate. In the absence of anti-aliasing filtering, it would therefore alias any input signals whose frequency is more than half the data rate. To mitigate this, a two-pole low-pass filter is provided at the input of the ADC. This anti-aliasing filter can be set by the user to have a bandwidth of one-half the data rate or one-fourth the data rate. Setting the anti-aliasing filter pole to ½ the output data rate provides less aggressive anti-aliasing filtering, but maximizes bandwidth and is adequate for most applications. Setting the pole to ¼ the data rate reduces bandwidth for a given data rate, but provides more aggressive anti-aliasing.

The ADXL362's anti-aliasing filter defaults to the more conservative setting, where bandwidth is set to ¼ the output data rate.

POWER SAVINGS FEATURES

The ADXL362 was designed for the most power-conscious applications, and as such includes several features, described in this section, for enabling power savings at the system level as well as at the device level.

ULTRA-LOW POWER CONSUMPTION IN ALL MODES

At the device level, the most obvious power saving feature of the ADXL362 is its ultra-low current consumption in all configurations: the ADXL362 consumes between 1.1 μA (typ) and 5 μA (typ) across all data rates up to 400 Hz and all supply voltages up to 3.6V (see Figure 4). An even lower-power, 350 nA (typ) motion-triggered Wake-Up Mode is provided for simple motion detection applications that require even lower power consumption than 1 μA.

At these current levels, the accelerometer consumes less power in full operation than many other system components' standby currents, and is therefore optimal for applications that require continuous acceleration monitoring and very long battery life. As the accelerometer is always on, it can act as a motion-activated switch and signal to the rest of the system when to turn on, thereby managing power at the system level.

No less important than its low operating current, the ADXL362's 10 nA (typ) Standby current contributes to much longer battery life in applications that spend most of their time in a "sleep" state and wake up via an external trigger.

MOTION DETECTION

The ADXL362 features built-in logic that detects Activity (presence of acceleration above a threshold) and Inactivity (lack of acceleration above a threshold).

Detection of an activity or inactivity event is indicated in the Status register and can also be configured to generate an interrupt. In addition, the activity status of the device – that is, whether it is "moving" or "stationary" – is indicated by the Awake bit, described on page 11.

Activity and Inactivity detection can be used when the accelerometer is in either Measurement Mode or Wake-Up Modes.

Activity Detection

An Activity event is detected when acceleration stays above a specified threshold for a specified time period.

Referenced and Absolute Configurations

Activity detection can be configured as Referenced or Absolute.

When using Absolute Activity detection, acceleration samples are compared to a user-set threshold to determine whether motion is present. For example, if a threshold of 0.5*g* is set and the acceleration on the z-axis is 1*g* for longer than the user-defined Activity time, the Activity status is asserted.

In many applications, it is advantageous for activity detection to be based not on an absolute threshold but on a deviation from a reference point or orientation. This is particularly useful as it removes the effect on Activity detection of the static 1*g* imposed by gravity. When an accelerometer is stationary, its output can reach 1*g*, even when it is not moving. In Absolute Activity, if the threshold were set to less than 1*g*, activity would immediately be detected in this case.

In the Referenced configuration, Activity is detected when acceleration samples are at least a user-set amount *above* an internally-defined reference, for the user-defined amount of time. The reference is calculated when Activity detection is engaged, so activity is only detected when the acceleration has deviated sufficiently from the initial orientation.

The Referenced configuration results in a very sensitive Activity detection that detects even the most subtle motion events.

Fewer False Positives

Ideally, the intent of Activity detection is to wake up a system only when motion is intentional, ignoring noise or small, unintentional movements. In addition to being sensitive to subtle motion events, the ADXL362 Activity detection algorithm is also designed to be robust in filtering out undesired triggers.

The ADXL362 activity detection functionality includes a timer that can be used to filter out unwanted motion and ensure that only sustained motion is recognized as Activity. The duration of this timer, as well as the acceleration threshold, are user-adjustable from 1 sample (i.e., no timer) to up to 20 seconds of motion.

Note that the Activity timer is operational in Measurement Mode only. In Wake-Up Mode, one-sample Activity detection is used.

Inactivity Detection

An Inactivity event is detected when acceleration remains below a specified threshold for a specified time. Inactivity detection can also be configured as Referenced or Absolute.

When using Absolute Inactivity detection, acceleration samples are compared to a user-set threshold for the user-set time to determine the absence of motion. The Absolute configuration should be used for implementing free-fall detection.

When using Referenced Inactivity detection, Inactivity is detected if acceleration samples are within *less than* a user-specified amount of an internally-defined reference, for a user-defined amount of time.

Referenced Inactivity, like Referenced Activity, is particularly useful for eliminating the effects of the 1*g* due to gravity. With

Absolute Inactivity, if the Inactivity threshold is set lower than 1 *g*, a device resting motionless does not detect Inactivity. With Referenced Inactivity, the same device under the same configuration does detect Inactivity.

The Inactivity timer can be set to anywhere from 2.5 ms (1 sample at 400 Hz ODR) to almost 90 minutes (65535 samples at 12.5Hz ODR) of inactivity, This means the accelerometer can be configured such that it must be stationary for up to 90 minutes before putting its system to sleep. The wide range of timer settings means that in applications where power conservation is critical, the system can be put to sleep after very short periods of inactivity; and in applications where continuous operation is critical, the system will stay on for as long as any motion at all is present.

Linking Activity and Inactivity Detection

The activity and inactivity detection functions can be used concurrently and processed manually by a host processor, or they can be configured to interact in several ways:

Default Mode: activity and inactivity detection are both enabled and all interrupts must be serviced by a host processor; that is, a processor must read each interrupt before it is cleared and can be used again.

Linked Mode: Activity and Inactivity detection are linked to each other such that only one of the functions is enabled at any given time. Once activity is detected, the device is assumed to be moving or "awake" and stops looking for activity: inactivity is expected as the next event, so only Inactivity detection operates. When inactivity is detected, the device is assumed to be stationary or "asleep". Now activity is expected as the next event, so only Activity detection operates.

In this mode, each interrupt must be serviced by a host processor before the next is enabled.

Loop Mode: motion detection operates as described in Linked Mode, but interrupts do not need to be serviced by a host processor. This configuration simplifies the implementation of commonly-used motion detection, and enhances power savings by reducing the amount of power used in bus communication.

Autosleep: In Linked or Loop mode, enabling Autosleep will cause the device to autonomously enter Wake-Up Mode (see p. 8) when inactivity is detected, and re-enter Measurement Mode when activity is detected.

Using The Awake Bit

The Awake bit is a status bit that indicates whether the ADXL362 is "awake" or "asleep". The device is "awake" when it has seen an Activity condition, and "asleep" when it has seen an Inactivity condition.

The Awake signal can be mapped to the INT1 or INT2 pin, and can thus be used as a status output to connect or disconnect power to downstream circuitry based on the Awake status of the accelerometer. Used in conjunction with Loop Mode, this configuration implements a trivial, autonomous motion-activated switch as shown in Figure 15.

If the turn-on time of downstream circuitry can be tolerated, this motion switch configuration can save significant system-level power by eliminating the standby current consumption of the rest of the application. This standby current can often exceed the full operating current of the ADXL362.

FIFO

The ADXL362 includes a deep 512-sample FIFO (first-in, first-out) buffer. The FIFO provides benefits primarily in two ways.

First, appropriate use of the FIFO enables system-level power savings by enabling the host processor to sleep for extended periods of time while the accelerometer autonomously collects data. Alternatively, using the FIFO to collect data can unburden the host while it tends to other tasks.

Second, the FIFO can be used in a Triggered mode to record all data *leading up to* an activity detection event, thereby providing context for the event. In the case of a system that identifies impact events, for example, the accelerometer can keep the entire system off while it stores acceleration data in its FIFO and look for an Activity event. When the impact event occurs, data that was collected prior to the event is frozen in the FIFO. The accelerometer can now wake the rest of the system and transfer this data to the host processor, thereby providing context for the impact event. In general, the more context available, the more intelligent decisions a system can make, so a deep FIFO is especially useful. The ADXL362 FIFO can store up to over 13 seconds of data, providing a clear picture of events prior to an Activity trigger.

All FIFO modes of operation, as well as the structure of the FIFO and instructions for retrieving data from it, are described in further detail in the Applications Information FIFO section on page 31.

COMMUNICATIONS

SPI Instructions

The ADXL362's digital interface is implemented with system-level power savings in mind. The following features enhance power savings:

- Burst reads and writes reduce the number of SPI communication cycles required to configure the part.
- Concurrent operation of Activity and Inactivity detection enables "set it and forget it" operation. Linked and Loop Modes further reduce

communications power by enabling clearing of interrupts without processor intervention.

- The FIFO is implemented such that consecutive samples can be read continuously via a multi-byte read of unlimited length, so one Read FIFO instruction can clear the entire contents of the FIFO. In many other accelerometers, each Read instruction retrieves only one sample. This FIFO construction also allows the use of direct memory access (DMA) to read the FIFO contents.

Bus Keepers

The ADXL362 includes bus keepers on all digital interface pins: MISO, MOSI, SCLK, /CS, INT1, and INT2. Bus keepers are used to prevent tri-state bus lines from floating when nothing is driving them, thus preventing through-current in any gate inputs that are on the bus.

MSB Registers

Acceleration and temperature measurements are converted to 12-bit values and transmitted via SPI using two registers per measurement. To read a full sample set of 3-axis acceleration data, six registers must be read.

Many applications do not require the accuracy that 12-bit data provides and prefer instead to save system-level power. The MSB registers XDATA, YDATA, and ZDATA enable this tradeoff. These registers contain the eight MSB's of the x-, y-, and z-axis acceleration data, so reading them effectively provides 8-bit acceleration values. Importantly, only three (consecutive) registers must be read to retrieve a full data set, significantly reducing the time during which the SPI bus is active and drawing current.

12-bit and 8-bit data are available simultaneously so can be used in a single application, depending on the needs of the application at a given time. For example, the processor can read 12-bit data while higher resolution is required, and switch to 8-bit data (simply by reading a different set of registers) when application requirements change.

ADDITIONAL FEATURES

FREE-FALL DETECTION

Many digital-output accelerometers include a built-in free-fall detection feature. In the ADXL362, this function can be implemented using the Inactivity interrupt. Refer to the Applications Information section on page 31 for more details including suggested threshold and timing values.

SELECTABLE OUTPUT DATA RATES

The ADXL362 can report acceleration data at various data rates ranging from 12.5 Hz to 400 Hz. The internal low-pass filter pole is automatically set to ¼ or ½ the selected ODR, based on the HALF_BW to ensure the Nyquist sampling criterion is met and no aliasing occurs.

Current consumption varies somewhat with output data rate as shown in Figure 4, remaining below 5.0 µA over the entire range of data rates and operating voltages.

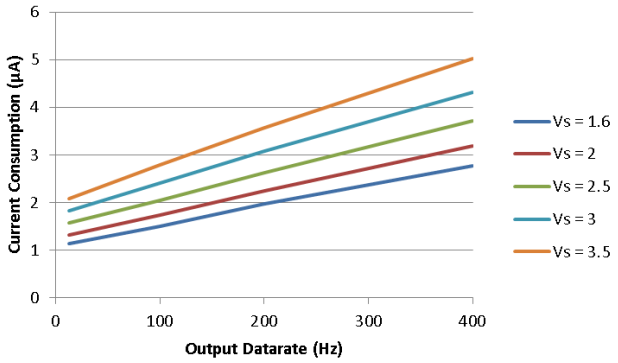

Figure 4. Current Consumption vs Output Data Rate at Several Supply Voltages

SELECTABLE MEASUREMENT RANGES

The ADXL362 has a selectable measurement ranges of ±2, ±4, and ±8 *g*. Acceleration samples are always converted by a 12-bit analog-to-digital converter (ADC), so sensitivity scales with *g*-range. Ranges and corresponding sensitivity values are listed in Table 1.

When acceleration exceeds the measurement extremes, data is clipped at the measurement range value, but no damage is caused to the accelerometer. The Absolute Maximum Ratings for acceleration on Page 3 indicates the acceleration level at which permanent damage may be caused to the device.

USING AN EXTERNAL CLOCK

The ADXL362 has a built-in clock that, by default, serves as the time base for internal operations. If desired, an external clock may be provided instead.

The external clock must operate at 51.2 kHz ± TBD%.

ODR and bandwidth scale proportionally with the clock. The ADXL362 provides a discrete number of options for ODR. Output data rates other than those provided can be achieved by selecting an appropriate clock frequency. For example, to achieve an 80 Hz ODR, the 100 Hz setting can be used with a clock frequency that is 80% of nominal, or 41.0 kHz. Bandwidth automatically scales to ½ or ¼ of the ODR (based on the HALF_BW setting), and this ratio is preserved regardless of clock frequency.

Power consumption also scales with clock frequency: higher clock rates increase power consumption. Figure 5 shows how power consumption varies with clock rate.

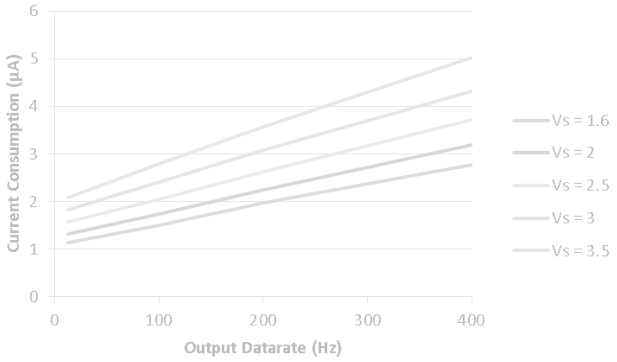

Figure 5. Current Consumption vs External Clock Rate [PLACEHOLDER]

SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL362 features an option to synchronize acceleration sampling to an external trigger.

SELF TEST

The ADXL362 incorporates a self-test feature that effectively tests its mechanical and electronic systems simultaneously. When the self-test function is invoked, an electrostatic force is applied to the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change in all three axes.

USER REGISTER PROTECTION

The ADXL362 includes user register protection for single event upsets (SEUs). A single event upset (SEU) is a change of state caused by ions or electromagnetic radiation striking a sensitive node in a microelectronic device. The state change is a result of the free charge created by ionization in or close to an important node of a logic element (for example, memory "bit"). The SEU itself is not considered permanently damaging to transistor or circuit functionality, but can create erroneous register values.

The registers protected from SEU are Registers 0x20 to 0x2E.

Protection is implemented via a 99-bit error-correcting (Hamming-type) code and detects both single- and double-bit errors. The check bits are recomputed any time a write to any of the protected registers occurs. At any time, if the stored version of the check bits is not in agreement with the current check bit calculation, the err_user_reg status bit is set.

This bit is set on an unconfigured device and clears upon the first register write.

TEMPERATURE SENSOR

The ADXL362 includes an integrated temperature sensor that can be used to monitor internal system temperature or improve the temperature stability of the device via calibration, for example. Acceleration outputs vary with temperature at a rate of 0.5 mg/°C (typ), but the relationship to temperature is repeatable and can therefore be calibrated.

SERIAL COMMUNICATIONS

The ADXL362 communicates via 4-wire SPI and operates as a slave. Data transmitted from the ADXL362 to the master device during writes to the ADXL362 should be ignored.

As shown in Figure 7 to Figure 11, the MISO pin is in a high impedance state, held by a bus keeper, except when the ADXL362 is actually sending read data, in order to conserve bus power.

The ADXL362 should be wired for SPI communication as shown in the connection diagram in Figure 6. The recommended SPI clock speeds are 1 MHz to 5 MHz (max speed TBD MHz), with 12 pF maximum loading.

The SPI timing scheme follows CPHA = CPOL = 0.

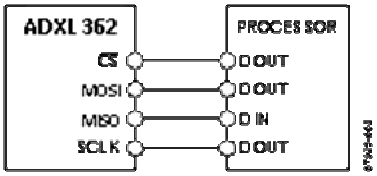

Figure 6. 4-Wire SPI Connection Diagram

SPI COMMANDS

The SPI port uses a multi-byte structure where the first byte is a command. The ADXL362 command set is:

- 0x0A : write register
- 0x0B : read register
- 0x0D : read FIFO

Read and Write Register Commands

The command structure for the read register and write register commands is as follows, and as shown in Figure 7 and Figure 8:

</CS down> <command byte (0x0A or 0x0B)> <address byte> <data byte> <additional data bytes for multi-byte> … </CS up>

The read and write register commands support multi byte (burst) read/write access. The waveform diagrams for multi-byte read and write commands are shown in Figure 9 and Figure 10.

Read FIFO Command

Reading from the FIFO buffer is a command structure that does not have an address:

</CS down> <command byte (0x0D)> <data byte> <data byte> … </CS up>

It is recommended that an even number of bytes be read (using a multi-byte transaction) since each sample consists of two bytes: 2 bits of axis information and 14 bits of data. If an odd number of bytes is read, it is assumed that the desired data was read and the second half of the last sample is discarded so a read from the FIFO always starts on a properly aligned even-byte boundary. Data is presented least significant byte first, followed by the most significant byte.

MULTI-BYTE TRANSFERS

Multi-byte transfers, also known as burst transfers, are supported for all SPI commands: register read, register write, and FIFO read commands. It is recommended that data be read using multi-byte transfers to ensure a concurrent and complete set of x-, y-, and z-acceleration (and temperature, where applicable) data is read.

The FIFO runs on the serial port clock during FIFO reads and can sustain bursting at the SPI clock rate as long as the SPI clock is 1 MHz or faster.

Register Read/Write Auto Increment

A register read or write command begins with the address specified in the command and auto-increments for each additional byte in the transfer. To avoid address wrapping and side effects of reading registers multiple times, the auto-increment halts at the invalid Register Address 63 (0x3F).

INVALID ADDRESSES AND ADDRESS FOLDING

The ADXL362 has a 6-bit address bus, mapping only 64 registers in the possible 256 register address space. The addresses will not fold to repeat the registers at addresses above 64. Attempted access to register addresses above 64 are mapped to the invalid register at 63 (0x3F) and have no functional effect.

Address 0x00 to Address 0x2E are for customer access, as described in the register map. Addresses 0x2F to Address 0x3F are reserved for factory use.

LATENCY RESTRICTIONS

Reading any of the data registers (0x08 to 0x0A or 0x0E to 0x15) clears the data ready interrupt. There is up to an 80 µs delay from reading a register to the clearing of the data ready interrupt.

Other register reads, register writes, and FIFO reads have no latency restrictions.

INVALID COMMANDS

Commands other than 0x0A, 0x0B, and 0x0D have no effect. The MISO output remains in a high impedance state, and the bus keeper holds the MISO line at its last value.

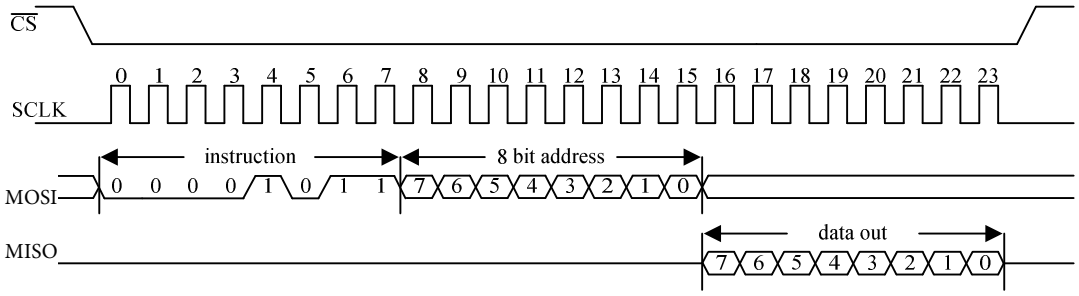

Figure 7. Register Read

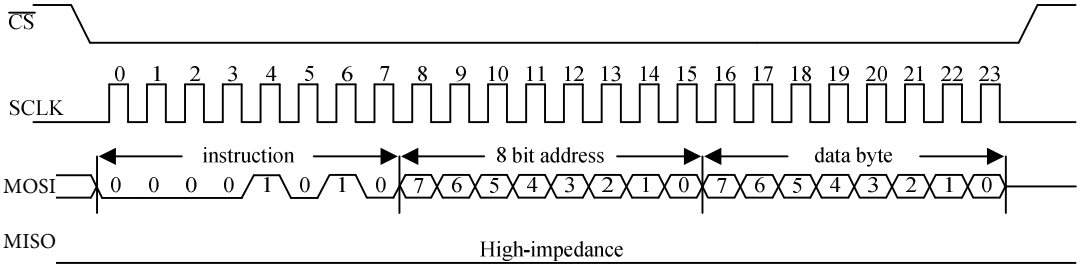

Figure 8. Register Write

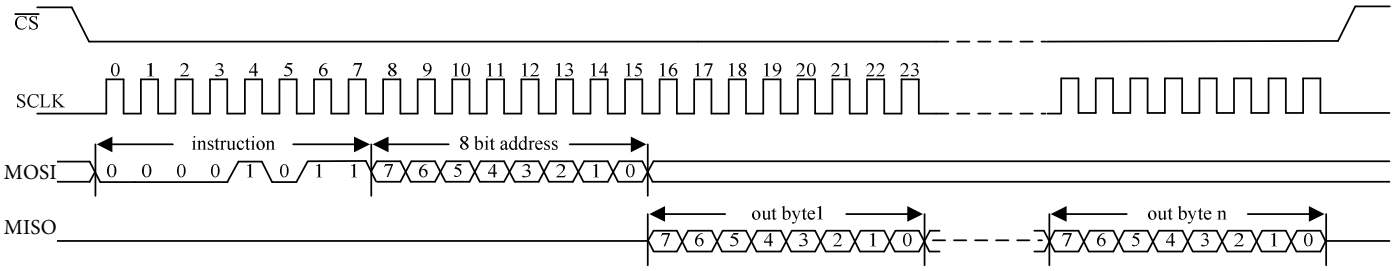

Figure 9. Burst Read

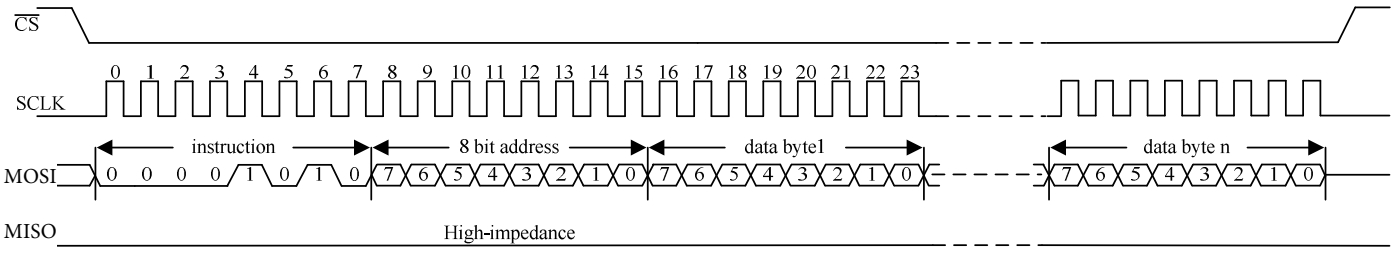

Figure 10. Burst Write

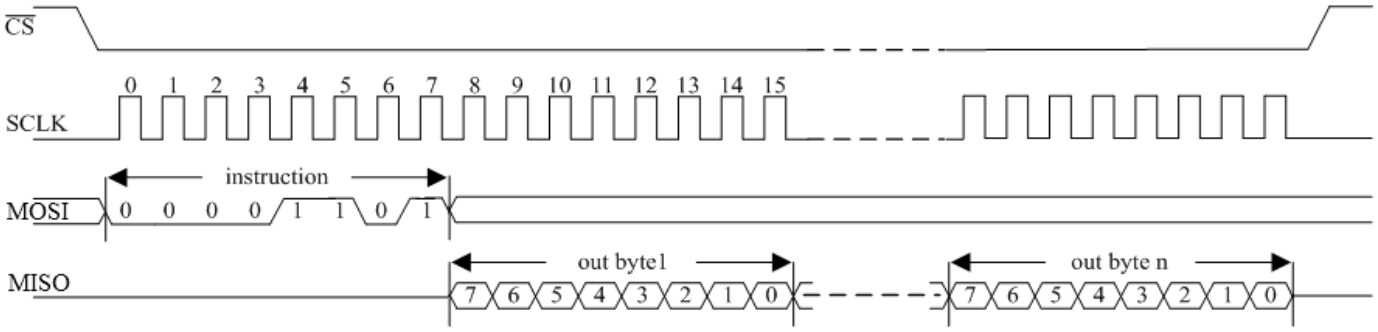

Figure 11. FIFO FIFO Read

REGISTER MAP

Table 8. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	DEVID_AD	[7:0]	DEVID_AD[7:0]								0xAD	R
0x01	DEVID_MST	[7:0]	DEVID_MST[7:0]								0x1D	R
0x02	PARTID	[7:0]	PARTID[7:0]								0xF2	R
0x03	REVID	[7:0]	REVID[7:0]								0x01	R
0x08	XDATA	[7:0]	XDATA[7:0]								0x00	R
0x09	YDATA	[7:0]	YDATA[7:0]								0x00	R
0x0A	ZDATA	[7:0]	ZDATA[7:0]								0x00	R
0x0B	STATUS	[7:0]	ERR_USER_REGS	AWAKE	INACT	ACT	FIFO_OVERRUN	FIFO_WATERMARK	FIFO_READY	DATA_READY	0x40	R
0x0C	FIFO_Entries_L	[7:0]	FIFO_Entries_L[7:1]							LSB	0x00	R
0x0D	FIFO_Entries_H	[7:0]	FIFO_Entries_H[7:2]						MSB	FIFO_Entries_H[0]	0x00	R
0x0E	XDATA_L	[7:0]	XDATA_L[7:1]							LSB	0x00	R
0x0F	XDATA_H	[7:0]	SX				MSB	XDATA_H[2:0]			0x00	R
0x10	YDATA_L	[7:0]	YDATA_L[7:1]							LSB	0x00	R
0x11	YDATA_H	[7:0]	SX				MSB	YDATA_H[2:0]			0x00	R
0x12	ZDATA_L	[7:0]	ZDATA_L[7:1]							LSB	0x00	R
0x13	ZDATA_H	[7:0]	SX				MSB	ZDATA_H[2:0]			0x00	R
0x14	TEMP_L	[7:0]	TEMP_L[7:1]							LSB	0x00	R
0x15	TEMP_H	[7:0]	SX				MSB	TEMP_H[2:0]			0x00	R
0x16	Reserved	[7:0]	Reserved[7:0]								0x00	R
0x17	Reserved	[7:0]	Reserved[7:0]								0x00	R
0x1F	SOFT_RESET	[7:0]	SOFT_RESET[7:0]								0x00	W
0x20	THRESH_ACT_L	[7:0]	THRESH_ACT_L[7:1]							LSB	0x00	RW
0x21	THRESH_ACT_H	[7:0]	UNUSED					MSB	THRESH_ACT_H[1:0]		0x00	RW
0x22	TIME_ACT	[7:0]	TIME_ACT[7:0]								0x00	RW
0x23	THRESH_INACT_L	[7:0]	THRESH_INACT_L[7:1]							LSB	0x00	RW
0x24	THRESH_INACT_H	[7:0]	UNUSED					MSB	THRESH_INACT_H[1:0]		0x00	RW
0x25	TIME_INACT_L	[7:0]	TIME_INACT_L[7:1]							LSB	0x00	RW
0x26	TIME_INACT_H	[7:0]	MSB	TIME_INACT_H[6:0]							0x00	RW
0x27	ACT_INACT_CTL	[7:0]	RES		LINKLOOP		INACT_REF	INACT_EN	ACT_REF	ACT_EN	0x00	RW
0x28	FIFO_CONTROL	[7:0]	UNUSED				AH	FIFO_TEMP	FIFO_MODE		0x00	RW
0x29	FIFO_Samples	[7:0]	FIFO_Samples[7:0]								0x80	RW
0x2A	INTMAP1	[7:0]	INT_LOW	AWAKE	INACT	ACT	FIFO_OVERRUN	FIFO_WATERMARK	FIFO_READY	DATA_READY	0x00	RW
0x2B	INTMAP2	[7:0]	INT_LOW	AWAKE	INACT	ACT	FIFO_OVERRUN	FIFO_WATERMARK	FIFO_READY	DATA_READY	0x00	RW
0x2C	FILTER_CTL	[7:0]	RANGE		RES	HALF_BW	EXT_SAMPLE	ODR			0x13	RW
0x2D	POWER_CTL	[7:0]	RES	EXT_CLK	LOW_NOISE		WAKEUP	AUTOSLEEP	MEASURE		0x00	RW
0x2E	SELF_TEST	[7:0]	UNUSED							ST	0x00	RW

REGISTER DETAILS

This section describes the functions of the ADXL362 registers. The ADXL362 powers up with default register values as shown in the register map on page 18.

Note that any changes to the registers before the POWER_CTL register (Registers 0x00 to 0x2C) should be made with the device in Standby. If changes are made while the ADXL362 is in Measurement Mode, it is possible that they may effective for only part of a measurement.

DEVICE ID REGISTER

Address: 0x00, Reset: 0xAD, Name: DEVID_AD

This register contains an Analog Devices device ID of 0xAD.

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	1	1	0	1

DEVICE ID: 0x1D REGISTER

Address: 0x01, Reset: 0x1D, Name: DEVID_MST

This register contains an Analog Devices MEMS device ID of 0x1D.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	1	1	0	1

PART ID: 0xF2 REGISTER

Address: 0x02, Reset: 0xF2, Name: PARTID

This register contains the device ID of 0xF2 (362 octal).

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	0	0	1	0

SILICON REVISION ID REGISTER

Address: 0x03, Reset: 0x01, Name: REVID

This register contains a product revision ID, beginning with 0x01 and incrementing for each subsequent revision.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	1

X-AXIS DATA (8 MSB) REGISTER

Address: 0x08, Reset: 0x00, Name: XDATA

This register holds the 8 most-significant bits of the x-axis acceleration data. This limited-resolution data register is provided for use in power-conscious applications where 8 bits of data are sufficient: energy can be conserved by reading only 1 byte of data per axis, rather than 2.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

Y-AXIS DATA (8 MSB) REGISTER

Address: 0x09, Reset: 0x00, Name: YDATA

This register holds the 8 most-significant bits of the y-axis acceleration data. This limited-resolution data register is provided for use in power-conscious applications where 8 bits of data are sufficient: energy can be conserved by reading only 1 byte of data per axis, rather than 2.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

Z-AXIS DATA (8 MSB) REGISTER

Address: 0x0A, Reset: 0x00, Name: ZDATA

This register holds the 8 most-significant bits of the z-axis acceleration data. This limited-resolution data register is provided for use in power-conscious applications where 8 bits of data are sufficient: energy can be conserved by reading only 1 byte of data per axis, rather than 2.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

STATUS REGISTER

Address: 0x0B, Reset: 0x00, Name: STATUS

This register includes the following bits that describe various conditions of the ADXL362.

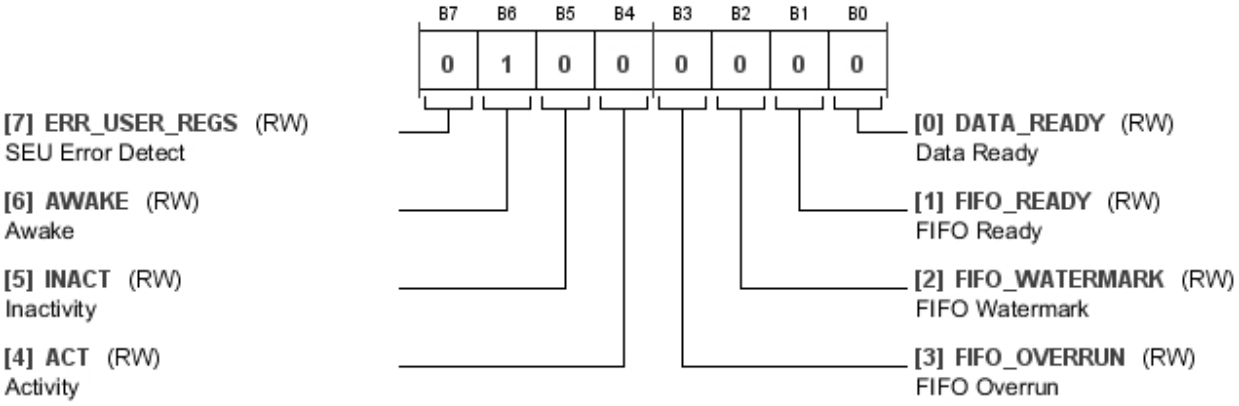

Table 9. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	ERR_USER_REGS		SEU Error Detect. A '1' indicates one of two things: either an SEU event, such as an alpha particle of power glitch, has disturbed a user register setting; or the ADXL362 is not configured. This bit is high on startup and soft reset and will reset as soon as any register write commands are performed.	0x0	RW
6	AWAKE		Indicates whether the accelerometer is in an "active" (AWAKE = 1) or "inactive" (AWAKE = 0) state, based on the activity and inactivity functionality. Activity and inactivity detection must be in Linked Mode or Loop Mode (LINK/LOOP bits in ACT_INACT_CTL register) to enable Autosleep. Otherwise this bit defaults to a '1' and should be ignored.	0x0	RW
5	INACT		Inactivity. A '1' indicates that the Inactivity detection function has detected an inactivity or a free-fall condition.	0x0	RW
4	ACT		Activity. A '1' indicates that the Activity detection function has detected an over-threshold condition.	0x0	RW
3	FIFO_OVERRUN		FIFO Overrun. A '1' indicates that the FIFO has overrun or overflowed, such that new data replaces unread data. Further details are provided in the FIFO Interrupts Section on page 33.	0x0	RW
2	FIFO_WATERMARK		FIFO Watermark. A '1' indicates that the FIFO contains at least the desired number of samples, as set in the FIFO_SAMPLES register. Further details are provided in the FIFO Interrupts Section on page 33.	0x0	RW
1	FIFO_READY		FIFO Ready. A '1' indicates that there is at least one sample available in the FIFO output buffer. Further details are provided in the FIFO Interrupts Section on page 33.	0x0	RW
0	DATA_READY		Data Ready. A '1' indicates that a new valid sample is available to be read. This bit clears when a FIFO read is performed. Further details are provided in the Data Ready Interrupt Section on page 33.	0x0	RW

FIFO ENTRIES REGISTERS

These registers indicate the number of valid data samples present in the FIFO buffer. This number ranges from 0 to 512, or 0x00 to 0x200. FIFO_ENTRIES_L contains the least significant byte. FIFO_ENTRIES_H contains the two most significant bits. Bits 15:10 of FIFO_ENTRIES_H are unused.

Address: 0x0C, Reset: 0x00, Name: FIFO_ENTRIES_L

Address: 0x0D, Reset: 0x00, Name: FIFO_ENTRIES_H

B15	B14	B13	B12	B11	B10	B9	B8
x	x	x	x	x	x	MSB	0

X-AXIS DATA REGISTERS

These two registers contain the sign-extended x-axis acceleration data. XDATA_L contains the 8 least-significant bits (LSB's), and XDATA_H contains the 4 most-significant bits (MSB's) of the 12-bit value.

The sign extension bits (B15:12, denoted SX below) will have the same value as the MSB (B11).

Address: 0x0E, Reset: 0x00, Name: XDATA_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x0F, Reset: 0x00, Name: XDATA_H

B15	B14	B13	B12	B11	B10	B9	B8
SX	SX	SX	SX	MSB	0	0	0

Note: SX denotes a sign extension bit.

Y-AXIS DATA REGISTERS

These two registers contain the sign-extended y-axis acceleration data. YDATA_L contains the 8 least-significant bits (LSB's), and YDATA_H contains the 4 most-significant bits (MSB's) of the 12-bit value.

The sign extension bits (B15:12, denoted SX below) will have the same value as the MSB (B11).

Address: 0x10, Reset: 0x00, Name: YDATA_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x11, Reset: 0x00, Name: YDATA_H

B15	B14	B13	B12	B11	B10	B9	B8
SX	SX	SX	SX	MSB	0	0	0

Note: SX denotes a sign extension bit.

Z-AXIS DATA REGISTERS

These two registers contain the sign-extended z-axis acceleration data. ZDATA_L contains the 8 least-significant bits (LSB's), and ZDATA_H contains the 4 most-significant bits (MSB's) of the 12-bit value.

The sign extension bits (B15:12, denoted SX below) will have the same value as the MSB (B11).

Address: 0x12, Reset: 0x00, Name: ZDATA_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x13, Reset: 0x00, Name: ZDATA_H

B15	B14	B13	B12	B11	B10	B9	B8
SX	SX	SX	SX	MSB	0	0	0

Note: SX denotes a sign extension bit.

TEMPERATURE DATA REGISTERS

These two registers contain the sign-extended temperature sensor output data. TEMP_L contains the 8 least-significant bits (LSB's), and TEMP_H contains the 4 most-significant bits (MSB's) of the 12-bit value. The value is sign-extended, so bits B15:B12 of TEMP_H will be all 0's or all 1's based on the value of bit B11.

The sign extension bits (B15:12, denoted SX below) will have the same value as the MSB (B11).

Address: 0x14, Reset: 0x00, Name: TEMP_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x15, Reset: 0x00, Name: TEMP_H

B15	B14	B13	B12	B11	B10	B9	B8
SX	SX	SX	SX	MSB	0	0	0

Note: SX denotes a sign extension bit.

SOFT RESET REGISTER

Address: 0x1F, Reset: 0x00, Name: SOFT_RESET

Writing the code 0x52 (“R”) to this register immediately resets the ADXL362. All register settings are cleared and the sensor is placed in Standby. Interrupt pins are configured to a high output impedance mode, held to a valid state by bus keepers.

This is a write-only register. If read, data in it is always 0x00.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

ACTIVITY THRESHOLD REGISTERS

This 11-bit unsigned value sets the threshold for activity detection. This value is set in codes; the value in Gees depends on the measurement range setting selected:

THRESH_ACT [Gees] = THRESH_ACT [codes] / sensitivity [codes/Gee]

To detect activity, the absolute value of the 12-bit acceleration data is compared with the 11-bit (unsigned) THRESH_ACT value. More details are provided in the Motion Detection section on page 10.

The THRESH_ACT_L register contains the least significant byte and the THRESH_ACT_H register contains the most significant bits of the THRESH_ACT value.

Address: 0x20, Reset: 0x00, Name: THRESH_ACT_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x21, Reset: 0x00, Name: THRESH_ACT_H

B15	B14	B13	B12	B11	B10	B9	B8
x	x	x	x	x	MSB	0	0

ACTIVITY TIME REGISTER

Address: 0x22, Reset: 0x00, Name: TIME_ACT

The Activity timer implements a robust activity detection that minimizes false positive motion triggers. When the timer is used, only sustained motion will trigger Activity detection. Refer to the Fewer False Positives section on page 10 for additional information.

The value in this register sets the number of consecutive samples that must have at least one axis greater than the Activity threshold (set by THRESH_ACT) for an Activity event to be detected.

The time in seconds is given by (TIME_ACT / ODR), where TIME_ACT is the value set in this register and ODR is the output data rate, set in the FILTER_CTL register (Address 0x2C).

Setting the Activity time to 0x00 has the same result as setting this time to 0x01: Activity is detected when a single acceleration sample has at least one axis greater than the Activity threshold (THRESH_ACT).

When the accelerometer is in Wake-up Mode, the TIME_ACT value is ignored and Activity is detected based on a single acceleration sample.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0

INACTIVITY THRESHOLD REGISTERS

This 11-bit unsigned value sets the threshold for inactivity detection. This value is set in codes; the value in Gees depends on the measurement range setting selected:

THRESH_INACT [Gees] = THRESH_INACT [codes] / sensitivity [codes/Gee]

To detect inactivity, the absolute value of the 12-bit acceleration data is compared with the 11-bit (unsigned) THRESH_INACT value. More details are provided in the Motion Detection section on page 10.

The THRESH_INACT_L register contains the least significant byte and the THRESH_INACT_H register contains the most significant bits of the THRESH_INACT value.

Address: 0x23, Reset: 0x00, Name: THRESH_INACT_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x24, Reset: 0x00, Name: THRESH_INACT_H

B15	B14	B13	B12	B11	B10	B9	B8
x	x	x	x	x	MSB	0	0

INACTIVITY TIME REGISTERS

The 16-bit value in these registers sets the number of consecutive samples that must have all axes lower than the inactivity threshold (set by THRESH_INACT) for an Inactivity event to be detected.

The time in seconds can be calculated as (TIME_INACT / ODR), where TIME_INACT is the value set in this register and ODR is the output data rate, set in the FILTER_CTL register (Address 0x2C).

The 16-bit value allows for long inactivity detection times. The maximum value is 0xFFFF or 65,535 samples. At the lowest output data rate, 12.5 Hz, this equates to almost 90 minutes. This means the accelerometer can be configured such that it must be stationary for up to 90 minutes before putting its system to sleep.

Setting the Activity time to 0x00 has the same result as setting this time to 0x01: Activity is detected when a single acceleration sample has at least one axis greater than the Activity threshold (THRESH_INACT).

Address: 0x25, Reset: 0x00, Name: TIME_INACT_L

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	LSB

Address: 0x26, Reset: 0x00, Name: TIME_INACT_H

B15	B14	B13	B12	B11	B10	B9	B8
MSB	0	0	0	0	0	0	0

ACTIVITY/INACTIVITY CONTROL REGISTER

Address: 0x27, Reset: 0xX0, Name: ACT_INACT_CTL

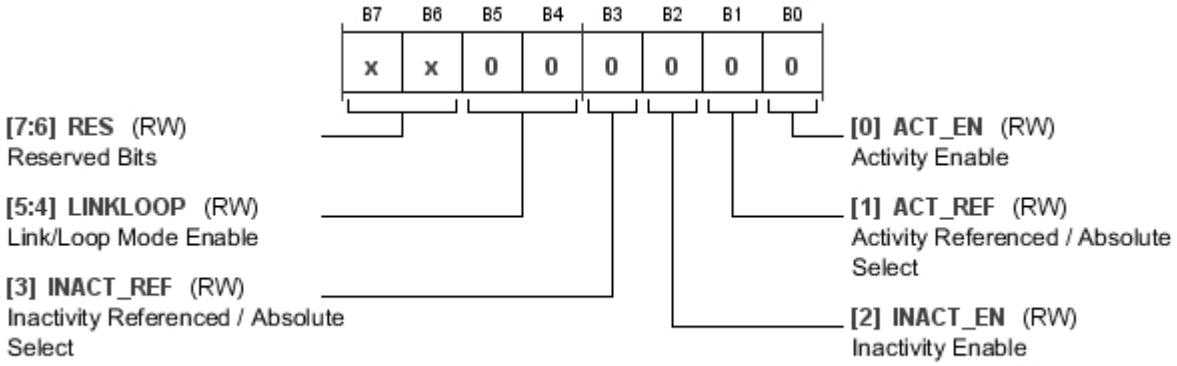

Table 10. Bit Descriptions for ACT_INACT_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	UNUSED		Unused bits.	0xX	RW
[5:4]	LINK/LOOP	0X	Default Mode : Activity and Inactivity detection are both enabled and their interrupts (if mapped) must be acknowledged by the host processor by reading the STATUS register. Autosleep is disabled in this mode. Use this mode for Free-Fall Detection applications.	0x0	RW
		10	Linked Mode : Activity and Inactivity detection are linked sequentially such that only one is enabled at a time. Their interrupts (if mapped) must be acknowledged by the host processor by reading the STATUS register.		
		11	Loop Mode: Activity and Inactivity detection are linked sequentially such that only one is enabled at a time, and their interrupts are internally acknowledged (do not need to be serviced by the host processor). Both ACT_EN and ENACT_EN (bits 2 and 0 in this register) must be set to 1 for Linked or Loop Mode to be used. Otherwise, Default Mode is used. For additional information, refer to the Linking Activity and Inactivity Detection on page 11.		
3	INACT_REF		Referenced / Absolute Inactivity Select. When '1', the Inactivity detection function operates in Referenced Mode. When '0', the Inactivity detection function operates in Absolute Mode.	0x0	RW
2	INACT_EN		Inactivity Enable. When '1', enables the Inactivity (Under-Threshold) functionality.	0x0	RW
1	ACT_REF		Referenced / Absolute Activity Select. When '1', the Activity detection function operates in Referenced Mode. When '0', the Activity detection function operates in Absolute Mode.	0x0	RW
0	ACT_EN		Activity Enable. When '1', enables the Activity (Over-Threshold) functionality.	0x0	RW

FIFO CONTROL REGISTER

Address: 0x28, Reset: 0x00, Name: FIFO_CONTROL

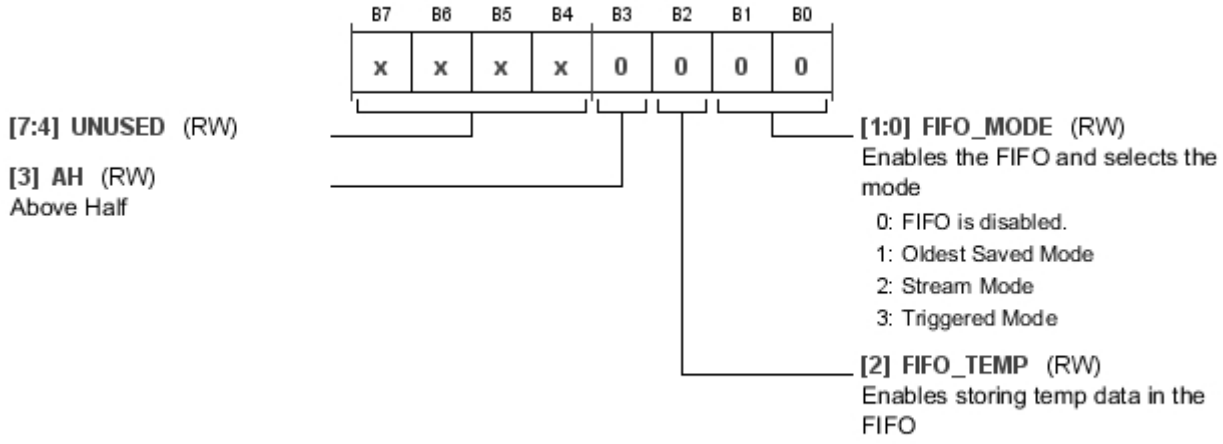

Table 11. Bit Descriptions for FIFO_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	UNUSED		Unused bits.	0x0	RW
3	AH		Above Half. This bit is the MSB of the FIFO_SAMPLES register, allowing FIFO Samples a range of 0 to 511.	0x0	RW
2	FIFO_TEMP		When '1', temperature data is stored in the FIFO along with x-, y-, and z-axis acceleration data.	0x0	RW
[1:0]	FIFO_MODE		Enables the FIFO and selects the mode.	0x0	RW
		00	FIFO is disabled.		
		01	Oldest Saved Mode		
		10	Stream Mode		
		11	Triggered Mode		

FIFO SAMPLES REGISTER

Address: 0x29, Reset: 0x00, Name: FIFO_SAMPLES

The value in this register specifies number of samples to store in the FIFO. The AH bit in the FIFO Control Register (Address 0x28) is used as the MSB of this value. The full range of FIFO Samples is 0 to 511.

The default value of this register is 0x80 to avoid triggering the FIFO Watermark interrupt (see page 33).

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0

Address: 0x28, Reset: 0x00, Name: FIFO_CONTROL (duplicated from page 25 to indicate AH bit)

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	MSB	X	X	X

AH

INT1/INT2 FUNCTION MAP REGISTERS

Address: 0x2A, Reset: 0x00, Name: INTMAP1

These registers configure the INT1/INT2 interrupt pins, respectively. Bits B6:B0 select which function(s) will generate an interrupt on the pin. If its corresponding bit is 1, the function will generate an interrupt on the INT pin. Bit B7 configures whether the pin operates in active high (B7 low) or active low (B7 high) mode.

Any number of functions can be selected simultaneously for each pin. If multiple functions are selected, their conditions are OR'ed together to determine the INT pin state. The status of each individual function can be determined by reading the STATUS register. If no interrupts are mapped to an INT pin, the pin remains in a high impedance state, held to a valid logic state by a bus keeper.

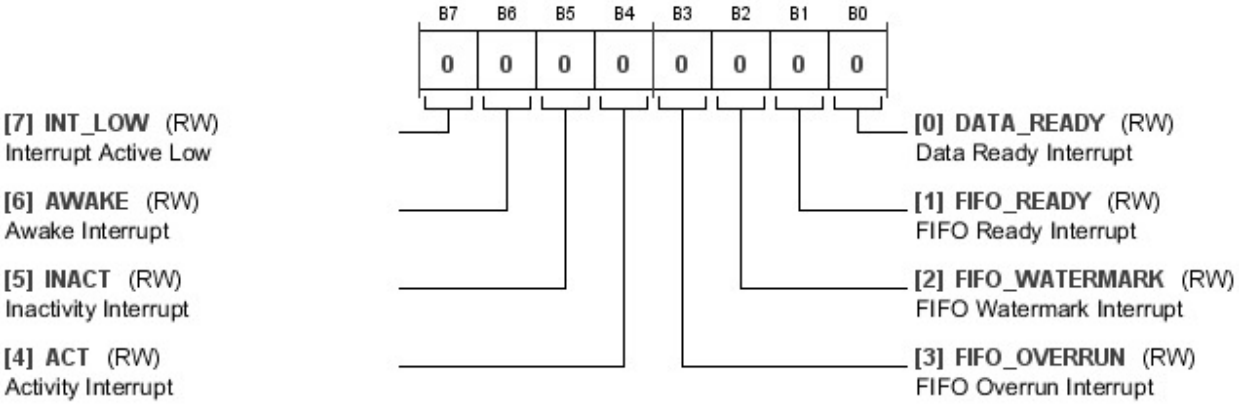

Table 12. Bit Descriptions for INTMAP1

Bits	Bit Name	Settings	Description	Reset	Access
7	INT_LOW		If '1', INT1 pin is Active Low.	0x0	RW
6	AWAKE		A '1' maps Awake status to INT1 pin.	0x0	RW
5	INACT		A '1' maps Inactivity status to INT1 pin.	0x0	RW
4	ACT		A '1' maps Activity status to INT1 pin.	0x0	RW
3	FIFO_OVERRUN		A '1' maps FIFO Overrun status to INT1 pin.	0x0	RW
2	FIFO_WATERMARK		A '1' maps FIFO Watermark status to INT1 pin.	0x0	RW
1	FIFO_READY		A '1' maps FIFO Ready status to INT1 pin.	0x0	RW
0	DATA_READY		A '1' maps Data Ready status to INT1 pin.	0x0	RW

Address: 0x2B, Reset: 0x00, Name: INTMAP2

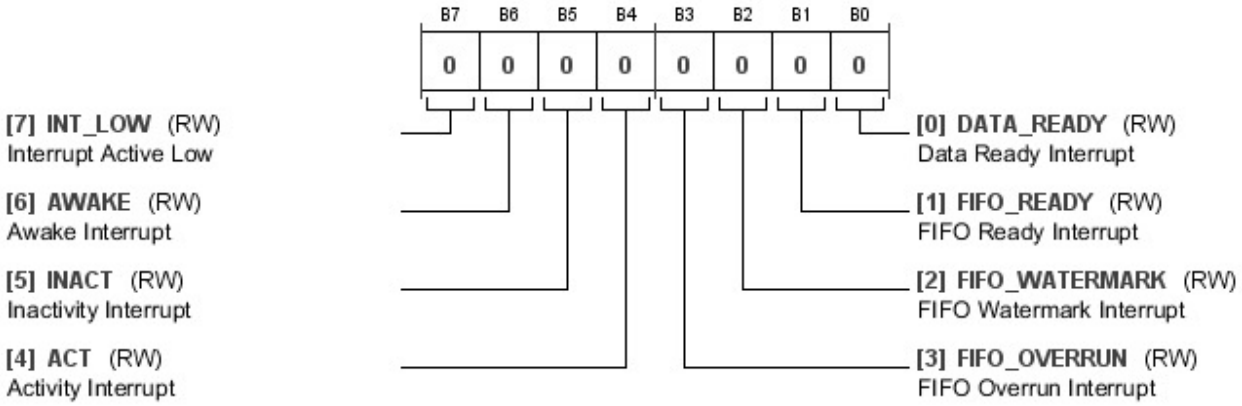

Table 13. Bit Descriptions for INTMAP2

Bits	Bit Name	Settings	Description	Reset	Access
7	INT_LOW		If '1', INT2 pin is Active Low.	0x0	RW
6	AWAKE		A '1' maps Awake status to INT2 pin.	0x0	RW
5	INACT		A '1' maps Inactivity status to INT2 pin.	0x0	RW
4	ACT		A '1' maps Activity status to INT2 pin.	0x0	RW
3	FIFO_OVERRUN		A '1' maps FIFO Overrun status to INT2 pin.	0x0	RW
2	FIFO_WATERMARK		A '1' maps FIFO Watermark status to INT2 pin.	0x0	RW
1	FIFO_READY		A '1' maps FIFO Ready status to INT2 pin.	0x0	RW
0	DATA_READY		A '1' maps Data Ready status to INT2 pin.	0x0	RW

FILTER CONTROL REGISTER

Address: 0x2C, Reset: 0x00, Name: FILTER_CTL

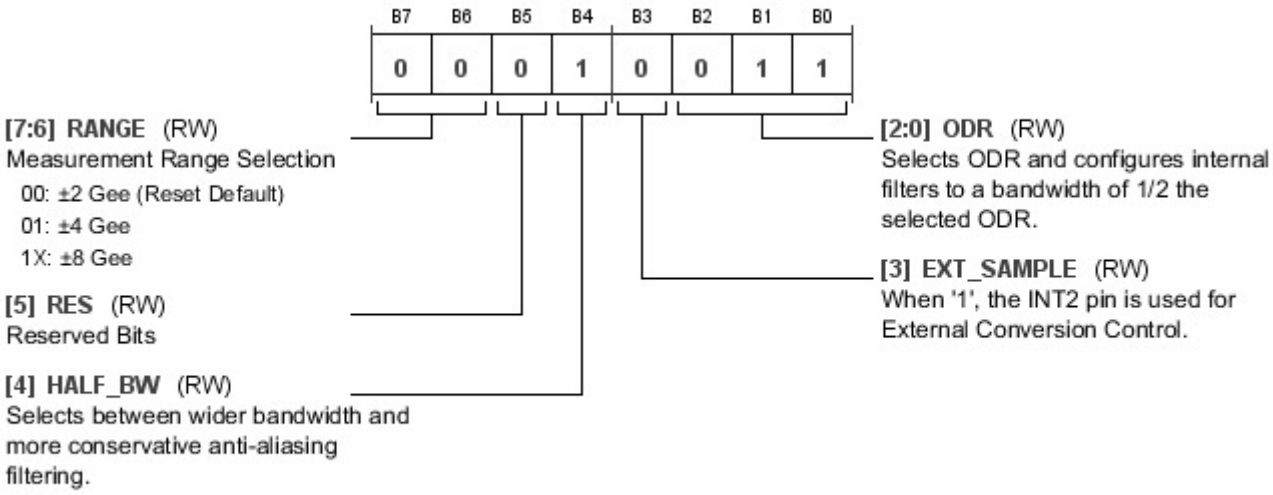

Table 14. Bit Descriptions for FILTER_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RANGE		Measurement Range Selection.	0x0	RW
		00	±2 Gee (Reset Default)		
		01	±4 Gee		
		1X	±8 Gee		
5	RES		Reserved.	0x0	RW
4	HALF_BW		When '1', the bandwidth of the anti-aliasing filters is set to ¼ the output data rate (ODR) for more conservative filtering. When '0', the bandwidth of the filters is set to ½ the ODR for a wider bandwidth. Additional information is provided in the Anti-Aliasing section on page 9.	0x1	
3	EXT_SAMPLE		When '1', the INT2 pin is used for External Conversion Control. Refer to the Synchronized Data Sampling section on page 33 for more information.	0x0	RW
[2:0]	ODR		Selects ODR and configures internal filters to a bandwidth of ½ or ¼ the selected ODR, depending on the HALF_BW bit setting.	0x0	RW
		000	12.5 Hz		
		001	25 Hz		
		010	50 Hz		
		011	100 Hz (Reset Default)		
		100	200 Hz		
		101...111	400 Hz		

POWER CONTROL REGISTER

Address: 0x2D, Reset: 0x00, Name: POWER_CTL

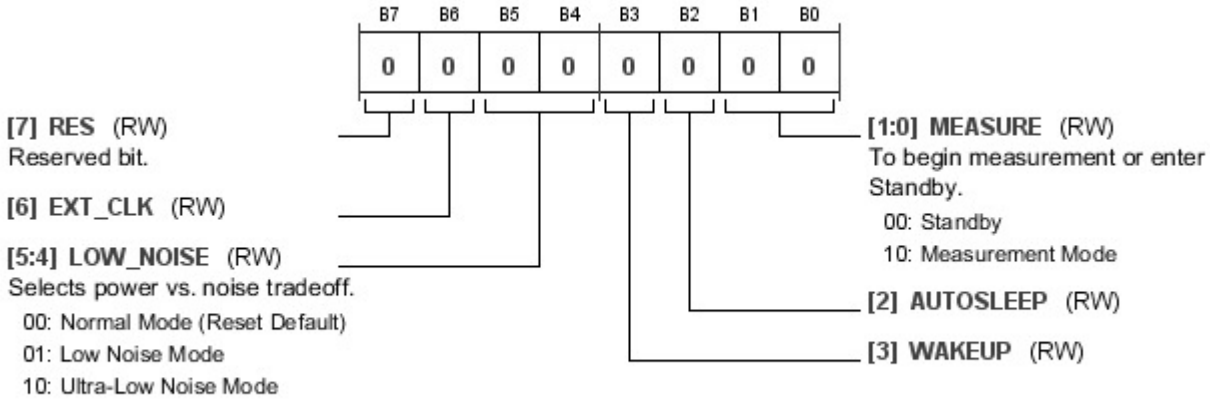

Table 15. Bit Descriptions for POWER_CTL

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved.	0x0	RW
6	EXT_CLK		When '1', the accelerometer runs off the external clock provided on the INT1 pin. Refer to the Using an External Clock section for additional details.	0x0	RW
[5:4]	LOW_NOISE		Selects power vs. noise tradeoff:	0x0	RW
		00	Normal Operation (Reset Default)		
		01	Low Noise Mode		
		10	Ultra-Low Noise Mode		
		11	Reserved		
3	WAKEUP		When '1', the part is operates in Wake-up Mode. Refer to the Operating Modes section for a detailed description of Wake-up Mode.	0x0	RW
2	AUTOSLEEP		When '1', Autosleep is enabled and the device enters Wake-up Mode automatically upon detection of Inactivity. Activity and inactivity detection must be in Linked Mode or Loop Mode (LINK/LOOP bits in ACT_INACT_CTL register) to enable Autosleep. Otherwise the bit is ignored. Refer to the Motion Detection section on page 10for details.	0x0	RW
[1:0]	MEASURE		Selects Measurement Mode or Standby.	0x0	RW
		00	Standby		
		01	Reserved		
		10	Measurement Mode		
		11	Reserved		

SELF TEST REGISTER

Address: 0x2E, Reset: 0x00, Name: SELF_TEST

Refer to the Self Test section on page 13 for information on the operation of the Self-Test feature, and on page 34 for guidelines on how to use this functionality.

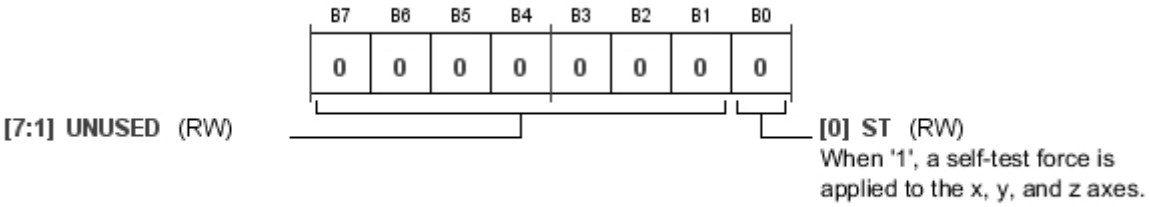

Table 16. Bit Descriptions for SELF_TEST

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	UNUSED			0x0	RW
0	ST		When '1', a self-test force is applied to the x, y, and z axes.	0x0	RW

APPLICATIONS INFORMATION

DEVICE CONFIGURATION

This section outlines the procedure for configuring the device and acquiring data. In general, the procedure follows the order of the register map, starting with register 0x20: THRESH_ACT_L.

1. Set Activity and Inactivity thresholds and timers: write to registers 0x20 – 0x26.

   For minimizing false positive motion triggers, set the TIME_ACT register greater than 1.
2. Configure Activity and Inactivity functions: write to register 0x27.
3. Configure FIFO: write to registers 0x28 – 0x29.
4. Map interrupts: write to registers 0x2A – 0x2B.
5. Configure general device settings: write to register 0x2C.
6. Turn measurement on: write to register 0x2D.

Settings for each of the registers vary based on application requirements. The registers are further described in the Register Details section, which starts on page 19.

Example: Implementing Free-Fall Detection

Many digital-output accelerometers include a built-in free-fall detection feature. In the ADXL362, this function can be implemented using the Inactivity interrupt.

When an object is in true free-fall, acceleration on all axes is 0 *g*. Thus, free-fall detection is achieved by looking for acceleration on all axes to fall below a certain threshold (close to 0 *g*) for a certain amount of time.

The Inactivity detection functionality, when used in Absolute Mode, does exactly this. To use inactivity to implement free-fall detection, set the value in THRESH_INACT to the desired free-fall threshold. Values between 300 m*g* and 600 m*g* are recommended; the register setting for these values varies based on the *g*-range setting of the device:

THRESH_INACT = threshold value [*g*] * scale factor [LSB/*g*]

Set the value in TIME_INACT to implement the minimum amount of time that the acceleration on all axes must be less than the free-fall threshold to generate a free-fall condition. Values between 100 ms and 350 ms are recommended; the register setting for this varies based on the output data rate:

TIME_INACT = time [s] × data rate [Hz]

When a free-fall condition is detected, the inactivity status sets to '1' and, if the function is mapped to an interrupt pin, an inactivity interrupt triggers on that pin.

Startup Routine

The following startup routine configures the ADXL362 for a typical free-fall application. This routine assumes a 2*g* measurement range and 100Hz output data rate.

1. Write 0x96 (150 codes) to register 0x23: sets free-fall threshold to 600 m*g*.
2. Write 0x03 to register 0x25: sets free-fall time to 30 ms.
3. Write 0x0C to register 0x27: enables Absolute Inactivity detection.
4. Write 0x20 to register 0x2A or 0x2B to map the Inactivity interrupt to INT1 or INT2, respectively.
5. Write 0x83 to register 0x2C: configures the accelerometer to ±8*g* range, 100 Hz ODR (output data rate).
6. Write 0x02 to register 0x2D to begin measurement.

Implementation of a complete fall detection application is described in application note AN-1023, *Fall Detection Application by Using 3-Axis Accelerometer ADXL345*.

FIFO

The FIFO is a 512-sample memory buffer that can be used to save power, unburden the host processor, and autonomously record data.

The 512 FIFO samples can be allotted as either:

- 170 sample sets of concurrent three-axis data; *or*
- 128 sample sets of concurrent three-axis and temperature data

The FIFO operates in one of the four modes described in this section.

FIFO Disabled

When the FIFO is disabled, no data is stored in it and any data already in it is cleared.

The FIFO is disabled by setting the FIFO_MODE bits in the FIFO_CONTROL register (address 0x28) to binary value 0b00.

Oldest Saved Mode

In Oldest Saved Mode, the FIFO accumulates data until it is full, and then stops. Additional data is collected only when space is made available by reading samples out of the FIFO buffer.

The FIFO is placed into Oldest Saved Mode by setting the FIFO_MODE bits in the FIFO_CONTROL register (address 0x28) to binary value 0b01.

Stream Mode

In Stream Mode, the FIFO always contains the most recent data. The oldest sample is discarded if space is needed to make room for a newer sample.

Stream Mode is useful for unburdening a host processor. The processor can tend to other tasks while data is collected in the FIFO. When the FIFO fills to a certain number of samples (specified by FIFO_SAMPLES), it triggers a Watermark Interrupt. At this point, the host processor can read the contents of the entire FIFO, and then return to its other tasks as the FIFO fills again.

The FIFO is placed into Stream Mode by setting the FIFO_MODE bits in the FIFO_CONTROL register (address 0x28) to binary value 0b10.

Triggered Mode

In Triggered Mode, the FIFO saves samples surrounding an Activity detection event. The operation is similar to a One-time Run trigger on an oscilloscope.

The FIFO is placed into Triggered Mode by setting the FIFO_MODE bits in the FIFO_CONTROL register (address 0x28) to binary value 0b11.

Configuration

The FIFO is configured via registers 0x28 and 0x29. Settings are described in detail on page 25.

Retrieving Data from FIFO

FIFO data is read by issuing a FIFO read command, described in the SPI Commands section. Data is formatted as a 16-bit value as represented in Table 17.

When reading data, the least-significant byte (Bits B7:B0) is read first, followed by the most-significant byte (Bits B15:B8). Bits B11:B0 represent the 12-bit, two's complement acceleration or temperature data. Bits B13:B12 are sign extension bits, and bits B15:B14 indicate the type of data, as indicated in Table 17.

Table 17. FIFO Buffer Data Format

B7	B6	B5	B4	B3	B2	B1	B0
Data							LSB

B15	B14	B13	B12	B11	B10	B9	B8
Data Type: 00: x-axis 01: y-axis 10: z-axis 11: temp		Sign Extension		MSB	Data		

Due to the 16-bit data format, it is required that data be read from the FIFO two bytes at a time. If a multi-byte read is performed, the number of bytes read should always be an even number. Multi-byte reads of FIFO data can be performed with no limit on the number of bytes read. If additional bytes are read after the FIFO is empty, the data in them will be 0x00.

As each sample set is acquired, it is written into the FIFO in the following order:

<X-Axis>

<Y-Axis >

<Z-Axis >

<Temperature> ***[optional]***

This pattern repeats until the FIFO is full, at which point the behavior depends on the FIFO Mode (see the FIFO section on page 31). If the FIFO has insufficient space for four data entries (or three entries if temperature is not being stored), then an incomplete sample set may be stored.

FIFO data is output on a per datum basis: as each data item is read, the same amount of space is freed up in the stack. Again, this may lead to incomplete sample sets being present in the FIFO.

For additional system-level FIFO applications, refer to application note AN-1025, *Utilization of the First In, First Out (FIFO) Buffer in Analog Devices, Inc. Digital Accelerometers*.

INTERRUPTS

Several of the built-in functions of the ADXL362 can trigger interrupts to alert the host processor of certain status conditions. Functionality of these interrupts is described in this section.

Interrupt Pins

Interrupts may be mapped to either (or both) of two designated output pins, INT1 and INT2, by setting the appropriate bits in the INTMAP1 and INTMAP2 registers, respectively. All functions can be used simultaneously. If multiple interrupts are mapped to one pin, the OR combination of the interrupts determines the status of the pin.

If no functions are mapped to an interrupt pin, that pin is automatically configured to a high-impedance (high-Z) state. The pins are placed in this state upon a reset as well.

When a certain status condition is detected, the pin that condition is mapped to is activated. The configuration of the pin is active high by default, so that when it is activated the pin goes high. However, this configuration can be switched to active low by setting the INT_LOW pin in the appropriate INTMAP register.

The INT pins may be connected to the interrupt input of a host processor and interrupts responded to with an interrupt routine. Because multiple functions can be mapped to the same

pin, the STATUS register can be used to determine which condition caused the interrupt to trigger.

Interrupts can be cleared in one of several ways:

- Reading the STATUS registers clears activity and inactivity interrupts.
- Reading from the data registers (Addresses 0x08 to 0x0A or 0x0E to 0x15) clears DATA_READY interrupt.
- Reading enough data from the FIFO buffer so that interrupt conditions are no longer met clears FIFO_READY, WATERMARK, and FIFO_OVERRUN interrupts.

Both interrupt pins are push-pull low impedance pins with output impedance TBD. Both have bus keepers that hold them to a valid logic state when they are in a high-impedance mode.

It is recommended that interrupts be disabled when their settings, such as thresholds, timings or other values, are configured, to prevent interrupts from being falsely triggered during configuration.

Alternate Functions

The INT1 and INT2 pins can be configured for use as input pins instead of for signaling interrupts. INT1 is used as an external clock input when the EXT_CLK bit (Bit 6) in the POWER_CTL register (Address 0x2D) is set. INT2 is used as the trigger input for synchronized sampling if the EXT_SAMPLE bit (Bit 3) in the FILTER_CTL register (Address 0x2C) is set. One or both of these alternate functions can be used concurrently; however, if an interrupt pin is used for its alternate function it cannot simultaneously be used to signal interrupts.

External clocking and data synchronization are both described in the Applications Information section on page 31.

Activity and Inactivity Interrupts

The ACT bit (Bit 4) and INACT bit (Bit 5) are set when activity and inactivity are detected, respectively. Detection procedures and criteria are described in the Motion Detection section on page 10.

Data Ready Interrupt

The DATA_READY bit (Bit 0) is set when new valid data is available and is cleared when no new data is available.

The DATA_READY bit does not set while any of the data registers -- 0x08 to 0x0A, 0x0E to 0x15 -- are being read. If DATA_READY = 0 prior to a register read and new data becomes available during the register read, then DATA_READY remains 0 until the read is complete and only then sets to 1.

If DATA_READY = 1 prior to a register read, then it is cleared at the start of the register read.

If DATA_READY = 1 prior to a register read and new data becomes available during the register read, then DATA_READY is cleared to 0 at the start of the register read and remains 0 throughout the read. When the read is complete, DATA_READY is set to 1.

FIFO Interrupts

Watermark

The FIFO_WATERMARK bit (Bit 2) is set when the number of samples stored in the FIFO is equal to or exceeds the number specified in the FIFO_SAMPLES register (Address 0x29) along with the AH bit in the FIFO_CONTROL register (Bit 3, Address 0x28). The FIFO_WATERMARK bit is cleared automatically when enough samples are read from the FIFO such that the number of samples remaining is lower than that specified.

If the number of FIFO Samples is set to 0, the Watermark Interrupt will be set. To avoid unexpectedly triggering this interrupt, the default value of the FIFO_SAMPLES register is 0x80.

FIFO Ready

The FIFO_READY bit (Bit 1) is set when there is at least one valid sample available in the FIFO output buffer. This bit is cleared when no valid data is available in the FIFO.

Overrun

The FIFO_OVERRUN bit (Bit 3) is set when the FIFO has overrun or overflowed, such that new data replaces unread data. This may indicate a full FIFO that has not yet been emptied, or a clocking error caused by a slow SPI transaction. If the FIFO is configured to Oldest Saved Mode, an Overrun event indicates that there is insufficient space available for a new sample.

The FIFO_OVERRUN bit is automatically cleared when the contents of the FIFO are read.

When the FIFO is disabled, the FIFO_OVERRUN bit is cleared.

SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL362 features an option to synchronize acceleration sampling to an external trigger. This feature is enabled by the EXT_SAMPLE bit (Bit 3) in the FILTER_CTL Register (Address 0x2C). When this bit is set to '1', the INT2 pin is automatically reconfigured for use as the sync trigger input.

When external triggering is enabled, it is up to the system designer to ensure that the sampling frequency meets system requirements. Sampling too infrequently will cause aliasing. Noise can be lowered by oversampling; however, sampling at too high a frequency may not allow enough time for the accelerometer to process the acceleration data and convert it to valid digital output.

Signal integrity is maintained when Nyquist criteria are met. An internal anti-aliasing filter is available in the ADXL362 and can assist the system designer in maintaining signal integrity. To

prevent aliasing, the filter bandwidth should be set to a frequency no greater than ½ the sampling rate. For example, when sampling at 100 Hz, the filter pole should be set no higher than 50 Hz. The filter pole is set via the ODR bits in the FILTER_CTL register (Address 0x2C). The filter bandwidth is set to ½ the ODR set via these bits. Even though the ODR is ignored (as the data rate is set by the external trigger), the filter is still applied at the specified bandwidth.

Due to internal timing requirements, the trigger signal applied to pin INT2 must meet the following criteria:

- The trigger signal is active high.
- The pulse width of the trigger signal must be at least 25 µs.
- The trigger must be deasserted for at least 25 µs before it is reasserted.
- The maximum sampling frequency supported is TBD Hz.
- The minimum sampling frequency is set only by system requirements. Samples need not be polled at any minimum rate; however, if samples are polled at a rate lower than the bandwidth set by the anti-aliasing filter, then aliasing may occur.

USING AN EXTERNAL CLOCK

The ADXL362 has a built-in clock that, by default, is used for clocked internal operations. If desired, an external clock may be provided and used.

To use an external clock, the EXT_CLK bit (Bit 6) in the POWER_CTL register (Address 0x2D) must be set. Setting this bit reconfigures the INT1 pin to an input pin on which the clock should be provided.

The external clock must operate at 51.2 kHz.

SELF TEST

The self-test function, described on page 13, is enabled via the ST bit in the SELF_TEST register, Address 0x2E. The recommended procedure for using the self-test functionality is outlined as follows:

1. Read acceleration data for the x-, y-, and z-axes.
2. Assert self-test by setting the ST bit in the SELF_TEST register, Address 0x2E.
3. Wait 1/ODR for the output to settle to its new value.
4. Read acceleration data for the x-, y-, and z-axes.
5. Compare to the values from Step 1. If the difference falls within the self-test output change specification presented in Table 1, then the device passes self-test and is deemed operational.
6. Deassert self-test by clearing the ST bit in the SELF_TEST register, Address 0x2E.

Because the electrostatic force is proportional to V_S^2, and the sensitivity of the device is ratiometric to V_S, the output change varies with V_S. This effect is shown in Figure 12.

Figure 12. Self-Test Output Change vs Supply Voltage [PLACEHOLDER]

OPERATION AT VOLTAGES OTHER THAN 2.0 V

The ADXL362 is tested and specified at a supply voltage of V_S = 2.0 V; however, it can be powered with a V_S as high as 3.3 V (nominal; 3.6V max) or as low as 1.8 V (nominal; 1.6V min). Some performance parameters change as the supply voltage changes, including the supply current, noise, offset, sensitivity, and self-test.

The effect on current consumption of varying supply voltage is shown in Figure 4.

The effect on noise of varying supply voltage is shown in Table 6 and Table 7.

Table TBD summarizes the effect on offset and noise of varying supply voltage.

Finally, the effect on self-test output delta is shown in Figure 12.

MECHANICAL CONSIDERATIONS FOR MOUNTING

The ADXL362 should be mounted on the PCB in a location close to a hard mounting point of the PCB to the case. Mounting the ADXL362 at an unsupported PCB location, as shown in Figure 13, may result in large, apparent measurement errors due to undampened PCB vibration. Locating the accelerometer near a hard mounting point ensures that any PCB vibration at the accelerometer is above the accelerometer's mechanical sensor resonant frequency and, therefore, effectively invisible to the accelerometer. Multiple mounting points, close to the sensor, and/or a thicker PCB also help to reduce the effect of system resonance on the performance of the sensor.

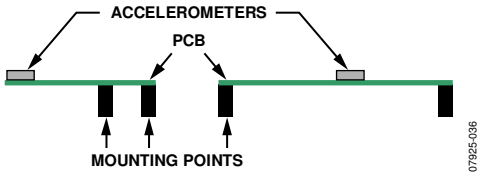

Figure 13. Incorrectly Placed Accelerometers

POWER SUPPLY DECOUPLING

A 1 µF tantalum capacitor (C_S) at V_S and a 0.1 µF ceramic capacitor ($C_{I/O}$) at $V_{DD\ I/O}$ placed close to the ADXL362 supply pins is recommended to adequately decouple the accelerometer from noise on the power supply. If additional decoupling is necessary, a resistor or ferrite bead, no larger than 100 Ω, in series with V_S may be helpful. Additionally, increasing the bypass capacitance on V_S to a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor may also improve noise.

Care should be taken to ensure that the connection from the ADXL362 ground to the power supply ground has low impedance because noise transmitted through ground has an effect similar to noise transmitted through V_S. It is recommended that V_S and $V_{DD\ I/O}$ be separate supplies to minimize digital clocking noise on the V_S supply. If this is not possible, additional filtering of the supplies, as previously mentioned, may be necessary.

APPLICATION CIRCUITS

This section includes a few application circuits, highlighting useful features of the ADXL362.

Power Supply Decoupling

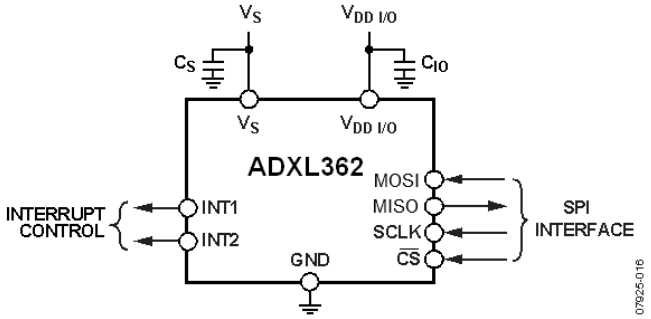

Figure 14. Application Diagram showing recommended bypass capacitors

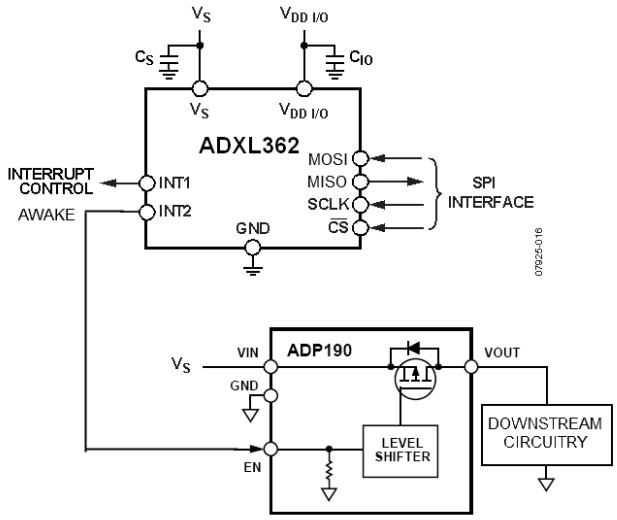

Figure 15. Application Diagram for using the AWAKE signal, mapped to INT2 pin, to drive a high-side power switch (e.g., the ADP190) that controls power to downstream circuitry

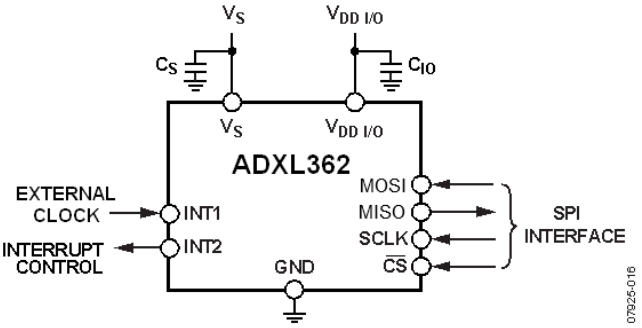

Figure 16. Application diagram for using the INT1 pin as an input for an external clock. In this mode, the external clock determines all accelerometer timing including output data rate and bandwidth.

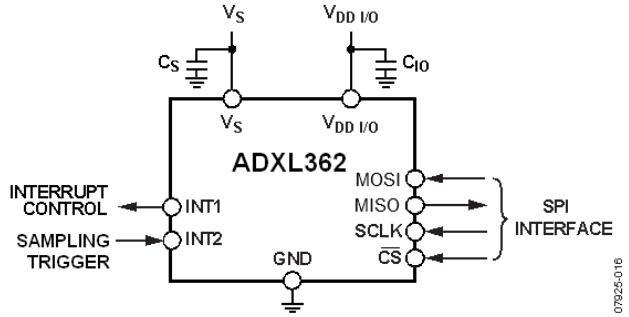

Figure 17. Application diagram for using the INT2 pin as an trigger for synchronized sampling. Acceleration samples are taken every time this trigger is activated.

AXES OF ACCELERATION SENSITIVITY

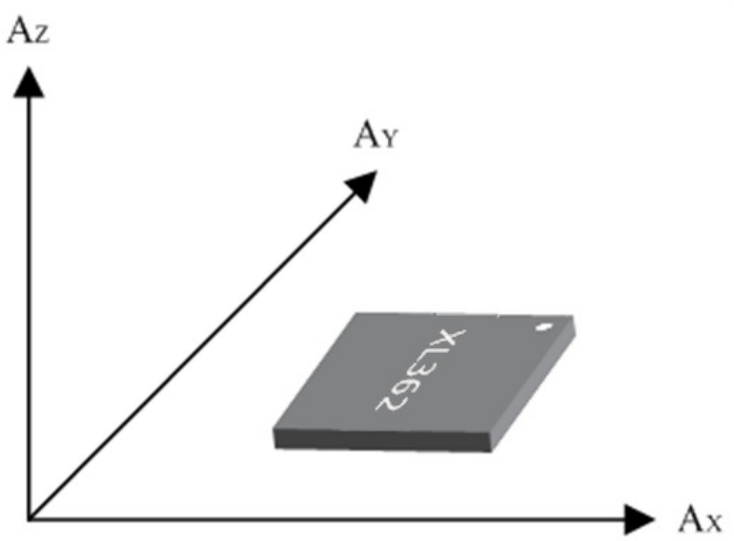

Figure 18. Axes of Acceleration Sensitivity (Corresponding Output Increases When Accelerated Along the Sensitive Axis)

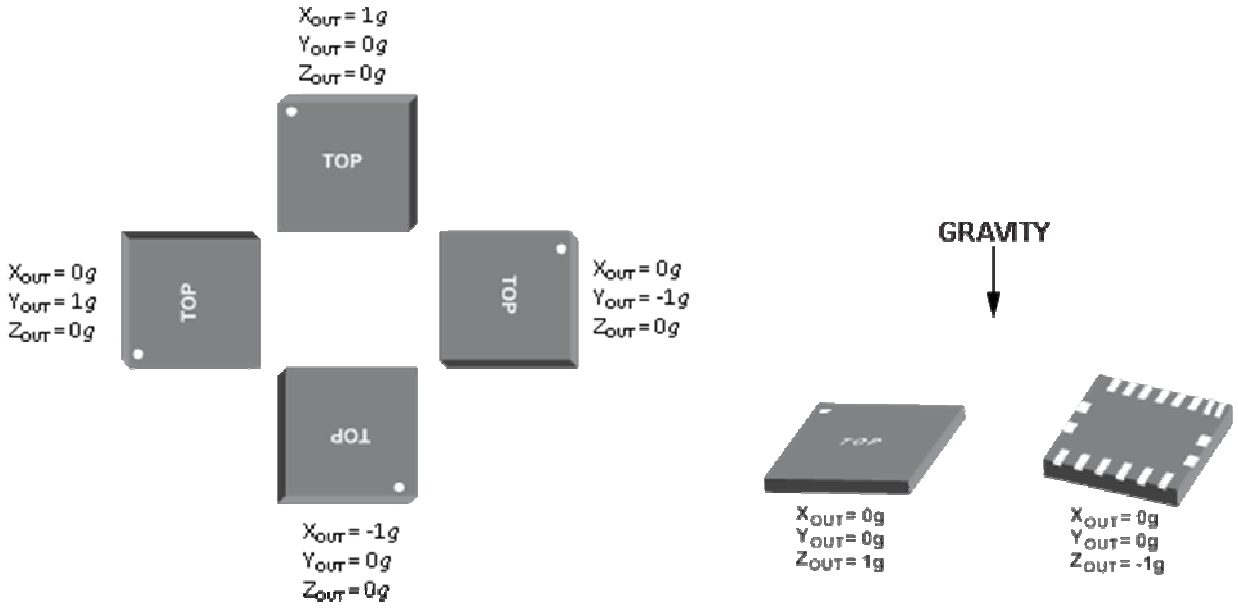

Figure 19. Output Response vs. Orientation to Gravity

LAYOUT AND DESIGN RECOMMENDATIONS

Figure 20 shows the recommended printed wiring board land pattern.

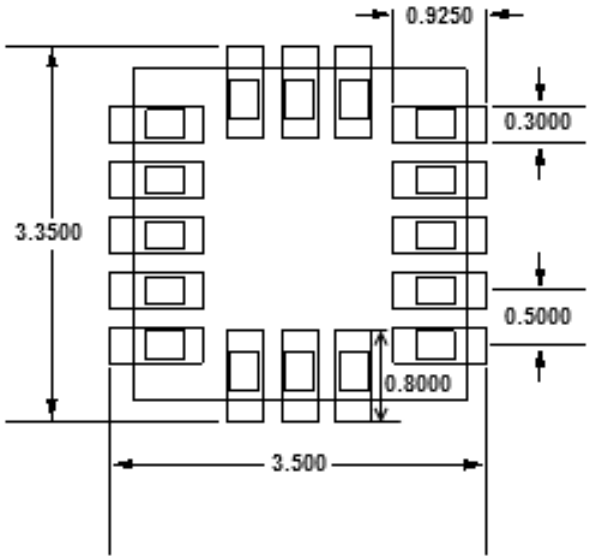

Figure 20. Recommended Printed Wiring Board Land Pattern
(Dimensions shown in millimeters)

RECOMMENDED SOLDERING PROFILE

Figure 21and Table 18 provide details about the recommended soldering profile.

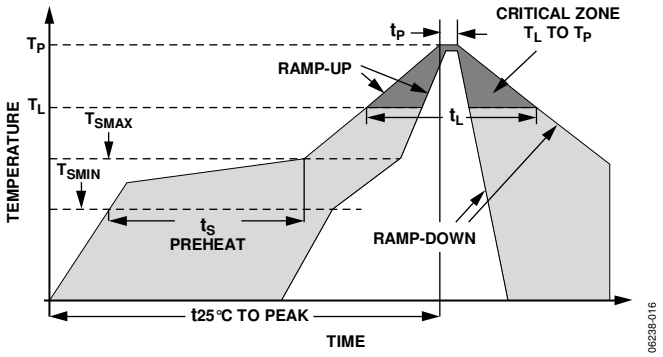

Figure 21. Recommended Soldering Profile

Table 18. Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX})(t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec max	3°C/sec max
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

OUTLINE DIMENSIONS

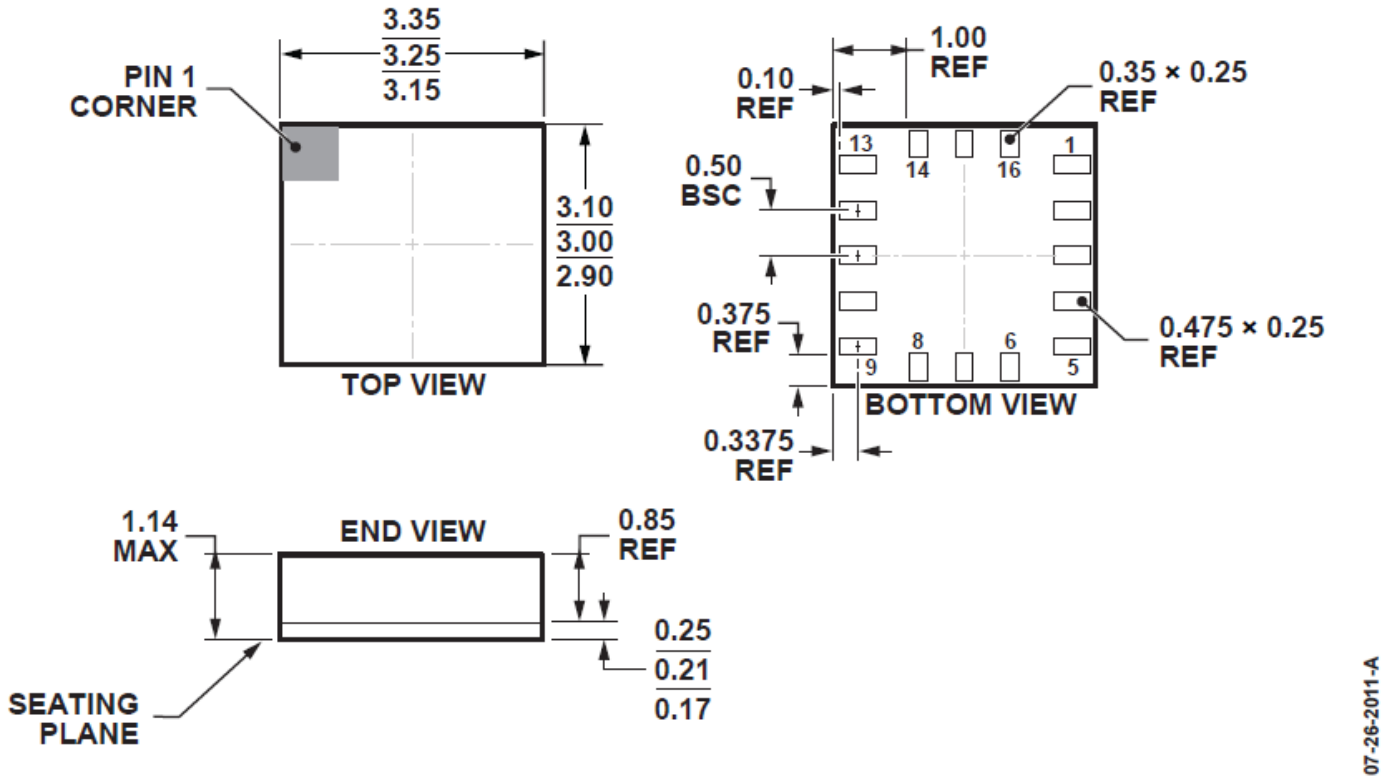

Figure 5. 16-Terminal Land Grid Array [LGA]
(CC-16-3)
Solder Terminations Finish Is Au over Ni
Dimensions shown in millimeters

ORDERING GUIDE

The ordering guide will be available when the ADXL362 releases to production. In the meantime, please visit www.analog.com/adxl362 to order samples.

NOTES

PR10776-0-5/12(PrB)