features

- **12-Bit, 21-MSPS, Analog-to-Digital Converter**
- **Very-Low Power: 70 mW Minimum Power-Down Mode: 4 mW**
- **Very-Low Input-Referred Noise: 75-dB SNR Typical at 0-dB Gain**
- **Novel Optical-Black (OB) Calibration**
- **Low-Aperture Delay**
- **Single 3-V Supply Operation**
- **DNL: <±0.5 LSB and INL: <±1.5 LSB Typical at 0-dB Gain**
- **Programmable-Gain Range: 0 dB to 36 dB, Gain Resolution of 0.05 dB/Step**
- **48-Pin TQFP Package**

applications

- **Digital Still Camera, Digital Video Camera**

description

The VSP1221 is a highly-integrated mixed-signal IC used for signal conditioning and analog-to-digital conversion at the output of a CCD array. The IC has a correlated double sampler (CDS) and an analog programmable-gain amplifier (PGA) stage followed by an analog-to-digital converter (ADC) and a digital PGA stage. The CDS is used to sample the CCD signal and is followed by the analog PGA stage. The ADC is a12-bit, 21-MSPS pipelined ADC. The digital PGA provides further amplification.

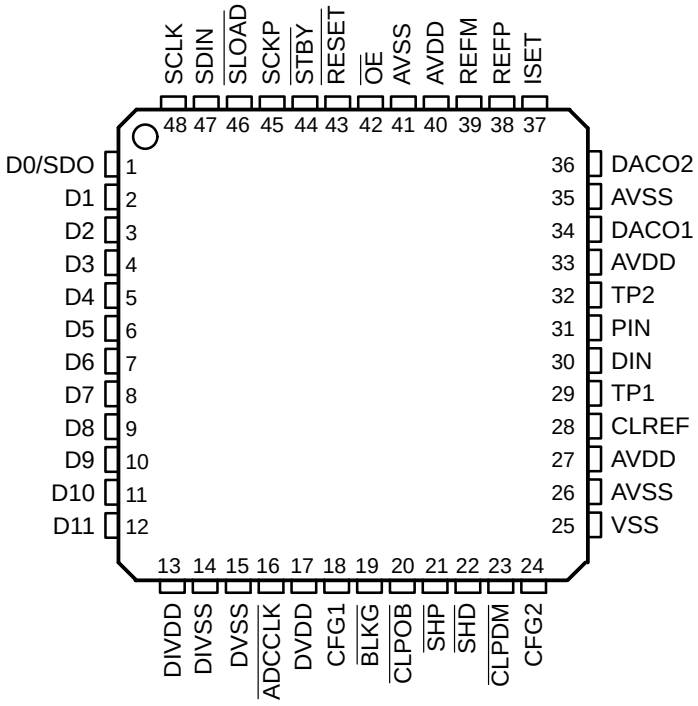
Additionally, there is an offset calibration loop for optical-black correction. The optical-black reference level is user-programmable. The chip also has two eight-bit digital-to-analog converters (DAC) for external analog setting.

The chip has a serial port for configuring internal control registers.

The VSP1221 is available in a 48-pin TQFP package and operates from a single 3-V power supply.

pin assignments

PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Terminal Functions

TERMINAL NAME	TERMINAL PIN	TYPE	DESCRIPTION
D0 SDO	1	DO	D0 = Bit 0 ADC output, least-significant bit (LSB) SDO = Serial data output (used for register read back)
D1	2	DO	Bit 1 ADC output
D2	3	DO	Bit 2 ADC output
D3	4	DO	Bit 3 ADC output
D4	5	DO	Bit 4 ADC output
D5	6	DO	Bit 5 ADC output
D6	7	DO	Bit 6 ADC output
D7	8	DO	Bit 7 ADC output
D8	9	DO	Bit 8 ADC output
D9	10	DO	Bit 9 ADC output
D10	11	DO	Bit 10 ADC output
D11	12	DO	Bit 11 ADC output, most-significant bit (MSB)
DIVDD	13	P	Power supply for digital I/O
DIVSS	14	P	Digital ground for digital I/O
DVSS	15	P	Digital ground
$\overline{\text{ADCCLK}}$	16	DI	ADC clock
DVDD	17	P	Digital power supply
CFG1	18	DI	Configuration pin1
$\overline{\text{BLKG}}$	19	DI	Blanking pulse: High = Normal operation Low = Digital output as programmed in the blanking register (see the *blanking register* section)
$\overline{\text{CLPOB}}$	20	DI	Optical-black clamping pulse (default = active low)
$\overline{\text{SHP}}$	21	DI	CDS reference sampling pulse (default = active low)
$\overline{\text{SHD}}$	22	DI	CDS data sampling pulse (default = active low)
$\overline{\text{CLPDM}}$	23	DI	Dummy clamping pulse (default = active low)
CFG2	24	DI	Configuration pin 2
VSS	25	P	Substrate ground
AVSS	26, 35, 41	P	Analog ground
AVDD	27, 33, 40	P	Analog power supply
CLREF	28	AO	External decoupling for clamp voltage
TP1	29	AIO	Test point
DIN	30	AI	CCD signal input
PIN	31	AI	Input ground
TP2	32	AIO	Test point
DAC01	34	AO	General-purpose eight-bit DAC output voltage
DAC02	36	A0	General-purpose eight-bit DAC output voltage
ISET	37	AO	Internal bias-current setting

NOTE: P: Power Supply, AI: Analog input, AO: Analog output, AIO: Analog input/output, DI: Digital input, DO: Digital output

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL PIN	TYPE	DESCRIPTION
REFP	38	AO	External decoupling for internal positive reference
REFM	39	AO	External decoupling for internal negative reference
$\overline{OE}$	42	DI	Output data enable: High = Normal operation Low = Digital output high-impedance state
$\overline{RESET}$	43	DI	Hardware reset (active low)
$\overline{STBY}$	44	DI	Hardware power down (active low)
SCKP	45	DI	SCKP – Serial clock polarity: High = Sample serial data on rising edge of serial clock (pin 48) Low = Sample serial data on falling edge of serial clock (pin 48)
$\overline{SLOAD}$	46	DI	Serial data latch
SDIN	47	DI	Serial data input
SCLK	48	DI	Serial clock input

NOTE: P: Power supply, AI: Analog input, AO: Analog output, AIO: Analog input/output, DI: Digital input, DO: Digital output

functional block diagram

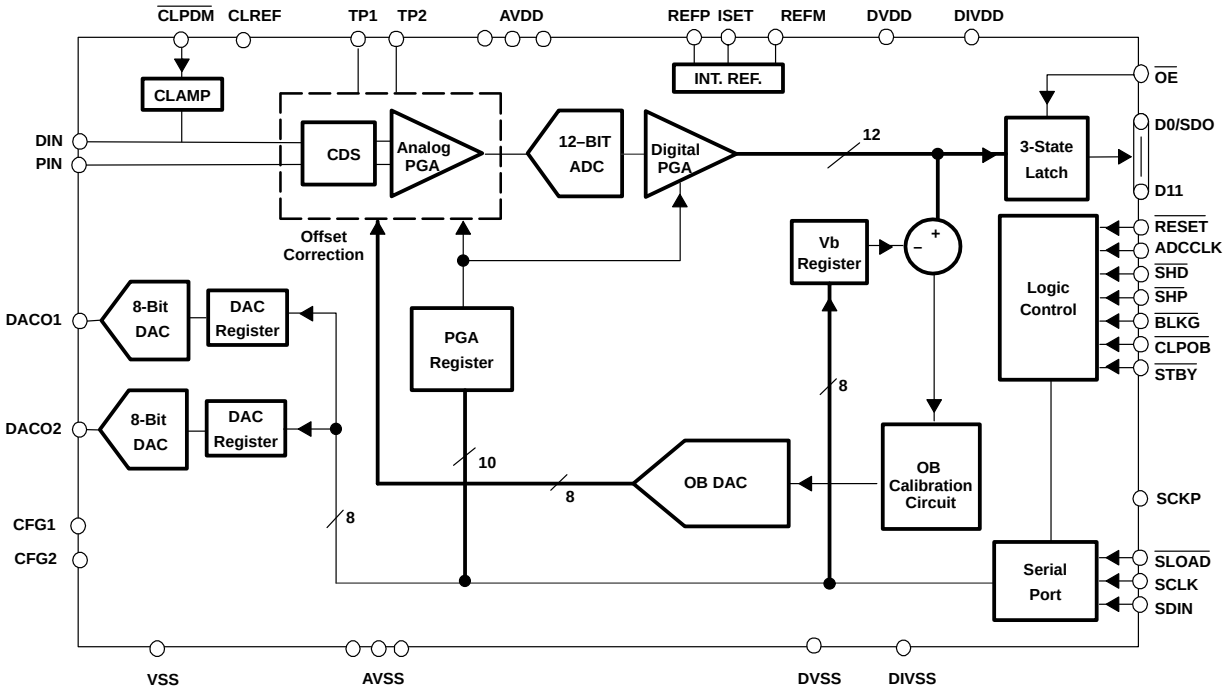


Figure 1. Internal Block Diagram of the VSP1221

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AV_{DD}, DV_{DD}, DIV_{DD} . . . . . –0.3 V to 6.5 V
Analog input voltage . . . . . –0.3 V to AVDD + 0.3 V
Digital input voltage . . . . . –0.3 V to DVDD + 0.3 V
Junction temperature, T_J . . . . . 0°C to 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature, (10 sec) . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics

general specifications

All typical specifications are at T_A = 25°C, all power supply voltages = 3 V, and conversion rate = 21 MHz, unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
AV_{DD}	Analog supply voltage		2.7	3.0	3.3	V
DV_{DD}	Digital supply voltage		2.7	3.0	3.3	V
DIV_{DD}	Digital I/O supply voltage		1.8		3.3	V
AV_{DD}	Operating current		20	24	29	mA
DV_{DD}	Operating current		2	4	6	mA
DIV_{DD}	Operating current		0.5	1	4	mA
	Power dissipation	Normal mode	80	90	100	mW
	Power dissipation	Power-down mode	1	2	4	mW
Reference						
	Positive reference voltage	1 µF to ground (pin 38)	1.95	2.05	2.2	V
	Negative reference voltage	1 µF to ground (pin 39)	0.7	0.75	0.9	V
	External bandgap voltage reference	100 kΩ to ground (pin 37)		1.00		V
	Bandgap temperature coefficient			100		PPM/°C
Temperature Range						
T_A	Operating temperature		–20		75	°C
Digital Input						
V_{IH}	Logic-high input voltage		0.8DIVDD			V
V_{IL}	Logic-low input voltage				0.2DIVDD	V
I_{IH}	Logic-high input current	DIV_{DD} = 3 V	–10		10	µA
I_{IL}	Logic-low input current	DIV_{DD} = 3 V	–10		10	µA
C_I	Input capacitance			5		pF
Digital Output						
V_{OH}	Logic-high output voltage	I_{OH} = 50 µA, DIV_{DD} = 3 V	0.8DIVDD			V
V_{OL}	Logic-low output voltage	I_{OL} = 50 µA, DIV_{DD} = 3 V			0.2DIVDD	V
I_{OZ}	High-impedance-state output current		–10		10	µA
C_O	Output capacitance	C_O		5	15	pF

electrical characteristics (continued)

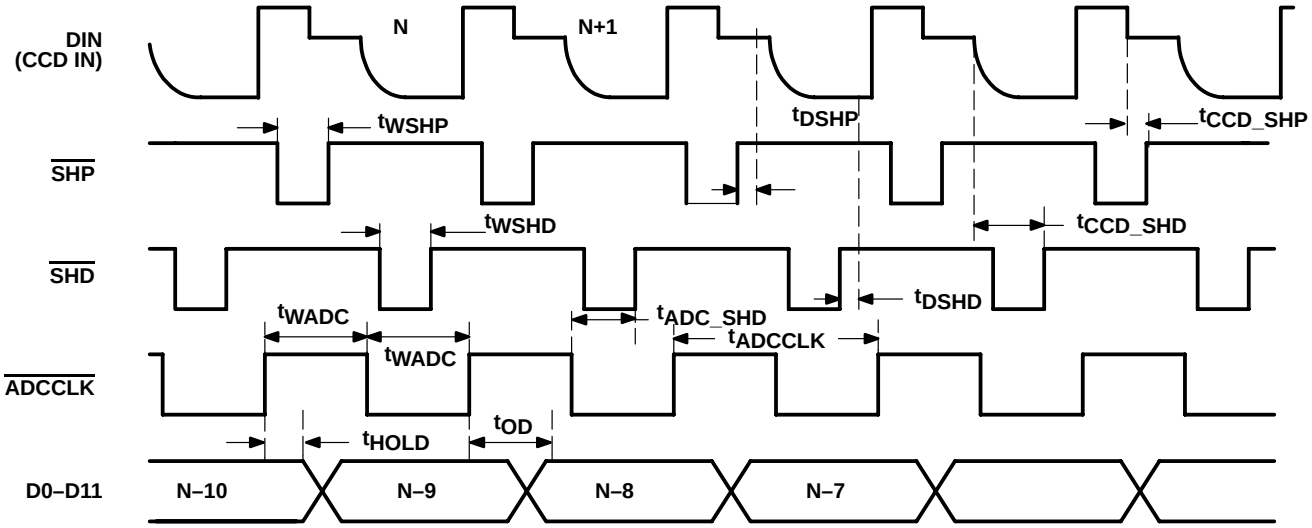
device specifications

All typical specifications are at T_A = 25°C, all power supply voltages = 3 V, and conversion rate = 21 MHz. unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Channel					
Input signal level for full-scale output	Single ended, gain= 0 dB		1000		mV
Input capacitance			8		pF
Input referred noise	Gain = 0 dB		130	360	μV
Integral nonlinearity	Gain = 0 dB	±1.5	±2	±5	LSB
Differential nonlinearity	Gain = 0 dB	±0.5	±0.75	+1.5/–1	LSB
Data latency			10		Clocks
Conversion rate				21	MHz
PGA					
Gain control code			10		Bits
Maximum gain	Gain code = 1011010000 (720 Decimal)		36		dB
Minimum gain	Gain code = 0000000000		0		dB
Gain resolution			0.05		dB
Integral nonlinearity		±0.02	±0.05	±0.4	dB
Differential nonlinearity		±0.02	±0.05	±0.3	dB
Analog-to-Digital Converter (ADC)					
Resolution			12		Bits
Conversion rate				21	MHz
No missing codes					
Integral nonlinearity			±1		LSB
Differential nonlinearity			±0.50		LSB
Data latency			3.5 (fixed)		Clocks
General-Purpose Digital-to-Analog Converter (DAC)					
Resolution			8		Bits
Integral nonlinearity			±0.1	±1	LSB
Differential nonlinearity			±0.1	±1	LSB
Output voltage range		0		AVDD	V
Output settling time	10-pF external load. Settle to 1 mV		4		μs
Serial Interface					
Clock frequency	DIV_{DD} = 3 V			40	MHz
Optical-Black Calibration					
Maximum correctable CCD black level				100	mV
Convergence time	Black level = 100 mV, gain = 12 dB, OB reference level = 0	440		550	Clocks
Calibration error	Gain = 0–20dB		±1	±2	LSB
	Gain = 20–26 dB		±1	±4	
	Gain = 26–32 dB		±2	±4	
	Gain = 32–36 dB		±4	±8	

timing requirements

sample and conversion timing



PARAMETERS		MIN	TYP	MAX	UNIT
t_{ADCCLK}	ADC clock period	46			ns
t_{WADC}	ADC high or low width	23			ns
t_{WSHP}	SHP pulse width	5			ns
t_{WSHD}	SHD pulse width	5			ns
t_{CCE_SHP}	CCD reset start to SHP rising edge	See Note 1			
t_{CCD_SHD}	CCD data start to SHD rising edge	See Note 2			
t_{ADC_SHD}	ADC falling edge to SHD rising edge	15		35	ns
t_{DSHP}	Sampling delay, reset	1.0	1.75	3.0	ns
t_{DSHD}	Sampling delay, data	4.0	5.0	7.0	ns
t_{HOLD}	Output hold time	4			ns
t_{OD}	Output delay	4		15	ns

NOTES: 1. Best performance if $t_{CCD\_SHP} > 15$ ns
Good performance if 10 ns < $t_{CCD\_SHP} < 15$ ns
Poor performance if $t_{CCD\_SHP} < 10$ ns
2. Best performance if $t_{CCD\_SHD} > 19$ ns
Good performance if 10 ns < $t_{CCD\_SHD} < 19$ ns
Poor performance if $t_{CCD\_SHD} < 15$ ns

Figure 2. Sample and Conversion Timing

serial interface timing

standard functionality, SCKP (pin 45) = high (sample data on rising edge of SCLK), operation = write

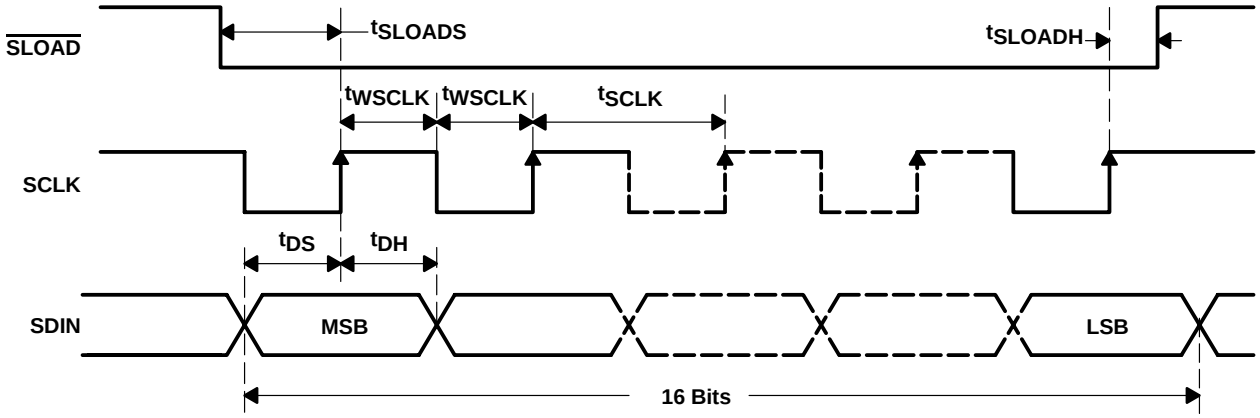
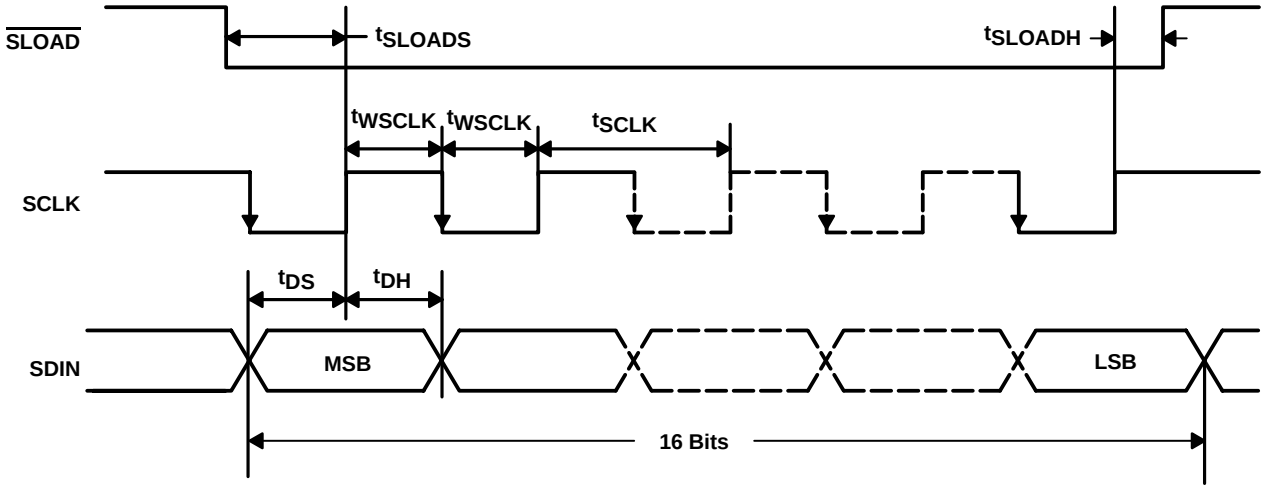


Figure 3. Serial Interface Timing for Write, SCKP = High

standard functionality, SCKP (pin 45) = low (sample data on falling edge of SCLK), operation = write



PARAMETERS		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	25			ns
t_{WSCLK}	SCLK high or low width	12.5			ns
t_{SLOADS}	$\overline{SLOAD}$ to SCLK setup time	5			ns
t_{SLOADH}	SCLK to $\overline{SLOAD}$ hold time	2			ns
t_{DS}	Data setup time	5			ns
t_{DH}	Data hold time	2			ns

NOTE: Serial data is in MSB first order.
For write operation, MSB = 0 (see the *serial data format* section)

Figure 4. Serial Interface Timing for Write, SCKP = Low

serial interface timing (continued)

standard functionality, SCKP (pin 45) = high, operation = read

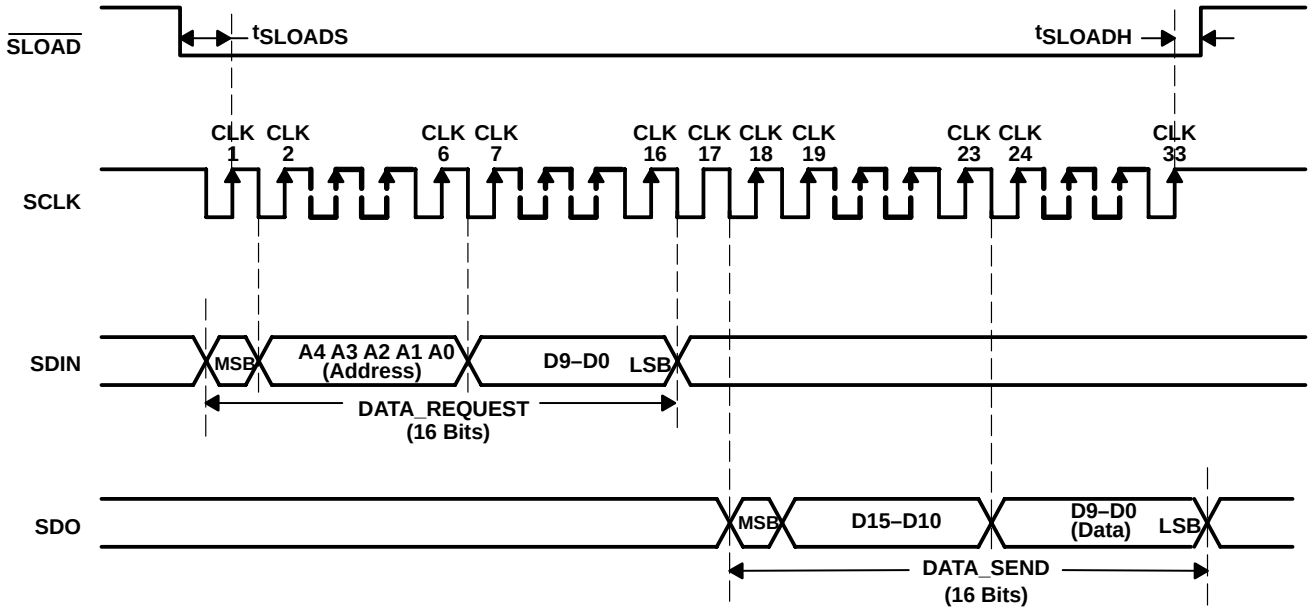


Figure 5. Serial Interface Timing for Read, SCKP = High

Device register values can be read back serially from the SDO pin (pin 1). For serial data read, user first sends a 16 bit DATA_REQUEST on the SDIN pin (pin 47). The format is as follows:

DATA_REQUEST on SDIN

SD15	SD14–SD10	SD9–SD0
1	Required register address	Don't Care

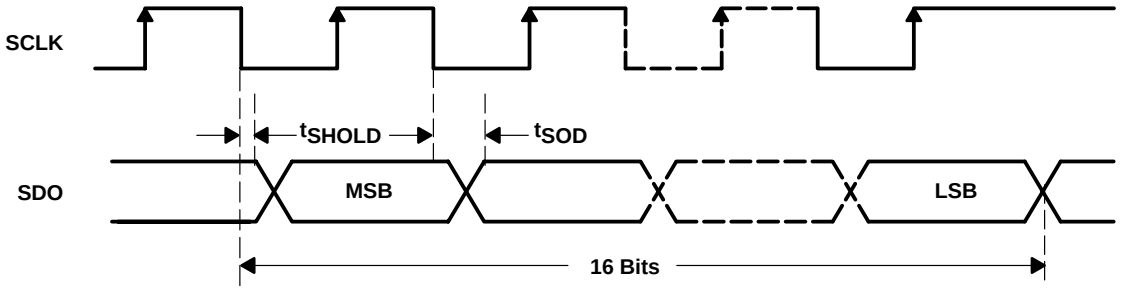
Although the length of DATA_REQUEST is 16 bits, the ten LSBs are don't cares. Also, note that SD15 (RD/$\overline{WR}$) should be 1 for register read (see the *serial data format* section). The register address portion of DATA_REQUEST is decoded and the register data value (DATA_SEND) is available on the SDO pin at the rising edge of CLK18 (see Figure 5) if $\overline{SLOAD}$ is low at that time. If $\overline{SLOAD}$ is high at that time, then DATA_SEND is available when $\overline{SLOAD}$ goes low again. The format of DATA_SEND is as follows:

DATA_SEND on SDO

SD15–SD10	SD9–SD0
Don't Care	Required register address

Although the length of DATA_SEND is 16 bits, the six MSBs are don't cares.

SDO timing



PARAMETERS		MIN	TYP	MAX	UNIT
t_{SHOLD}	Data output hold time	5			ns
t_{SOD}	Data output delay			13	ns

NOTE: Data output transition occurs at the falling edge of SCLK; so data should be sampled at the rising edge of SCLK. Since the SDO pin is multiplexed with the D0 pin, $\overline{OE}$ (pin 42) should be low.

Figure 6. Serial Interface Timing Between SCLK and SDO

standard functionality, SCKP (pin 45) = low, operation = read

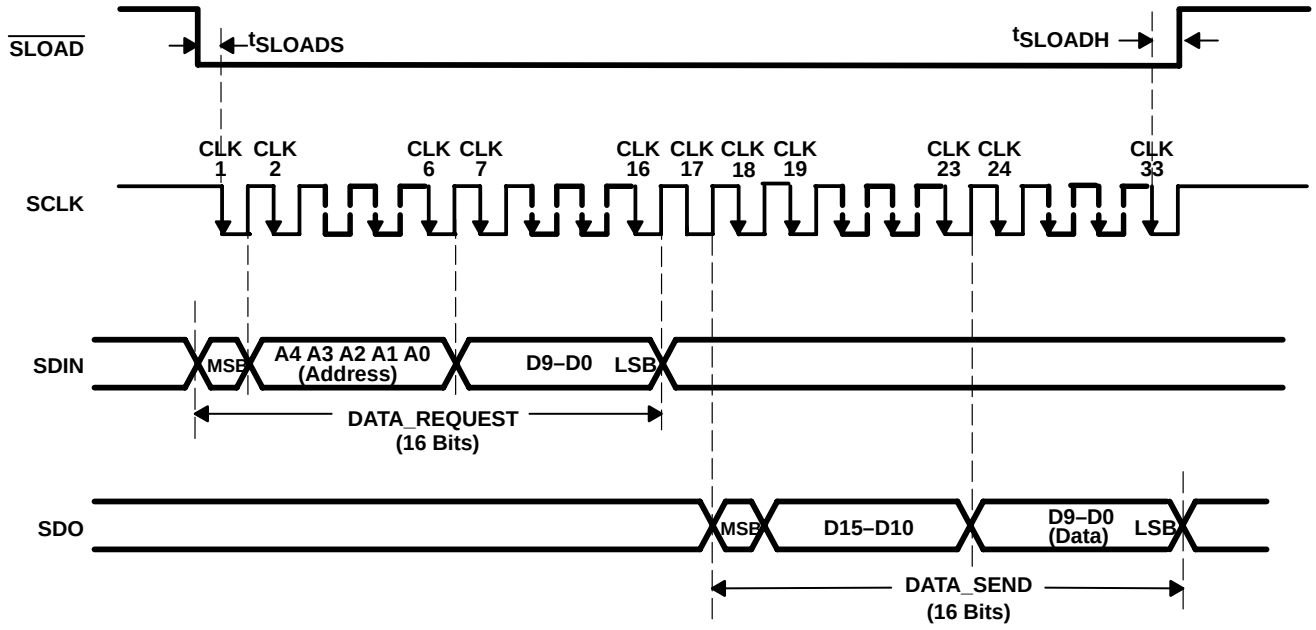


Figure 7. Serial Interface Timing for Read, SCKP = Low

The SDO timing is the same as before, except that data should be sampled at the falling edge of SCLK.

serial data format

standard functionality

The serial data is always grouped in 16-bit blocks with the following format. Multiple 16-bit blocks can be send through the SDIN pin (pin 47) keeping $\overline{\text{SLOAD}}$ (pin 46) low.

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{\text{WR}}$	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	←——Register Address——→					←——————Register Data——————→									

RD/$\overline{\text{WR}}$ = 0, Write into registers
RD/$\overline{\text{WR}}$ = 1, Read from registers

register description (see Note 3)

REGISTER ADDRESS					REGISTER NAME	REGISTER FUNCTION
A4	A3	A2	A1	A0		
0	0	0	0	0	Control register	Mode control
0	0	0	0	1	PGA register	Gain control
0	0	0	1	0	User DAC1 register	User DAC1 control
0	0	0	1	1	User DAC2 register	User DAC2 control
0	0	1	0	0	Reserved	Reserved
0	0	1	0	1	Reserved	Reserved
0	0	1	1	0	OB register	OB level control
0	0	1	1	1	Blanking register	Blanking output control
0	1	0	0	0	Signal polarity register	Clock signal polarity control
0	1	0	0	1	Timing register 1	$\overline{\text{ADCCLK}}$
0	1	0	1	0	Timing register 2	$\overline{\text{SHP}}$

NOTE 3: The register values are updated as soon as the register is written. It may take 0 to 9 ADCCLK cycles for it to have effect on the device.

control register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	0	0	0	STBYZ	CLAMPPIN	OB	RE-SERVED	RESERVED			RE-SERVED	RE-SERVED	RTSY
	← Address →					← Data →									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0	RTSY	0	RTSY=0, no change RTSY=1, reset all register bits to their default settings
SD1	RESERVED	0	Reserved
SD2	RESERVED	0	Reserved
SD3–SD5	RESERVED	All 0	Reserved
SD6	RESERVED	X	Reserved
SD7	OB	1	OB=0, optical-black calibration disable† OB=1, optical-black calibration enable
SD8	CLAMPPIN‡	1	CLAMPPIN=1, disable clamping on PIN (pin 31), connect PIN directly to ground. CLAMPPIN=0, enable clamping on PIN (pin 31), connect PIN to ground via capacitor.
SD9	STBYZ	1	STBYZ=0, device in power-down mode (software power down) STBYZ=1, no change

† Under this condition, previous value of black level remains unchanged.
‡ See the *CCD input* section

programmable-gain amplifier (PGA) register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	0	0	1	MSB				GAIN					LSB
	← Address →					← Data →									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–DS9	GAIN	All 0	Programmable-gain control Gain step = 0.05 dB Minimum gain = 0 dB Maximum gain = 36 dB

Code	Gain
0000000000	0 dB
0000000001	0.05 dB
.	
.	
.	
1011001111	35.95 dB
1011010000	36.00 dB
Higher codes	36.00 dB

user DAC1 register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	0	1	0	Reserved	PDZ1	MSB LSB	DACIN1						
	← Address →					← Data →									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–DS7	DACIN1	All 0	Eight-bit digital input to DAC1
SD8	PDZ1	0	PDZ1 = 0, DAC1 in power-down mode PDZ1 = 1, DAC1 in functional mode
SD9	Reserved	0	Reserved

user DAC2 register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	0	1	1	Reserved	PDZ2	MSB	DACIN2						LSB
	← Address →					← Data →									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–DS7	DACIN2	All 0	Eight-bit digital input to DAC2
SD8	PDZ2	0	PDZ1 = 0, DAC2 in power-down mode PDZ1 = 1, DAC2 in functional mode
SD9	Reserved	0	Reserved

OB register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	1	1	0	Reserved		MSB	OBLEVEL						LSB
	← Address →					← Data →									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–DS9	OBLEVEL	01000000J (64 LSBs)	OB reference level Code — OB Level 00000000 — 0 LSB 00000001 — 1 LSB . . 11111110 — 254 LSBs 11111111 — 255 LSBs
SD8–SD9	Reserved	All 0	Reserved

blanking register

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	0	1	1	1	MSB					BLKGVAL				LSB
	←Address→					←Data→									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–DS9	BLKGVAL	All 0	Output data when $\overline{BLKG}$ (pin 19) is low Code — Output data (blanking level) 0000000000 — 0 LSB 0000000001 — 1 LSB . . 1111111110 — 1022 LSBs 1111111111 — 1023 LSBs
SD8–SD9	Reserved	All 0	Reserved

signal polarity register (see Note 4)

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	1	0	0	0	Reserved					SPDZ	ADCZ	OBZ	BLZ	CLZ
	←Address→					←Data→									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0	CLZ	0	CLZ = 0, $\overline{CLPDM}$ (pin 23) = active low CLZ = 1, $\overline{CLPDM}$ (pin 23) = active high
SD1	BLZ	0	BLZ = 0, $\overline{BLKG}$ (pin 19) = active low BLZ = 1, $\overline{BLKG}$ (pin 19) = active high
SD2	OBZ	0	OBZ = 0, $\overline{CLPOB}$ (pin 20) = active low OBZ = 1, $\overline{CLPOB}$ (pin 20) = active high
SD3	ADCZ	0	ADCZ = 0, $\overline{ADCCLK}$ (pin 16) = active low ADCZ = 1, $\overline{ADCCLK}$ (pin 16) = active high
SD4	SPDZ	0	SPDZ = 0, $\overline{SHP}$ (pin 21) = active low, $\overline{SHD}$ (pin 22) = active low SPDZ = 1, $\overline{SHP}$ (pin 21) = active high, $\overline{SHD}$ (pin 22) = active high
SD5–SD9	Reserved	All 0	Reserved

NOTE 4: For this register to take effect, bit SD4 of timing register 1 must be 0.

timing register 1

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	1	0	0	1	Reserved					BYPZ	MSB	ADCDELAY		LSB
	←Address→					←Data→									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–SD3	ADCDELAY	All 0	Delay ADC clock by programmed value Delay step = 0.8 ns
			Code Delay
			0000 0 0001 0.8 ns . . 1110 11.2 ns 1111 12.0 ns
SD4	BYPZ	1	BYPZ = 0, signal polarity and programmable delay enable (see Note 5) BYPZ = 1, signal polarity and programmable delay disable
SD5–SD9	Reserved	All 0	Reserved

NOTE 5: When BYPZ = 0, the internal delays of SHP and SHD will increase approximately by 3 ns

timing register 2 (see Note 6)

SD15 MSB	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0 LSB
RD/$\overline{WR}$	0	1	0	1	0	Reserved		MSB	SHDDELAY		LSB	MSB	SHPDELAY		LSB
	←Address→					←Data→									

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD0–SD3	SHPDELAY	All 0	Delay SHP clock by programmed value Delay step = 0.8 ns
			Code Delay
			0000 0 0001 0.8 ns . 1110 11.2 ns 1111 12.0 ns
SD4–SD7	SHDDELAY	All 0	Delay SHD clock by programmed value Delay step = 0.8 ns
			Code Delay
			0000 0 0001 0.8 ns . 1110 11.2 ns 1111 12.0 ns
SD8–SD9	Reserved	All 0	Reserved

NOTE 6: For this register to take effect, bit SD4 of timing register 1 must be 0 (see the *timing register 1* section.

PRINCIPLES OF OPERATION

introduction

The principle functions of the VSP1221 are described below. The sections discussed are:

- CDS
- ADC
- PGA
- Voltage and current reference
- Serial interface
- Timing
  - $\overline{\text{SHP}}$, $\overline{\text{SHD}}$ AND $\overline{\text{ADCCLK}}$
  - $\overline{\text{CLPDM}}$
  - $\overline{\text{BLKG}}$
  - $\overline{\text{CLPOB}}$
  - $\overline{\text{OE}}$
  - $\overline{\text{RESET}}$
- Optical-black calibration
- Standby mode
- General-purpose DAC

Before describing the individual blocks, a simplified block diagram of the VSP1221 is presented in Figure 8.

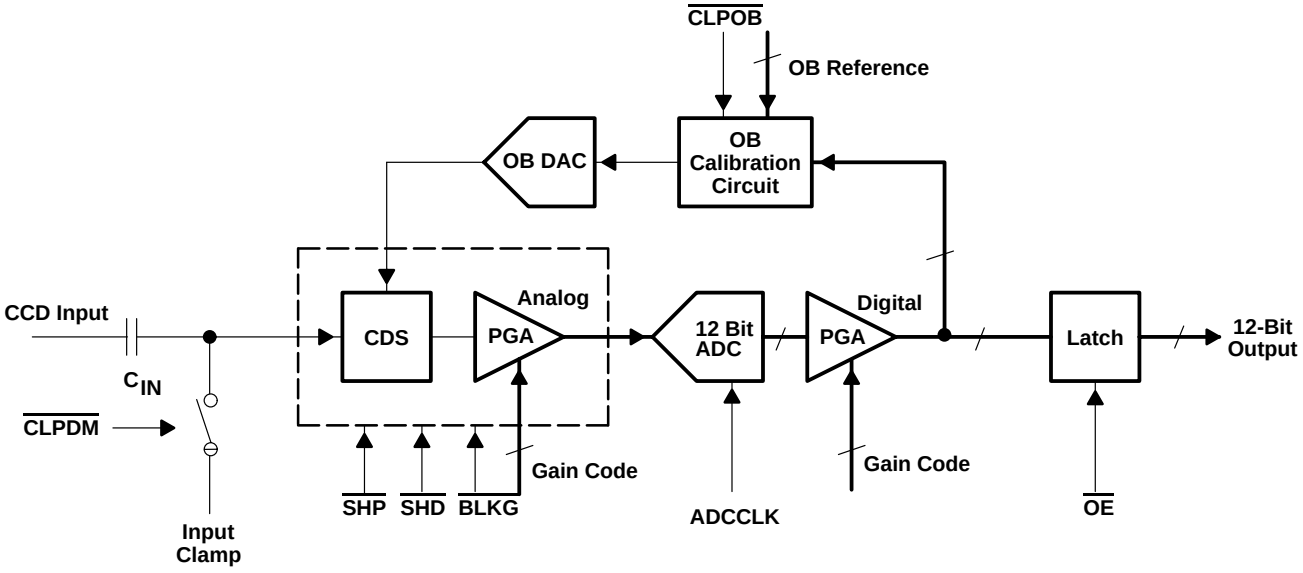


Figure 8. Simplified Block Diagram of the VSP1221

PRINCIPLES OF OPERATION

CDS

The output signal from the CCD is fed to the correlated double sampler (CDS) through off-chip coupling capacitor C_{in} (a 0.22-µF capacitor is recommended for C_{in}). The CCD signal is sampled twice during one pixel period: at the reference level ($\overline{SHP}$) and at the data level ($\overline{SHD}$). Subtracting these two samples extracts the pixel value and reduces the reset noise and other low-frequency noises that are present at the output of the CCD signal.

ADC

The output analog signal from the analog PGA stage is passed to the 12-bit analog-to-digital converter (ADC). The ADC employs a three-stage pipelined architecture to achieve high-throughput and low-power consumption. Fully-differential implementation and digital-error correction ensures 12-bit resolution.

PGA

VSP1221 has a programmable gain amplifier (PGA) which is composed of analog and digital stages. The total gain range is 0 dB–36 dB in 0.05-dB steps. The gain can be adjusted by programming the PGA register through the serial port, see the *programmable gain amplifier (PGA) register* section.

voltage reference

All the reference voltages and the bias currents used by the device are created by an internal bandgap circuit. Connecting an external 100-kΩ resistor from ISET (pin 37) to ground provides the bias current. The voltage at the ISET pin is 1 V and the reference current is 10 µA (1 V/100 kΩ). The reference voltages for the ADC are REFP (2.05 V) and REFM (0.75 V). They are available on pins 38 and 39, respectively. The full-scale range of the ADC is twice the difference between REFP and REFM. Pins REFP and REFM should be heavily decoupled with appropriate capacitors (1 µF recommended).

serial interface

standard functionality

A simple three-wire (SCLK, SDIN, and $\overline{SLOAD}$) serial interface is provided to allow writing/reading the internal registers of the VSP1221. The serial data SDIN (pin 47) is 16 bits long. The MSB (most significant bit) is set to 0 for writing to and to 1 for reading from the internal registers. Following this, there are five address bits for accessing and ten data bits for writing to the particular registers. During a read operation, data from the particular register is available on SDO (pin 1). To enable serial read/write, $\overline{SLOAD}$ (pin 46) should be pulled low. Sending blocks of 16-bit data to SDIN can program multiple registers. The polarity of the serial clock (SCLK, pin 48) can be controlled by SCKP (pin 45). For serial interface timing see the *serial data format* section; for serial data format and description of the internal registers see the *register description* section.

timing

A description of the different timing signals of the VSP1221 follows. The timing diagram in *sample and conversion timing* section has additional information. Note that the polarity of $\overline{SHP}$/$\overline{SHD}$, $\overline{ADCCLK}$, $\overline{CLPDM}$, $\overline{BLKG}$, and $\overline{CLPOB}$ can be programmed to be active low or active high (see the *signal polarity register* section). The timing diagram in the *timing specifications* section is based on active-low polarity.

PRINCIPLES OF OPERATION

SHP, SHD, and ADCCLK

SHP/SHD are used for correlated double sampling of the CCD signal. Sample reference (SHP) is used to sample the reference level of the CCD signal, and sample data (SHD) is used to sample the data level. The ADC clock (ADCCLK) is used to latch the output of the ADC to the external pins. SHP, SHD, and ADCCLK are used to generate internal timing signals using the on-chip timing generator for proper synchronization of different blocks. SHP, SHD, and ADCCLK can be internally delayed by programming the timing registers through the serial port (see the *timing register 1* and *timing register 2* sections.

The following is recommended to get the best performance:

SHP and SHD must first be aligned based on the CCD signal and timing shown in Figure 2 (t_{DSHP} and t_{DSHD}). It is observed that if output data switches at the instant of sampling (t_{DSHP}), the device noise performance degrades. The data switches a few ns after the rising edge of ADCCLK (t_{OD}). To improve performance, ADCCLK can be varied within the t_{ADC_SHD} range.

CLPDM

The CCD signal is capacitively coupled to the VSP1221 because the dc level of the CCD signal is usually too high and might damage the chip. The purpose of the CLPDM signal is to clamp the ac-coupling capacitor C_{in} to establish the proper dc bias for the CDS. The dc bias for the CDS is set to the clamp voltage, which is around 800 mV below the supply voltage. The clamp voltage can be decoupled with an external capacitor at CLREF (pin 28). This helps in charging the ac-coupling capacitor C_{in} faster, since the charge will be provided by the decoupling capacitor. Recommended value for the decoupling capacitor is 1 µF. The dummy pixel clamp (CLPDM) signal is usually available during the dummy pixels of the CCD and is applied at the line rate of the CCD sensor.

BLK

Some CCDs have large transient output signals during blanking intervals. Such signals might drive the VSP1221 into saturation and can cause long recovery times. To prevent this, the VSP1221 has an input-blanking function which disconnects the CCD input from the CDS when it receives the blanking (BLKG) signal. Additionally, the output from the VSP1221 during blanking will be equal to the value programmed in the blanking register. The blanking level can be adjusted by programming the blanking register through the serial port (see the *blanking register* section).

CLPOB

The optical-black clamp (CLPOB) pulse is used for optical-black calibration (explained in the *optical-black calibration* section). The CLPOB pulse is given to the device during optical-black pixels of the CCD.

OE

Output enable (OE) is used to latch the output data to the output pins. When OE is low, data is latched to the output pins (D0–D11); when it is high, the output is 3-state.

RESET

When the reset (RESET) signal is pulled low (hardware reset), all the internal registers are reset to their default values. In addition, The device also has a software-reset option that allows setting the RTSY bit in the control register through the serial port (see the *control register* section). See the *control register* section for the default values of the internal registers. In addition to resetting the registers, hardware reset also resets the output of the OB DAC to zero. However, to exactly reset the OB DAC to zero, RESET must be kept low for approximately 600 ns.

PRINCIPLES OF OPERATION

optical-black calibration

Optical-black calibration (OB) is used to clamp the CCD *black* level to the user-defined OB reference level. In CCDs, thermally generated electrons produce a significant amount of charge even at room temperature. So, even in the absence of light (*black* level), thermal electrons generate a considerable amount of current in CCDs. Thus, the CCD black level will carry a residual signal, also known as the CCD offset, which is typically of the order of 50 mV. This residual signal will reduce the effective dynamic range of the CCD input, resulting in a degradation of image quality. An offset voltage must be subtracted from the CCD black level so that the difference between the CCD black level and the offset voltage is equal to the reference OB level programmed by the user. The reference OB level is much lower than the CCD black level, so that the effective dynamic range of the CCD input increases and the image quality improves. The offset voltage has to be determined based on the CCD black level. There are certain CCD pixels which are not exposed to light (optical-black pixels) and the CCD signal corresponding to these pixels represent the CCD black level. Thus, the offset voltage is determined during the optical-black pixels, and the offset voltage is kept constant and is subtracted from the CCD input to cancel the CCD offset during normal image pixels.

OB calibration in the VSP1221 is done in a closed feedback loop. The difference between the CCD black level and the offset voltage is compared with the user-defined OB reference level at the output of the digital PGA stage. The error is fed to an OB calibration circuit which generates a step proportional to the error and a sign based on the sign of the error. The step and the sign are then given to the OB DAC, which generates an analog voltage that updates the offset voltage at the input of the CDS. If the error is positive, the offset voltage is increased; if the error is negative, the offset voltage is decreased. This continues in a closed feedback loop until the difference between the CCD black level and the offset voltage converges to the OB reference level. The OB calibration circuit has been designed so that a 100-mV CCD black level converges to *zero* reference OB level within 500–750 pixel clocks. Convergence time increases with an increase in gain. Convergence is faster if the CCD black level is smaller than 100 mV. A plot of the convergence time as a function of the PGA gain is shown in the *performance plots* section. Since the feedback loop includes the CDS, the PGA, and the ADC, it also cancels any offset introduced by these blocks. The OB reference level can be adjusted by programming the OB register through the serial port (see the *OB register* section)

standby mode (power-down mode)

To save power, the VSP1221 can be put into standby mode (power-down mode) both through hardware and software. Pulling the $\overline{\text{STBY}}$ signal low puts the device into standby mode (hardware power-down). In this mode, the reference is pulled down, all the functional blocks are disabled, the output is *all zero,* and the power dissipation is zero. The power-up time is of the order of 10 ms. Software power down can be exercised by resetting the STBYZ bit in the control register through the serial port (see the *control register* section). This is similar to hardware power down, except that the reference is not pulled down. Hence, the power dissipation is around 4 mW and the power-up time is of the order of 10 μs. The user can still program all the internal registers during both hardware and software power down.

general purpose DAC

The VSP1221 has two eight-bit general-purpose digital-to-analog converters (DACs) that can be used for external analog settings. The output voltage of each DAC can be independently set and has a range of 0 V to the supply voltage with eight-bit resolution. The digital input to the DACs can be set by programming the user DAC1 and User DAC2 registers through the serial port (see the *user DAC1 register* and *user DAC2 register* sections). When not used in the system, the DACs can be put in standby mode by programming the above-mentioned registers. The DACs are, by default, in standby mode. The average power consumed by each DAC is approximately 1 mW.

APPLICATION INFORMATION

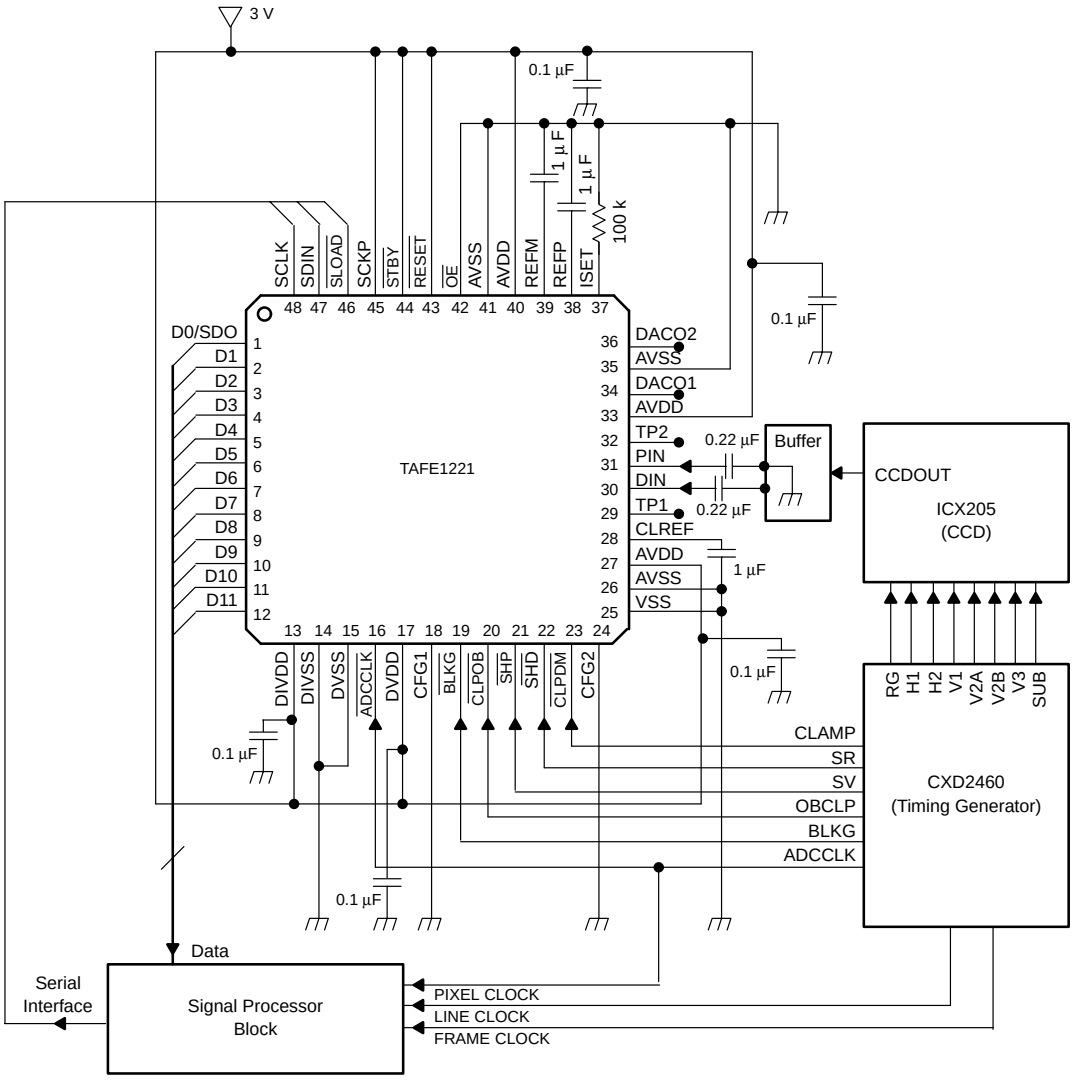


Figure 9. Application Diagram of the VSP1221

NOTE:

The application circuits shown are typical examples of the operation of the devices. Texas Instruments cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third-party patents and other rights due to the same.

APPLICATION INFORMATION

CCD input

The CCD output may need an off-chip external buffer in order to drive the input capacitive load of the VSP1221. The buffer output is applied to DIN (pin 30) through an ac-coupling capacitor. It is advisable to connect PIN (pin 31) to the buffer ground through a similar ac-coupling capacitor for the following reason: since the input stage of the VSP1221 is differential, the input to the CDS is the voltage difference between DIN and PIN. Hence, if the noise path for DIN and PIN are similar, the noise can be effectively cancelled. This is not the case if the noise paths are different. However, PIN can also be connected directly to ground. In this case, bit SD8 (CLAMPPIN) of the control register should be 1 (see the *control register* section). If PIN is connected to an ac-coupling capacitor, it is recommended to set bit SD8 (CLAMPPIN) of the control register to 0 so that the ac-coupling capacitor is charged to a fixed clamp voltage. The recommended value for the ac coupling capacitor is 0.22 μF.

reference decoupling

Pins REFP (pin 38) and REFM (pin 39) should be connected to ground by means of decoupling capacitors. A 1-μF ceramic capacitor is recommended for reference decoupling. For better high-frequency decoupling, 0.1 μF ceramic capacitors may be used in parallel. The decoupling capacitors should be placed as close as possible to the reference pins.

clamp decoupling

To decouple the clamp voltage, a 1-μF ceramic capacitor may be connected to CLREF (pin 28). See the $\overline{CLPDM}$ section for further details.

internal bias current setting

To set the internal bias current, ISET (pin 37) should be connected to ground through a 100-kΩ resistor. *However, no capacitor should be connected to the ISET pin.*

power supply, grounding, and device decoupling

The VSP1221 has several power-supply pins. Each major internal analog block has a dedicated AVDD supply pin (pins 27, 33, and 40). The DVDD supply pin (pin 17) powers all internal digital circuitry. Both AVDD and DVDD work with 3-V power supplies. DIVDD and DIGND (pins 13 and 14) supply power to the output digital driver (D0–D11). DIVDD is independent of DVDD and can be operated from 1.8 V to 3.3 V. This allows the outputs to interface with digital ASICs requiring different supply voltages

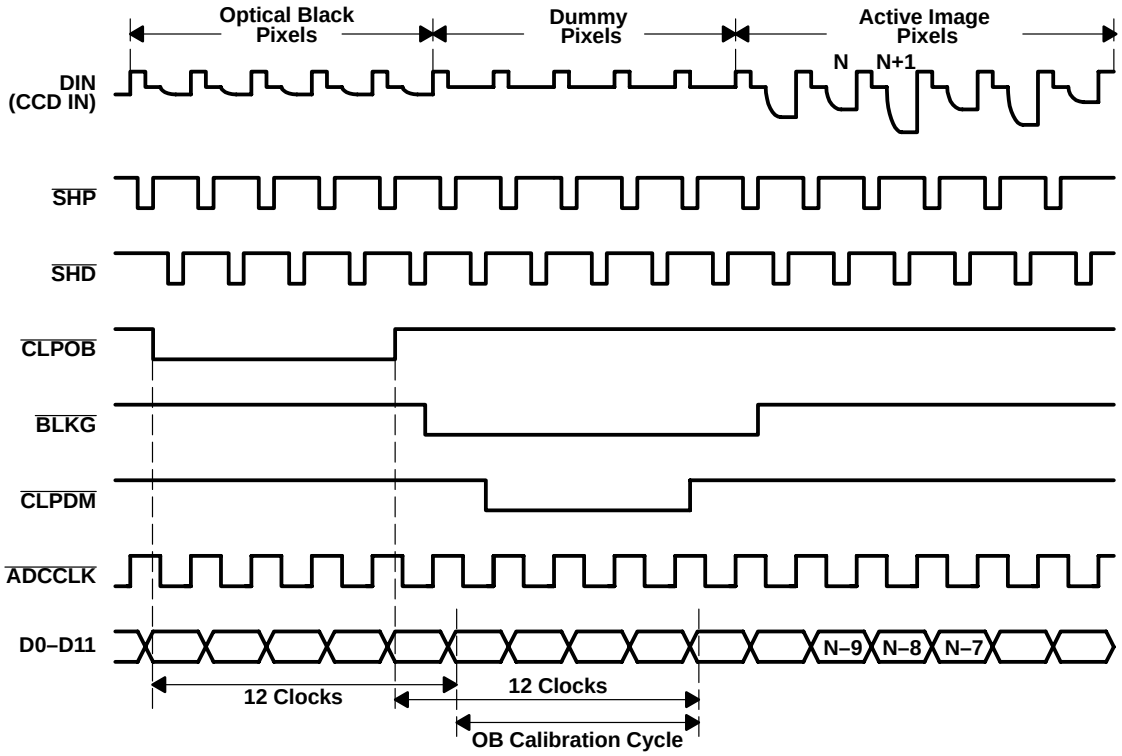
General design practices should apply to the PCB to limit high-frequency transients and noise that are fed back into the supply lines. This requires adequate bypassing of the supply pins. In the case of power supply decoupling, 0.1-μF ceramic capacitors are sufficient to keep the impedance low over a wide frequency range. Since their effectiveness depends largely on the proximity to the individual supply pin, all decoupling capacitors should be placed as close as possible to the supply pins.

To reduce high-frequency and noise coupling, it is highly recommended to short the digital and analog grounds immediately outside the package. This can be accomplished by running a low-impedance line under the package between pins DVSS and AVSS.

APPLICATION INFORMATION

data output

It is recommended to keep the capacitive loading on the output data lines as low as possible (typically less than 15 pF). Larger capacitive loads demand higher charging-current surges which can feed back into the analog portion of the VSP1221 and affect its performance. If the data lines are long, it is advisable to use external buffers or latches, which will also provide the added benefit of isolating the VSP1221 from any digital noise that may couple back. In addition, resistors in series with each data line will help in minimizing the surge current. Typical resistor values are 40–50 Ω.



NOTES: A. OB Calibration latency is 12 clocks. So, OB update starts 12 clocks after $\overline{\text{CLPOB}}$ is pulled low and stops 12 clocks after $\overline{\text{CLPOB}}$ is pulled high.
B. If active image pixels are located immediately after $\overline{\text{CLPOB}}$ goes high, the OB update will affect the adjacent 12 pixels.
C. The device clocks are stopped during $\overline{\text{BLKG}}$ and $\overline{\text{CLPDM}}$. Therefore, if these signals appear immediately after $\overline{\text{CLPOB}}$ goes high, the OB calibration update for the subsequent 12 clocks will stop. So, its recommended to delay $\overline{\text{BLKG}}$ and $\overline{\text{CLPDM}}$ by at least 12 pixels after $\overline{\text{CLPOB}}$ goes high.

Figure 10. System Timing Diagram Example

APPLICATION INFORMATION

performance plots

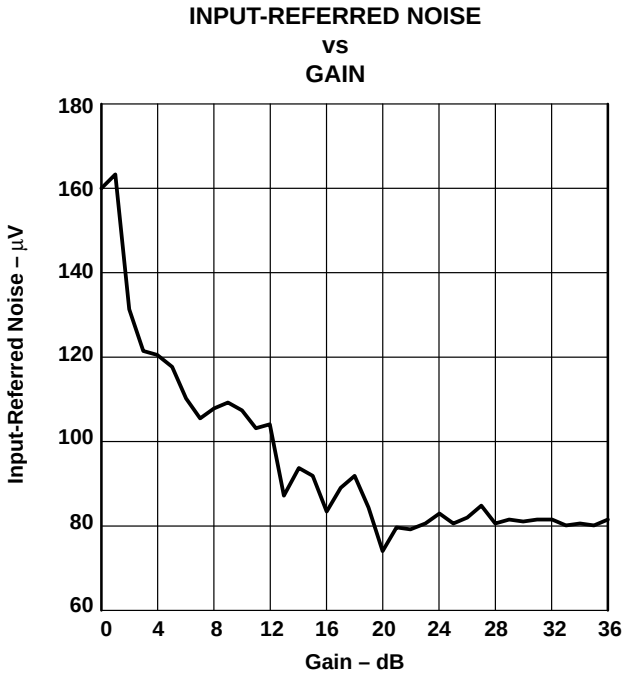


Figure 11

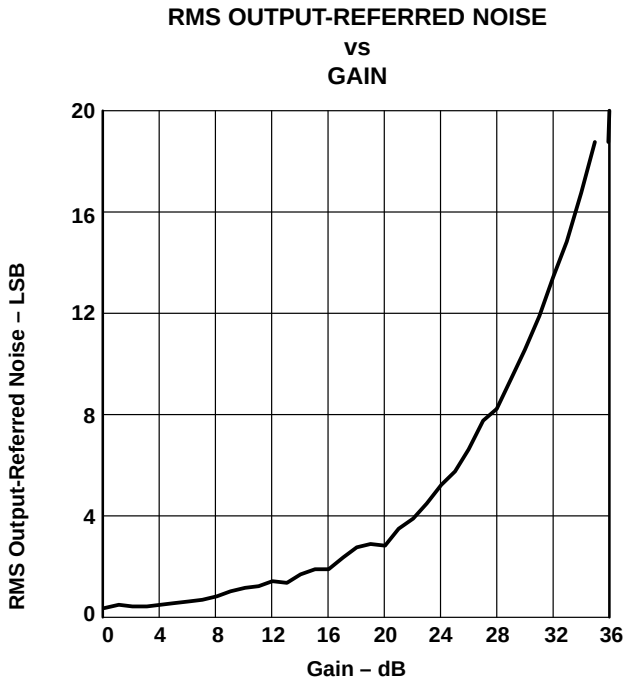


Figure 12

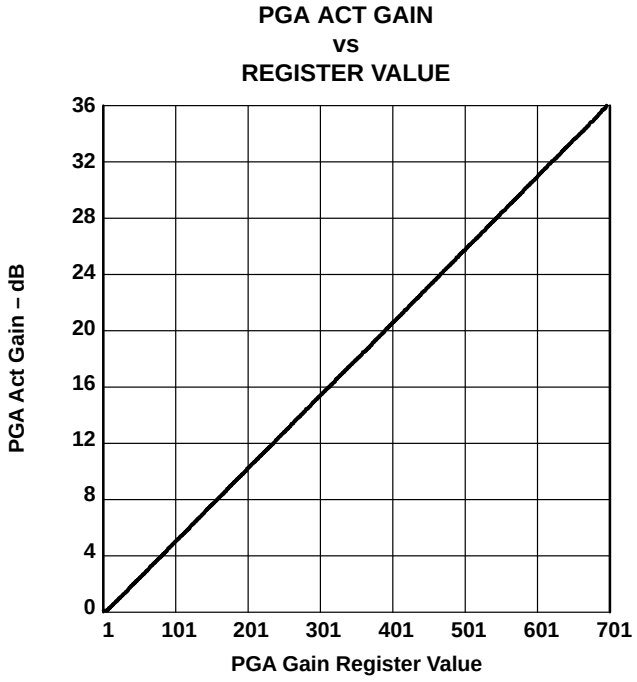


Figure 13

APPLICATION INFORMATION

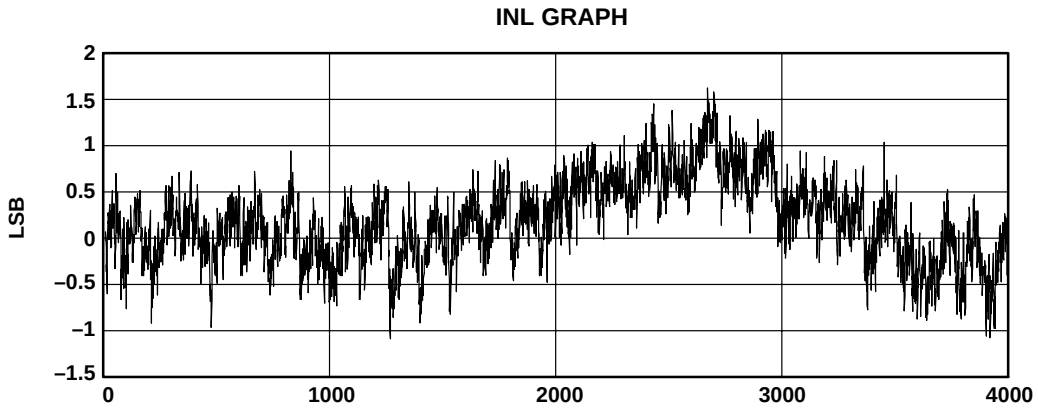


Figure 14

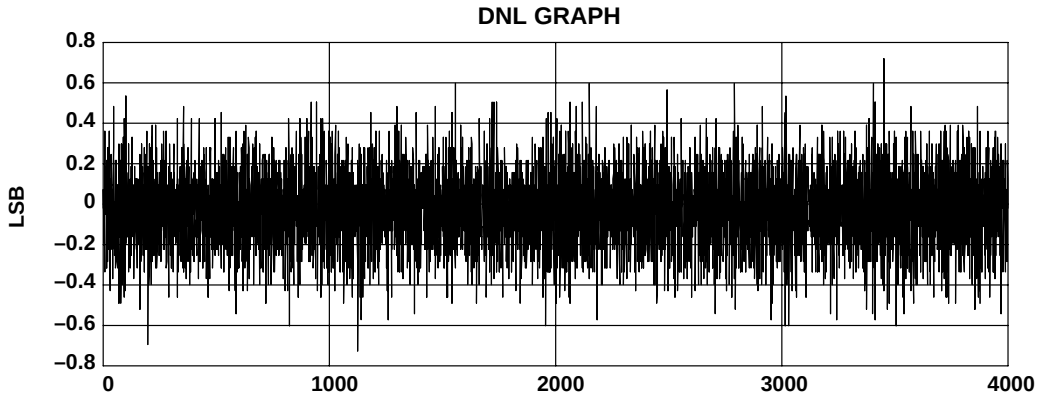


Figure 15

APPLICATION INFORMATION

POWER CONSUMPTION vs FREQUENCY

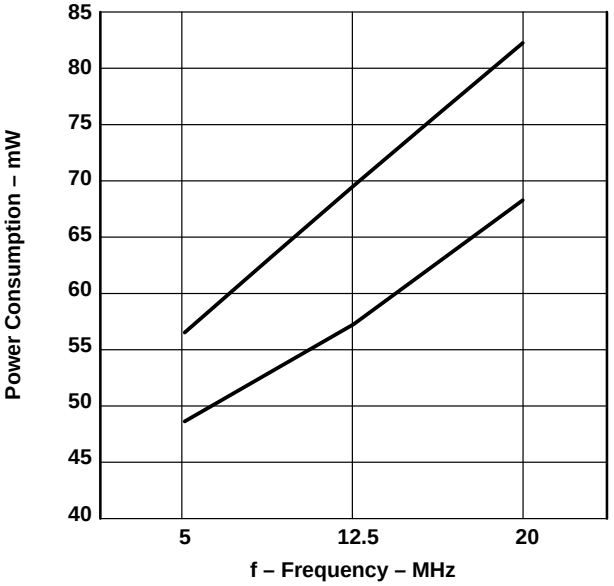


Figure 16

OPTICAL-BLACK-VALUE CONVERGENCE vs NUMBER OF ADCCLKs

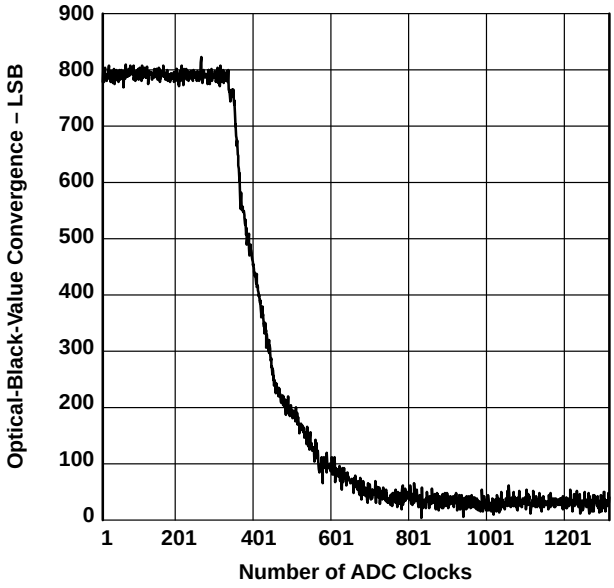
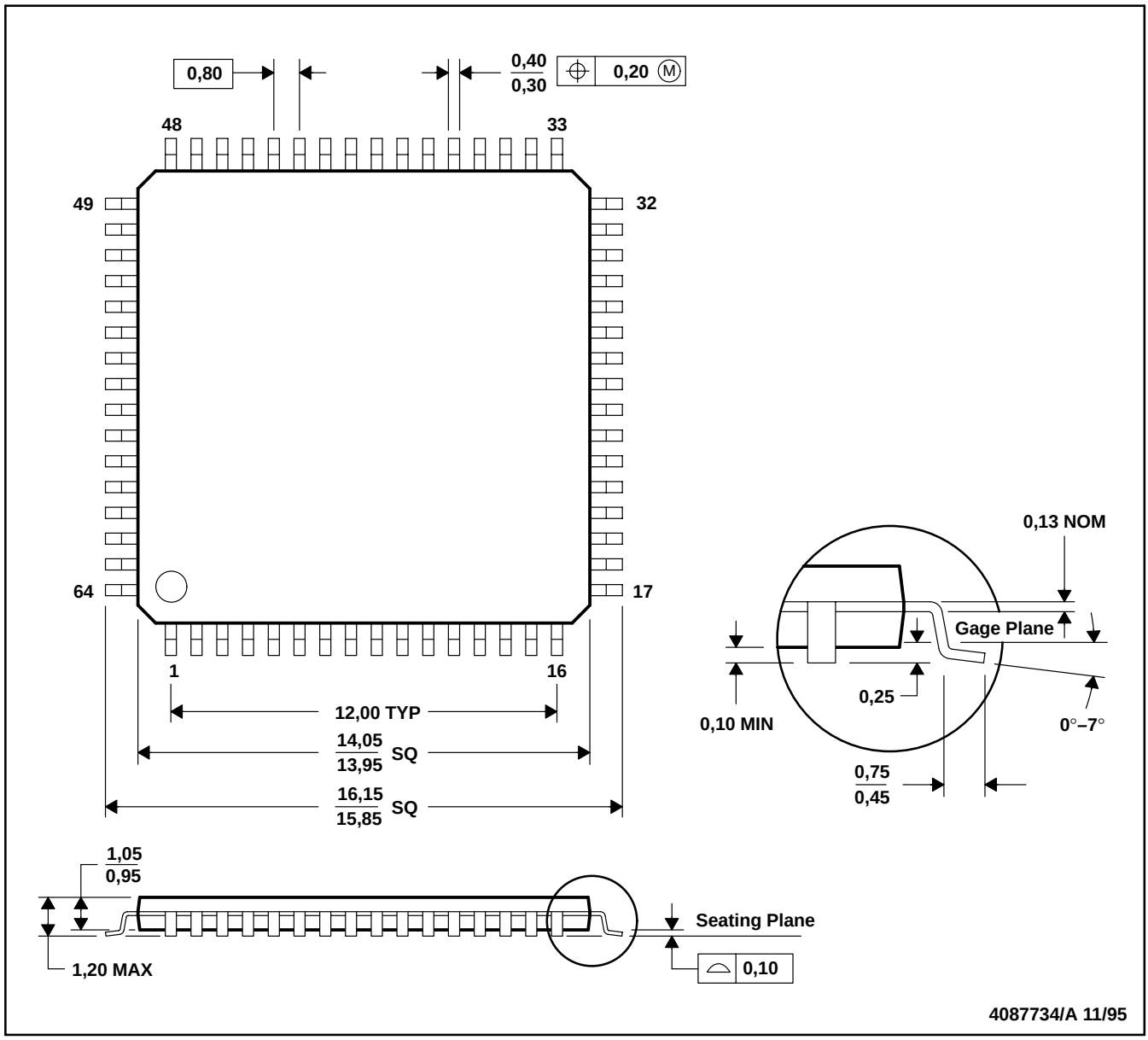


Figure 17

MECHANICAL DATA

PBR (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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