



Internal Memory (RAM and ROM)

User Guide



101 Innovation Drive
San Jose, CA 95134
www.altera.com

UG-01068-4.3



© 2013 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



This user guide describes the megafunctions that implement the following memory modes:

- RAM:1-Port—Single-port RAM
- RAM:2-Port—Dual-port RAM
- ROM:1-Port—Single-port ROM
- ROM:2-Port—Dual-port ROM

Altera provides two megafunctions to implement the memory modes—the ALTSYNCRAM and ALTDPRAM megafunctions. The Quartus® II software automatically selects one of these megafunctions to implement the memory modes. The selection depends on the target device, memory modes, and features of the RAM and ROM.



This user guide assumes that you are familiar with megafunctions and how to create them. If you are unfamiliar with Altera® megafunctions or the MegaWizard™ Plug-In Manager, refer to the *Introduction to Megafunctions User Guide*.

Features

The internal memory blocks provide the following features:

- Memory Modes Configuration
- Memory Block Types
- Write and Read Operations Triggering
- Port Width Configuration
- Mixed-width Port Configuration
- Maximum Block Depth Configuration
- Clocking Modes and Clock Enable
- Address Clock Enable
- Byte Enable
- Asynchronous Clear
- Read Enable
- Read-During-Write
- Power-Up Conditions and Memory Initialization
- Error Correction Code

Device Support

Altera internal memory blocks are available for Arria®, Cyclone®, HardCopy®, MAX®, and Stratix® device series. However, ROM memory blocks are not available for MAX device series.

This section describes the parameter settings for the memory modes that you can configure through the parameter editors. You can find the parameter editors under the **Memory Compiler** category when you launch the MegaWizard Plug-In Manager.



Altera recommends that you use the parameter editor to configure and build your RAM and ROM memory blocks to ensure that the combination of your selected options are valid.

Table 2–1 lists the parameter settings for the RAM:1-Port.

Table 2–1. RAM:1-Port Parameter Settings

Option	Legal Values	Default value	Description
Parameter Settings: Widths/Blk Type/Cls			
How wide should the 'q' output bus be?	—	8	Specifies the width of the 'q' output bus. For more information, refer to “Port Width Configuration” on page 3–7 .
How many <X>-bit words of memory?	—	256	Specifies the number of <X>-bit words.
What should the memory block type be?	Auto, M-RAM, M4K, M512, M9K, M10K, M144K, MLAB, M20K, LCs	Auto	Specifies the memory block type. The types of memory block that are available for selection depends on your target device. For more information refer to “Memory Block Types” on page 3–4 .
Set the maximum block depth to	Auto, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536	Auto	Specifies the maximum block depth in words. For more information refer to “Maximum Block Depth Configuration” on page 3–9 .
What clocking method would you like to use?	Single clock or Dual Clock: use separate 'input' and 'output' clocks	Single clock	Specifies the clocking method to use. Single clock —A single clock and a clock enable controls all registers of the memory block. Dual Clock: use separate 'input' and 'output' clocks —An input and an output clock controls all registers related to the data input and output to/from the memory block including data, address, byte enables, read enables, and write enables. For more information, refer to “Clocking Modes and Clock Enable” on page 3–10 .

Table 2-1. RAM:1-Port Parameter Settings

Option		Legal Values	Default value	Description
Parameter Settings: Regs/ClkEn/Byte Enable/Aclrs				
Which ports should be registered? The following options are available: <ul style="list-style-type: none"> ■ 'data' and 'wren' input ports ■ 'address' input port ■ 'q' output port 		On/Off	On	Specifies whether to register the input and output ports.
Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s)		On/Off	Off	Specifies whether to turn on the option to create one clock enable signal for each clock signal.
More Options	Use clock enable for port A input registers	On/Off	Off	Specifies whether to use clock enable for port A input registers.
	Use clock enable for port A output registers	On/Off	Off	Specifies whether to use clock enable for port A output registers.
	Create an 'addrsstall_a' input port.	On/Off	Off	Specifies whether to create a addrsstall_a input port. You can create this port to act as an extra active low clock enable input for the address registers. For more information, refer to "Address Clock Enable" on page 3-12.
Create byte enable for port A		On/Off	Off	Specifies whether to create a byte enable for port A. Turn on this option if you want to mask the input data so that only specific bytes, nibbles, or bits of data are written. For more information, refer to "Byte Enable" on page 3-13.
What is the width of a byte for byte enables?		MLAB: 5 or 10 Other memory block types: 8 or 9 M10K and M20K: 8 , 9 , or 10	MLAB: 5 Other memory block types: 8	Specifies the byte width of the byte enable port. The width of the data input port must be divisible by the byte size. For more information, refer to "Byte Enable" on page 3-13.
Create an 'aclr' asynchronous clear for the registered ports.		On/Off	Off	Specifies whether to create an asynchronous clear port for the registered data, wren, address, q, and byteena_a ports. For more information, refer to "Asynchronous Clear" on page 3-14.
More Options	'q' port	On/Off	Off	Turn on this option for the 'q' port to be affected by the asynchronous clear signal. The disabled ports are not affected by the asynchronous clear signal.

Table 2-1. RAM:1-Port Parameter Settings

Option	Legal Values	Default value	Description
Create a 'rden' read enable signal	On/Off	Off	Specifies whether to create a read enable signal. For more information, refer to “Read Enable” on page 3-15 .
Parameter Settings: Read During Write Option			
What should the q output be when reading from a memory location being written to?	New data, Don't Care	New data	Specifies the output behavior when read-during-write occurs. New Data —New data is available on the rising edge of the same clock cycle on which it was written. Don't Care —The RAM outputs “don't care” or “unknown” values for read-during-write operation. For more information, refer to “Read-During-Write” on page 3-16 .
Get x's for write masked bytes instead of old data when byte enable is used	On/Off	On	Turn on this option to obtain 'X' on the masked byte. For M10K and M20K memory block, this option is not available if you specify New Data as the output behavior when RDW occurs.
Parameter Settings: Mem Init			
Do you want to specify the initial content of the memory?	No, leave it blank or Yes, use this file for the memory content data	No, leave it blank	Specifies the initial content of the memory. To initialize the memory to zero, select No, leave it blank . To use a memory initialization file (.mif) or a hexadecimal (Intel-format) file (.hex), select Yes, use this file for the memory content data . For more information, refer to “Power-Up Conditions and Memory Initialization” on page 3-18 .
Allow In-System Memory Content Editor to capture and update content independently of the system clock	On/Off	Off	Specifies whether to allow In-System Memory Content Editor to capture and update content independently of the system clock.
The 'Instance ID' of this RAM is	—	None	Specifies the RAM ID.

Table 2–2 lists the parameter settings for the RAM:2-Port.

Table 2–2. RAM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
Parameter Settings: General			
How will you be using the dual port RAM?	With one read port and one write port or With two read /write ports	With one read port and one write port	Specifies how you use the dual port RAM.
How do you want to specify the memory size?	As a number of words or As a number of bits	As a number of words	Determines whether to specify the memory size in words or bits.
Parameter Settings: Widths/ Blk Type			
How many <X>-bit words of memory?	—	256	Specifies the number of <X>-bit words.
Use different data widths on different ports	On/Off	Off	Specifies whether to use different data widths on different ports.
When you select With one read port and one write port , the following options are available: ■ How wide should the 'q_a' output bus be? ■ How wide should the 'data_a' input bus be? ■ How wide should the 'q' output bus be?	—	8	Specifies the width of the input and output ports. For more information, refer to “Port Width Configuration” on page 3–7 .
When you select With two read/write ports , the following options are available: ■ How wide should the 'q_a' output bus be? ■ How wide should the 'q_b' output bus be?			
What should the memory block type be?	Auto, M-RAM, M4K, M512, M9K, M10K, M144K, MLAB, M20K, LCs	Auto	Specifies the memory block type. The types of memory block that are available for selection depends on your target device. For more information refer to “Memory Block Types” on page 3–4 .
How should the memory be implemented?	Use default logic cell style or Use Stratix M512 emulation logic cell style	Use default logic cell style	Specifies the logic cell implementation options. This option is enabled only when you choose LCs memory type.

Table 2–2. RAM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
Set the maximum block depth to	Auto, 32, 64, 128, 256, 512, 1024, 2048, 4096	Auto	Specifies the maximum block depth in words. This option is enabled only when you set the memory block type to Auto . For more information refer to “Maximum Block Depth Configuration” on page 3–9 .
Parameter Settings: Clks/Rd, Byte En			
What clocking method would you like to use?	<p>When you select With one read port and one write port, the following values are available:</p> <ul style="list-style-type: none"> ■ Single clock ■ Dual clock: use separate ‘input’ and ‘output’ clocks ■ Dual clock: use separate ‘read’ and ‘write’ clock <p>When you select With two read/write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ Single clock ■ Dual clock: use separate ‘input’ and ‘output’ clocks ■ Dual clock: use separate clocks for A and B ports 	Single clock	<p>Specifies the clocking method to use.</p> <p>Single clock—A single clock and a clock enable controls all registers of the memory block.</p> <p>Dual Clock: use separate ‘input’ and ‘output’ clocks—An input and an output clock controls all registers related to the data input and output to/from the memory block including data, address, byte enables, read enables, and write enables.</p> <p>Dual clock: use separate ‘read’ and ‘write’ clock—A write clock controls the data-input, write-address, and write-enable registers while the read clock controls the data-output, read-address, and read-enable registers.</p> <p>Dual clock: use separate clocks for A and B ports—Clock A controls all registers on the port A side; clock B controls all registers on the port B side. Each port also supports independent clock enables for both port A and port B registers, respectively.</p> <p>For more information, refer to “Clocking Modes and Clock Enable” on page 3–10.</p>

Table 2–2. RAM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
When you select With one read port and one write port , the following option is available: Create a 'rden' read enable signal	—	Off	Specifies whether to create a read enable signal for port B. For more information, refer to “Read Enable” on page 3–15 .
When you select With two read/write ports , the following option is available: Create a 'rden_a' and 'rden_b' read enable signal			Specifies whether to create a read enable signal for port A and B. For more information, refer to “Read Enable” on page 3–15 .
Create byte enable for port A	—	Off	Specifies whether to create a byte enable for port A and B. Turn on these options if you want to mask the input data so that only specific bytes, nibbles, or bits of data are written. The option to create a byte enable for port B is only available when you select two read/write ports. For more information, refer to “Byte Enable” on page 3–13 .
Create byte enable for port B			
Enable error checking and correcting (ECC) to check and correct single bit errors and detect double errors	On/Off	Off	Specifies whether to enable the ECC feature that corrects single bit errors and detects double errors at the output of the memory. This option is only available in devices that support M144K memory block type. For more information, refer to “Error Correction Code” on page 3–19 .
Enable error checking and correcting (ECC) to check and correct single bit errors, double adjacent bit errors, and detect triple adjacent bit errors	On/Off	Off	Specifies whether to enable the ECC feature that corrects single bit errors, double adjacent bit errors, and detects triple adjacent bit errors at the output of the memory. This option is only available in devices that support M20K memory block type. For more information, refer to “Error Correction Code” on page 3–19 .

Table 2-2. RAM:2-Port Parameter Settings

Option		Legal Values	Default values	Description
Parameter Settings: Regs/Clkens/Aclrs				
<p>Which ports should be registered?</p> <p>When you select With one read port and one write port, the following options are available:</p> <ul style="list-style-type: none"> ■ 'data', 'waddress', and 'wren' write input ports ■ 'raddress' and 'rden' read input port ■ Read output port(s) 'q' <p>When you select With two read/write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ 'data_a', 'waddress_a', and 'wren_a' write input ports ■ Read output port(s) 'q'_a and 'q'_b 		On/Off	On	Specifies whether to register the read or write input and output ports.
More Options	<p>When you select With one read port and one write port, the following options are available:</p> <ul style="list-style-type: none"> ■ 'data' port ■ 'waddress' port ■ 'wren' port ■ 'raddress' port ■ 'q_b' port <p>When you select With two read/write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ 'data_a' port ■ 'data_b' port ■ 'waddress_a' port ■ 'waddress_b' port ■ 'wren_a' port ■ 'wren_b' port ■ 'q_a' port ■ 'q_b' port 	On/Off	On	The read and write input ports are turned on by default. You only need to specify whether to register the Q output ports.

Table 2–2. RAM:2-Port Parameter Settings

Option		Legal Values	Default values	Description
Create one clock enable signal for each clock signal.		On/Off	Off	Specifies whether to turn on the option to create one clock enable signal for each clock signal. For more information, refer to “Clocking Modes and Clock Enable” on page 3–10.
More Options	<p>When you select With one read port and one write port, the following option is available:</p> <p>Use clock enable for write input registers</p> <p>When you select With two read /write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ Use clock enable for port A input registers ■ Use clock enable for port B input registers ■ Use clock enable for port A output registers ■ Use clock enable for port B output register 	On/Off	Off	<p>Clock enable for port B input and output registers are turned on by default. You only need to specify whether to use clock enable for port A input and output registers.</p> <p>For more information, refer to “Clocking Modes and Clock Enable” on page 3–10.</p>

Table 2-2. RAM:2-Port Parameter Settings

Option		Legal Values	Default values	Description
More Options	<p>When you select With one read port and one write port, the following options are available:</p> <ul style="list-style-type: none"> ■ Create an 'wr_addrsstall' input port. ■ Create an 'rd_addrsstall' input port. <p>When you select With two read/write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ Create an 'addrsstall_a' input port. ■ Create an 'addrsstall_b' input port. 	On/Off	Off	<p>Specifies whether to create clock enables for address registers. You can create these ports to act as an extra active low clock enable input for the address registers.</p> <p>For more information, refer to "Address Clock Enable" on page 3-12.</p>
Create an 'aclr' asynchronous clear for the registered ports.		On/Off	Off	<p>Specifies whether to create an asynchronous clear port for the registered ports.</p> <p>For more information, refer to "Asynchronous Clear" on page 3-14.</p>
More Options	<p>When you select With one read port and one write port, the following options are available:</p> <ul style="list-style-type: none"> ■ 'rdaddress' port ■ 'q_b' port <p>When you select With two read/write ports, the following options are available:</p> <ul style="list-style-type: none"> ■ 'q_a' port ■ 'q_b' port 	On/Off	Off	<p>Specifies whether the 'rdaddress', 'q_a', and 'q_b' ports are cleared by the <code>aclr</code> port.</p>

Table 2-2. RAM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
Parameter Settings: Output 1			
<p>When you select With one read port and one write port, the following option is available: How should the q output behave when reading a memory location that is being written from the other port?</p> <p>When you select With two read /write ports, the following option is available: How should the q_a and q_b outputs behave when reading a memory location that is being written from the other port?</p>	<p>Old memory contents appear or I do not care</p>	<p>I do not care</p>	<p>Specifies the output behavior when read-during-write occurs.</p> <p>Old memory contents appear—The RAM outputs reflect the old data at that address before the write operation proceeds.</p> <p>I do not care—This option functions differently when you turn it on depending on the following memory block type you select:</p> <ul style="list-style-type: none"> ■ When you set the memory block type to Auto, M144K, M512, M4K, M9K, M10K, M20K or any other block RAM, the RAM outputs ‘don’t care’ or “unknown” values for read-during-write operation without analyzing the timing path. ■ When you set the memory block type to MLAB (for LUTRAM), the RAM outputs ‘don’t care’ or ‘unknown’ values for read-during-write operation but analyzes the timing path to prevent metastability. <p>For more information, refer to “Read-During-Write” on page 3-16.</p>
<p>Do not analyze the timing between write and read operation. Metastability issues are prevented by never writing and reading at the same address at the same time.</p>	<p>On/Off</p>	<p>Off</p>	<p>Turn on this option when you want the RAM to output ‘don’t care’ or unknown values for read-during-write operation without analyzing the timing path.</p> <p>This option is only available for LUTRAM and is enabled when you set memory block type to MLAB.</p>

Table 2-2. RAM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
Parameter Settings: Output 2 (This tab is only available when you select two read/ write ports)			
What should the 'q_a' output be when reading from a memory location being written to?	New data, Old Data	New data	<p>Specifies the output behavior when read-during-write occurs.</p> <p>New Data—New data is available on the rising edge of the same clock cycle on which it was written.</p> <p>Old Data—The RAM outputs reflect the old data at that address before the write operation proceeds.</p> <p>For more information, refer to “Read-During-Write” on page 3-16.</p>
What should the 'q_b' output be when reading from a memory location being written to?			
Get x's for write masked bytes instead of old data when byte enable is used	On/Off	On	Turn on this option to obtain 'X' on the masked byte.
Parameter Settings: Mem Init			
Do you want to specify the initial content of the memory?	No, leave it blank or Yes, use this file for the memory content data	No, leave it blank	<p>Specifies the initial content of the memory.</p> <p>To initialize the memory to zero, select No, leave it blank.</p> <p>To use a memory initialization file (.mif) or a hexadecimal (Intel-format) file (.hex), select Yes, use this file for the memory content data.</p> <p>For more information, refer to “Power-Up Conditions and Memory Initialization” on page 3-18.</p>

Table 2-3 lists the parameter settings for the ROM:1-Port.

Table 2-3. ROM:1-Port Parameter Settings

Option	Legal Values	Default values	Description
Parameter Settings: General Page			
How wide should the 'q' output bus be?	—	8	Specifies the width of the 'q' output bus. For more information, refer to “Port Width Configuration” on page 3-7 .
How many <X>-bit words of memory?	—	256	Specifies the number of <X>-bit words.
What should the memory block type be?	Auto, M4K, M9K, M144K, M10K, M20K	Auto	Specifies the memory block type. The types of memory block that are available for selection depends on your target device. For more information, refer to “Memory Block Types” on page 3-4 .
Set the maximum block depth to	Auto, 32, 64, 128, 256, 512, 1024, 2048, 4096	Auto	Specifies the maximum block depth in words. For more information, refer to “Maximum Block Depth Configuration” on page 3-9 .
What clocking method would you like to use?	Single clock or Dual clock: use separate 'input' and 'output' clocks	Single clock	Specifies the clocking method to use. Single clock —A single clock and a clock enable controls all registers of the memory block Dual clock (Input and Output clock)—The input clock controls the address registers and the output clock controls the data-out registers. There are no write-enable, byte-enable, or data-in registers in ROM mode. For more information, refer to “Clocking Modes and Clock Enable” on page 3-10 .
Parameter Settings: Regs/Cken/Aclrs			
Which ports should be registered? 'q' output port	On/Off	On	Specifies whether to register the 'q' output port.
Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s)	On/Off	Off	Specifies whether to turn on the option to create one clock enable signal for each clock signal.

Table 2-3. ROM:1-Port Parameter Settings

Option		Legal Values	Default values	Description
More Options	Use clock enable for port A input registers	On/Off	Off	Specifies whether to use clock enable for port A input registers.
	Use clock enable for port A output registers	On/Off	Off	Specifies whether to use clock enable for port A output registers.
	Create an 'addressstall_a' input port.	On/Off	Off	Specifies whether to create a addressstall_a input port. You can create this port to act as an extra active low clock enable input for the address registers. For more information, refer to "Address Clock Enable" on page 3-12.
Create an 'aclr' asynchronous clear for the registered ports.		On/Off	Off	Specifies whether to create an asynchronous clear port for the registered ports. For more information, refer to "Asynchronous Clear" on page 3-14.
More Options	'address' port	On/Off	Off	Specifies whether the 'address' port should be affected by the 'aclr' port.
	'q' port	On/Off	Off	Specifies whether the 'q' port should be affected by the 'aclr' port.
Create a 'rden' read enable signal		On/Off	Off	Specifies whether to create a read enable signal. For more information, refer to "Read Enable" on page 3-15.
Parameter Settings: Mem Init				
Do you want to specify the initial content of the memory?		Yes, use this file for the memory content data	Yes, use this file for the memory content data	Specifies the initial content of the memory. In ROM mode you must specify a memory initialization file (.mif) or a hexadecimal (Intel-format) file (.hex). The Yes, use this file for the memory content data option is turned on by default. For more information, refer to "Power-Up Conditions and Memory Initialization" on page 3-18.

Table 2-3. ROM:1-Port Parameter Settings

Option	Legal Values	Default values	Description
Allow In-System Memory Content Editor to capture and update content independently of the system clock	On/Off	Off	Specifies whether to allow In-System Memory Content Editor to capture and update content independently of the system clock
The 'Instance ID' of this ROM is	—	None	Specifies the ROM ID.

Table 2-4 lists the parameter settings for the ROM:2-Port.

Table 2-4. ROM:2-Port Parameter Settings

Option	Legal Values	Default values	Description
Parameter Settings: Widths/Blk Type			
How do you want to specify the memory size?	As a number of words or As a number of bits	As a number of words	Determines whether to specify the memory size in words or bits.
How many <X>-bit words of memory?	32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536	256	Specifies the number of <X>-bit words.
Use different data widths on different ports	On/Off	Off	Specifies whether to use different data widths on different ports. For more information, refer to “Mixed-width Port Configuration” on page 3-8.
How wide should the 'q_a' output bus be?	—	8	Specifies the width of the 'q_a' and 'q_b' output ports. For more information, refer to “Port Width Configuration” on page 3-7.
How wide should the 'q_b' output bus be?			
What should the memory block type be?	Auto, M4K, M9K, M144K, M10K, M20K, MLAB	Auto	Specifies the memory block type. The types of memory block that are available for selection depends on your target device For more information, refer to “Memory Block Types” on page 3-4.
Set the maximum block depth to	Auto, 128, 256, 512, 1024, 2048, 4096	Auto	Specifies the maximum block depth in words. This option is enabled only when you choose Auto as the memory block type. For more information, refer to “Maximum Block Depth Configuration” on page 3-9.

Table 2-4. ROM:2-Port Parameter Settings

Option		Legal Values	Default values	Description
Parameter Settings: Clks/Rd, Byte En				
What clocking method would you like to use?		<p>Single clock</p> <p>or</p> <p>Dual Clock: use separate 'input' and 'output' clocks</p> <p>or</p> <p>Dual clock: use separate clocks for A and B ports</p>	Single clock	<p>Specifies the clocking method to use.</p> <p>Single clock—A single clock and a clock enable controls all registers of the memory block</p> <p>Dual Clock: use separate 'input' and 'output' clocks—The input clock controls the address registers and the output clock controls the data-out registers. There are no write-enable, byte-enable, or data-in registers in ROM mode.</p> <p>Dual clock: use separate clocks for A and B ports—Clock A controls all registers on the port A side; clock B controls all registers on the port B side. Each port also supports independent clock enables for both port A and port B registers, respectively.</p> <p>For more information, refer to "Clocking Modes and Clock Enable" on page 3-10.</p>
Create a 'rden_a' and 'rden_b' read enable signals		—	Off	<p>Specifies whether to create read enable signals.</p> <p>For more information, refer to "Read Enable" on page 3-15.</p>
Parameter Settings: Regs/Clks/Aclrs				
Read output port(s) 'q_a' and 'q_b'		On/Off	On	Specifies whether to register the 'q_a' and 'q_b' output ports.
More Options	'q_a' port	On/Off	On	Specifies whether to register the 'q_a' output port.
	'q_b' port	On/Off	On	Specifies whether to register the 'q_b' output port.
Create one clock enable signal for each clock signal.		On/Off	Off	Specifies whether to turn on the option to create one clock enable signal for each clock signal.

Table 2-4. ROM:2-Port Parameter Settings

Option		Legal Values	Default values	Description
More Options	Use clock enable for port A input registers	On/Off	Off	Specifies whether to use clock enable for port A input registers.
	Use clock enable for port A output registers	On/Off	Off	Specifies whether to use clock enable for port A output registers.
	Create an 'addressstall_a' input port.	On/Off	Off	Specifies whether to create addressstall_a and addressstall_b input ports. You can create these ports to act as an extra active low clock enable input for the address registers. For more information, refer to "Address Clock Enable" on page 3-12.
	Create an 'addressstall_b' input port.			
Create an 'aclr' asynchronous clear for the registered ports.		On/Off	Off	Specifies whether to create an asynchronous clear port for the registered ports. For more information, refer to "Asynchronous Clear" on page 3-14.
More Options	'q_a' port	On/Off	Off	Specifies whether the 'q_a' port should be cleared by the aclr port.
	'q_b' port	On/Off	Off	Specifies whether the 'q_b' port should be cleared by the aclr port.
Parameter Settings: Mem Init				
Do you want to specify the initial content of the memory?		Yes, use this file for the memory content data	Yes, use this file for the memory content data	Specifies the initial content of the memory. In ROM mode you must specify a memory initialization file (.mif) or a hexadecimal (Intel-format) file (.hex). The Yes, use this file for the memory content data option is turned on by default. For more information, refer to "Power-Up Conditions and Memory Initialization" on page 3-18.
The initial content file should conform to which port's dimensions?		PORT_A or PORT_B	PORT_A	Specifies whether the initial content file conforms to port A or port B.

This section describes the features and functionality of the internal memory blocks and the ports of the ALTSYNCRAM and ALTDPRAM megafunctions.

Memory Modes Configuration

A memory block contains two address ports (port A and port B) with their respective output data ports, and you can use them for read and write operations depending on the memory mode you choose. The input and output ports shown in the block diagrams refer to the ports of the wrapper that contains the memory megafunction instantiated in it. The ports of the wrapper are mapped to the ports of either the ALTSYNCRAM or the ALTDPRAM megafunction depending on your memory configuration, and the port name reflects the memory features you create. For example, the name of the wrapper port `clockena` maps to the `clock_enable_input_a` port of the ALTSYNCRAM megafunction, which relates to the clock enable feature.

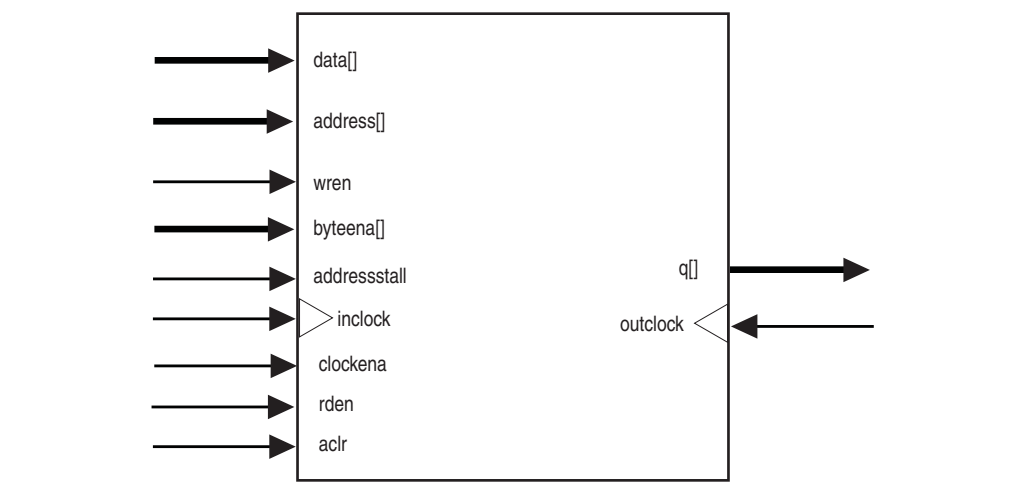
For more information about the ports of the ALTSYNCRAM and ALTDPRAM megafunctions, refer to [“ALTSYNCRAM and ALTDPRAM Megafunction Ports” on page 3–20](#).

Single-port RAM

In a single-port RAM, the read and write operations share the same address at port A, and the data is read from output port A.

[Figure 3–1](#) shows a block diagram of a typical single-port RAM.

Figure 3–1. Single-port RAM

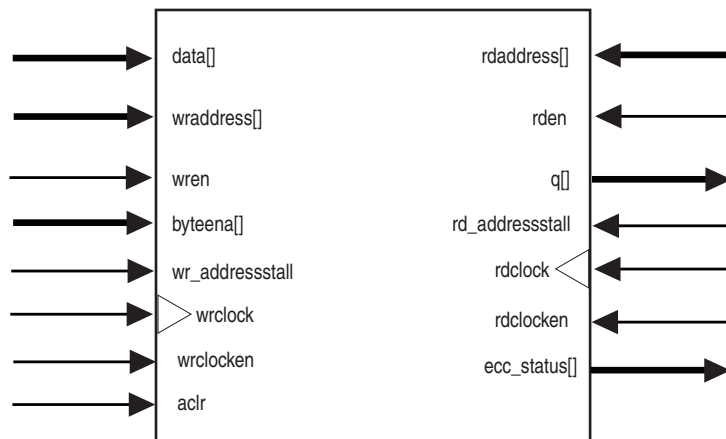


Simple Dual-port RAM

In simple dual-port RAM mode, a dedicated address port is available for each read and write operation (one read port and one write port). A write operation uses write address from port A while read operation uses read address and output from port B.

Figure 3–2 shows the block diagram of a simple dual-port RAM.

Figure 3–2. Simple Dual-Port RAM

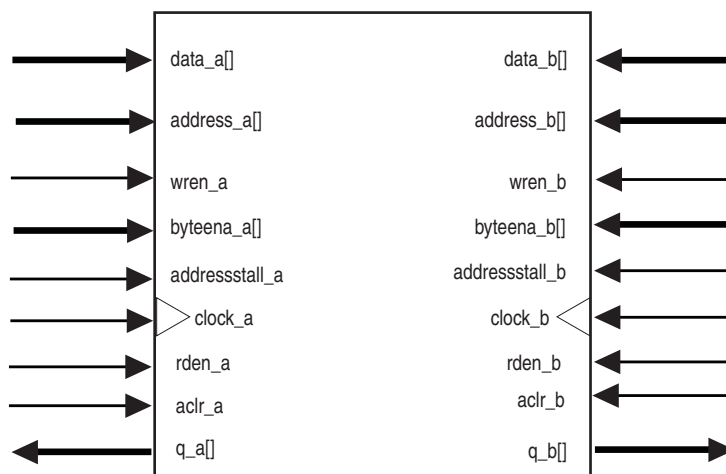


True Dual-port RAM

In true dual-port RAM mode, two address ports are available for read or write operation (two read/write ports). In this mode, you can write to or read from the address of port A or port B, and the data read is shown at the output port with respect to the read address port.

Figure 3–3 shows the block diagrams of a true dual-port RAM.

Figure 3–3. True Dual-port RAM

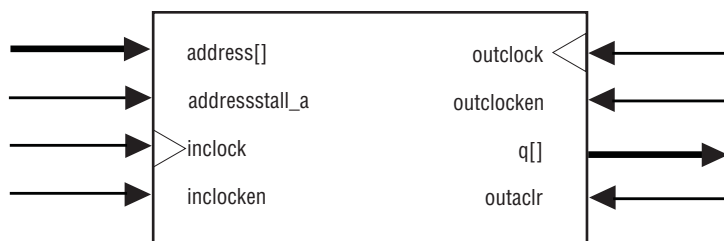


Single-port ROM

In single-port ROM, only one address port is available for read operation.

Figure 3-4 shows the block diagram of a single-port ROM.

Figure 3-4. Single-port ROM

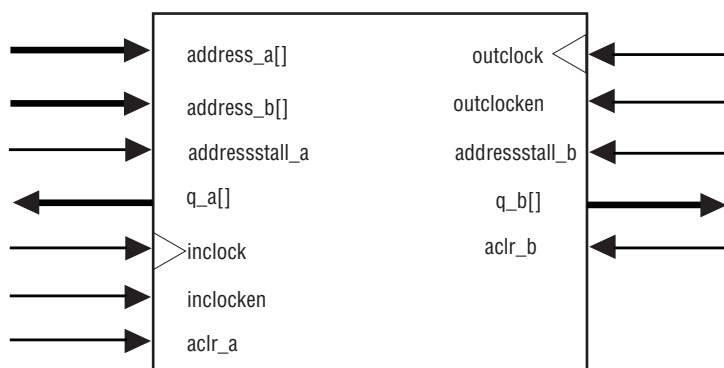


Dual-port ROM

The dual-port ROM has almost similar functional ports as single-port ROM. The difference is dual-port ROM has an additional address port for read operation.

Figure 3-4 shows the block diagram of a dual-port ROM.

Figure 3-5. Dual-port ROM



Memory Block Types

Altera provides various sizes of embedded memory blocks for various devices. The parameter editor allows you to implement your memory in the following ways:


- Select the type of memory blocks available based on your target device. Refer to [Table 3-1 on page 3-5](#). To select the appropriate memory block type for your device, obtain more information about the features of your selected internal memory block in your target device, such as the maximum performance, supported configurations (depth × width), byte enable, power-up condition, and the write and read operation triggering.
 - Use logic cells. As compared to internal memory resources, using logic cells to create memory reduces the design performance and utilizes more area. This implementation is normally used when you have used up all the internal memory resources. When logic cells are used, the parameter editor provides you with the following two types of logic cell implementations:
 - Default logic cell style—the write operation triggers (internally) on the rising edge of the write clock and have continuous read. This implementation uses less logic cells and is faster, but it is not fully compatible with the Stratix M512 emulation style.
 - Stratix M512 emulation logic cell style—the write operation triggers (internally) on the falling edge of the write clock and performs read only on the rising edge of the read clock.
 - Select the **Auto** option, which allows the software to automatically select the appropriate internal memory resource. When you set the memory block type to **Auto**, the compiler favors larger block types that can support the memory capacity you require in a single internal memory block. This setting gives the best performance and requires no logic elements (LEs) for glue logic. When you create the memory with specific internal memory blocks, such as M9K, the compiler is still able to emulate wider and deeper memories than the block type supported natively. The compiler spans multiple internal memory blocks (only of the same type) with glue logic added in the LEs as needed.
-  To obtain proper implementation based on the memory configuration you set, allow the Quartus II software to automatically choose the memory type. This gives the compiler the flexibility to place the memory function in any available memory resources based on the functionality and size.

Table 3–1 lists the options available for you to implement your memory blocks in various device families.

Table 3–1. Internal Memory Blocks in Altera Devices

Device Family	Memory Block Types								
	M512 ⁽¹⁾ (512 bits)	M4K (4 Kbits)	M-RAM ⁽²⁾ (512 Kbits)	MLAB ^{(3) (4)} (640 bits)	M9K (9 Kbits)	M144K (144 Kbits)	M10K (10 Kbits)	M20K (20 Kbits)	Logic Cell (LC)
Arria GX	✓	✓	✓	—	—	—	—	—	—
Arria II GX	—	—	—	✓	✓	—	—	—	✓
Arria II GZ	—	—	—	✓	✓	✓	—	—	✓
Arria V	—	—	—	✓	—	—	✓	—	✓
Cyclone, Cyclone II	—	✓	—	—	—	—	—	—	✓
Cyclone III, Cyclone IV	—	—	—	—	✓	—	—	—	✓
Cyclone V	—	—	—	✓	—	—	✓	—	✓
HardCopy II	—	✓	✓	—	—	—	—	—	✓
HardCopy III, HardCopy IV	—	—	—	✓	✓	✓	—	—	✓
Max V, Max II, Max 3000A, Max 7000	—	—	—	—	—	—	—	—	✓
Stratix, Stratix GX, Stratix II, Stratix II GX,	✓	✓	✓	—	—	—	—	—	✓
Stratix III, Stratix IV	—	—	—	✓	✓	✓	—	—	✓
Stratix V	—	—	—	✓	—	—	—	✓	✓

Notes to Table 3–8:

- (1) M512 blocks are not supported in true dual-port RAM mode, and dual-port ROM mode
- (2) M-RAM blocks are not supported in ROM mode.
- (3) For Stratix III devices, MLAB blocks are 320-bit in RAM mode and 640-bit in ROM mode.
- (4) MLAB blocks are not supported in simple dual-port RAM mode with mixed-width port feature, true dual-port RAM mode, and dual-port ROM mode.



To identify the type of memory block that the software selects to create your memory, refer to the fitter report after compilation.



For more information about internal memory blocks and the specifications, refer to the memory related chapters in your target device handbook.

Write and Read Operations Triggering

The internal memory blocks vary slightly in its supported features and behaviors. One important variation is the difference in the write and read operations triggering.

Table 3–2 lists the write and read operations triggering for various internal memory blocks.

Table 3–2. Write and Read Operations Triggering for internal Memory Blocks

internal Memory Blocks	Write Operation ⁽¹⁾	Read Operation
M10K	Rising clock edges	Rising clock edges
M20K	Rising clock edges	Rising clock edges
M144K	Rising clock edges	Rising clock edges
M9K	Rising clock edges	Rising clock edges
MLAB	Falling clock edges Rising clock edges (in Arria V, Cyclone V, and Stratix V devices only)	Rising clock edges ⁽²⁾
M-RAM	Rising clock edges	Rising clock edges
M4K	Falling clock edges	Rising clock edges
M512	Falling clock edges	Rising clock edges

Notes to Table 3–2:

- (1) Write operation triggering is not applicable to ROMs.
- (2) MLAB supports continuous reads. For example, when you write a data at the write clock rising edge and after the write operation is complete, you see the written data at the output port without the need for a read clock rising edge.

It is important that you understand the write operation triggering to avoid potential write contentions that can result in unknown data storage at that location.

Figure 3-6 and Figure 3-7 show the valid write operation that triggers at the rising and falling clock edge, respectively.

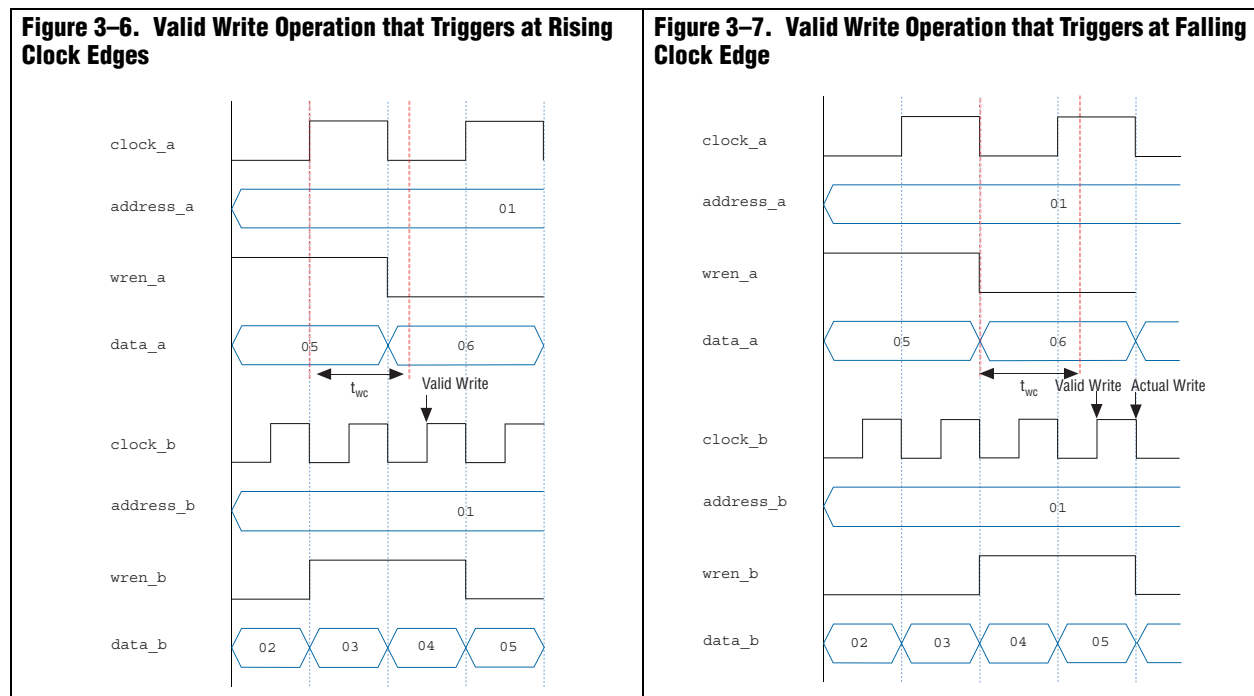


Figure 3-6 assumes that t_{wc} is the maximum write cycle time interval. Write operation of data 03 through port B does not meet the criteria and causes write contention with the write operation at port A, which result in unknown data at address 01. The write operation at the next rising edge is valid because it meets the criteria and data 04 replaces the unknown data.

Figure 3-7 assumes that t_{wc} is the maximum write cycle time interval. Write operation of data 04 through port B does not meet the criteria and therefore causes write contention with the write operation at port A that result in unknown data at address 01. The next data (05) is latched at the next rising clock edge that meets the criteria and is written into the memory block at the falling clock edge.



Data and addresses are latched at the rising edge of the write clock regardless of the different write operation triggering.

Port Width Configuration

The port width configuration is defined by the following equation:

Memory depth (number of words) × Width of the data input bus



For more information about the supported port width configuration for various internal memory blocks, refer to the memory related chapters in your target device handbook.

If your port width configuration (either the depth or the width) is more than the amount an internal memory block can support, additional memory blocks (of the same type) are used. For example, if you configure your M9K as 512×36 , which exceeds the supported port width of 512×18 , two M9Ks are used to implement your RAM.

In addition to the supported configuration provided, you can set the memory depth to a non-power of two, but the actual memory depth allocated can vary. The variation depends on the type of resource implemented.

If the memory is implemented in dedicated memory blocks, setting a non-power of two for the memory depth reflects the actual memory depth. If the memory is implemented in logic cells (and not using Stratix M512 emulation logic cell style that can be set through the parameter editor), setting a non-power of two for the memory depth does not reflect the actual memory depth. In this case, you write to or read from up to $2^{\text{address_width}}$ memory locations even though the memory depth you set is less than $2^{\text{address_width}}$. For example, if you set the memory depth to 3, and the RAM is implemented using logic cells, your actual memory depth is 4.

When you implement your memory using dedicated memory blocks, you can check the actual memory depth by referring to the fitter report.

Mixed-width Port Configuration

Only dual-port RAM and dual-port ROM support mixed-width port configuration for all memory block types except when they are implemented with LEs. The support for mixed-width port depends on the width ratio between port A and port B. In addition, the supporting ratio varies for various memory modes, memory blocks, and target devices.



MLABs do not have native support for mixed-width operation, thus the option to select MLABs is disabled in the parameter editor. However, the Quartus II software can implement mixed-width memories in MLABs by using more than one MLAB. Therefore, if you select **AUTO** for your memory block type, it is possible to implement mixed-width port memory using multiple MLABs.



For more information about width ratio that supports mixed-width port, refer to your relevant device handbook.

Memory depth of 1 word is not supported in simple dual-port and true dual-port RAMs with mixed-width port. The parameter editor prompts an error message when the memory depth is less than 2 words. For example, if the width for port A is 4 bits and the width for port B is 8 bits, the smallest depth supported by the RAM is 4 words. This configuration results in memory size of 16 bits (4×4) and can be represented by memory depth of 2 words for port B. If you set the memory depth to 2 words that results in memory size of 8 bits (2×4), it can only be represented by memory depth of 1 word for port B, and therefore the width of the port is not supported.

Maximum Block Depth Configuration

You can limit the maximum block depth of the dedicated memory block you use. The memory block can be sliced to your desired maximum block depth. For example, the capacity of an M9K block is 9,216 bits, and the default memory depth is 8K, in which each address is capable of storing 1 bit ($8K \times 1$). If you set the maximum block depth to 512, the M9K block is sliced to a depth of 512 and each address is capable of storing up to 18 bits (512×18).

You can use this option to save power usage in your devices. However, this parameter might increase the number of LEs and affects the design performance.

Table 3-3 lists the estimated dynamic power usage for different slice type that is applied to an $8K \times 36$ (M9K RAM block) design in a Stratix III EP3SE50 device.

Table 3-3. Power Usage Setting for $8K \times 36$ (M9K) Design of a Stratix III Device

M9K Slice Type	Dynamic Power (mW)	ALUT Usage	M9Ks
$8K \times 1$ (default setting)	51.49	0	36
$4K \times 2$	20.28 (39%)	38	36
$2K \times 4$	10.80 (21%)	44	36
$1K \times 9$	6.08 (12%)	125	32
512×18	4.51 (9%)	212	32
256×36	6.36 (12%)	467	32

When the RAM is sliced shallower, the dynamic power usage decreases. However, for a RAM block with a depth of 256, the power used by the extra LEs starts to outweigh the power gain achieved by shallower slices.

You can also use this option to reduce the total number of memory blocks used (but at the expense of LEs). From Table 3-3, the $8K \times 36$ RAM uses 36 M9K RAM blocks with a default slicing of $8K \times 1$. By setting the maximum block depth to 1K, the $8K \times 36$ RAM can fit into 32 M9K blocks.

The maximum block depth must be in a power of two, and the valid values vary among different dedicated memory blocks.

Table 3-4 lists the valid range of maximum block depth for various internal memory blocks.

Table 3-4. Valid Range of Maximum Block Depth for Various internal Memory Blocks

internal Memory Blocks	Valid Range ⁽¹⁾
M10K	256–8K
M20K	512–16K
M144K	2K–16K
M9K	256–8K
MLAB	32–64 ⁽²⁾
M512	32–512
M4K	128–4K
M-RAM	4K–64K

Notes to Table 3-4:

- (1) The maximum block depth must be in a power of two.
- (2) The maximum block depth setting (64) for MLAB is not available for Arria V, Cyclone V, and Stratix III devices.

The parameter editor prompts an error message if you enter an invalid value for the maximum block depth. Altera recommends that you set the value to **Auto** if you are not sure of the appropriate maximum block depth to set or the setting is not important for your design. This setting enables the compiler to select the maximum block depth with the appropriate port width configuration for the type of internal memory block of your memory.

Clocking Modes and Clock Enable

Altera internal memory supports various types of clocking modes depending on the memory mode you select.

Table 3-5 lists the internal memory clocking modes.

Table 3-5. Clocking Modes

Clocking Modes	Single-port RAM	Simple Dual-port RAM	True Dual-port RAM	Single-port ROM	Dual-port ROM
Single clock	✓	✓	✓	✓	✓
Read/Write	—	✓	—	—	—
Input/Output	✓	✓	✓	✓	✓
Independent	—	—	✓	—	✓



Asynchronous clock mode is only supported in MAX series of devices, and not supported in Stratix and newer devices. However, Stratix III and newer devices support asynchronous read memory for simple dual-port RAM mode if you choose MLAB memory block with unregistered rdaddress port.



The clock enable signals are not supported for write address, byte enable, and data input registers on Arria V, Cyclone V, and Stratix V MLAB blocks.

Single Clock Mode

In the single clock mode, a single clock, together with a clock enable, controls all registers of the memory block.

Read/Write Clock Mode

In the read/write clock mode, a separate clock is available for each read and write port. A read clock controls the data-output, read-address, and read-enable registers. A write clock controls the data-input, write-address, write-enable, and byte enable registers.

Input/Output Clock Mode

In input/output clock mode, a separate clock is available for each input and output port. An input clock controls all registers related to the data input to the memory block including data, address, byte enables, read enables, and write enables. An output clock controls the data output registers.

Independent Clock Mode

In the independent clock mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side; clock B controls all registers on the port B side.



You can create independent clock enable for different input and output registers to control the shut down of a particular register for power saving purposes. From the parameter editor, click **More Options** (beside the clock enable option) to set the available independent clock enable that you prefer.

Address Clock Enable

The address clock enable (addressstall) port is an active high asynchronous control signal that holds the previous address value for as long as the signal is enabled. When the memory blocks are configured in dual-port RAMs or dual-port ROMs, you can create independent address clock enable for each address port.

To configure the address clock enable feature, click **More Options** located beside the clock enable option on the parameter editor. Turn on **Create an 'addressstall_a' input port** or **Create an 'addressstall_b' input port** to create an addressstall port.

Figure 3–8 and Figure 3–9 show the results of address clock enable signal during the read and write operations, respectively.

Figure 3–8. Address Clock Enable During Read Operation

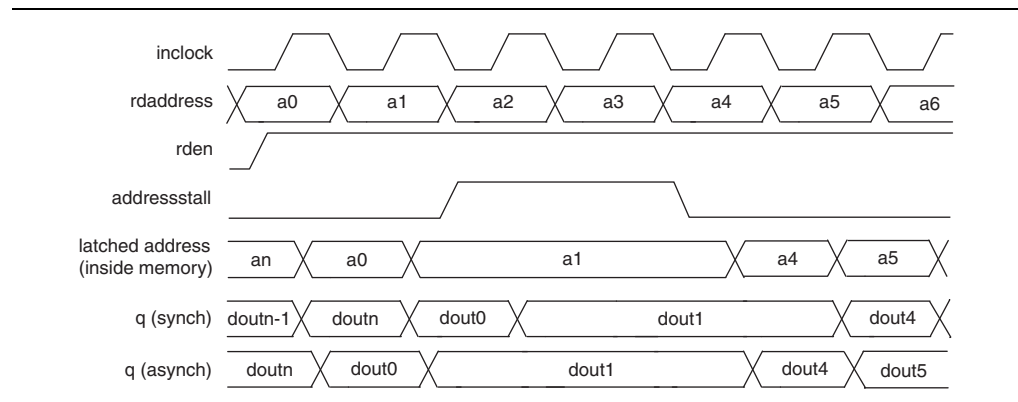
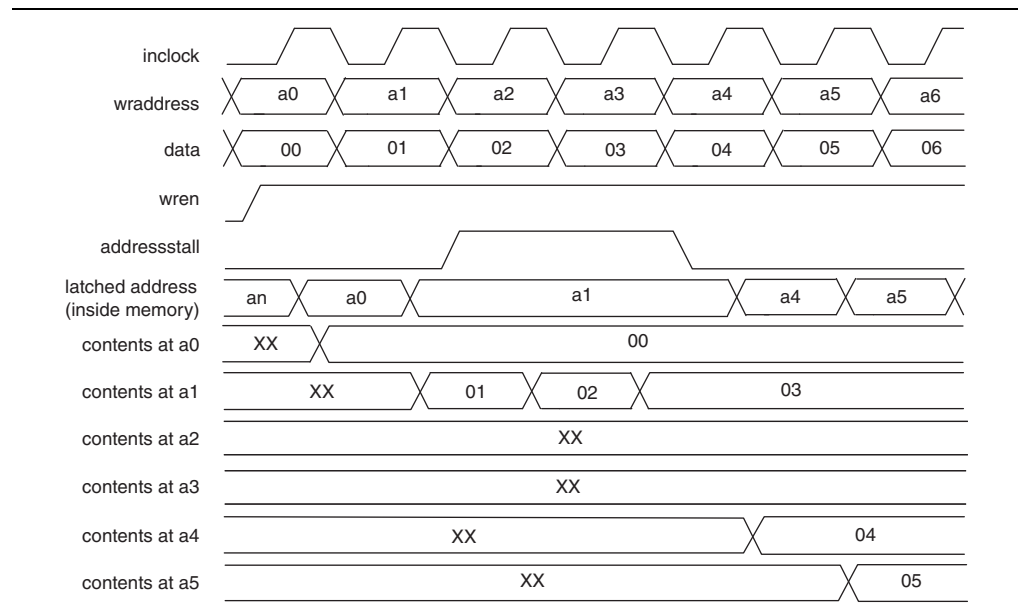


Figure 3–9. Address Clock Enable During Write Operation



Byte Enable

All internal memory blocks that are implemented as RAMs support byte enables that mask the input data so that only specific bytes, nibbles, or bits of data are written. The unwritten bytes or bits retain the previously written value.

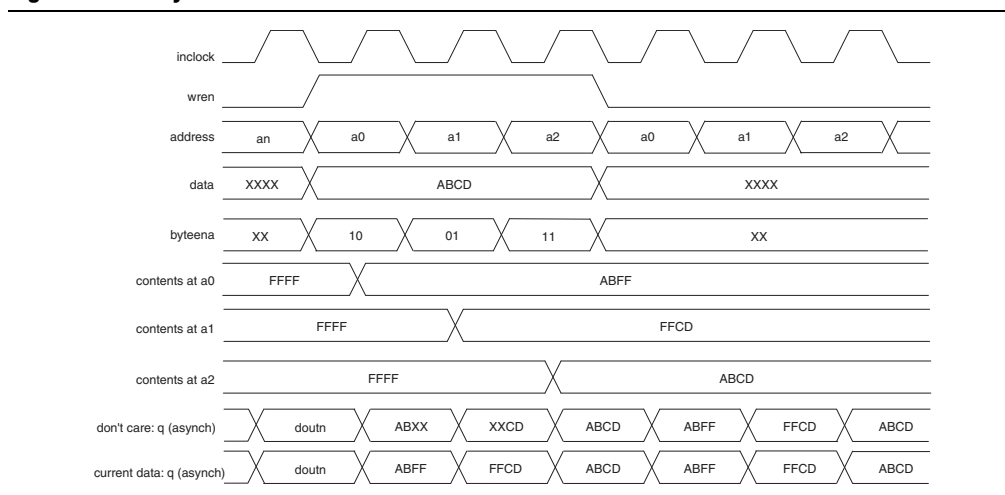
The least significant bit (LSB) of the byte-enable port corresponds to the least significant byte of the data bus. For example, if you use a RAM block in x18 mode and the byte-enable port is 01, data [8..0] is enabled and data [17..9] is disabled. Similarly, if the byte-enable port is 11, both data bytes are enabled.

You can specifically define and set the size of a byte for the byte-enable port. The valid values are 5, 8, 9, and 10, depending on the type of internal memory blocks. The values of 5 and 10 are only supported by MLAB.

To create a byte-enable port, the width of the data input port must be a multiple of the size of a byte for the byte-enable port. For example, if you use an MLAB memory block, the byte enable is only supported if your data bits are multiples of 5, 8, 9 or 10, that is 10, 15, 16, 18, 20, 24, 25, 27, 30, and so on. If the width of the data input port is 10, you can only define the size of a byte as 5. In this case, you get a 2-bit byte-enable port, each bit controls 5 bits of data input written. If the width of the data input port is 20, then you can define the size of a byte as either 5 or 10. If you define 5 bits of input data as a byte, you get a 4-bit byte-enable port, each bit controls 5 bits of data input written. If you define 10 bits of input data as a byte, you get a 2-bit byte-enable port, each bit controls 10 bits of data input written.

Figure 3-10 shows the results of the byte enable on the data that is written into the memory, and the data that is read from the memory.

Figure 3-10. Byte Enable Functional Waveform



When a byte-enable bit is deasserted during a write cycle, the corresponding masked byte of the **q** output can appear as a “Don't Care” value or the current data at that location. This selection is only available if you set the read-during-write output behavior to **New Data**.



For more information about the masked byte and the **q** output, refer to “Read-During-Write” on page 3-16.

Asynchronous Clear

The internal memory blocks in the Arria II GX, Arria II GZ, Cyclone III, HardCopy III, HardCopy IV, Stratix III, Stratix IV, Stratix V, and newer device families support the asynchronous clear feature used on the output latches and output registers. Therefore, if your RAM does not use output registers, clear the RAM outputs using the output latch asynchronous clear. The asynchronous clear feature allows you to clear the outputs even if the *q* output port is not registered. However, this feature is not supported in MLAB memory blocks.

The outputs stay cleared until the next clock. However, in Arria V, Cyclone V, and Stratix V devices, the outputs stay cleared until the next read.



You cannot use the asynchronous clear port to clear the contents of the internal memory. Use the asynchronous clear port to clear the contents of the input and output register stages only.

Table 3-6 lists the asynchronous clear effects on the input ports for various devices in various memory settings.

Table 3-6. Asynchronous Clear Effects on the Input Ports for Various Devices in Various Memory Settings

Memory Mode	Cyclone, Stratix, and Stratix GX	Arria GX, Cyclone II, HardCopy II, Stratix II, and Stratix II GX	Arria II GX, Arria II GZ, Arria V, Cyclone III, Cyclone V, HardCopy III, HardCopy IV, Stratix III, Stratix IV, Stratix V, and newer devices
Single-port RAM	All registered input ports can be affected except for the following ports and conditions: <ul style="list-style-type: none"> wren port for M512 data/wren/address ports for MRAM (byteena port can be affected) LCs are implemented ⁽¹⁾ 	All registered input ports are not affected. ⁽¹⁾	All registered input ports are not affected. ⁽¹⁾
Single dual-port RAM and True dual-port RAM	All input registered ports can be affected except for MRAM.	All registered input ports are not affected.	Only registered input read address port can be affected.
Single-port ROM	Registered address input port can be affected.	All registered input ports are not affected.	Registered input address port can be affected.
Dual-port ROM	Registered address input port can be affected.	All registered input ports are not affected.	All registered input ports are not affected.

Note to Table 3-6:

(1) When LCs are implemented in this memory mode, registered output port is not affected.



During a read operation, clearing the input read address asynchronously corrupts the memory contents. The same effect applies to a write operation if the write address is cleared.



Beginning from Arria V, Cyclone V, and Stratix V devices onwards, an output clock signal is needed to successfully recover the output latch from an asynchronous clear signal. This implies that in a single clock mode true dual-port RAM, setting clock enabled on the registered output may affect the recovery of the unregistered output because they share the same output clock signal. To avoid this, provide an output clock signal (with clock enabled) to the output latch to deassert an asynchronous clear signal from the output latch.

Read Enable

Support for the read enable feature depends on the target device, memory block type, and the memory mode you select. [Table 3-7](#) lists the memory configurations for various device families that support the read enable feature.

Table 3-7. Read-Enable Support in Various Device Families

Memory Modes	Arria II GX, Cyclone III, HardCopy III, Stratix III and newer devices		Other Cyclone and Stratix Devices	
	M9K, M144K, M10K, M20K	MLAB	M512, M4K	M-RAM
Single-port RAM	✓	—	—	—
Simple dual-port RAM	✓	—	✓	—
True dual-port RAM	✓	—	—	—
Tri-port RAM	✓	—	✓	—
Single-port ROM	✓	—	—	—
Dual-port ROM	✓	—	—	—

If you create the read-enable port and perform a write operation (with the read enable port deasserted), the data output port retains the previous values that are held during the most recent active read enable. If you activate the read enable during a write operation, or if you do not create a read-enable signal, the output port shows the new data being written, the old data at that address, or a “Don't Care” value when read-during-write occurs at the same address location.



For more information about the read-during-write output behavior, refer to the [“Read-During-Write”](#) on page 3-16.

Read-During-Write

The read-during-write (RDW) occurs when a read and a write target the same memory location at the same time. The RDW operates in the following two ways:

- Same-port
- Mixed-port

Same-Port RDW

The same-port RDW occurs when the input and output of the same port access the same address location with the same clock.

The same-port RDW has the following output choices:

- **New Data**—New data is available on the rising edge of the same clock cycle on which it was written.
- **Old Data**—The RAM outputs reflect the old data at that address before the write operation proceeds.



Old Data is not supported for M10K and M20K memory blocks in single-port RAM and true dual-port RAM.

- **Don't Care**—The RAM outputs “don't care” values for the RDW operation.

Mixed-Port RDW

The mixed-port RDW occurs when one port reads and another port writes to the same address location with the same clock.

The mixed-port RDW has the following output choices:

- **Old Data**—The RAM outputs reflect the old data at that address before the write operation proceeds.



Old Data is supported for single clock configuration only.

- **Don't Care**—The RAM outputs “don't care” or “unknown” values for RDW operation without analyzing the timing path.



For LUTRAM, this option functions differently whereby when you enable this option, the RAM outputs “don't care” or “unknown” values for RDW operation but analyzes the timing path to prevent metastability. Therefore, if you want the RAM to output “don't care” values without analyzing the timing path, you have to turn on the **Do not analyze the timing between write and read operation. Metastability issues are prevented by never writing and reading at the same address at the same time** option.

Selecting RDW Output Choices for Various Memory Blocks

The available output choices for the RDW behavior vary, depending on the types of RDW and internal memory block in use.

Table 3–8 lists the available output choices for the same-port, and mixed-port RDW for various internal memory blocks.

Table 3–8. Output Choices for the Same-Port and Mixed-Port Read-During-Write

Memory Block Types	Single-port RAM ⁽¹⁾	Simple dual-port RAM ⁽²⁾	True dual-port RAM	
	Same port RDW	Mixed-port RDW	Same port RDW ⁽³⁾	Mixed-port RDW ⁽⁴⁾
M512	No parameter editor ⁽⁵⁾	Old Data Don't Care	NA	
M4K			No parameter editor ⁽⁵⁾	Old Data Don't Care
M-RAM		Don't Care		Don't Care
MLAB	Don't Care	Old Data Don't Care	NA MLAB is not supported in true dual-port RAM	
M9K	Don't Care New Data ⁽⁶⁾ Old Data	Old Data Don't Care	New Data ⁽⁶⁾ Old Data	Old Data Don't Care
M144K				
M10K	New Data ⁽⁶⁾ Don't Care			
M20K	Old Data Don't Care			
LCs	No parameter editor ⁽⁵⁾	Old Data Don't Care	NA	

Notes to Table 3–8:

- (1) Single-port RAM only supports same-port RDW, and the clocking mode must be either single clock mode, or input/output clock mode.
- (2) Simple dual-port RAM only supports mixed-port RDW, and the clocking mode must be either single clock mode, or input/output clock mode.
- (3) The clocking mode must be either single clock mode, input/output clock mode, or independent clock mode.
- (4) The clocking mode must be either single clock mode, or input/output clock mode.
- (5) There is no option page available from the parameter editor in this mode. By default, the new data flows through to the output.
- (6) There are two types of new data behavior for same-port RDW that you can choose from the parameter editor. When byte enable is applied, you can choose to read old data, or 'X' on the masked byte. The respective parameter values are:
 - **NEW_DATA_WITH_NBE_READ** for old data on masked byte.
 - **NEW_DATA_NO_NBE_READ** for x on masked byte.



The RDW old data mode is not supported when the Error Correction Code (ECC) is engaged.



If you are not concerned about the output when RDW occurs and would like to improve performance, you can select **Don't Care**. Selecting **Don't Care** increases the flexibility in the type of memory block being used, provided you do not assign block type when you instantiate the memory block.

Power-Up Conditions and Memory Initialization

Power-up conditions depend on the type of internal memory blocks in use and whether or not the output port is registered.

Table 3–9 lists the power-up conditions in the various types of internal memory blocks.

Table 3–9. Power-Up Conditions for Various internal Memory Blocks

internal Memory Blocks	Power-Up Conditions
M512	Outputs cleared
M4K	Outputs cleared
M-RAM	Outputs cleared if registered, otherwise unknown
MLAB	Outputs cleared if registered, otherwise reads memory contents
M9K	Outputs cleared
M144K	Outputs cleared
M10K	Outputs cleared
M20K	Outputs cleared

The outputs of M512, M4K, M9K, M144K, M10K, and M20K blocks always power-up to zero, regardless of whether the output registers are used or bypassed. Even if a memory initialization file is used to pre-load the contents of the memory block, the output is still cleared.

MLAB and M-RAM blocks power-up to zero only if output registers are used. If output registers are not used, MLAB blocks power-up to read the memory contents while M-RAM blocks power-up to an unknown state.



When the memory block type is set to **Auto** in the parameter editor, the compiler is free to choose any memory block type, in which the power-up value depends on the chosen memory block type. To identify the type of memory block the software selects to implement your memory, refer to the fitter report after compilation.

All memory blocks (excluding M-RAM) support memory initialization via the Memory Initialization File (**.mif**) or Hexadecimal (Intel-format) file (**.hex**). You can include the files using the parameter editor when you configure and build your RAM. For RAM, besides using the **.mif** file or the **.hex** file, you can initialize the memory to zero or 'X'. To initialize the memory to zero, select **No, leave it blank**. To initialize the content to 'X', turn on **Initialize memory content data to XX..X on power-up in simulation**. Turning on this option does not change the power-up behavior of the RAM but initializes the content to 'X'. For example, if your target memory block is M4K, the output is cleared during power-up (based on Table 3–9 on page 3–18). The content that is initialized to 'X' is shown only when you perform the read operation.



The Quartus II software searches for the altsyncram `init_file` in the project directory, the project db directory, user libraries, and the current source file location.

Error Correction Code

Error correction code (ECC) allows you to detect and correct data errors at the output of the memory. The Stratix III and Stratix IV M144K memory blocks have built-in ECC support of up to x64-wide simple dual-port mode while the Stratix V M20K memory blocks have built-in ECC support of x32-wide simple dual-port mode. The ECC in Stratix III and IV can perform single-error-correction double-error detection (SECCDED), in which it can detect and fix a single-bit error or detect two-bit errors (without fixing). The Stratix V ECC feature can perform single error correction, double adjacent error correction, and triple adjacent error detection, in which it can detect and fix a single bit error event or a double adjacent error event, or detect three adjacent errors without fixing the errors. However, the Stratix V ECC feature cannot detect four or more errors.

The ECC feature is not supported in the following conditions:

- mixed-width port feature is used
- byte-enable feature is engaged



The Mixed-port RDW for old data mode is not supported when the ECC feature is engaged. The result for RDW is **Don't Care**.

The M144K ECC status is communicated via a three-bit status flag `eccstatus[2..0]`, while the M20K ECC status is communicated with a two-bit ECC status flag `eccstatus[1..0]` where `eccstatus[1]` corresponds to the signal `e` (error) and `eccstatus[0]` corresponds to the signal `ue` (uncorrectable error).

Table 3-10 lists the truth table for the ECC status flags.

Table 3-10. Truth Table for ECC Status Flags

Status	M144K	M20K	
	eccstatus[2..0]	eccstatus[1..0]	
		eccstatus[1] e	eccstatus[0] ue
No error	000	0	0
Single error and fixed	011	—	—
Double error and no fix	101	—	—
Illegal	001	0	1
	010		
	100		
	11X		
A correctable error occurred and the error has been corrected at the outputs; however, the memory array has not been updated.	—	1	0
An uncorrectable error occurred and uncorrectable data appears at the output.	—	1	1



You can also use the ALTECC_ENCODER and the ALTECC_DECODER megafunctions to implement the ECC external to your memory blocks. For more information, refer to the *Integer Arithmetic Megafunctions User Guide*.

ALTSYNCRAM and ALTDPRAM Megafunction Ports

Table 3–11 lists the input and output ports for the ALTSYNCRAM megafunction.

Table 3–11. ALTSYNCRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
data_a	Input	Optional	Data input to port A of the memory. The data_a port is required if the operation_mode is set to any of the following values: <ul style="list-style-type: none"> ■ SINGLE_PORT ■ DUAL_PORT ■ BIDIR_DUAL_PORT
address_a	Input	Yes	Address input to port A of the memory. The address_a port is required for all operation modes.
wren_a	Input	Optional	Write enable input for address_a port. The wren_a port is required if the operation_mode is set to any of the following values: <ul style="list-style-type: none"> ■ SINGLE_PORT ■ DUAL_PORT ■ BIDIR_DUAL_PORT
rden_a	Input	Optional	Read enable input for address_a port. The rden_a port is supported depending on your selected memory mode and memory block. For more information about the read enable feature, refer to “Read Enable” on page 3–15.
byteena_a	Input	Optional	Byte enable input to mask the data_a port so that only specific bytes, nibbles, or bits of the data are written. The byteena_a port is not supported in the following conditions: <ul style="list-style-type: none"> ■ If implement_in_les parameter is set to ON ■ If operation_mode parameter is set to ROM For more information about byte enable feature and the criterion that you must follow to use the feature correctly, refer to “Byte Enable” on page 3–13.
addressstall_a	Input	Optional	Address clock enable input to hold the previous address of address_a port for as long as the addressstall_a port is high. For more information about address clock enable feature, refer to “Address Clock Enable” on page 3–12.

Table 3–11. ALTSYNCRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
q_a	Output	Yes	<p>Data output from port A of the memory.</p> <p>The q_a port is required if the operation_mode parameter is set to any of the following values:</p> <ul style="list-style-type: none"> ■ SINGLE_PORT ■ BIDIR_DUAL_PORT ■ ROM <p>The width of q_a port must be equal to the width of data_a port.</p>
data_b	Input	Optional	<p>Data input to port B of the memory.</p> <p>The data_b port is required if the operation_mode parameter is set to BIDIR_DUAL_PORT.</p>
address_b	Input	Optional	<p>Address input to port B of the memory.</p> <p>The address_b port is required if the operation_mode parameter is set to the following values:</p> <ul style="list-style-type: none"> ■ DUAL_PORT ■ BIDIR_DUAL_PORT
wren_b	Input	Yes	<p>Write enable input for address_b port.</p> <p>The wren_b port is required if operation_mode is set to BIDIR_DUAL_PORT.</p>
rden_b	Input	Optional	<p>Read enable input for address_b port.</p> <p>The rden_b port is supported depending on your selected memory mode and memory block</p> <p>For more information about the read enable feature, refer to “Read Enable” on page 3–15.</p>
byteena_b	Input	Optional	<p>Byte enable input to mask the data_b port so that only specific bytes, nibbles, or bits of the data are written.</p> <p>The byteena_b port is not supported in the following conditions:</p> <ul style="list-style-type: none"> ■ If implement_in_les parameter is set to ON ■ If operation_mode parameter is set to SINGLE_PORT, DUAL_PORT, or ROM <p>For more information about byte enable feature and the criterion that you must follow to use the feature correctly, refer to “Byte Enable” on page 3–13.</p>
addressstall_b	Input	Optional	<p>Address clock enable input to hold the previous address of address_b port for as long as the addressstall_b port is high.</p> <p>For more information about address clock enable feature, refer to “Address Clock Enable” on page 3–12.</p>
q_b	Output	Yes	<p>Data output from port B of the memory.</p> <p>The q_b port is required if the operation_mode is set to the following values:</p> <ul style="list-style-type: none"> ■ DUAL_PORT ■ BIDIR_DUAL_PORT <p>The width of q_b port must be equal to the width of data_b port.</p>

Table 3–11. ALTSYNCRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description										
clock0	Input	Yes	The following table describes which of your memory clock must be connected to the clock0 port, and port synchronization in different clocking modes:										
			<table><tr><th>Clocking Mode</th><th>Descriptions</th></tr><tr><td>Single clock</td><td>Connect your single source clock to clock0 port. All registered ports are synchronized by the same source clock.</td></tr><tr><td>Read/Write</td><td>Connect your write clock to clock0 port. All registered ports related to write operation, such as data_a port, address_a port, wren_a port, and byteena_a port are synchronized by the write clock.</td></tr><tr><td>Input Output</td><td>Connect your input clock to clock0 port. All registered input ports are synchronized by the input clock.</td></tr><tr><td>Independent clock</td><td>Connect your port A clock to clock0 port. All registered input and output ports of port A are synchronized by the port A clock</td></tr></table>	Clocking Mode	Descriptions	Single clock	Connect your single source clock to clock0 port. All registered ports are synchronized by the same source clock.	Read/Write	Connect your write clock to clock0 port. All registered ports related to write operation, such as data_a port, address_a port, wren_a port, and byteena_a port are synchronized by the write clock.	Input Output	Connect your input clock to clock0 port. All registered input ports are synchronized by the input clock.	Independent clock	Connect your port A clock to clock0 port. All registered input and output ports of port A are synchronized by the port A clock
			Clocking Mode	Descriptions									
			Single clock	Connect your single source clock to clock0 port. All registered ports are synchronized by the same source clock.									
			Read/Write	Connect your write clock to clock0 port. All registered ports related to write operation, such as data_a port, address_a port, wren_a port, and byteena_a port are synchronized by the write clock.									
			Input Output	Connect your input clock to clock0 port. All registered input ports are synchronized by the input clock.									
Independent clock	Connect your port A clock to clock0 port. All registered input and output ports of port A are synchronized by the port A clock												

Table 3–11. ALTSYNCRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description										
clock1	Input	Optional	The following table describes which of your memory clock must be connected to the clock1 port, and port synchronization in different clocking modes:										
			<table><tr><th>Clocking Mode</th><th>Descriptions</th></tr><tr><td>Single clock</td><td>Not applicable. All registered ports are synchronized by clock0 port.</td></tr><tr><td>Read/Write</td><td>Connect your read clock to clock1 port. All registered ports related to read operation, such as address_b port, rden_b port, and q_b port are synchronized by the read clock.</td></tr><tr><td>Input Output</td><td>Connect your output clock to clock1 port. All the registered output ports are synchronized by the output clock.</td></tr><tr><td>Independent clock</td><td>Connect your port B clock to clock1 port. All registered input and output ports of port B are synchronized by the port B clock.</td></tr></table>	Clocking Mode	Descriptions	Single clock	Not applicable. All registered ports are synchronized by clock0 port.	Read/Write	Connect your read clock to clock1 port. All registered ports related to read operation, such as address_b port, rden_b port, and q_b port are synchronized by the read clock.	Input Output	Connect your output clock to clock1 port. All the registered output ports are synchronized by the output clock.	Independent clock	Connect your port B clock to clock1 port. All registered input and output ports of port B are synchronized by the port B clock.
			Clocking Mode	Descriptions									
			Single clock	Not applicable. All registered ports are synchronized by clock0 port.									
			Read/Write	Connect your read clock to clock1 port. All registered ports related to read operation, such as address_b port, rden_b port, and q_b port are synchronized by the read clock.									
			Input Output	Connect your output clock to clock1 port. All the registered output ports are synchronized by the output clock.									
Independent clock	Connect your port B clock to clock1 port. All registered input and output ports of port B are synchronized by the port B clock.												
clocken0	Input	Optional	Clock enable input for clock0 port.										
clocken1	Input	Optional	Clock enable input for clock1 port.										
clocken2	Input	Optional	Clock enable input for clock0 port.										
clocken3	Input	Optional	Clock enable input for clock1 port.										

Table 3–11. ALTSYNCRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
aclr0 aclr1	Input	Optional	<p>Asynchronously clear the registered input and output ports. The <code>aclr0</code> port affects the registered ports that are clocked by <code>clock0</code> clock, while the <code>aclr1</code> port affects the registered ports that are clocked by <code>clock1</code> clock.</p> <p>The asynchronous clear effect on the registered ports can be controlled through their corresponding asynchronous clear parameter, such as <code>outdata_aclr_a</code>, <code>address_aclr_a</code>, and so on.</p> <p>For more information about the asynchronous clear parameters, refer to “Asynchronous Clear” on page 3–14.</p>
eccstatus	Output	Optional	<p>A 3-bit wide error correction status port. Indicate whether the data that is read from the memory has an error in single-bit with correction, fatal error with no correction, or no error bit occurs.</p> <p>In Stratix V devices, the M20K ECC status is communicated with two-bit wide error correction status port. The M20K ECC detects and fixes a single bit error event or a double adjacent error event, or detects three adjacent errors without fixing the errors.</p> <p>The <code>eccstatus</code> port is supported if all the following conditions are met:</p> <ul style="list-style-type: none"> ■ <code>operation_mode</code> parameter is set to <code>DUAL_PORT</code> ■ <code>ram_block_type</code> parameter is set to <code>M144K</code> or <code>M20K</code> ■ <code>width_a</code> and <code>width_b</code> parameter have the same value ■ Byte enable is not used <p>For more information about the ECC features, restrictions, and the output status definitions, refer to “Error Correction Code” on page 3–19.</p>

Table 3–12 lists the input and output ports for the ALTDPRAM megafunction.

Table 3–12. ALTDPRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
data	Input	Yes	<p>Data input to the memory.</p> <p>The <code>data</code> port is required and the width must be equal to the width of the <code>q</code> port.</p>
wraddress	Input	Yes	<p>Write address input to the memory.</p> <p>The <code>wraddress</code> port is required and must be equal to the width of the <code>raddress</code> port.</p>
wren	Input	Yes	<p>Write enable input for <code>wraddress</code> port.</p> <p>The <code>wren</code> port is required.</p>
raddress	Input	Yes	<p>Read address input to the memory.</p> <p>The <code>raddress</code> port is required and must be equal to the width of <code>wraddress</code> port.</p>

Table 3–12. ALTDPRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
<code>rden</code>	Input	Optional	<p>Read enable input for <code>rdaddress</code> port.</p> <p>The <code>rden</code> port is supported when the <code>use_eab</code> parameter is set to <code>OFF</code>. The <code>rden</code> port is not supported when the <code>ram_block_type</code> parameter is set to <code>MLAB</code>.</p> <p>Instantiate the ALTSYNCRAM megafunction if you want to use read enable feature with other memory blocks.</p>
<code>byteena</code>	Input	Optional	<p>Byte enable input to mask the <code>data</code> port so that only specific bytes, nibbles, or bits of data are written. The <code>byteena</code> port is not supported when <code>use_eab</code> parameter is set to <code>OFF</code>. It is supported in Arria II GX, Stratix III, Cyclone III, and newer devices with the <code>ram_block_type</code> parameter set to <code>MLAB</code>.</p> <p>For more information about byte enable feature and the criterion that you must follow to use the feature correctly, refer to “Byte Enable” on page 3–13.</p>
<code>wraddressstall</code>	Input	Optional	<p>Write address clock enable input to hold the previous write address of <code>wraddress</code> port for as long as the <code>wraddressstall</code> port is high.</p> <p>For more information about address clock enable feature, refer to “Address Clock Enable” on page 3–12.</p>
<code>rdaddressstall</code>	Input	Optional	<p>Read address clock enable input to hold the previous read address of <code>rdaddress</code> port for as long as the <code>wraddressstall</code> port is high.</p> <p>The <code>rdaddressstall</code> port is only supported in Stratix II, Cyclone II, Arria GX, and newer devices except when the <code>rdaddress_reg</code> parameter is set to <code>UNREGISTERED</code>.</p> <p>For more information about address clock enable feature, refer to “Address Clock Enable” on page 3–12.</p>
<code>q</code>	Output	Yes	<p>Data output from the memory.</p> <p>The <code>q</code> port is required, and must be equal to the width <code>data</code> port.</p>

Table 3–12. ALTDPRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description								
inclock	Input	Yes	<div>The following table describes which of your memory clock must be connected to the inclock port, and port synchronization in different clocking modes:</div> <table><tr><th>Clocking Mode</th><th>Descriptions</th></tr><tr><td>Single clock</td><td>Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.</td></tr><tr><td>Read/Write</td><td>Connect your write clock to inclock port. All registered ports related to write operation, such as data port, wraddress port, wren port, and byteena port are synchronized by the write clock.</td></tr><tr><td>Input/Output</td><td>Connect your input clock to inclock port. All registered input ports are synchronized by the input clock.</td></tr></table>	Clocking Mode	Descriptions	Single clock	Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.	Read/Write	Connect your write clock to inclock port. All registered ports related to write operation, such as data port, wraddress port, wren port, and byteena port are synchronized by the write clock.	Input/Output	Connect your input clock to inclock port. All registered input ports are synchronized by the input clock.
Clocking Mode	Descriptions										
Single clock	Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.										
Read/Write	Connect your write clock to inclock port. All registered ports related to write operation, such as data port, wraddress port, wren port, and byteena port are synchronized by the write clock.										
Input/Output	Connect your input clock to inclock port. All registered input ports are synchronized by the input clock.										
outclock	Input	Yes	<div>The following table describes which of your memory clock must be connected to the outclock port, and port synchronization in different clocking modes:</div> <table><tr><th>Clocking Mode</th><th>Descriptions</th></tr><tr><td>Single clock</td><td>Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.</td></tr><tr><td>Read/Write</td><td>Connect your read clock to outclock port. All registered ports related to read operation, such as rdaddress port, rdren port, and q port are synchronized by the read clock.</td></tr><tr><td>Input/Output</td><td>Connect your output clock to outclock port. The registered q port is synchronized by the output clock.</td></tr></table>	Clocking Mode	Descriptions	Single clock	Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.	Read/Write	Connect your read clock to outclock port. All registered ports related to read operation, such as rdaddress port, rdren port, and q port are synchronized by the read clock.	Input/Output	Connect your output clock to outclock port. The registered q port is synchronized by the output clock.
Clocking Mode	Descriptions										
Single clock	Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock.										
Read/Write	Connect your read clock to outclock port. All registered ports related to read operation, such as rdaddress port, rdren port, and q port are synchronized by the read clock.										
Input/Output	Connect your output clock to outclock port. The registered q port is synchronized by the output clock.										
inclocken	Input	Optional	Clock enable input for inclock port.								

Table 3–12. ALTDPRAM Megafunction Input and Output Ports Description

Port Name	Type	Required	Description
outclocken	Input	Optional	Clock enable input for outclock port.
aclr	Input	Optional	Asynchronously clear the registered input and output ports. The asynchronous clear effect on the registered ports can be controlled through their corresponding asynchronous clear parameter, such as <code>indata_aclr</code> , <code>wraddress_aclr</code> , and so on. For more information about the asynchronous clear parameters, refer to “Asynchronous Clear” on page 3–14 .

This section describes the design example provided with this user guide. You can download design examples from the following locations:

- On the [Quartus II Development Software Literature](#) page, in the **Using Megafunctions** section under **Memory Compiler**
- On the [Literature: User Guides](#) webpage, with this user guide

The following design files can be found in **Internal_Memory_DesignExample.zip**:

- **ecc_encoder.v**
- **ecc_decoder.v**
- **true_dp_ram.v**
- **top_dpam.v**
- **true_dp_ram.vt**
- **true_dp.do**
- **true_dp.qar** (Quartus II design file)

Simulate the designs using the ModelSim®-Altera software to generate a waveform display of the device behavior. For more information about the ModelSim-Altera software, refer to the [ModelSim-Altera Software Support](#) page on the Altera website. The support page includes links to such topics as installation, usage, and troubleshooting.

External ECC Implementation with True-Dual-Port RAM

The ECC features are only supported internally in simple dual-port RAM by Stratix III and Stratix IV devices when the M144K is implemented or by Stratix V when the M20K is implemented. Therefore, this design example describes how ECC features can be implemented in other RAM modes, regardless of the type of device memory block you use. It also demonstrates the features of the same-port and mixed-port read-during-write behaviors.

This design example uses a true dual-port RAM and illustrates how the ECC feature can be implemented external to the RAM. The ALTECC_ENCODER and ALTECC_DECODER megafunctions are required as the ALTECC_ENCODER megafunction encodes the data input before writing the data into the RAM, while the ALTECC_DECODER megafunction decodes the data output from the RAM before transferring the data out to other parts of the logic.

In this design example, the raw data width is 8 bits and is encoded by the ALTECC_ENCODER megafunction block to produce a 13-bit width data that is written into the true dual-port RAM when write-enable signal is asserted. Because the RAM mode has two dedicated write ports, another encoder is implemented for the other RAM input port.

Two ALTECC_DECODER megafunction blocks are also implemented at each of the data output ports of the RAM. When the read-enable signal is asserted, the encoded data is read from the RAM address and decoded by the ALTECC_DECODER megafunction blocks, respectively. The decoder shows the status of the data as no error detected, single-bit error detected and corrected, or fatal error (more than 1-bit error).

This example also includes a "corrupt zero bit" control signal at port A of the RAM. When the signal is asserted, it changes the state of the zero-bit (LSB) encoded data before it is written into the RAM. This signal is used to corrupt the zero-bit data storing through port A, and examines the effect of the ECC features.



This design example describes how ECC features can be implemented with the RAM for cases in which the ECC is not supported internally by the RAM. However, the design examples might not represent the optimized design or implementation.

Generating the ALTECC_ENCODER and ALTECC_DECODER Megafunctions with Dual-Port-RAM

To generate the ALTECC_ENCODER and ALTECC_DECODER megafunctions with the dual-port-RAM, follow these steps:

1. Open the **Internal_Memory_DesignExample.zip** file and extract **true_dp.qar**.
2. In the Quartus II software, open the **true_dp.qar** file and restore the archive file into your working directory.
3. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 of the MegaWizard Plug-In Manager appears.
4. Select **Create a new custom megafunction variation**.
5. Click **Next**. Page 2a of the MegaWizard Plug-In Manager appears.
6. In the MegaWizard Plug-In Manager pages, select or verify the configuration settings shown in [Table 4-1](#). Click **Next** to advance from one page to the next.

Table 4-1. Configuration Settings for the ALTECC_ENCODER Megafunction

MegaWizard Plug-In Manager Page	Option	Value
3	Currently selected device family:	Stratix III
	How do you want to configure this module?	Configure this module as an ECC encoder
	How wide should the data be?	8 bits
	Do you want to pipeline the functions?	Yes, I want an output latency of 1 clock cycle
	Create an 'aclr' asynchronous clear port	Not selected
	Create a 'clocken' clock enable clock	Not selected

7. Click **Finish**. The **ecc_encoder.v** module is built.
8. Repeat steps 3 to 5.

9. In the MegaWizard Plug-In Manager pages, select or verify the configuration settings shown in [Table 4-1](#). Click **Next** to advance from one page to the next.

Table 4-2. Configuration Settings for the ALTECC_DECODER Megafunction

MegaWizard Plug-In Manager Page	Option	Value
3	Currently selected device family:	Stratix III
	How do you want to configure this module?	Configure this module as an ECC decoder
	How wide should the data be?	13 bits
	Do you want to pipeline the functions?	Yes, I want an output latency of 1 clock cycle
	Create an 'aclr' asynchronous clear port	Not selected
	Create a 'clocken' clock enable clock	Not selected

10. Click **Finish**. The `ecc_decoder.v` module is built.



For more information about the options available from the ALTECC MegaWizard Plug-In Manager, refer to *Integer Arithmetic Megafunctions User Guide*.

11. Repeat steps 3 to 5.
12. In the MegaWizard Plug-In Manager pages, select or verify the configuration settings shown in [Table 4-1](#). Click **Next** to advance from one page to the next.

Table 4-3. Configuration Settings for the RAM:2-Port Megafunction (Part 1 of 2)

MegaWizard Plug-In Manager Page	Option	Value
2a	Megafunction	Under the Memory Compiler category, select RAM:2-Port
	Which device family will you be using?	Stratix IV
	Which type of output file do you want to create?	Verilog HDL
	What name do you want for the output file?	true_dp_ram
	Return to this page for another create operation	Turned off
Parameter Settings (General)	Currently selected device family:	Stratix III
	How will you be using the dual port ram?	With two read/write ports
	How do you want to specify the memory size?	As a number of words
Parameter Settings (Widths/Blk Type)	How many 8-bit words of memory?	16
	Use different data widths on different ports	Not selected
	How wide should the 'q_a' output bus be?	13
	What should the memory block type be?	M9K
	Set the maximum block depth to	Auto

Table 4-3. Configuration Settings for the RAM:2-Port Megafunction (Part 2 of 2)

MegaWizard Plug-In Manager Page	Option	Value
Parameter Settings (Clks/Rd, Byte En)	Which clocking method do you want to use?	Single clock
	Create 'rden_a' and 'rden_b' read enable signals	Not selected
	Byte Enable Ports	Not selected
Parameter Settings (Regs/Clkens.Aclrs)	Which ports should be registered?	All write input ports and read output ports
	Create one clock enable signal for each signal	Not selected
	Create an 'aclr' asynchronous clear for the registered ports	Not selected
Parameter Settings (Output 1)	Mixed Port Read-During-Write for Single Input Clock RAM	Old memory contents appear
Parameter Settings (Output 2)	Port A Read-During-Write Option	New Data
	Port B Read-During-Write Option	Old Data
Parameter Settings (Mem Init)	Do you want to specify the initial content of the memory?	
EDA	Generate netlist	Turned off
Summary	Variation file (.vhd)	Turned on
	AHDL Include file (.inc)	Turned off
	VHDL component declaration file (.cmp)	Turned on
	Quartus II symbol file (.bsf)	Turned off
	Instantiation template file(.vhd)	Turned off

13. Click **Finish**. The **true_dp_ram.v** module is built.

The **top_dpram.v** is a design variation file that contains the top level file that instantiates two encoders, a true dual-port RAM, and two decoders. To simulate the design, a testbench, **true_dp_ram.vt**, is created for you to run in the ModelSim-Altera software.

Simulating the Design

To simulate the design in the ModelSim-Altera software, follow these steps:

1. Unzip the **Internal_Memory_DesignExample.zip** file to any working directory on your PC.
2. Start the ModelSim-Altera software.
3. On the File menu, click **Change Directory**.
4. Select the folder in which you unzipped the files.
5. Click **OK**
6. On the Tools menu, point to **TCL** and click **Execute Macro**. The **Execute Do File** dialog box appears.

7. Select the **true_dp.do** file and click **Open**. The **true_dp.do** file is a script file that automates all the necessary settings, compiles and simulates the design files, and displays the simulation waveform.
8. Verify the result shown in the **Waveform Viewer** window.

You can rearrange signals, remove signals, add signals, and change the radix by modifying the script in **true_dp.do** accordingly.

Simulation Results

The top-level block contains the input and output ports shown in [Table 4-4](#).

Table 4-4. Top-level Input and Output Ports Representations

Ports Name	Ports Type	Descriptions
clock	Input	System Clock for the encoders, RAM, and decoders.
corrupt_dataa_bit0	Input	Registered active high control signal that 'twist' the zero bit (LSB) of input encoded data at port A before writing into the RAM. ⁽¹⁾
address_a data_a wren_a rden_a	Input	Address input, data input, write enable, and read enable to port A of the RAM. ⁽¹⁾
address_b data_b wren_b rden_b	Input	Address input, data input, write enable, and read enable to port B of the RAM. ⁽¹⁾
rdata1 err_corrected1 err_detected1 err_fatal1	Output	Output data read from port A of the RAM, and the ECC-status signals reflecting the data read. ⁽²⁾
rdata2 err_corrected2 err_detected2 err_fatal2	Output	Output data read from port B of the RAM, and the ECC-status signals reflecting the data read. ⁽²⁾

Notes to Table 4-4:

- (1) For input ports, only data signal goes through the encoder; others bypass the encoder and go directly to the RAM block. Because the encoder uses one pipeline, signals that bypass the encoder require additional pipelines before going to the RAM. This has been implemented in the top level.
- (2) The encoder and decoder each use one pipeline while the RAM uses two pipelines, making the total pipeline equal to four. Therefore, read data is only shown at output ports four clock cycles after the read enable is initiated.

Figure 4-1 shows the expected simulation waveform results in the ModelSim-Altera software.

Figure 4-1. Simulation Results

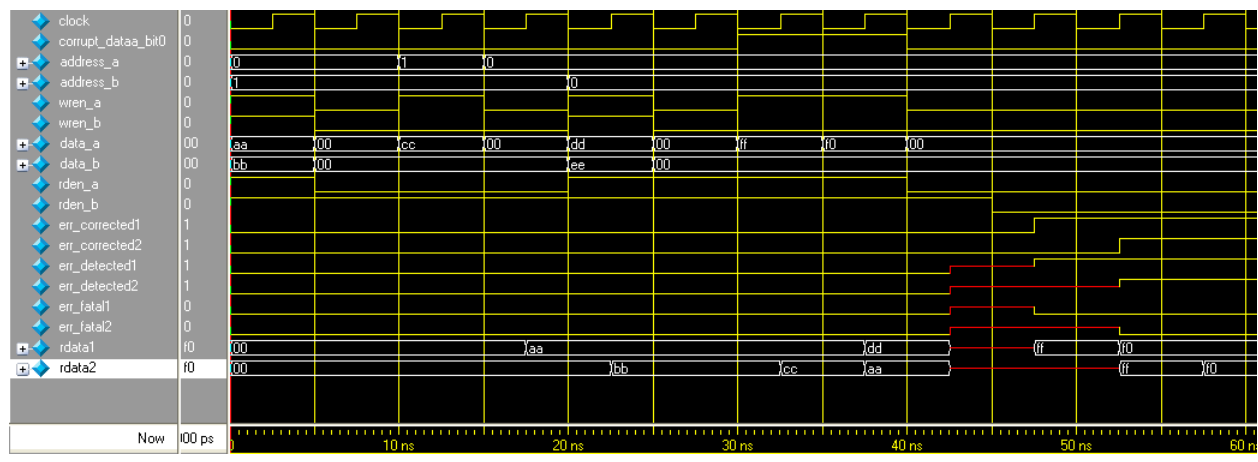


Figure 4-2 shows the timing diagram of when the same-port read-during-write occurs for each port A and port B of the RAM.

Figure 4-2. Same-Port Read-During-Write

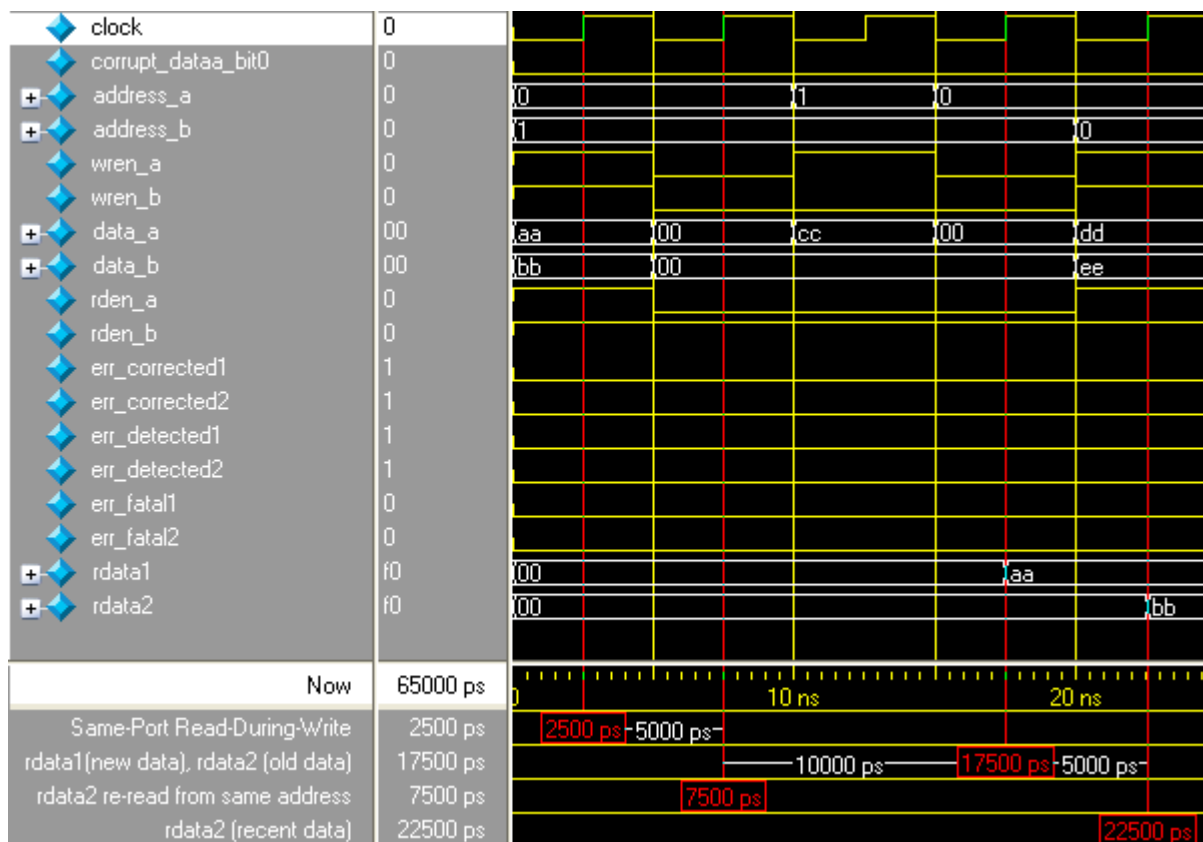
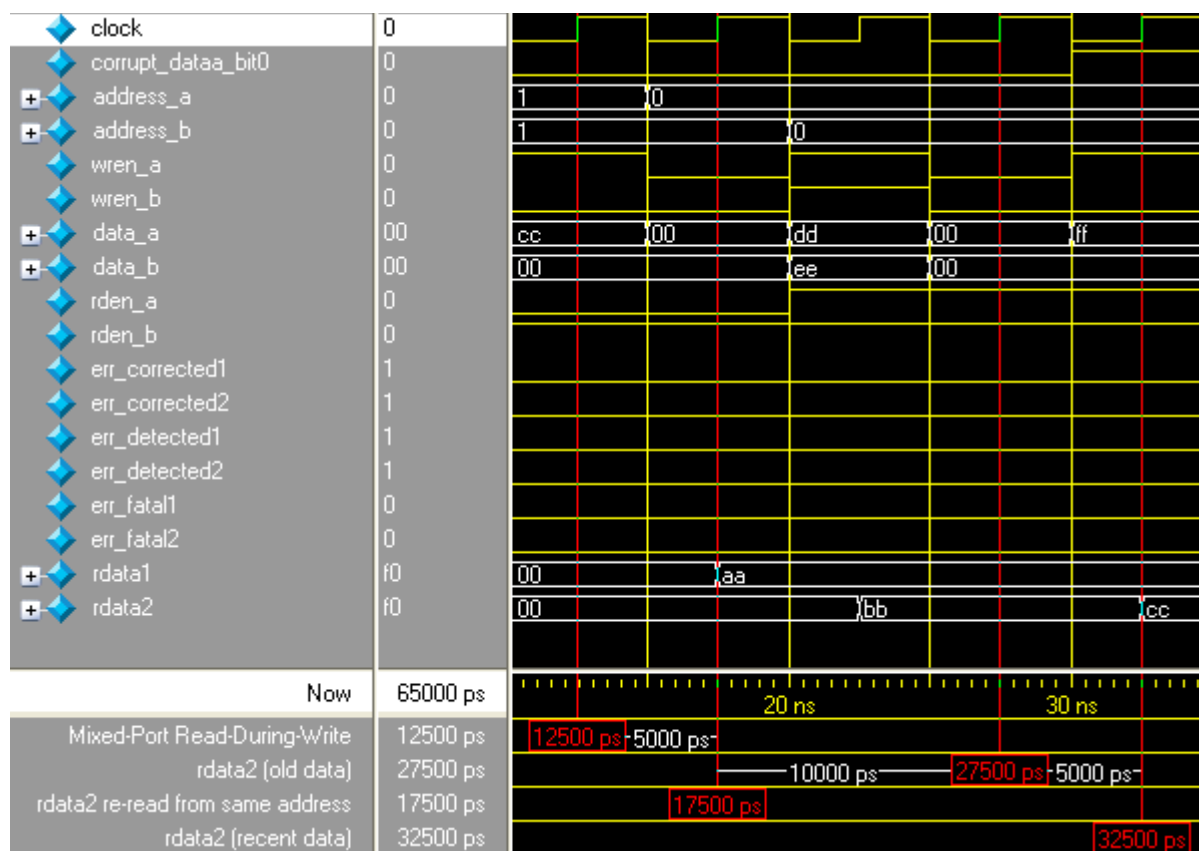


Figure 4-3 shows the timing diagram of when the mixed-port read-during-write occurs.

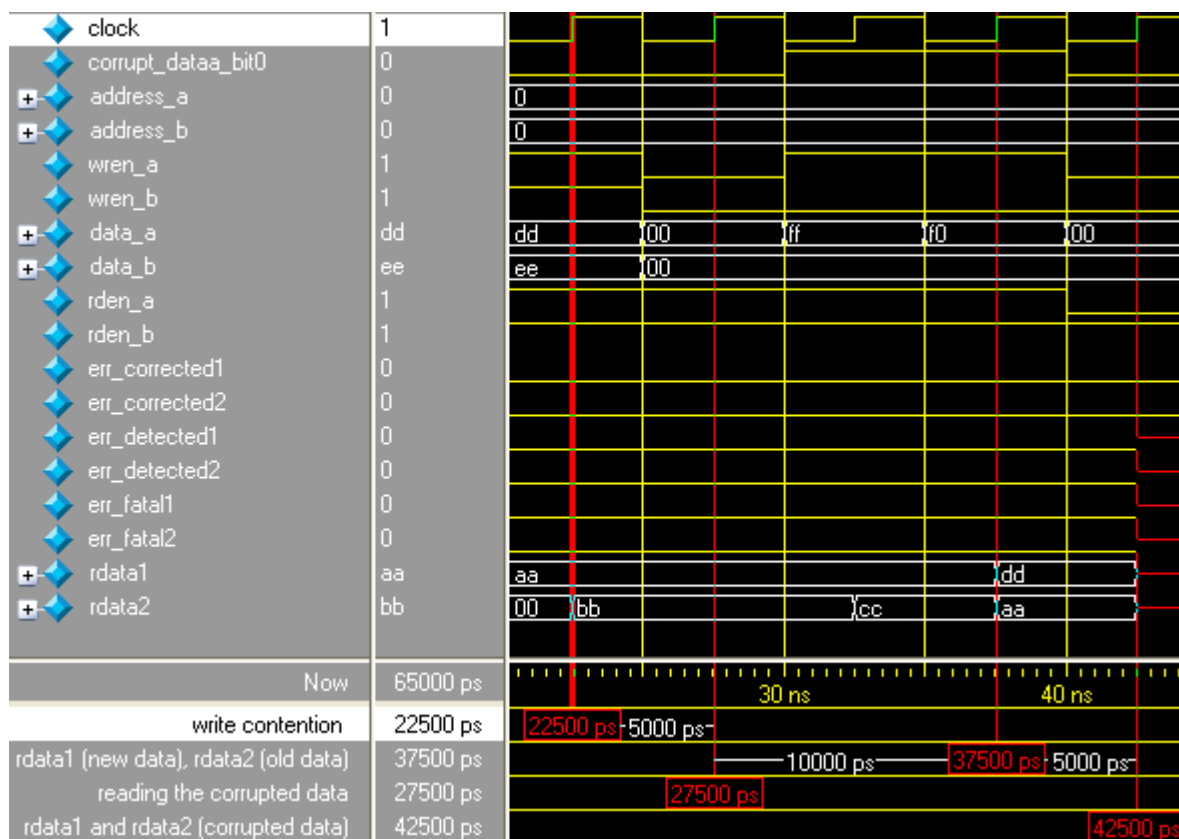
Figure 4–3. Mixed-Port Read-During-Write



At 12500 ps, mixed-port read-during-write occurs when data `cc` is both written to port A, and is reading from port B, simultaneously targeting the same address 1. Because the true dual-port RAM that is configured to mixed-port read-during-write is showing the old data, the `rdata2` port shows the old data `bb` after four clock cycles at 27500 ps. When the data is read again from the same address at the next rising clock edge at 17500 ps, the `rdata2` port shows the recent data `cc` at 32500 ps.

Figure 4-4 shows the timing diagram of when the write contention occurs.

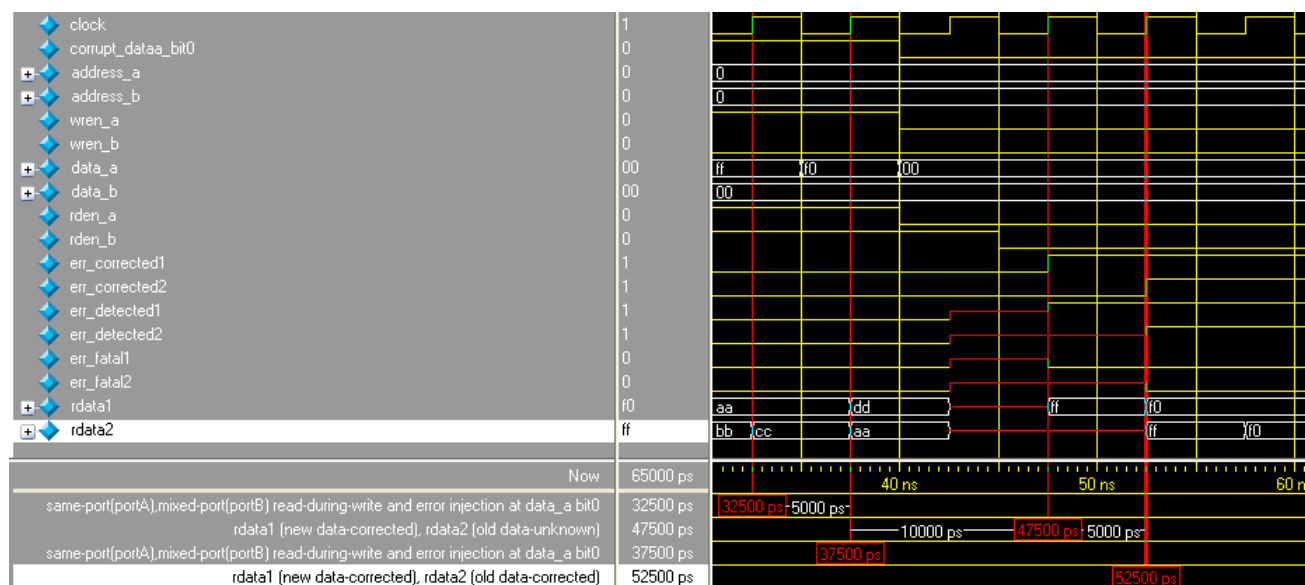
Figure 4-4. Write Contention




At 22500 ps, the write contention occurs when data dd and ee are written to address 0 simultaneously. Besides that, the same-port read-during-write also occurs for port A and port B. The setting for port A and port B for same-port read-during-write takes effect when the rdata1 port shows the new data dd and the rdata2 port shows the old data aa after four clock cycles at 37500 ps. When the data is read again from the same address at the next rising clock edge at 27500 ps, rdata1 and rdata2 ports show unknown values at 42500 ps. Apart from that, the unknown data input to the decoder also results in an unknown ECC status.

Figure 4-5 shows the timing diagram of the effect when an error is injected to twist the LSB of the encoded data at port A by asserting corrupt_dataa_bit0.

Figure 4-5. Error Injection– Asserting corrupt_dataa_bit0



At 32500 ps, same-port read-during-write occurs at port A while mixed-port read-during-write occurs at port B. The corrupt_dataa_bit0 is also asserted to corrupt the LSB of encoded data at port A; therefore, the storing data has the LSB corrupted, in which the intended data ff is corrupted, becomes fe, and stored at address 0. After four clock cycles at 47500 ps, the rdata1 port shows the new data ff that has been corrected by the decoder, and the ECC status signals, err_corrected1 and err_detected1, are asserted. For rdata2 port, old data (which is unknown) is shown and the ECC-status signal remains unknown.

 The decoders correct the single-bit error of the data shown at rdata1 and rdata2 ports only. The actual data stored at address 0 in the RAM remains corrupted, until new data is written.

At 37500 ps, the same condition happens to port A and port B. The difference is port B reads the corrupted old data fe from address 0. After four clock cycles at 52500 ps, the rdata2 port shows the old data ff that has been corrected by the decoder and the ECC status signals, err_corrected2 and err_detected2, are asserted to show the data has been corrected.

Document Revision History

Table 4–5 lists the revision history for this document.

Table 4–5. Document Revision History

Date	Version	Changes
November 2013	4.3	Updated Table 3–8 on page 3–17 to update M20K block information.
May 2013	4.2	Updated Table 3–4 on page 3–10 to fix a typographical error.
November 2012	4.1	<ul style="list-style-type: none"> ■ Added a note to the “Asynchronous Clear” on page 3–14 to state that internal contents cannot be cleared with the asynchronous clear signal. ■ Updated note in “Clocking Modes and Clock Enable” on page 3–10 to include Stratix V devices. ■ Added a note to the “Asynchronous Clear” on page 3–14 to clarify that clear deassertion on output latch is dependent on output clock.
January 2012	4.0	Added a note to Power-Up Conditions and Memory Initialization section.
November 2011	3.0	<ul style="list-style-type: none"> ■ Updated the RAM2:Port parameter settings. ■ Updated the Read-During-Write section. ■ Added M10K memory block information. ■ Added support information for Arria V and Cyclone V.
March 2011	2.0	Added new features for M20K memory block.
November 2009	1.0	Initial release