Migrating from the “B” to the New “D” DataFlash Family

Introduction

The new AT45DBxxxD family offers enhanced hardware and software features optimized for a wide variety of program code and data storage applications. The AT45DBxxxD family also utilizes an intelligent adaptive algorithm during erase and programming operations for superior endurance over the product’s lifetime. The “D” family DataFlash is offered in smaller form factor packages to dramatically reduce board real estate.

AT45DBxxxD Features

- **RapidS™ Serial Interface: 66 MHz Maximum Clock Frequency**
  - **SPI Compatible Modes 0 and 3**
- **JEDEC Standard Manufacturer and Device ID Read**
- **Security: 128-byte Security Register**
- **Software and Hardware Sector Protection**
  - **Individual Sectors can be protected**
- **Sector Lock Down**
  - **Individual sectors can be permanently locked**
- **One-time configurable page and buffer size**
- **TCSS time reduced to 5ns**
- **Deep power down - for power critical applications**
- **Sector Erase**
- **Chip Erase**
- **Endurance: 100,000 program/erase cycles per page (min)**
- **Packaging Options: 8-pin SOIC (narrow body), 8-pin SOIC (wide body), 8-CASON, 8-MLF, and 28-TSOP**

DataFlash®

Application Note

3644A–DFLASH–09/06

1. Command Sequences

1.1 Read Commands

The AT45DBxxx “D” family commands are fully backward compatible with the AT45DBxxx “B” family. For those customers using the legacy “inactive” modes, it is recommended to convert to the standard SPI commands. The inactive clock polarity high and low modes are referred to as legacy “inactive” modes. The legacy commands are supported in the “D” family to allow time for the system designers to make the necessary changes. These legacy commands will not be supported in our next generation products.

Table 1-1. Read Commands

Command	SCK Mode	“B” Family Opcode	“D” Family Opcode
Continuous Array Read (High Frequency = up to 66 MHz)	SPI Mode 0 or 3	N/A	0BH (new command)
Continuous Array Read (Low Frequency = up to 33 MHz)	SPI Mode 0 or 3	N/A	03H (new command)
Status Register Read	Inactive Clock Polarity Low or High[1]	57H	57H
JEDEC Standard Manufacturer and Device ID Read	SPI Mode 0 or 3	N/A	9FH

Note: 1. The 64M-bit density “D” version DataFlash does not support the legacy inactive modes.

2. New Features and Benefits

The “D” family features are fully independent, and individually selectable. The new features include JEDEC ID, individual sector protection, security register, permanent sector lockdown, sector erase, chip erase, deep power-down and “power of 2” binary page size option.

2.1 Manufacturer and Device ID Read

The “D” family supports the JEDEC standard for manufacturer and device ID read. The manufacturer and device ID may be used during the boot-load process to identify the device and select the appropriate device drivers. This feature is useful when system designers need to provide a different opcode to multiple memory devices on the board.

Table 2-1. Manufacturer and Device ID Read

Command	Opcode
Manufacturer and Device ID Read	9FH

2.2 Individual Sector Protection

Protecting the contents of a flash memory device has always been an important consideration. The “D” family features flexible sector protection, so that critical contents can be kept secure while unprotected sectors are programmed and erased.

The “D” family offers two protection methods, hardware and software controlled, for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{WP}$) pin. The selection of which sectors are to be protected or unprotected from program and erase operations is specified in the nonvolatile Sector Protection Register. The status of whether sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

Once sector protection is enabled by either method, the contents of the selected sector is protected and cannot be erased or programmed. Software sector protection is useful in applications in which the write protect ($\overline{WP}$) pin is not, or cannot be controlled by a host processor. The following command sequence is used to enable or to disable Sector Protection:

Table 2-2. Individual Sector Protection

Command	Byte1	Byte2	Byte3	Byte4
Enable Sector Protection	3DH	2AH	7FH	A9H
Disable Sector Protection	3DH	2AH	7FH	9AH

2.3 Sector Lockdown

The “D” family offers sector lockdown for secure code and data storage. The Lockdown mechanism allows each individual sector to be permanently locked so that it becomes read only. Once the sector is locked down, it can never be erased or programmed, and it can never be unlocked.

To issue the Sector Lockdown command, the chip select pin ($\overline{CS}$) must first be asserted as it would be for any other command. Once the $\overline{CS}$ has been asserted, the 4-byte opcode sequence must be clocked into the device in the correct order. After the last byte of command sequence has been clocked in, then three address bytes specifying any address within the sector to be locked down must be clocked into the device. After the last address bit has been clocked in, the $\overline{CS}$ must then be deasserted to initiate the internally self-timed lockdown sequence.

The lockdown sequence should take place in a maximum time of tp, during which time the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the lockdown sequence, then the lockdown status of the sector cannot be guaranted. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or byte and reissue the Sector Lockdown command if necessary.

Table 2-3. Sector Lockdown

Command	Byte1	Byte2	Byte3	Byte4
Enable Sector Lockdown	3DH	2AH	7FH	30H

2.4 Security Register

The “D” family devices contain a specialized register that can be used for security purposes in system design. The Security Register is a 128-byte one-time programmable (OTP) register that is divided into two sections. The first 64 bytes are user programmable. The remaining 64 bytes are factory programmed and will contain a unique number. The register is separate from the main array and is read and programmed using different commands in every device. Once the customer section of the security register is programmed, it will be permanently locked to prevent reprogramming. This means that once this section is programmed, it can never be altered. The security register can be used to store manufacturer serial numbers and/or a small encrypted security key for system authentication.

Table 2-4. Security Commands

Command	Opcode
Security Register Program	9AH+00H+00H+00H
Security Register Read	77H

2.5 Deep Power-Down

The Deep Power-down command allows the device to enter into the lowest power consumption mode. Once the device has entered the Deep Power-down mode, all instructions are ignored except for the Resume from Deep Power-down command.

Table 2-5. Deep Power-Down

Command	Opcode
Deep Power-down	B9H
Resume from Deep Power-down	ABH

2.6 "Power of 2" Binary Page Size Option

The "Power of 2" binary page size Configuration Register is a user-programmable nonvolatile register that allows the page size of the main memory to be configured for either binary page sizes (256/512/1024 bytes) or DataFlash standard page sizes (264/528/1056 bytes). The devices are initially shipped with the page size set to 264/528/1056 bytes. To change the page size to binary (256/512/1024 bytes), the "power of 2" page size command should be given. Once the device is configured for binary page size, it cannot be reconfigured again.

Table 2-6. "Power of 2" Page Size

Command	Byte1	Byte2	Byte3	Byte4
"Power of 2" page size	3DH	2AH	80H	A6H

2.7 Program and Erase Operations

The "D" family of devices utilizes an intelligent adaptive algorithm during the programming and the erase operations. The adaptive algorithm is used to provide superior endurance while minimizing the erase and the programming times. To optimize system performance, Atmel recommends the user poll the RDY/$\overline{\text{BUSY}}$ bit in the status instead of using fixed timing. In addition to page and block erase, "D" family offers additional erase granularity: Sector and Full Chip Erase.

2.8 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory.

Table 2-7. Sector Erase

Command	Opcode
Sector Erase	7CH

2.9 Chip Erase

Using the Chip Erase command can erase the entire main memory at one time.

Table 2-8. Chip Erase

Command	Opcode
Chip Erase	C7H+94H+80H+9AH

3. Design Considerations

The user needs to be aware of the following differences between the B and D versions of the AT45DBxxx family:

1. The erase and programming operations of the “D” family are internally self-timed. Therefore, it is recommended not to use a fixed timer for program and erase operations. In order to minimize the erase and programming times, the user should check the RDY/$\overline{\text{BUSY}}$ bit (bit 7) of the status register or the RDY/$\overline{\text{BUSY}}$ pin to determine the end of a program or an erase operation.
2. The “B” family supports three methods of polling the RDY/$\overline{\text{BUSY}}$ bit of the status register. The following are the three methods:
   a. The Status Register Read command (D7H) is issued each time the RDY/$\overline{\text{BUSY}}$ bit is polled.
   b. The Status Register Read command (D7H) is issued once, $\overline{\text{CS}}$ is held low and SCK is toggled continuously to update the RDY/$\overline{\text{BUSY}}$ status.
   c. The Status Register Read command (D7H) is issued once, $\overline{\text{CS}}$ is held low and SCK is stopped at a low level once the RDY/$\overline{\text{BUSY}}$ bit has been output. The RDY/BUSY status will continue to be output on the SO pin.

The “D” family is a fully synchronous design and requires the use of SCK each time the Ready/Busy status is checked using the Status Register Read command. The SCK must be toggled with $\overline{\text{CS}}$ held low in order to continuously poll the RDY/$\overline{\text{BUSY}}$ bit of the status register.

4. System Considerations

The RapidS serial interface is controlled by the clock SCK, serial input (SI) and chip select ($\overline{\text{CS}}$) pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash occurs during programming and erase operations. The regulator needs to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

5. Package Offerings

The following are the differences in the packaging offerings between the “B” and the “D” family devices:

Table 5-1. Package Offerings for 1M through 8M Densities

Package Type	1M		2M		4M		8M	
	45DB011B	45DB011D	45DB021B	45DB021D	45DB041B	45DB041D	45DB081B	45DB081D
8-CASON	N/A	N/A	Available	N/A	Available	N/A	Available	N/A
14-CBGA	Available	N/A	Available	N/A	Available	N/A	Available	N/A
8-MLF (narrow)	N/A	Available	N/A	Available	N/A	Available	N/A	Available
8-SOIC (narrow body)	N/A	Available	N/A	Available	N/A	Available	N/A	Available
8-SOIC (wide body)	Available	Available	Available	Available	Available	Available	N/A	Available
28-SOIC	N/A	N/A	Available	N/A	Available	N/A	Available	N/A
14-TSSOP	Available	N/A	N/A	N/A	N/A	N/A	N/A	N/A
28-TSOP	N/A	N/A	Available	N/A	Available	N/A	Available	N/A

Table 5-2. Package Offerings for 16M through 64M Densities

Package Type	16M		32M		64M	
	45DB161B	45DB161D	45DB321C	45DB321D	45DB642	45DB642D
8-CASON	Available	N/A	N/A	Available	N/A	Available
24-CBGA	Available	N/A	Available	N/A	N/A	N/A
44-CBGA	N/A	N/A	Available	N/A	N/A	N/A
8-MLF-N	N/A	N/A	N/A	Available	N/A	N/A
8-MLF-W	N/A	N/A	N/A	Available	N/A	N/A
8-SOIC (wide body)	N/A	Available	N/A	Q406	N/A	N/A
28-SOIC	Available	N/A	Available	N/A	N/A	N/A
28-TSOP	Available	Available	Available	Available	N/A	Available
40-TSOP	N/A	N/A	N/A	N/A	Available	N/A

6. DC Characteristics

The following are the differences in the DC Characteristics between the “B” and the “D” family devices:

Table 6-1. 1M Density

Symbol	Parameter	Parameter	AT45DB011B			AT45DB011D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		10	25		12	17	mA

Table 6-2. 2M Density

Symbol	Parameter	Parameter	AT45DB021B			AT45DB021D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35		12	17	mA

Table 6-3. 4M Density

Symbol	Parameter	Parameter	AT45DB041B			AT45DB041D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ =V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35		12	17	mA

Table 6-4. 8M Density

Symbol	Parameter	Parameter	AT45DB081B			AT45DB081D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35		12	17	mA

Table 6-5. 16M Density

Symbol	Parameter	Parameter	AT45DB161B			AT45DB161D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		9	15	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35		12	17	mA

Table 6-6. 32M Density

Symbol	Parameter	Parameter	AT45DB321C			AT45DB321D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		6	15		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	15		7	10	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		8	12	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	14	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		11	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		35	50		12	17	mA

Table 6-7. 64M Density

Symbol	Parameter	Parameter	AT45DB642			AT45DB642D			Units
			Min	Typ	Max	Min	Typ	Max	
I_{DP}	Deep Power-Down Current			N/A	N/A		5	10	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10		25	50	µA
I_{CC1}	Active Current, Read Operation	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10		N/A	N/A	mA
		f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	15	
		f = 50 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	15		N/A	N/A	
		f = 66 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		N/A	N/A		10	15	
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		20	35			25	mA

7. AC Characteristics

The following are the differences in the AC Characteristics between the “B” and the “D” family devices:

Table 7-1. 1M Density

Symbol	Parameter	AT45DB011B			AT45DB011D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			20			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time		120	200			400	µs
t_{COMP}	Page to Buffer Compare Time		120	200			400	µs
t_{EP}	Page Erase and Programming Time		10	20		14	35	ms
t_P	Page Programming Time		7	15		2	4	ms
t_{PE}	Page Erase Time		6	10		13	32	ms
t_{BE}	Block Erase Time		7	15		15	35	ms
t_{SE}	Sector Erase Time			N/A		0.8	2.5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-2. 2M Density

Symbol	Parameter	AT45DB021B			AT45DB021D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			20			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			250			400	µs
t_{COMP}	Page to Buffer Compare Time			250			400	µs
t_{EP}	Page Erase and Programming Time			20		14	35	ms
t_P	Page Programming Time			14		2	4	ms
t_{PE}	Page Erase Time			8		13	32	ms
t_{BE}	Block Erase Time			12		15	35	ms
t_{SE}	Sector Erase Time			N/A		0.8	2.5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-3. 4M Density

Symbol	Parameter	AT45DB041B			AT45DB041D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			20			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			250			400	µs
t_{COMP}	Page to Buffer Compare Time			250			400	µs
t_{EP}	Page Erase and Programming Time			20		14	35	ms
t_P	Page Programming Time			14		2	4	ms
t_{PE}	Page Erase Time			8		13	32	ms
t_{BE}	Block Erase Time			12		30	75	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-4. 8M Density

Symbol	Parameter	AT45DB081B			AT45DB081D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			20			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			250			400	µs
t_{COMP}	Page to Buffer Compare Time			250			400	µs
t_{EP}	Page Erase and Programming Time			20		17	40	ms
t_P	Page Programming Time			14		3	6	ms
t_{PE}	Page Erase Time			8		15	35	ms
t_{BE}	Block Erase Time			12		45	100	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-5. 16M Density

Symbol	Parameter	AT45DB081B			AT45DB081D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			20			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			250			400	µs
t_{COMP}	Page to Buffer Compare Time			250			400	µs
t_{EP}	Page Erase and Programming Time			20		17	40	ms
t_P	Page Programming Time			14		3	6	ms
t_{PE}	Page Erase Time			8		15	35	ms
t_{BE}	Block Erase Time			12		45	100	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-6. 32M Density

Symbol	Parameter	AT45DB321C			AT45DB321D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			40			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			40			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	100			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			350			400	µs
t_{COMP}	Page to Buffer Compare Time			350			400	µs
t_{EP}	Page Erase and Programming Time		16	50		17	40	ms
t_P	Page Programming Time		8	15		3	6	ms
t_{PE}	Page Erase Time		8	35		15	35	ms
t_{BE}	Block Erase Time		20	100		45	100	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s
t_{CE}	Chip Erase Time			N/A		TBD	TBD	s

Table 7-7. 64M Density - Serial/RapidS Interface

Symbol	Parameter	AT45DB642			AT45DB642D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			20			66	MHz
f_{SCK}	SCK Frequency for Continuous Read			15			66	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			700			400	µs
t_{COMP}	Page to Buffer Compare Time			700			400	µs
t_{EP}	Page Erase and Programming Time			20		17	40	ms
t_P	Page Programming Time			14		3	6	ms
t_{PE}	Page Erase Time			8		15	35	ms
t_{BE}	Block Erase Time			12		45	100	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s

Table 7-8. 64M Density - Rapid8™ 8-bit Interface

Symbol	Parameter	AT45DB642			AT45DB642D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			5			50	MHz
f_{SCK}	SCK Frequency for Continuous Read			3			50	MHz
t_{CSS}	$\overline{CS}$ Setup Time	250			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			5			ns
t_{XFR}	Page to Buffer Transfer Time			700			400	µs
t_{COMP}	Page to Buffer Compare Time			700			400	µs
t_{EP}	Page Erase and Programming Time			20		17	40	ms
t_P	Page Programming Time			14		3	6	ms
t_{PE}	Page Erase Time			8		15	35	ms
t_{BE}	Block Erase Time			12		45	100	ms
t_{SE}	Sector Erase Time			N/A		1.6	5	s

Conclusion

The “D” family DataFlash offers an easy migration path for designers and is available in smaller form factor packages. The “D” family is feature-rich, with a low pin count, and sequential access ideal for program code and data storage. There are no major software changes required in converting from the “B” family to the “D” family DataFlash devices.

In summary, the “D” family DataFlash devices deliver:

1. Fast Read Access
2. New Features
   - Security Register
   - Software and Hardware Sector Protection
   - Individual Sector Lockdown
   - JEDEC Standard Manufacturer and Device ID
3. Deep Power-Down for Power-Critical Applications
4. High Endurance
5. Superior Data Retention

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