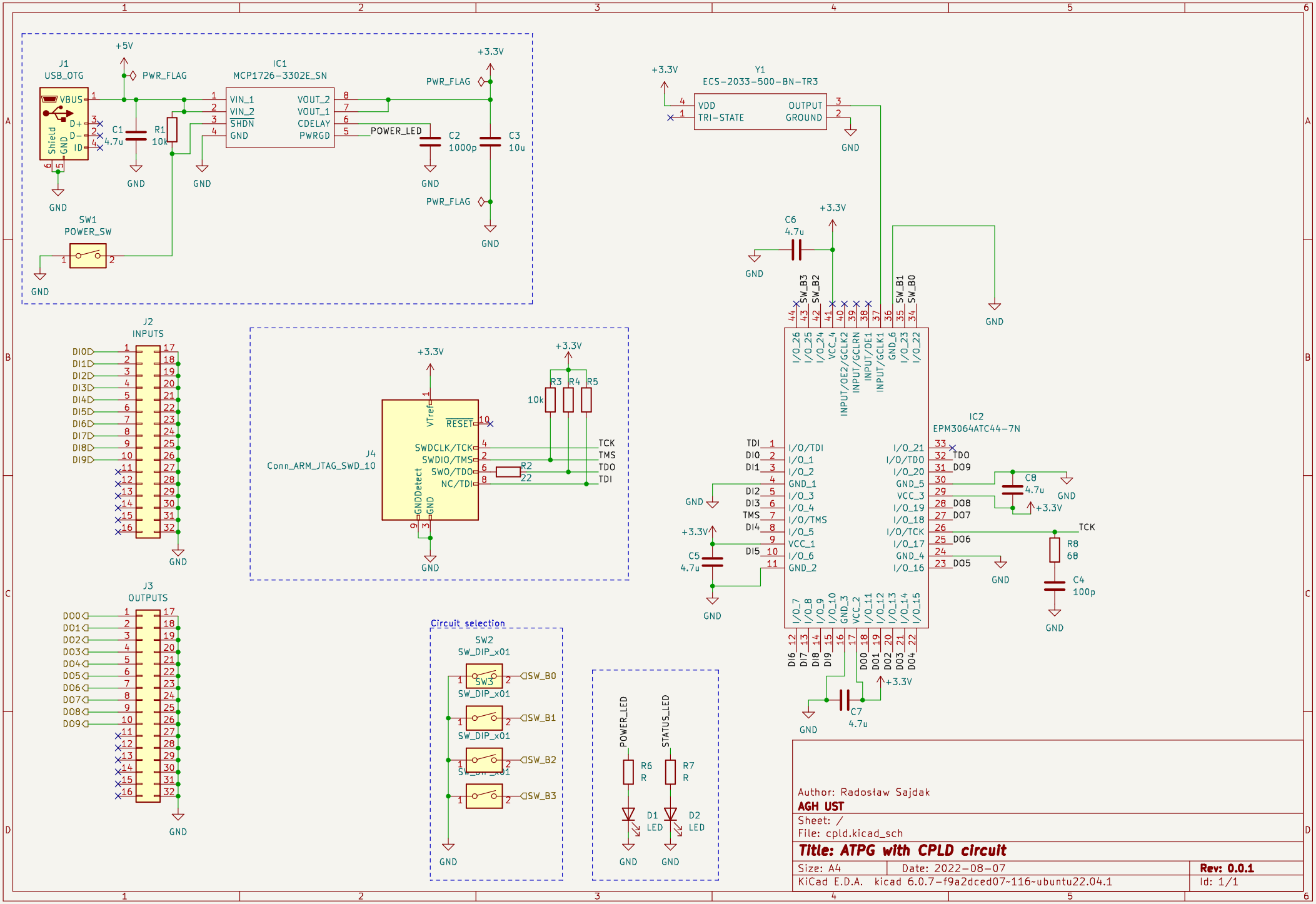
J1
USB_OTG
VBUS
D+
D-
ID
Shield
GND
+5V
PWR_FLAG
C1
4.7u
R1
10k
IC1
MCP1726-3302E_SN
VIN_1
VIN_2
SHDN
GND
VOUT_2
VOUT_1
CDELAY
PWRGD
POWER_LED
C2
1000p
C3
10u
+3.3V
SW1
POWER_SW
Y1
ECS-2033-500-BN-TR3
VDD
TRI-STATE
OUTPUT
GROUND
C6
4.7u
IC2
EPM3064ATC44-7N
I/O/TDI
I/O_1
I/O_2
GND_1
I/O_3
I/O_4
I/O/TMS
I/O_5
VCC_1
I/O_6
GND_2
I/O_21
I/O/TDO
I/O_20
GND_5
VCC_3
I/O_19
I/O_18
I/O/TCK
I/O_17
GND_4
I/O_16
I/O_26
I/O_25
I/O_24
VCC_4
INPUT/OE2/GCLK2
INPUT/GCLRN
INPUT/OE1
INPUT/GCLK1
GND_6
I/O_23
I/O_22
I/O_7
I/O_8
I/O_9
I/O_10
GND_3
VCC_2
I/O_11
I/O_12
I/O_13
I/O_14
I/O_15
SW_B3
SW_B2
SW_B1
SW_B0
TDI
DI0
DI1
DI2
DI3
TMS
DI4
DI5
DI6
DI7
DI8
DI9
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
DO9
TDO
TCK
C8
4.7u
R8
68
C4
100p
C5
4.7u
C7
4.7u
J2
INPUTS
J3
OUTPUTS
J4
Conn_ARM_JTAG_SWD_10
VTref
RESET
SWDCLK/TCK
SWDIO/TMS
SWO/TDO
NC/TDI
GNDDetect
R3
R4
R5
10k
R2
22
Circuit selection
SW2
SW_DIP_x01
SW3
SW_B0
SW_B1
SW_B2
SW_B3
POWER_LED
STATUS_LED
R6
R
R7
R
D1
LED
D2
LED
Author: Radosław Sajdak
AGH UST
Sheet: /
File: cpld.kicad_sch
Title: ATPG with CPLD circuit
Size: A4
Date: 2022-08-07
Rev: 0.0.1
KiCad E.D.A. kicad 6.0.7-f9a2dced07~116~ubuntu22.04.1
Id: 1/1