**Instruction Set Architecture**

* 2-op: IR shouldn’t start with “11”

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 4-bits: opcode | 3-bits src-mode | 3-bits src-reg | 3-bits dest-mode | 3-bits dest-reg |

* From IR0:IR3 -> opcode

|  |  |
| --- | --- |
| instruction | opcode |
| MOV | 0000 |
| ADD | 0001 |
| ADC | 0010 |
| SUB | 0011 |
| SBC | 0100 |
| AND | 0101 |
| OR | 0110 |
| XNOR | 0111 |
| CMP | 1000 |

* From IR4:IR6 -> src-mode code & From IR10:IR12 -> dest-mode code

|  |  |
| --- | --- |
| mode | code |
| REG-DIR | 000 |
| REG-INDIR | 001 |
| AUTOINC-DIR | 010 |
| AUTOINC-INDIR | 011 |
| AUTODEC-DIR | 100 |
| AUTODEC-INDIR | 101 |
| INDEXED-DIR | 110 |
| INDEXED-INDIR | 111 |

* From IR7:IR9 -> src-reg code & IR13:IR15 -> dest-reg code

|  |  |
| --- | --- |
| reg | code |
| R0 | 000 |
| R1 | 001 |
| R2 | 010 |
| R3 | 011 |
| R4 | 100 |
| R5 | 101 |
| R6 | 110 |
| R7 | 111 |

* 1-op: IR should start with “1110”

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1110 | 4-bits opcode | 3-bits dest-mode | 3-bits dest-reg | XX |

* From IR4:IR7 -> opcode

|  |  |
| --- | --- |
| instruction | opcode |
| INC | 0010 |
| DEC | 0011 |
| CLR | 0100 |
| INV | 0101 |
| LSR | 0110 |
| ROR | 0111 |
| RRC | 1000 |
| ASR | 1001 |
| LSL | 1010 |
| ROL | 1011 |
| RLC | 1100 |

* From IR8:IR10 -> dest-mode code

|  |  |
| --- | --- |
| mode | code |
| REG-DIR | 000 |
| REG-INDIR | 001 |
| AUTOINC-DIR | 010 |
| AUTOINC-INDIR | 011 |
| AUTODEC-DIR | 100 |
| AUTODEC-INDIR | 101 |
| INDEXED-DIR | 110 |
| INDEXED-INDIR | 111 |

* From IR11:IR13 -> dest-reg code

|  |  |
| --- | --- |
| reg | code |
| R0 | 000 |
| R1 | 001 |
| R2 | 010 |
| R3 | 011 |
| R4 | 100 |
| R5 | 101 |
| R6 | 110 |
| R7 | 111 |

* From IR14:IR15 -> Don’t Care
* Branch: IR should start with “110”

|  |  |  |
| --- | --- | --- |
| 110 | 3-bits opcode | 10 bits offset |

* From IR3:IR5 opcode

|  |  |
| --- | --- |
| instruction | opcode |
| BR | 000 |
| BEQ | 001 |
| BNE | 010 |
| BLO | 011 |
| BLS | 100 |
| BHI | 101 |
| BHS | 110 |

* No-op: IR should start with “11110”

|  |  |  |
| --- | --- | --- |
| 11110 | 1-bit opcode | XXXXXXXXXX |

* IR5 -> opcode

|  |  |
| --- | --- |
| instruction | opcode |
| HLT | 0 |
| NOP | 1 |

* From IR6:IR15 -> Don’t Care
* Jump Sub-Routine: IR should start with “11111”

|  |  |  |
| --- | --- | --- |
| 11111 | 2-bits opcode | XXXXXXXXX |

* From IR5:IR6 -> opcode

|  |  |
| --- | --- |
| instruction | opcode |
| JSR | 00 |
| RTS | 01 |
| INTERRUPT | 10 |
| IRET | 11 |

* From IR7:IR15 -> Don’t Care