|  |  |
| --- | --- |
| Reg direct | 2 |
| Auto inc direct | 4 |
| Auto dec direct | 4 |
| Indexed direct | 6 |
| Reg indirect | 4 |
| Auto inc indirect | 6 |
| Auto dec indirect | 6 |
| Indexed indirect | 8 |

**# of Clock Cycles**

**2-op instructions**

Fetch instruction = 2

Fetch src or dst:

Operation “2-op” = 2

Save in dst “2-op” = 1 --- except cmp = 0

End = 1

|  |  |  |
| --- | --- | --- |
| src | dst | Total number of clock cycles |
| Reg direct | Reg direct | 10 |
| Auto inc direct | 12 |
| Auto dec direct | 12 |
| Indexed direct | 14 |
| Reg indirect | 12 |
| Auto inc indirect | 14 |
| Auto dec indirect | 14 |
| Indexed indirect | 16 |
| Auto inc direct | Reg direct | 12 |
| Auto inc direct | 14 |
| Auto dec direct | 14 |
| Indexed direct | 16 |
| Reg indirect | 14 |
| Auto inc indirect | 16 |
| Auto dec indirect | 16 |
| Indexed indirect | 18 |
| Auto dec direct | Reg direct | 12 |
| Auto inc direct | 14 |
| Auto dec direct | 14 |
| Indexed direct | 16 |
| Reg indirect | 14 |
| Auto inc indirect | 16 |
| Auto dec indirect | 16 |
| Indexed indirect | 18 |
| Indexed direct | Reg direct | 14 |
| Auto inc direct | 16 |
| Auto dec direct | 16 |
| Indexed direct | 18 |
| Reg indirect | 16 |
| Auto inc indirect | 18 |
| Auto dec indirect | 18 |
| Indexed indirect | 20 |
| Reg indirect | Reg direct | 12 |
| Auto inc direct | 14 |
| Auto dec direct | 14 |
| Indexed direct | 16 |
| Reg indirect | 14 |
| Auto inc indirect | 16 |
| Auto dec indirect | 16 |
| Indexed indirect | 18 |
| Auto inc indirect | Reg direct | 14 |
| Auto inc direct | 16 |
| Auto dec direct | 16 |
| Indexed direct | 18 |
| Reg indirect | 16 |
| Auto inc indirect | 18 |
| Auto dec indirect | 18 |
| Indexed indirect | 20 |
| Auto dec indirect | Reg direct | 14 |
| Auto inc direct | 16 |
| Auto dec direct | 16 |
| Indexed direct | 18 |
| Reg indirect | 16 |
| Auto inc indirect | 18 |
| Auto dec indirect | 18 |
| Indexed indirect | 20 |
| Indexed indirect | Reg direct | 16 |
| Auto inc direct | 18 |
| Auto dec direct | 18 |
| Indexed direct | 20 |
| Reg indirect | 18 |
| Auto inc indirect | 20 |
| Auto dec indirect | 20 |
| Indexed indirect | 22 |

Total # of cycles for all instructions = 1024\*8 + 960 = 9152

Total # of instructions = 9\*64 = 576

**1-op instructions**

Fetch instruction = 2

Fetch dst:

|  |  |
| --- | --- |
| Reg direct | 2 |
| Auto inc direct | 4 |
| Auto dec direct | 4 |
| Indexed direct | 6 |
| Reg indirect | 4 |
| Auto inc indirect | 6 |
| Auto dec indirect | 6 |
| Indexed indirect | 8 |

Operation “1-op” = 2

Save in dst “1-op” = 1

End = 1

Total # of clock cycles:

|  |  |
| --- | --- |
| Reg direct | 8 |
| Auto inc direct | 10 |
| Auto dec direct | 10 |
| Indexed direct | 12 |
| Reg indirect | 10 |
| Auto inc indirect | 12 |
| Auto dec indirect | 12 |
| Indexed indirect | 14 |

Total # of cycles for all instructions = 88\*8 = 704

Total # of instructions = 11\*8 = 88

**Branching**

Fetch instruction = 2

Operation = 3

End = 1

Total # of clock cycles = 6

Total # of cycles for all instructions = 6\*7 = 42

Total # of instructions = 7

**No-op**

Fetch instruction = 2

End = 1

Total # of clock cycles = 3

Total # of cycles for all instructions = 3\*2 = 6

Total # of instructions = 2

CPI = (9152+704+42+6)/(576+88+7+2) = 14.72

**# of memory access**

**2-op instructions**

Fetch instruction = 1

Fetch src or dst:

|  |  |
| --- | --- |
| Reg direct | 0 |
| Auto inc direct | 1 |
| Auto dec direct | 1 |
| Indexed direct | 2 |
| Reg indirect | 1 |
| Auto inc indirect | 2 |
| Auto dec indirect | 2 |
| Indexed indirect | 3 |

Save in dst “2-op” = 1 --- register direct and cmp= 0

|  |  |  |
| --- | --- | --- |
| dst | src | Total number of clock cycles |
| Reg direct | Reg direct | 1 |
| Auto inc direct | 2 |
| Auto dec direct | 2 |
| Indexed direct | 3 |
| Reg indirect | 2 |
| Auto inc indirect | 3 |
| Auto dec indirect | 3 |
| Indexed indirect | 4 |
| Auto inc direct | Reg direct | 3 |
| Auto inc direct | 4 |
| Auto dec direct | 4 |
| Indexed direct | 5 |
| Reg indirect | 4 |
| Auto inc indirect | 5 |
| Auto dec indirect | 5 |
| Indexed indirect | 6 |
| Auto dec direct | Reg direct | 3 |
| Auto inc direct | 4 |
| Auto dec direct | 4 |
| Indexed direct | 5 |
| Reg indirect | 4 |
| Auto inc indirect | 5 |
| Auto dec indirect | 5 |
| Indexed indirect | 6 |
| Indexed direct | Reg direct | 4 |
| Auto inc direct | 5 |
| Auto dec direct | 5 |
| Indexed direct | 6 |
| Reg indirect | 5 |
| Auto inc indirect | 6 |
| Auto dec indirect | 6 |
| Indexed indirect | 7 |
| Reg indirect | Reg direct | 3 |
| Auto inc direct | 4 |
| Auto dec direct | 4 |
| Indexed direct | 5 |
| Reg indirect | 4 |
| Auto inc indirect | 5 |
| Auto dec indirect | 5 |
| Indexed indirect | 6 |
| Auto inc indirect | Reg direct | 4 |
| Auto inc direct | 5 |
| Auto dec direct | 5 |
| Indexed direct | 6 |
| Reg indirect | 5 |
| Auto inc indirect | 6 |
| Auto dec indirect | 6 |
| Indexed indirect | 7 |
| Auto dec indirect | Reg direct | 4 |
| Auto inc direct | 5 |
| Auto dec direct | 5 |
| Indexed direct | 6 |
| Reg indirect | 5 |
| Auto inc indirect | 6 |
| Auto dec indirect | 6 |
| Indexed indirect | 7 |
| Indexed indirect | Reg direct | 5 |
| Auto inc direct | 6 |
| Auto dec direct | 6 |
| Indexed direct | 7 |
| Reg indirect | 6 |
| Auto inc indirect | 7 |
| Auto dec indirect | 7 |
| Indexed indirect | 8 |

**1-op instructions**

Fetch instruction = 1

Fetch dst & save:

|  |  |
| --- | --- |
| Reg direct | 0 |
| Auto inc direct | 2 |
| Auto dec direct | 2 |
| Indexed direct | 3 |
| Reg indirect | 2 |
| Auto inc indirect | 3 |
| Auto dec indirect | 3 |
| Indexed indirect | 4 |

Total:

|  |  |
| --- | --- |
| Reg direct | 1 |
| Auto inc direct | 3 |
| Auto dec direct | 3 |
| Indexed direct | 4 |
| Reg indirect | 3 |
| Auto inc indirect | 4 |
| Auto dec indirect | 4 |
| Indexed indirect | 5 |

**Branching**

Fetch instruction = 1

Total = 1

**No-op**

Fetch instruction = 1

Total = 1