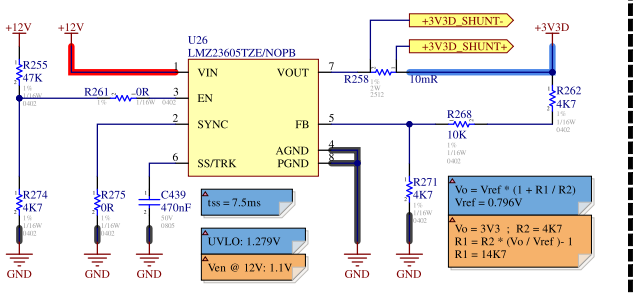
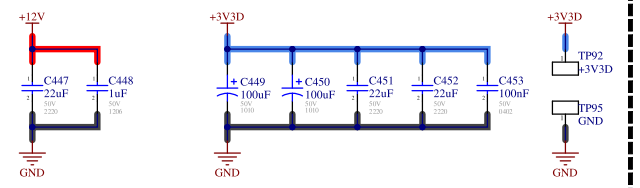
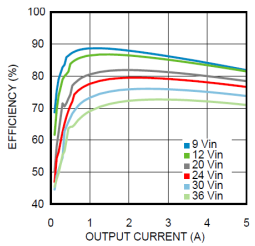
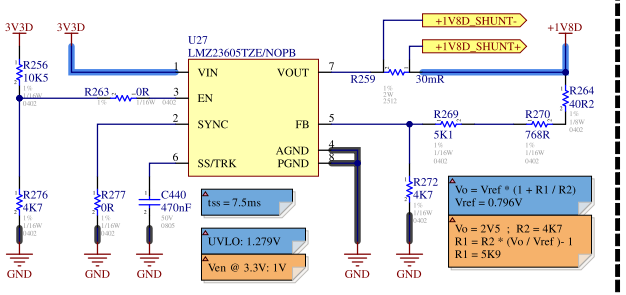
+3V3D

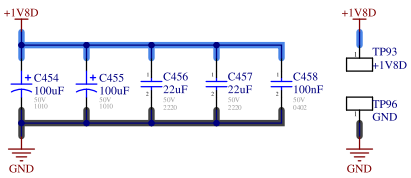


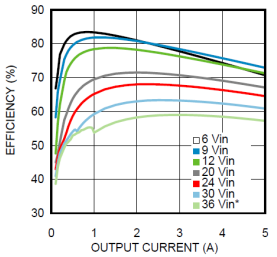




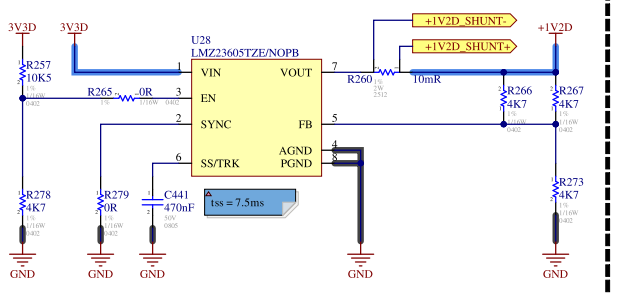
+1V8D

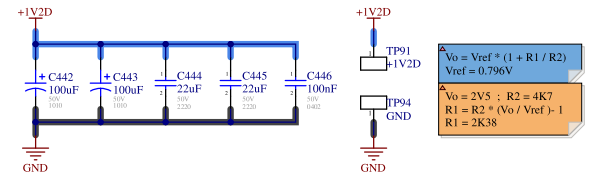


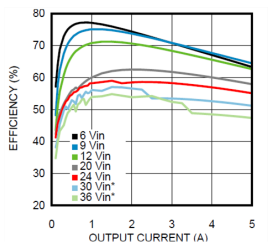




+1V2D







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The Spartan-6 FPGA can be powered up and powered down in any sequence. Because the three FPGA supply inputs must be valid to release the POR and can be supplied in any order, there is no FPGA-specific voltage sequencing requirement.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Speed Grade	Ramp Time	Units
V_{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V_{CCO2} (1)	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V_{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

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VCCINT: 3A @ 1V2D
VCCAUX: 250mA @ 3V3D
VCCIO: 6x 100mA @ 3V3D

6.405W

Sheet Name: POWER		
Project Title: PLEIADES		
Global Project: UdeS_S7_APP1		
Size: 11x17	Group: Group 1	Revision: A
Date	Sheet: 20 of 22	
Filename: POWER_FPGA.SchDoc	Designers: lacp3102, Pascal-Emmanuel Lachance, bilf0901, Frédéric Bilodeau	