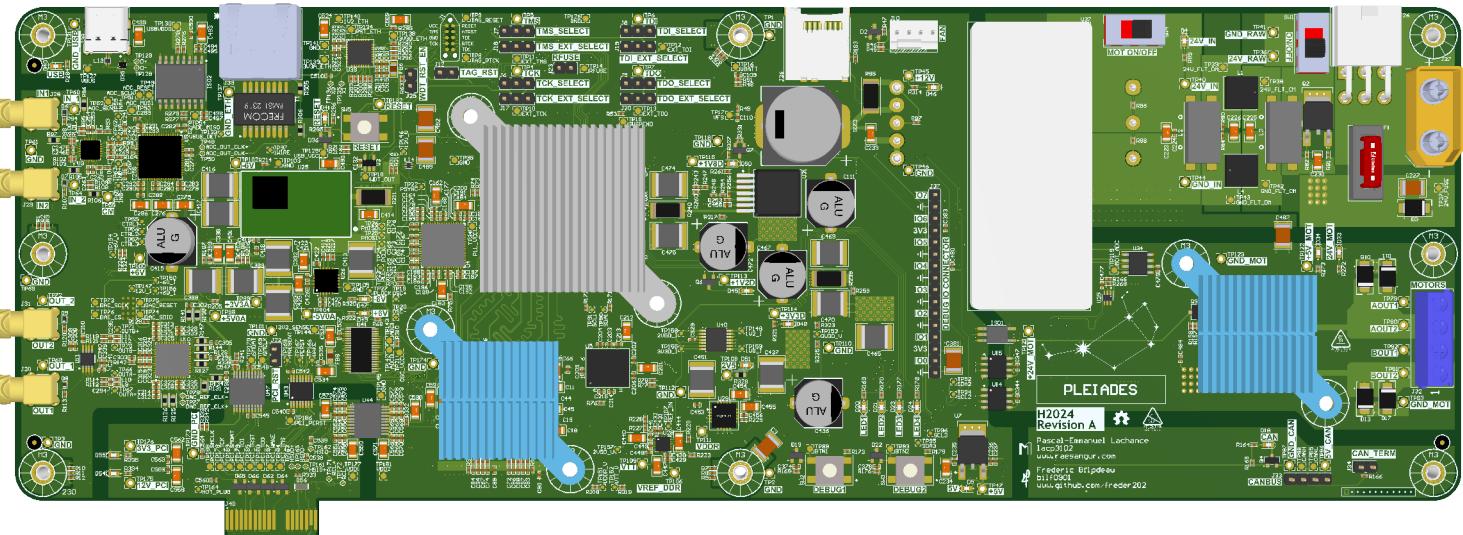


PLEIADES

LACP3102 - Pascal-Emmanuel Lachance
BILF0901 - Frédéric Bilodeau

Realistic View



Realistic View

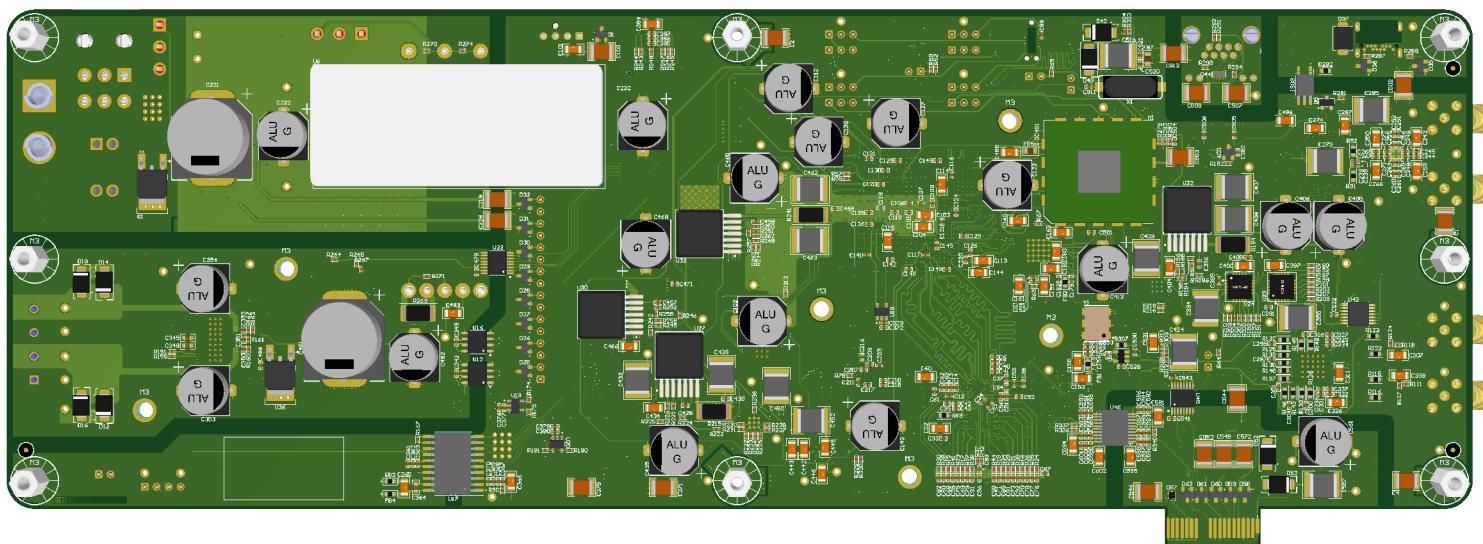
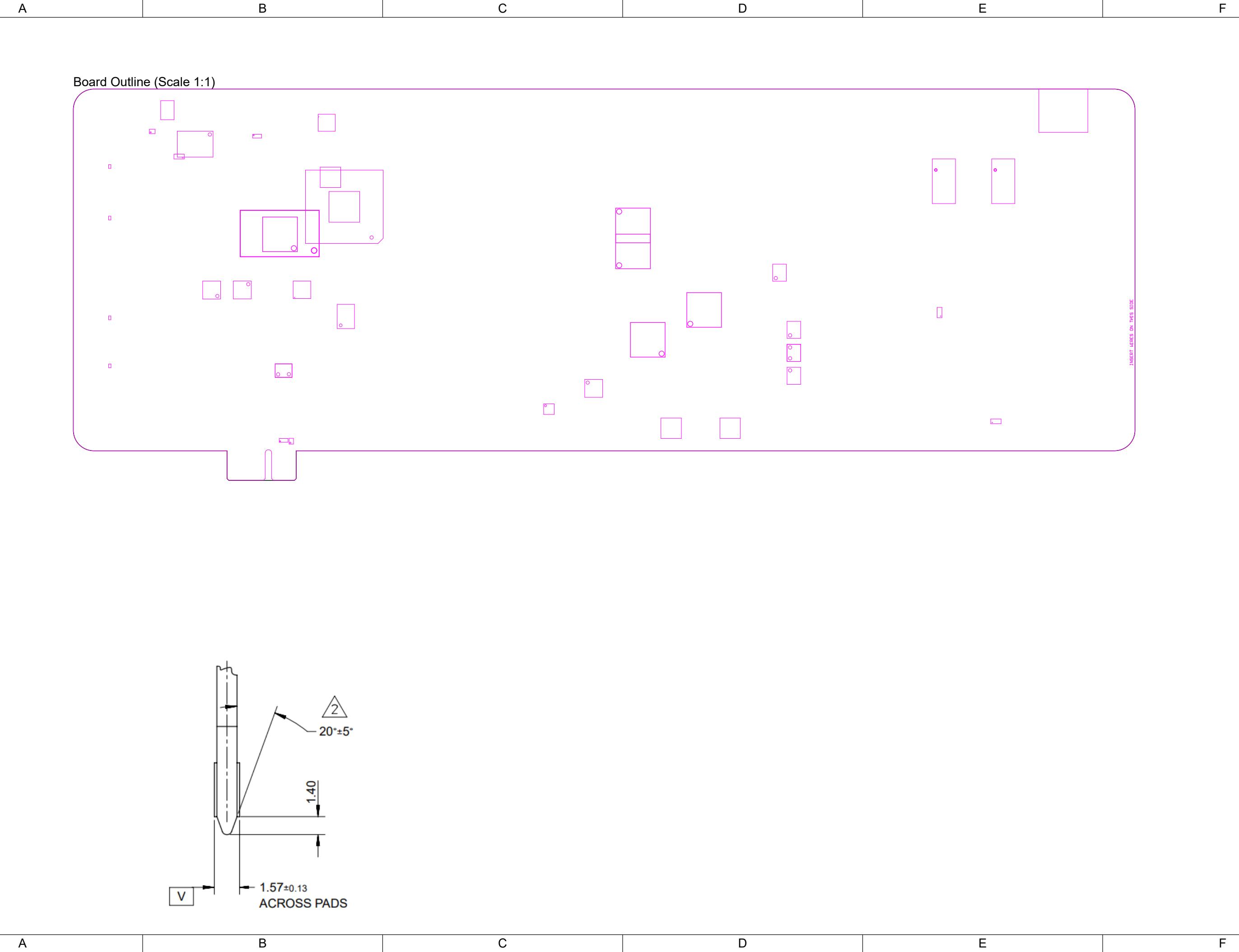


TABLE OF CONTENT

PAGE	TITLE	DESCRIPTION
1	TITLE	COVER PAGE
2	STACKUP	VIEW OF LAYER STACK DIMENSIONS AND MATERIALS
3	IMPEDANCES	DIMENSIONS FOR ALL REQUIRED IMPEDANCES
4	DIMENSIONS	PCB DIMENSIONS
5	ASSEMBLY VIEW	VIEW OF ALL FACES
6	PCB PRINTS	TOP VIEW OF ALL LAYERS
7	DRILL	DRILL DRAWING & DRILL TABLE

A	B	C	D	E	F
1	Layer Stack Legend				1
	Material	Layer	Thickness	Dielectric Material	Type
	Surface Material	Top Overlay			Gerber
1	CF-004	Top Solder	0.40mil(0.010mm)	Solder Resist	Legend GTO
	Prepreg	TOP	1.38mil(0.035mm)	ISO106/1080	Solder Mask GTS
	CF-004	GND1	3.15mil(0.080mm)	ISO106/1080	Signal GTL
	Core		0.69mil(0.018mm)		Dielectric
	CF-004	IN1	7.00mil(0.178mm)	S1170G	Signal G1
	Prepreg				Dielectric
	CF-004	GND2	3.15mil(0.080mm)	ISO106/1080	Signal G2
	Core		0.69mil(0.018mm)		Dielectric
2	CF-004	POW1	7.00mil(0.178mm)	S1170G	Signal G3
	Prepreg				Dielectric
	CF-004	GND3	3.15mil(0.080mm)	ISO106/1080	Signal G4
	Core		0.69mil(0.018mm)		Dielectric
	CF-004	POW2	7.00mil(0.178mm)	S1170G	Signal G5
	Prepreg				Dielectric
	CF-004	GND4	3.15mil(0.080mm)	ISO106/1080	Signal G6
	Core		0.69mil(0.018mm)		Dielectric
3	CF-004	GND5	7.00mil(0.178mm)	S1170G	Signal G7
	Prepreg				Dielectric
	CF-004	IN2	3.15mil(0.080mm)	ISO106/1080	Signal G8
	Core		0.69mil(0.018mm)		Dielectric
	CF-004	GND6	7.00mil(0.178mm)	S1170G	Signal G9
	Prepreg				Dielectric
	CF-004	BOT	3.15mil(0.080mm)	ISO106/1080	Signal G10
	Surface Material	Bottom Solder	1.38mil(0.035mm)	Solder Resist	Signal GBL
	Bottom Overlay		0.40mil(0.010mm)		Solder Mask GBS
				Legend GBO	
4			Total thickness: 64.35mil(1.634mm)		4



A

B

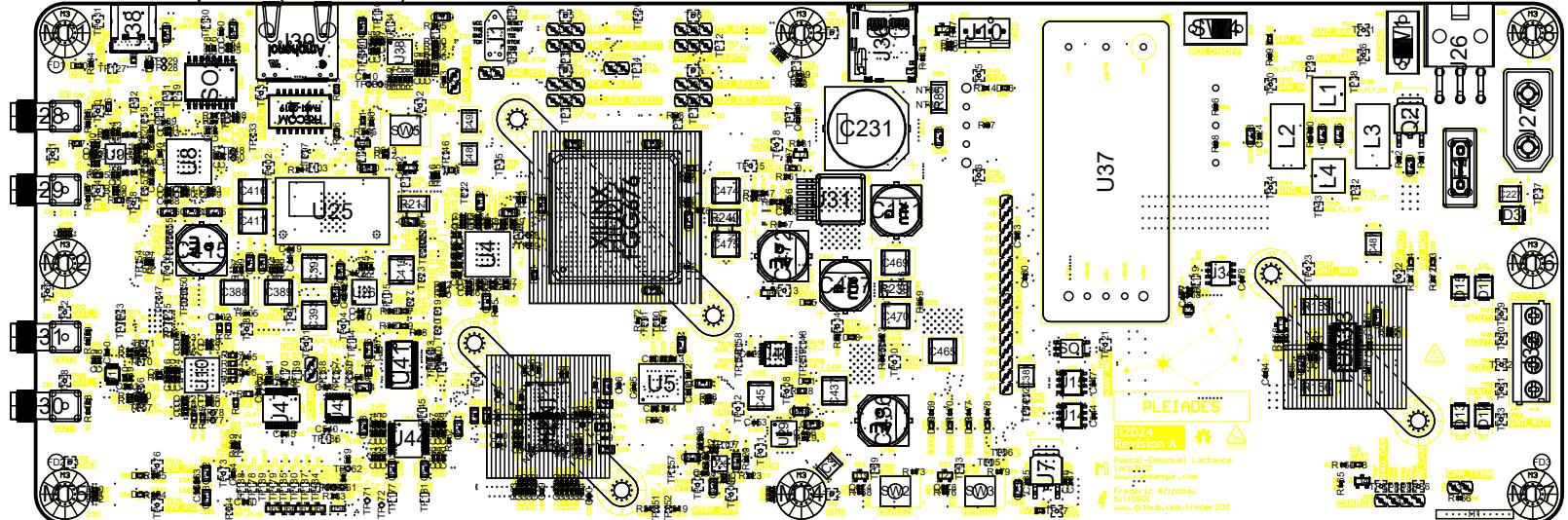
C

D

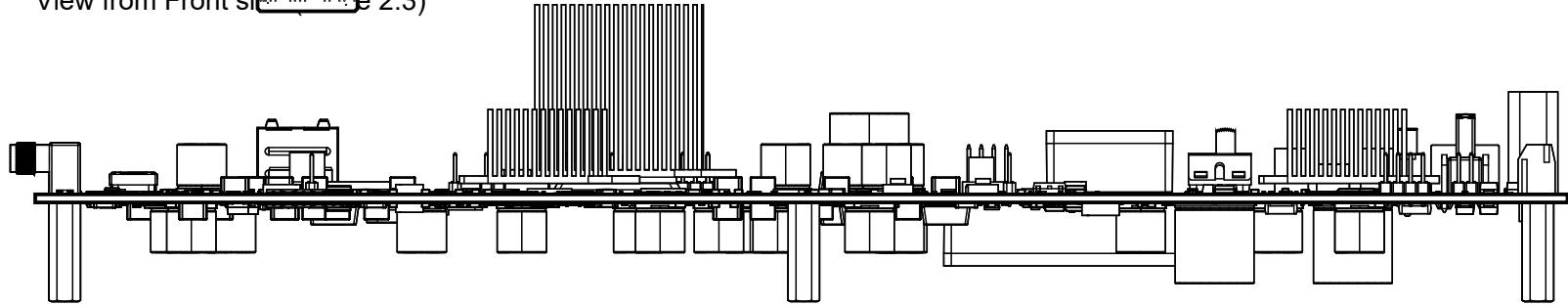
E

F

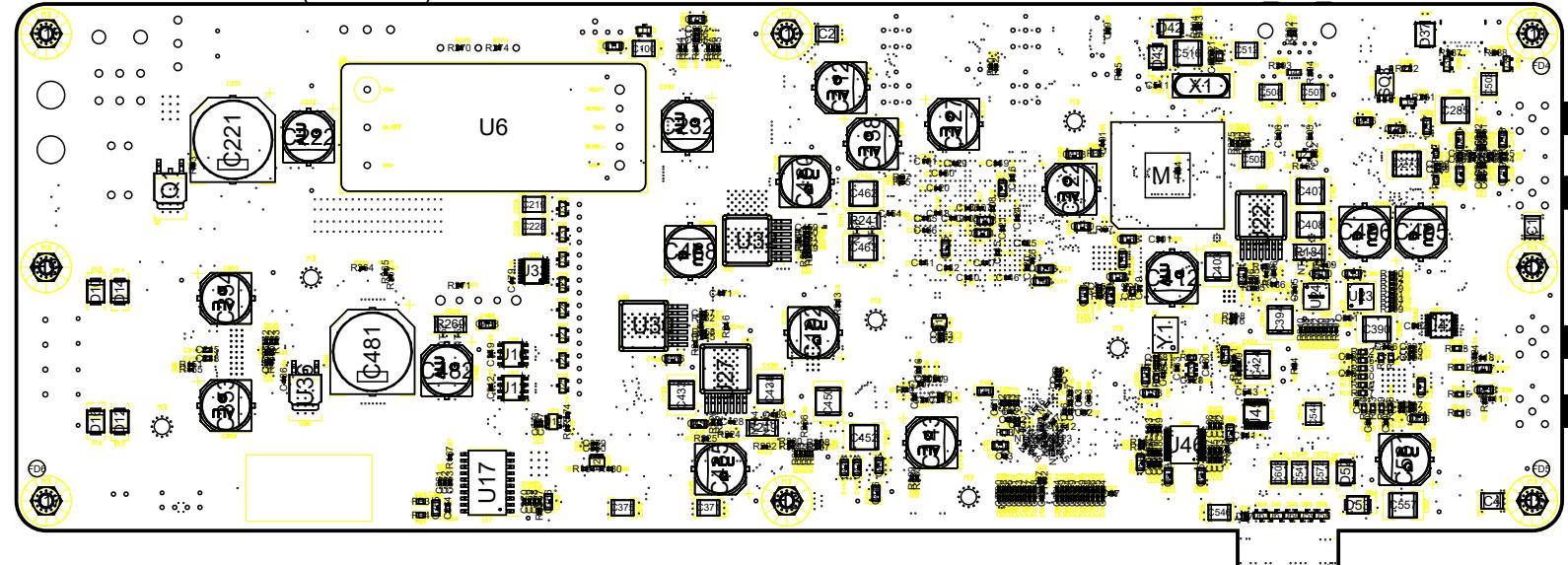
View from Top side (Scale 2:3)



View from Front side (Scale 2:3)



View from Bottom side (Scale 2:3)

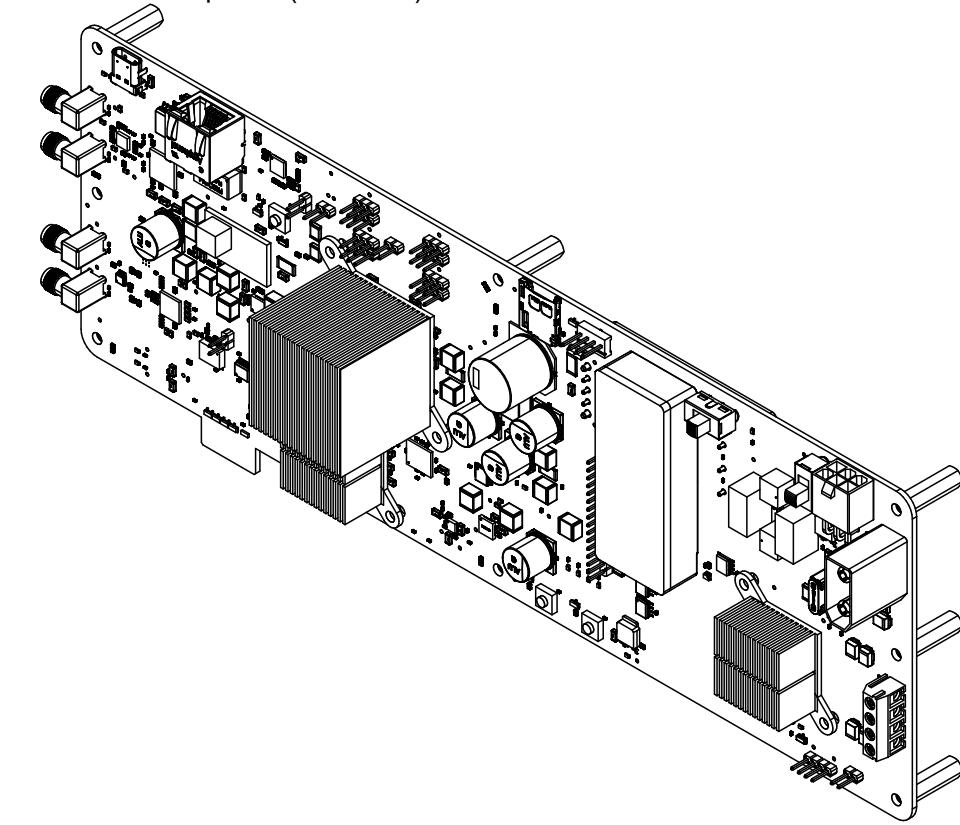


D

E

F

View from Top side (Scale 1:2)



A

B

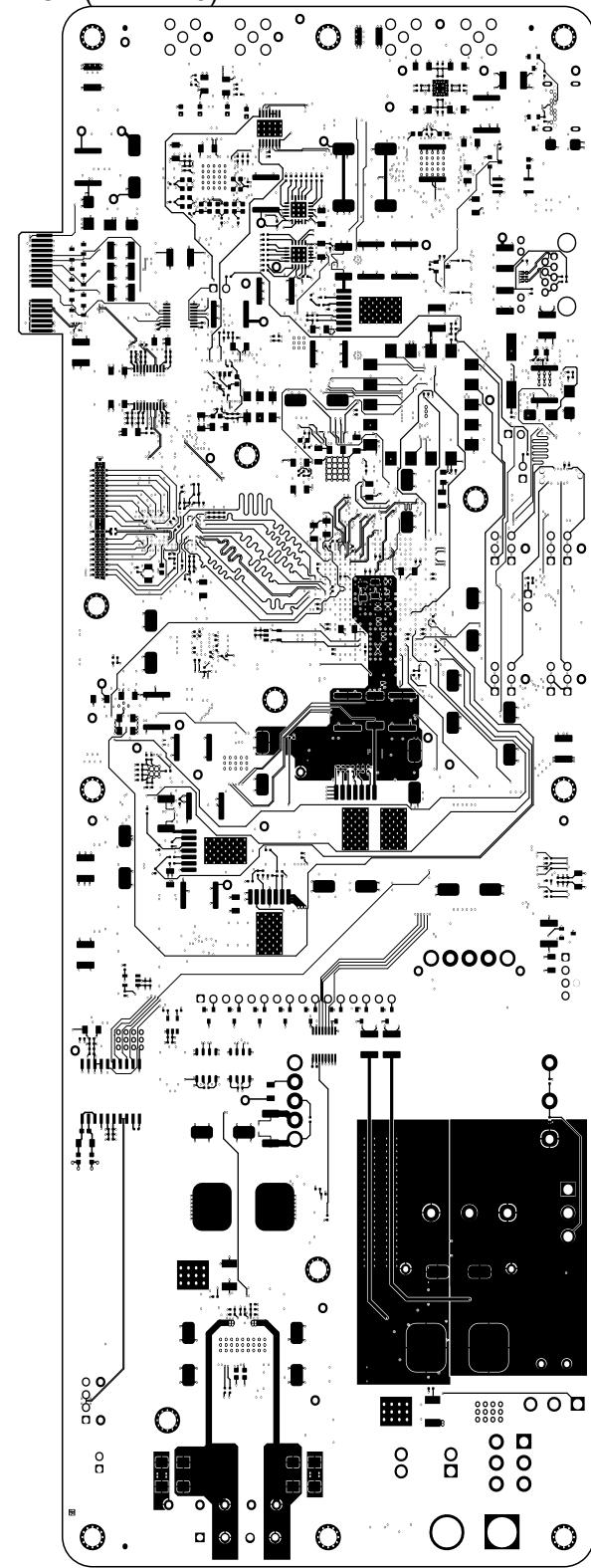
C

D

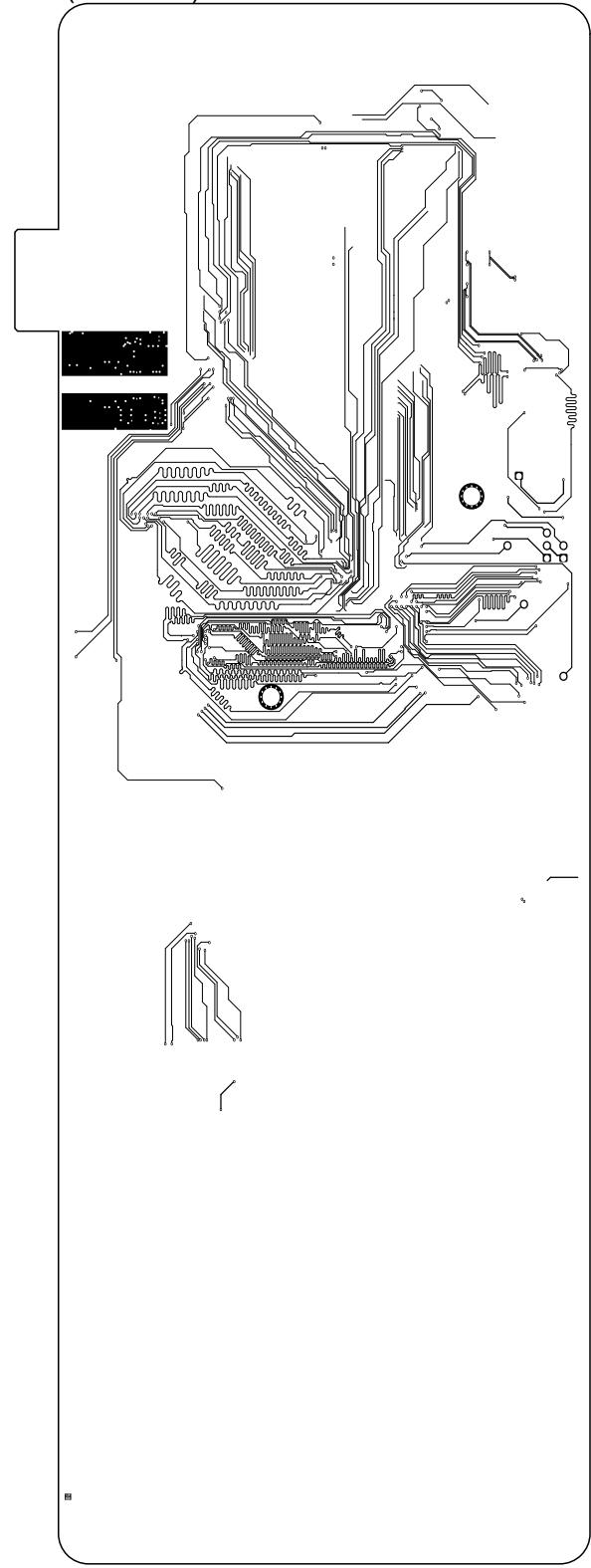
E

F

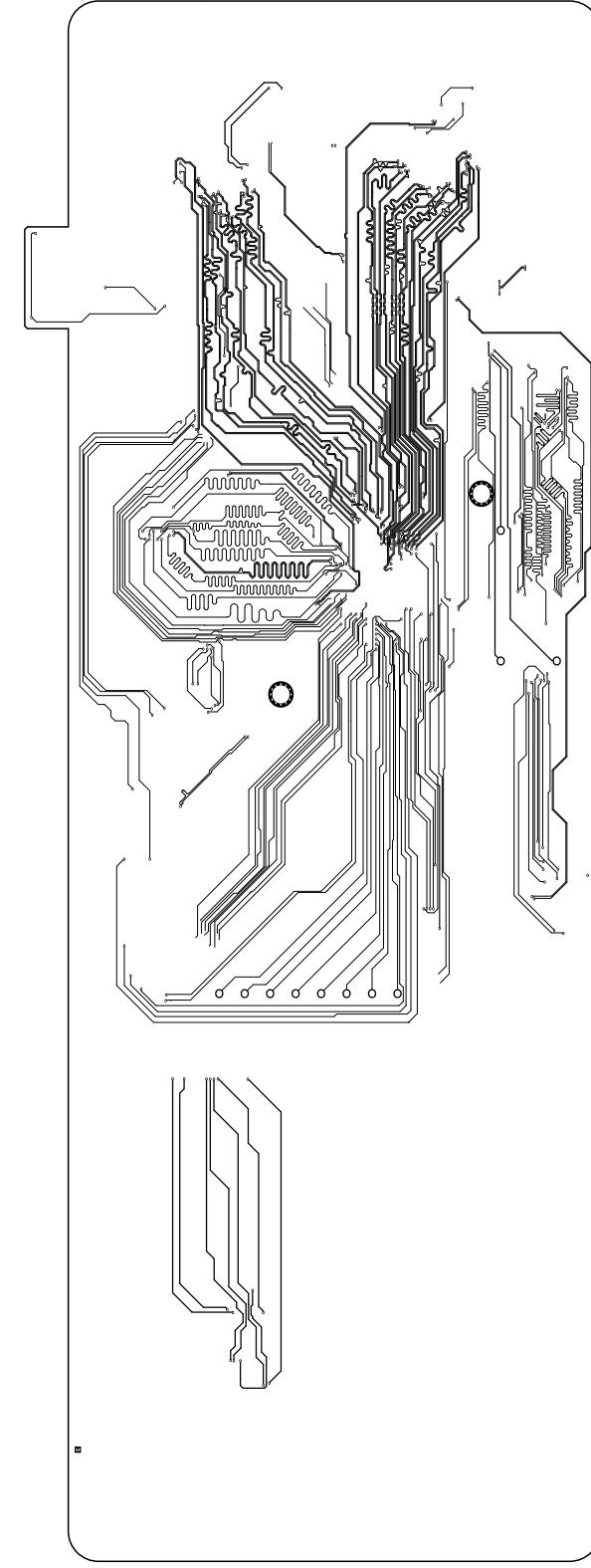
BOT (Scale 2:3)



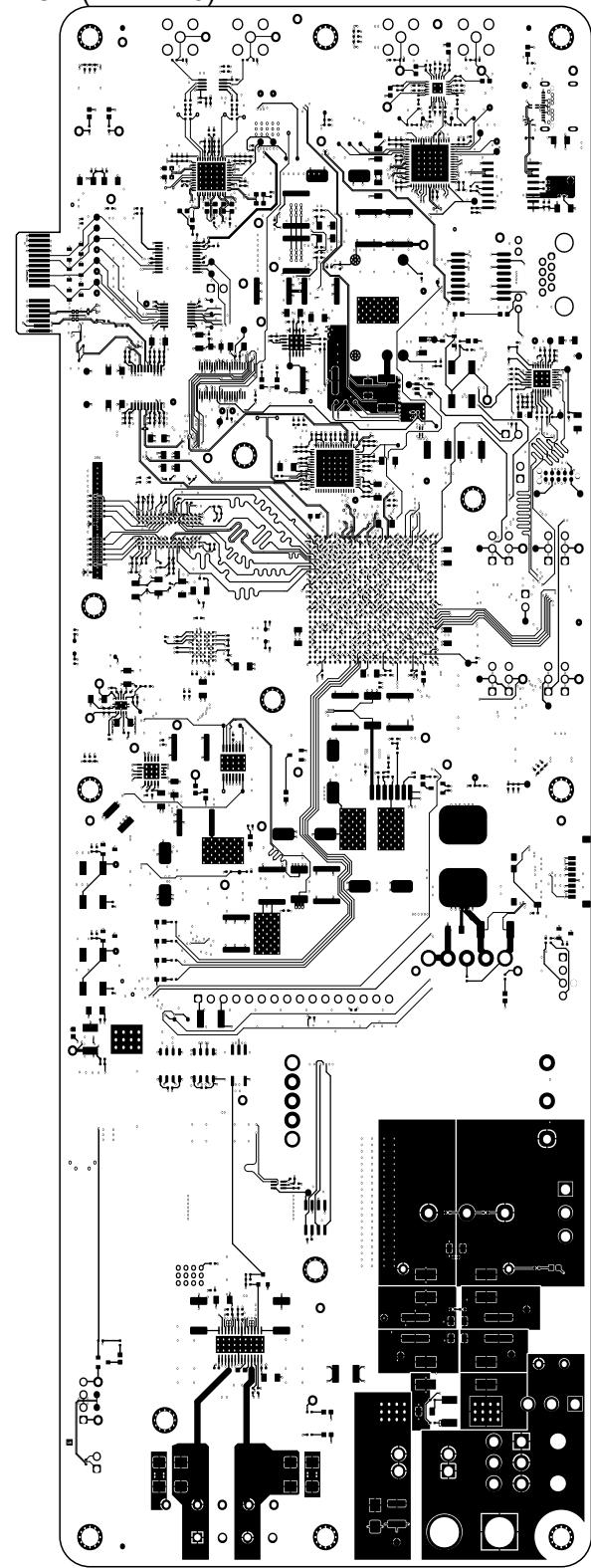
IN2 (Scale 2:3)



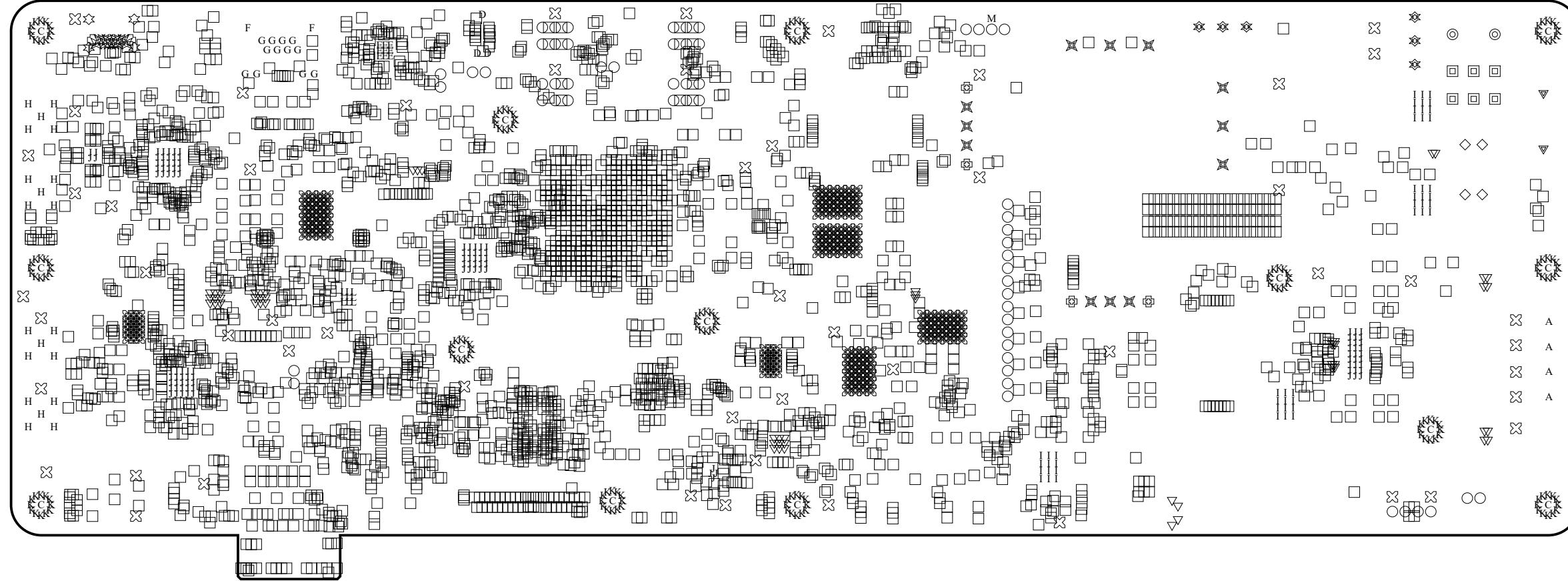
IN1 (Scale 2:3)



TOP (Scale 2:3)



Drill Drawing View (Scale 1:1)

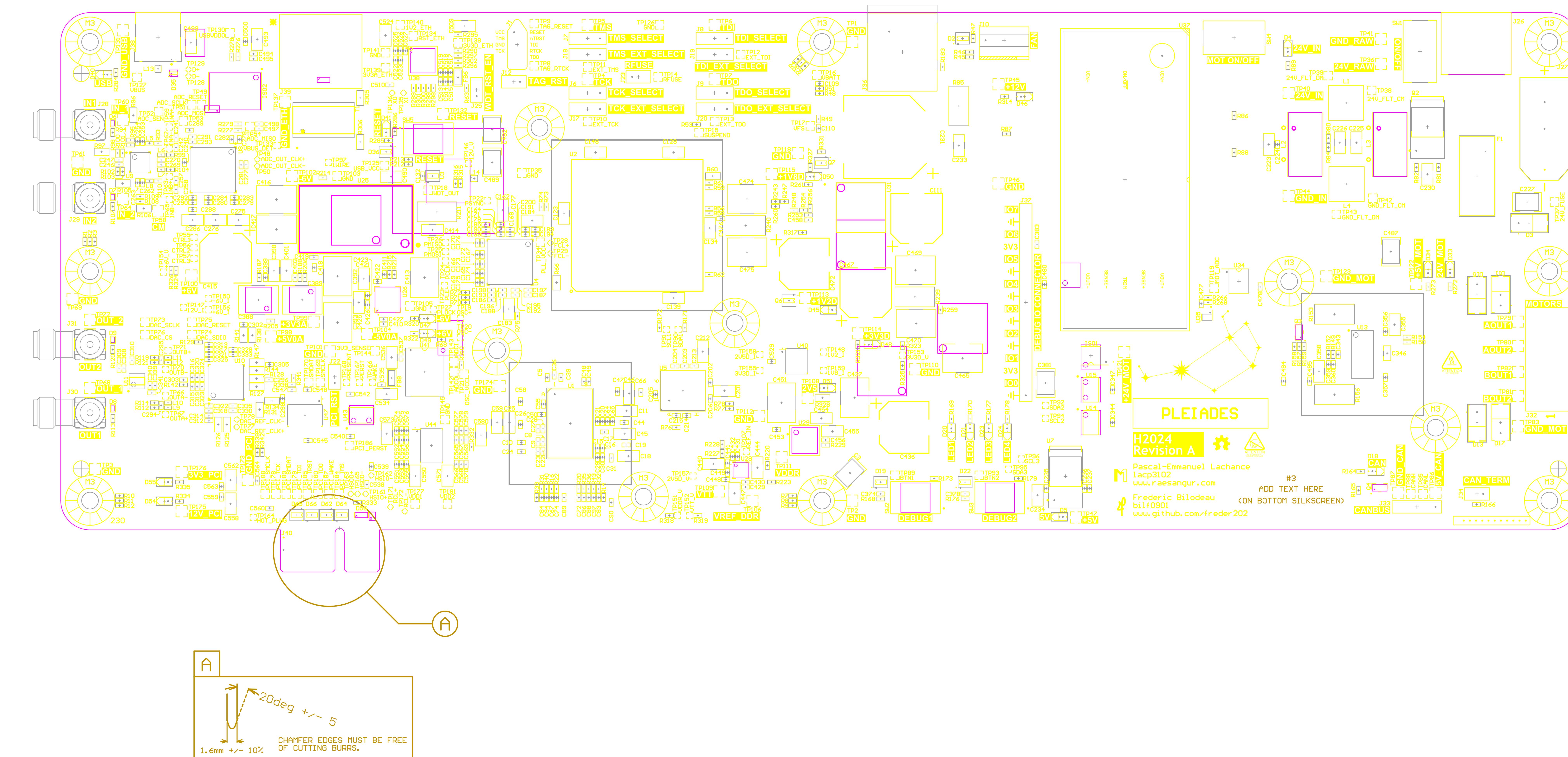


Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	2903	0.15mm	Plated	
J	110	0.20mm	Plated	
✖	225	0.25mm	Plated	
K	168	0.25mm	Plated	+/-0.10mm
L	9	0.30mm	Plated	
▽	55	0.30mm	Plated	
E	9	0.35mm	Plated	
❖	12	0.41mm	Plated	+/-0.10mm
I	48	0.51mm	Plated	
❖	4	0.51mm	Plated	+/-0.13mm
✚	2	0.66mm	Non-Plated	+/-0.10mm
G	12	0.89mm	Plated	
D	3	1.00mm	Plated	
✖	54	1.02mm	Plated	+/-0.20mm
○	58	1.12mm	Plated	
M	1	1.27mm	Non-Plated	
A	4	1.30mm	Plated	
❖	12	1.57mm	Plated	
H	20	1.65mm	Plated	
◇	4	1.78mm	Plated	+/-0.15mm
■	6	1.80mm	Plated	
❖	6	1.85mm	Plated	
✚	4	2.13mm	Plated	
◎	2	3.00mm	Non-Plated	
F	2	3.25mm	Plated	
C	14	3.43mm	Plated	+/-0.51mm
▽	2	5.84mm	Plated	+/-0.25mm
3749 Total				

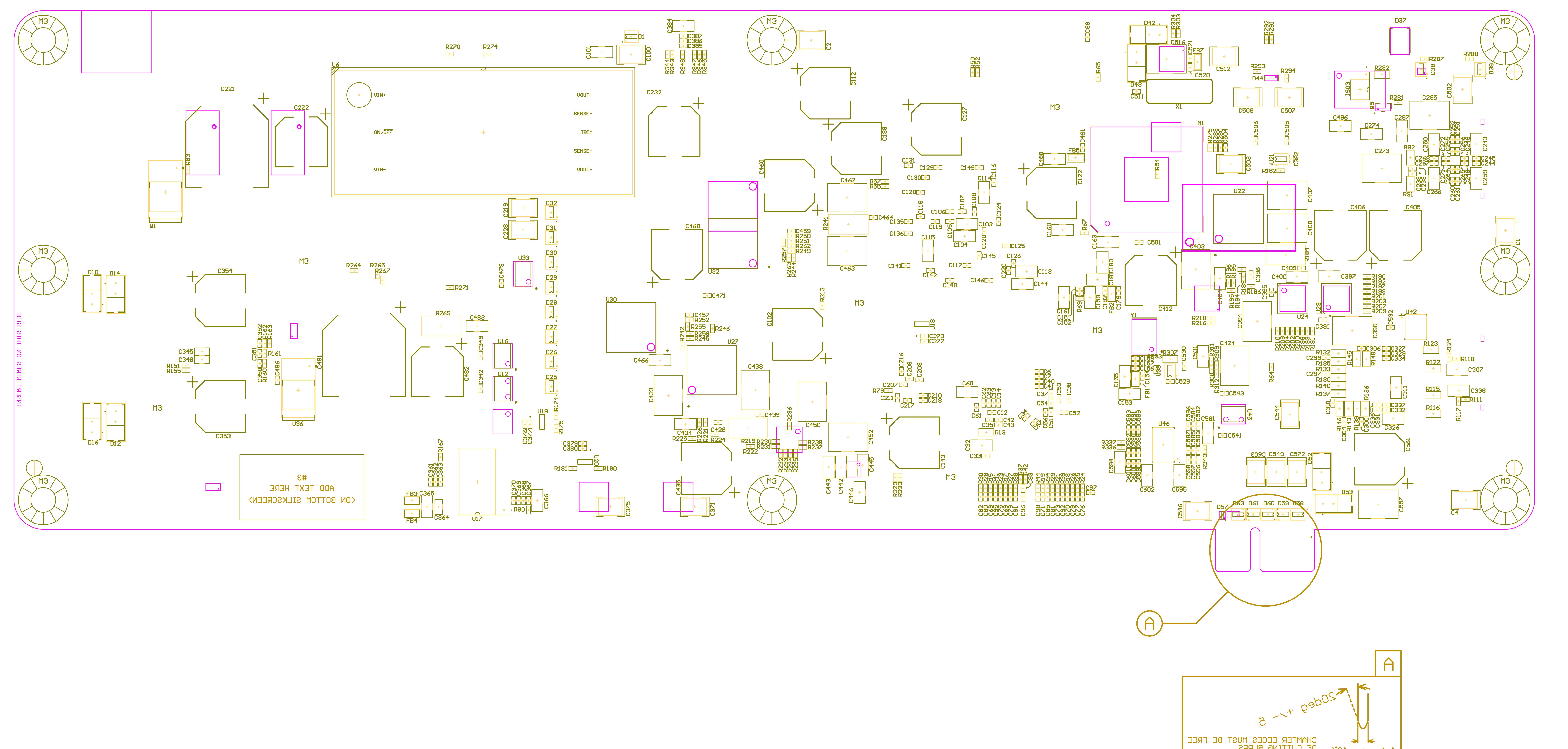
FABRICATION NOTES:

- [1] FABRICATE TO IPC CLASS 3 STANDARD.
- [2] FABRICATE PCB USING ONLY RoHS COMPLIANT MATERIALS.
FINAL PRODUCT SHALL BE ACCEPTABLE TO USE IN RoHS ASSEMBLY.
- [3] ADD MANUFACTURING MARKING (LOGO / DATE / UL MARKING / RoHS) ON SILKSCREEN BOTTOM SIDE OF PCB.
(.gbo), IN AREA MARKED #3 IN MANUFACTURING NOTES LAYER [M8].
- [4] MATERIAL SHALL MEET UL 94V-0 FAMMABILITY RATING.
- [5] DO NOT APPLY SILKSCREEN OVER EXPOSED COPPER OR SOLDERMASK EXPANSION.
CLIP SILKSCREEN AROUND EXPOSED COPPER.
CLIP SILKSCREEN AROUND SOLDERMASK EXPANSION.
- [6] DO NOT FILL VIAS OR PLATE OVER.
TREAT VIA-IN-PAD AS NORMAL PTH VIAS.
- [7] TENT VIAS WITH SOLDERMASK ACCORDING TO SOLDERMASK LAYERS.
- [8] DIAMETERS IN DRILL HOLE TABLE ARE FINISHED SIZES.
- [9] APPLY GREEN TRANSPARENT SOLDERMASK OVER BARE COPPER ACCORDING TO SOLDERMASKS LAYERS.
- [10] APPLY NON-CONDUCTIVE WHITE INK AFTER SOLDERMASK ACCORDING TO SILKSCREEN LAYERS.
- [11] APPLY ENIG SURFACE FINISH ON ALL EXPOSED COPPER
- [12] BOW AND TWIST SHALL NOT EXCEED 0.0075 INCH PER INCH.
- [13] ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION.
ALL DESIGN MODIFICATIONS MUST BE APPROVED BY CUSTOMER.
- [14] BOARD IS VIEWED FROM PRIMARY SIDE (LAYER 1 - TOP).
THE STACKUP HAS 12 CONDUCTIVE LAYERS.
ALL INNER CONDUCTIVE LAYERS ARE HALF OZ/IN THICK +/- 10%
TOP AND BOTTOM LAYERS ARE 1 OZ/IN THICK +/- 10%
- [15] MINIMUM TRACE WIDTH AND CLEARANCE ARE 3MILS / 3MILS
- [16] MINIMUM HOLE SIZE AFTER PLATING IS 6MILS. REFER TO DRILL TABLE FOR TOLERANCES.
- [17] APPLY SOLDER RESIST BETWEEN ALL SMT PADS.
FINEST SOLDERMASK NECK IS 3MIL BETWEEN PADS.
SOLDERMASK EXPANSION IS SET TO 3MIL ON ALL PADS.
- [18] CHAMFER BOARD EDGE AS PER DETAIL [A]
- [19] APPLY HUMISEAL 1A33 CONFORMAL COATING AS SPECIFIED BY M17-M18 LAYERS



ALL DIMENSIONS ARE IN THOUSANDS OF INCHES (MILS)	
PASCAL-EMMANUEL LACHANCE FREDERIC BILODEAU	TITLE: PLEIADES
DATE: 2024-03-12	PART NO.: REV: A
FILE NAME: Pleiares_PP.PcbDoc	DWG NO.: SCALE:

FABRICATION NOTE
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PLEIADES		ALL DIMENSIONS ARE IN THOUSANDS OF INCHES (MILS)			
REV:	A	TITLE:	PASCAL-EMMANUEL LACHANCE	FREDERIC BILODEAU	
SCALE:		PART NO.:			
Dwg No:		DATE:	2024-03-15		
FILE NAME:	Pleiades_PP.PCDoc				