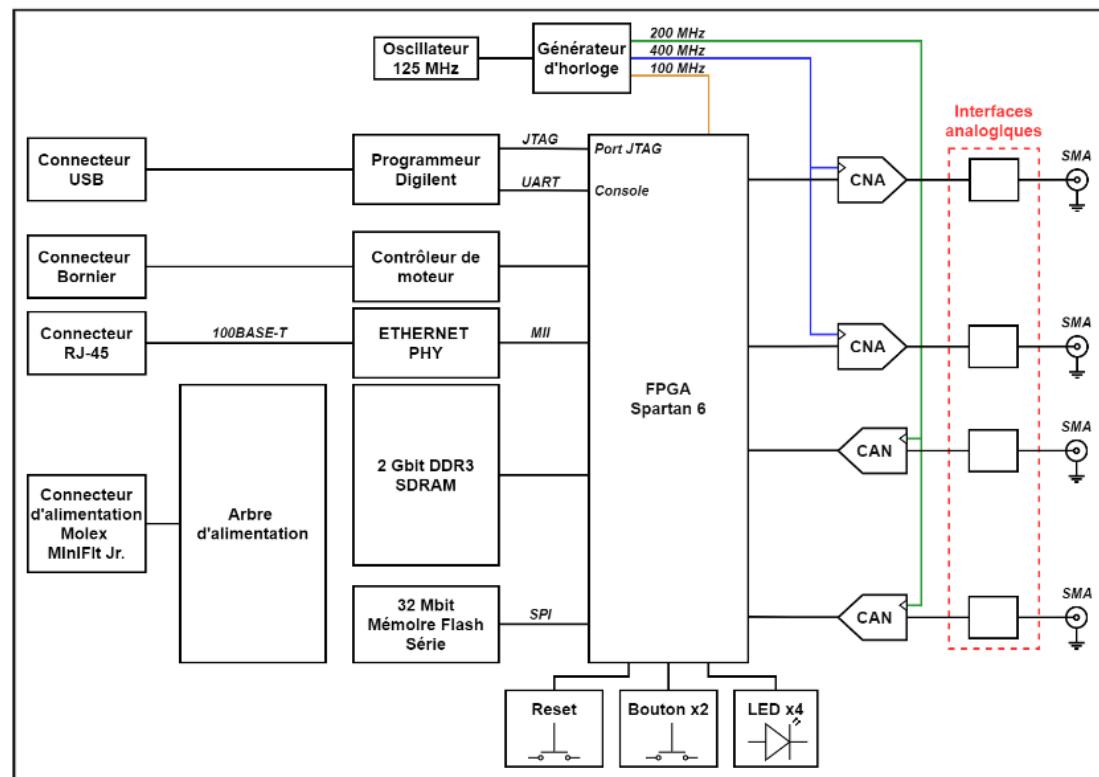


PLEIADES

LACP3102 - Pascal-Emmanuel Lachance
BILF0901 - Frédéric Bilodeau



NOTES FOR REVIEWERS:

Some functionalities not originally asked by the problem have been added for fun and to challenge ourselves.

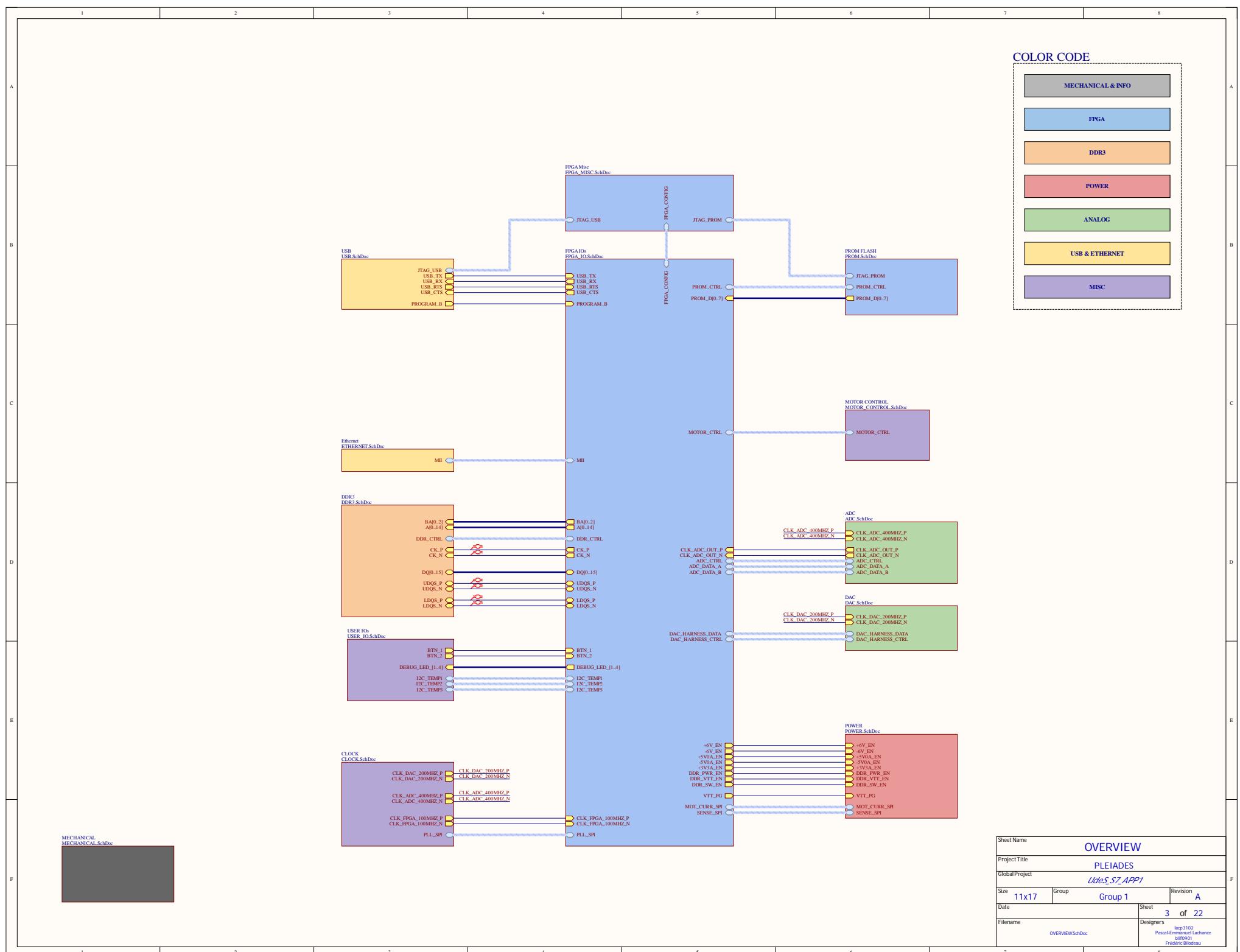
The following major changes have been done:

- Full Galvanic Isolation on 24V input and motor output
- Voltage and Current sensing on all major power rails
- A TAG-CONNECT programmation interface with JTAG source selection
- A USB-C connector
- A bunch of testpoints and debug features
- And more!

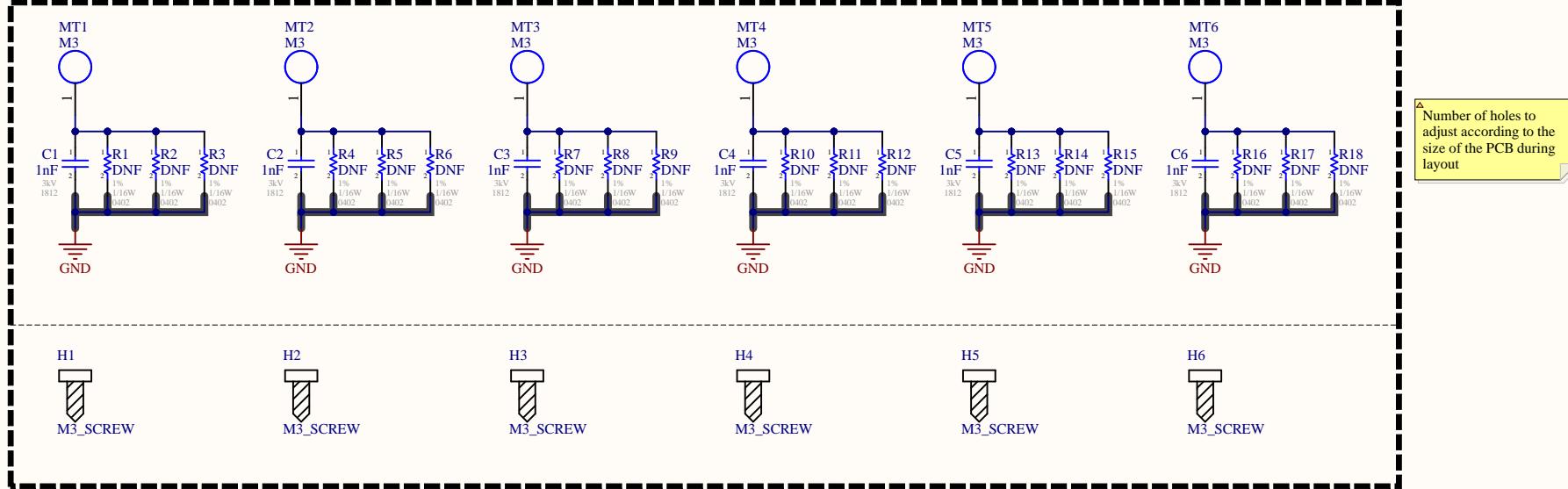
Note that a lot of resistors for patches have been added to strapping pins for configuration of all chips.

Sheet Name		TITLE PAGE	
Project Title		PLEIADES	
Global Project		<i>UdeS_S7_APP1</i>	
Size	Group	Revision	
11x17	Group 1	A	
Date	Sheet		1 of 22
Filename		Designers	
TITLE.SchDoc		iacp3102 Pascal-Emmanuel Lachance bilf0901 Frédéric Bilodeau	

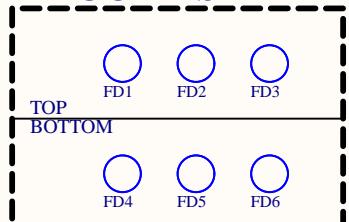
1	2	3	4	5	6	7	8
A							
RESISTORS DNF							
CAPACITORS DNF							
INDUCTORS DNF							
DIODES DNF							
COLOR CODE							
General Notes Assembly, Part Locations, Fabrication, Debug Information etc.							
Data sheet info Part information, addresses, registers, pull-up/pull-downs, etc.							
Calculations Values, tensions & currents, passives, etc.							
TODO Things that are left to be done, and who should do it							
Sheet Name INFO Project Title PLEIADES Global Project UdeS_S7_APP1 Size 11x17 Group Group 1 Revision A Date Sheet 2 of 22 Filename INFO.SchDoc Designers lcp3102 Pascal-Etienne Blachere bill0901 Frederic Blideau							



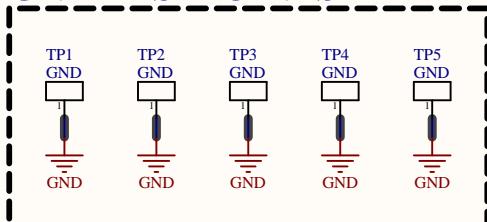
MOUNTING HOLES



FIDUCIALS



GND TESTPOINTS



Sheet Name

MECHANICAL

Project Title

PLEIADES

Global Project

UdeS_S7_APP1

Size

11x17

Group

Group 1

Revision

A

Date

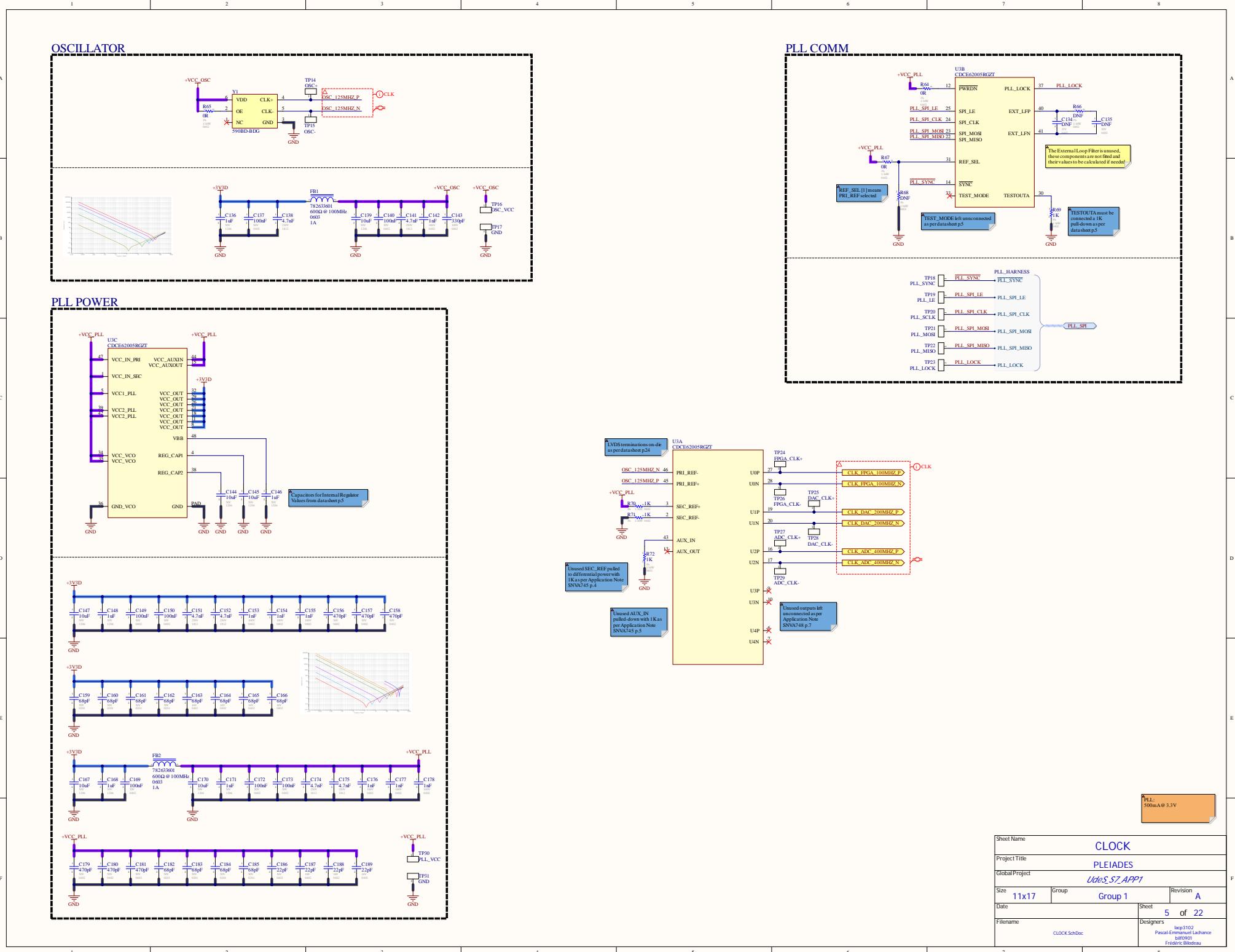
Sheet **4** of **22**

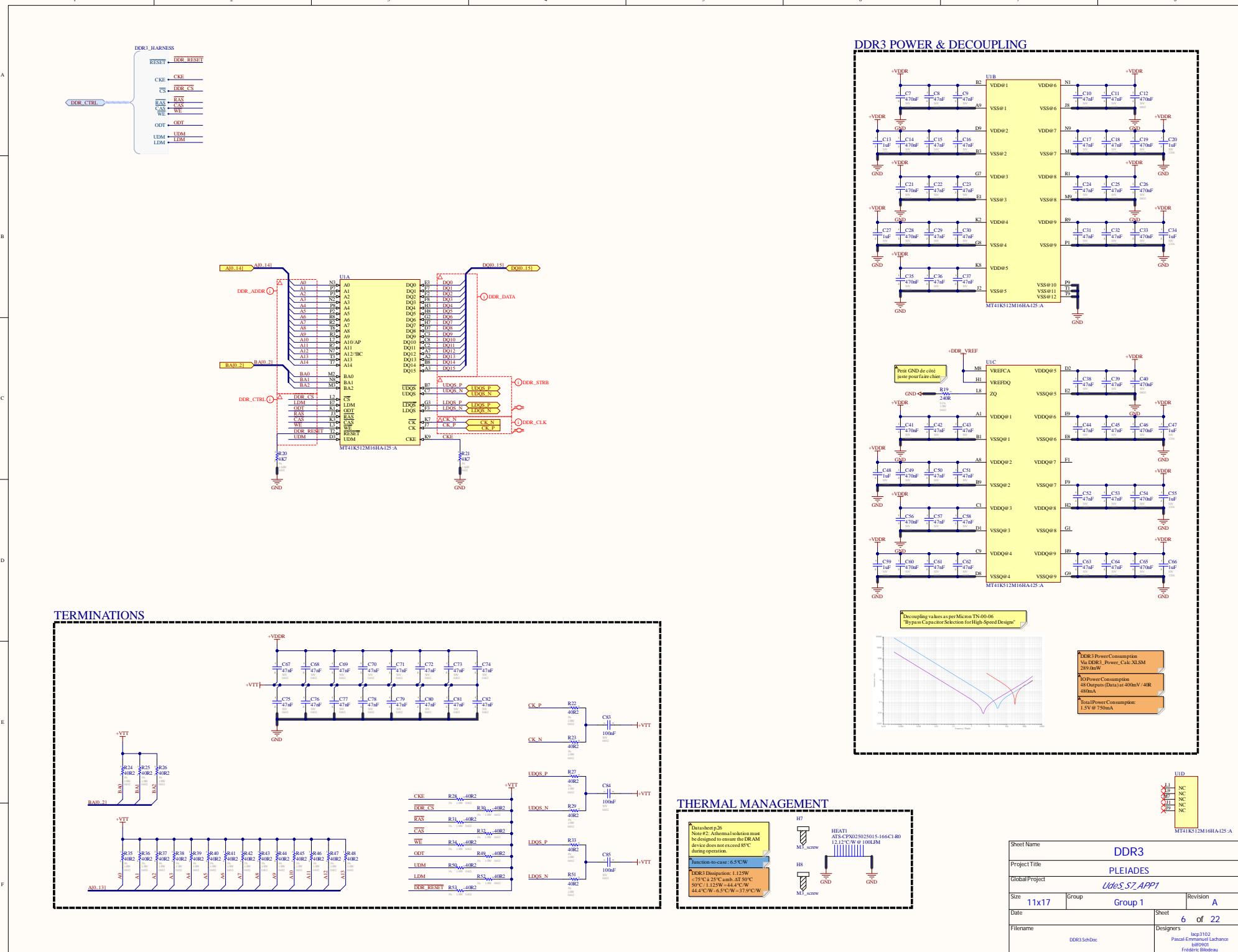
Filename

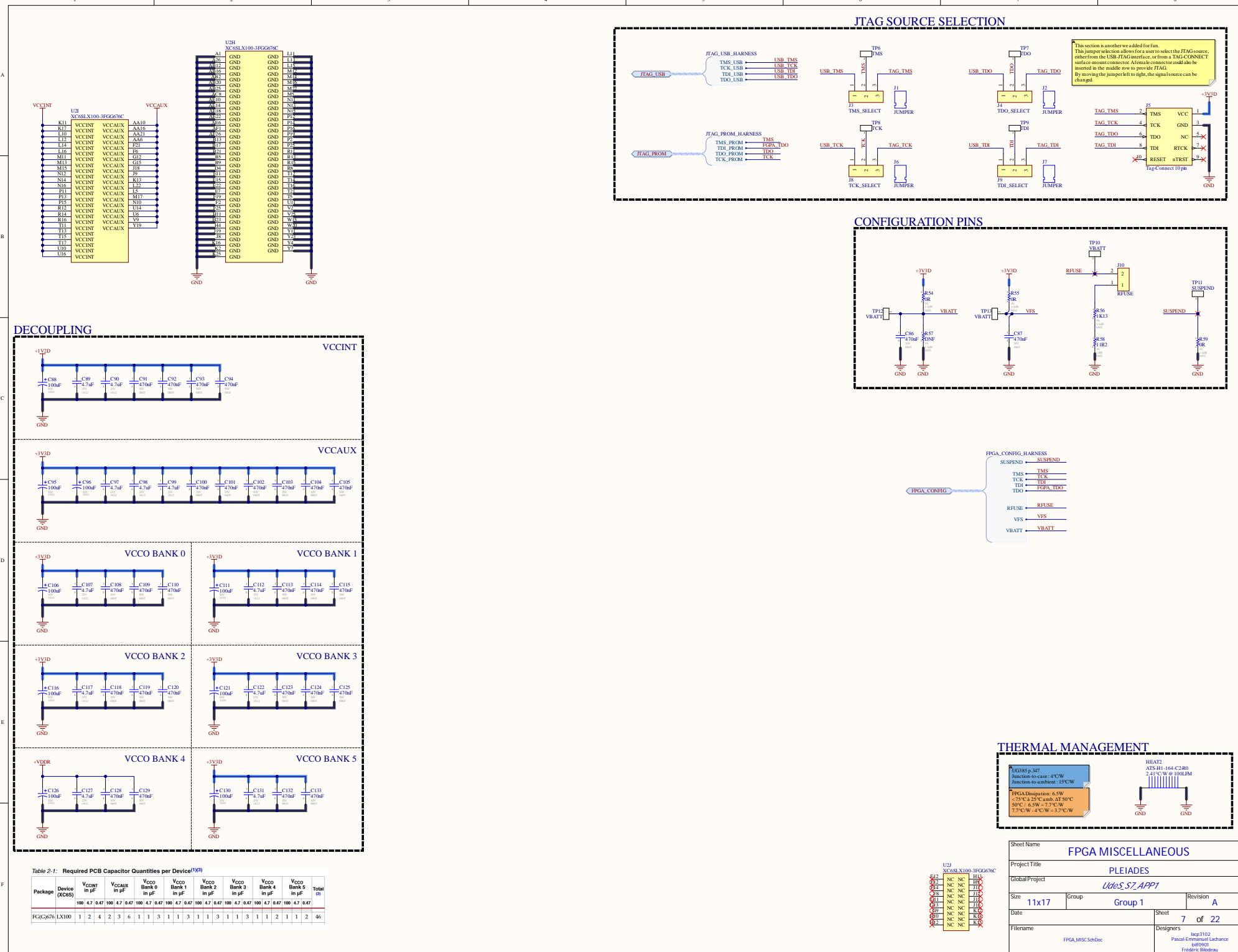
MECHANICAL.SchDoc

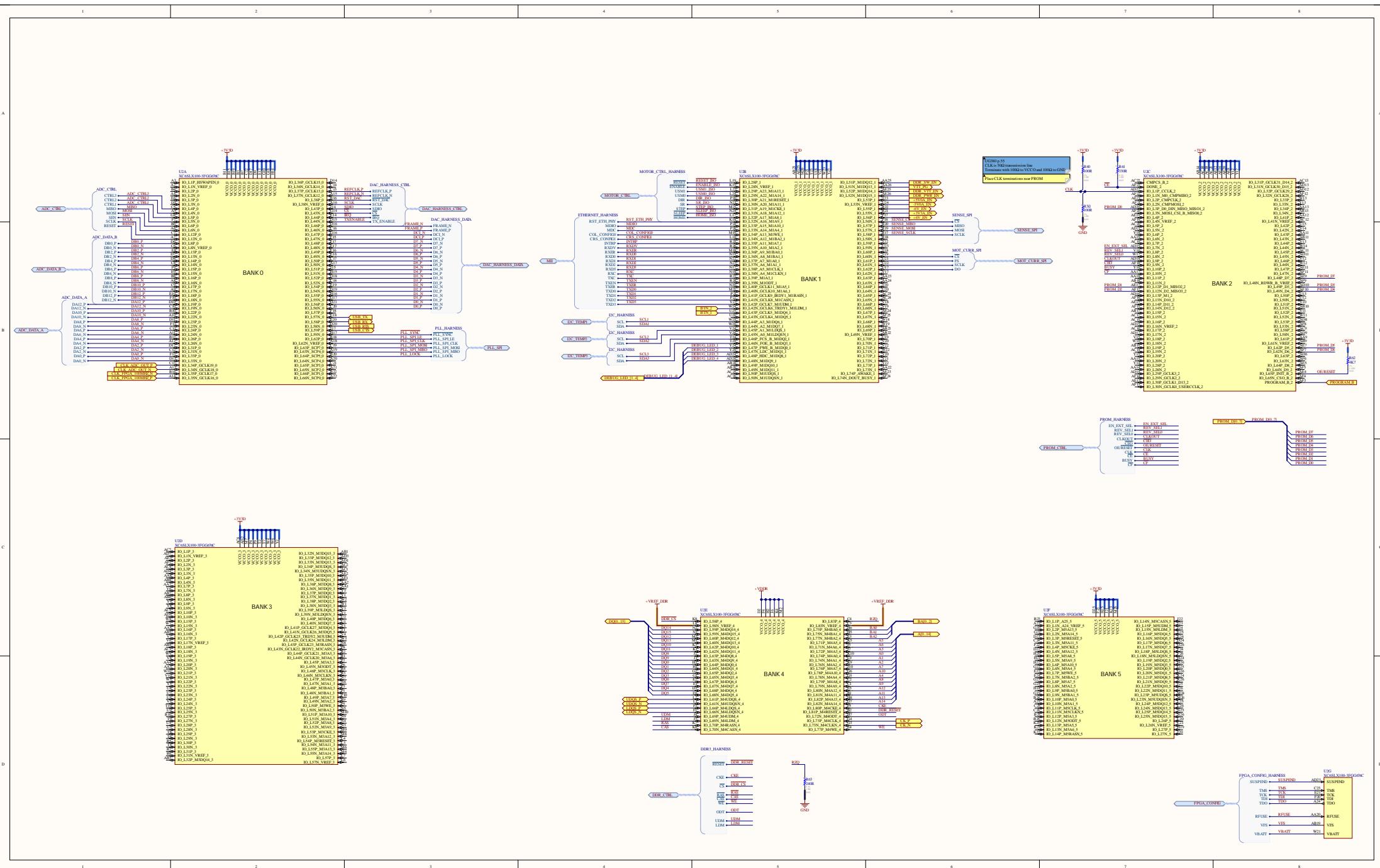
Designers

 lacp3102
 Pascal-Emmanuel Lachance
 bilf0901
 Frédéric Bilodeau

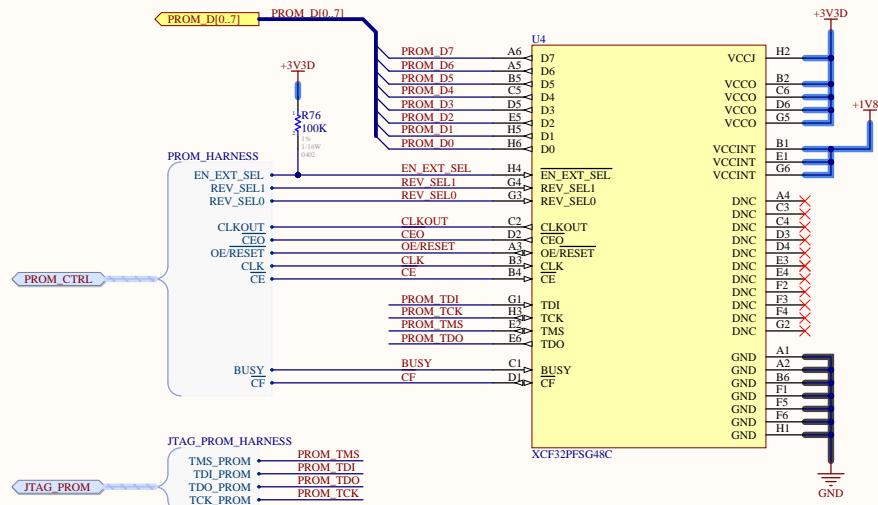
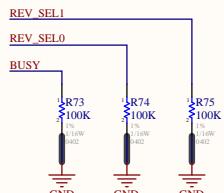






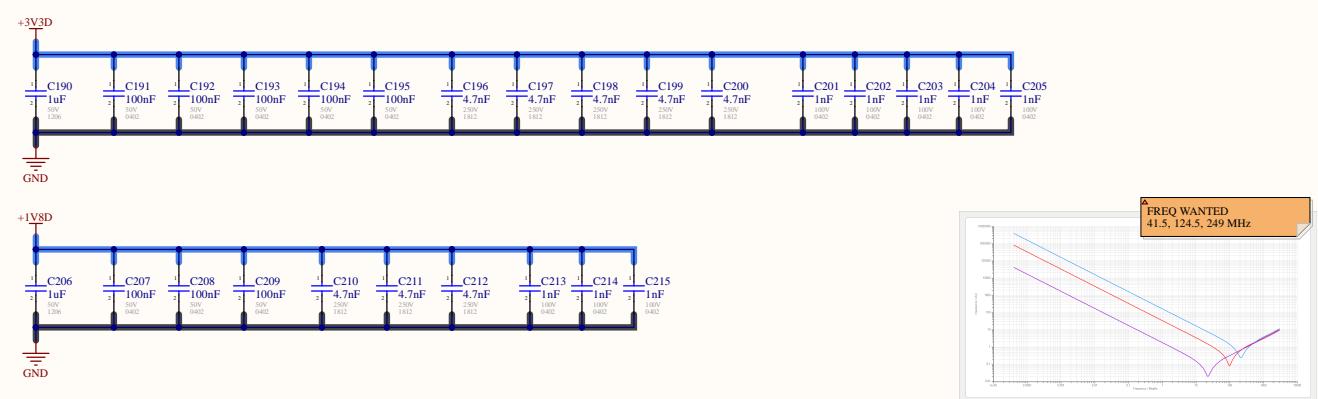


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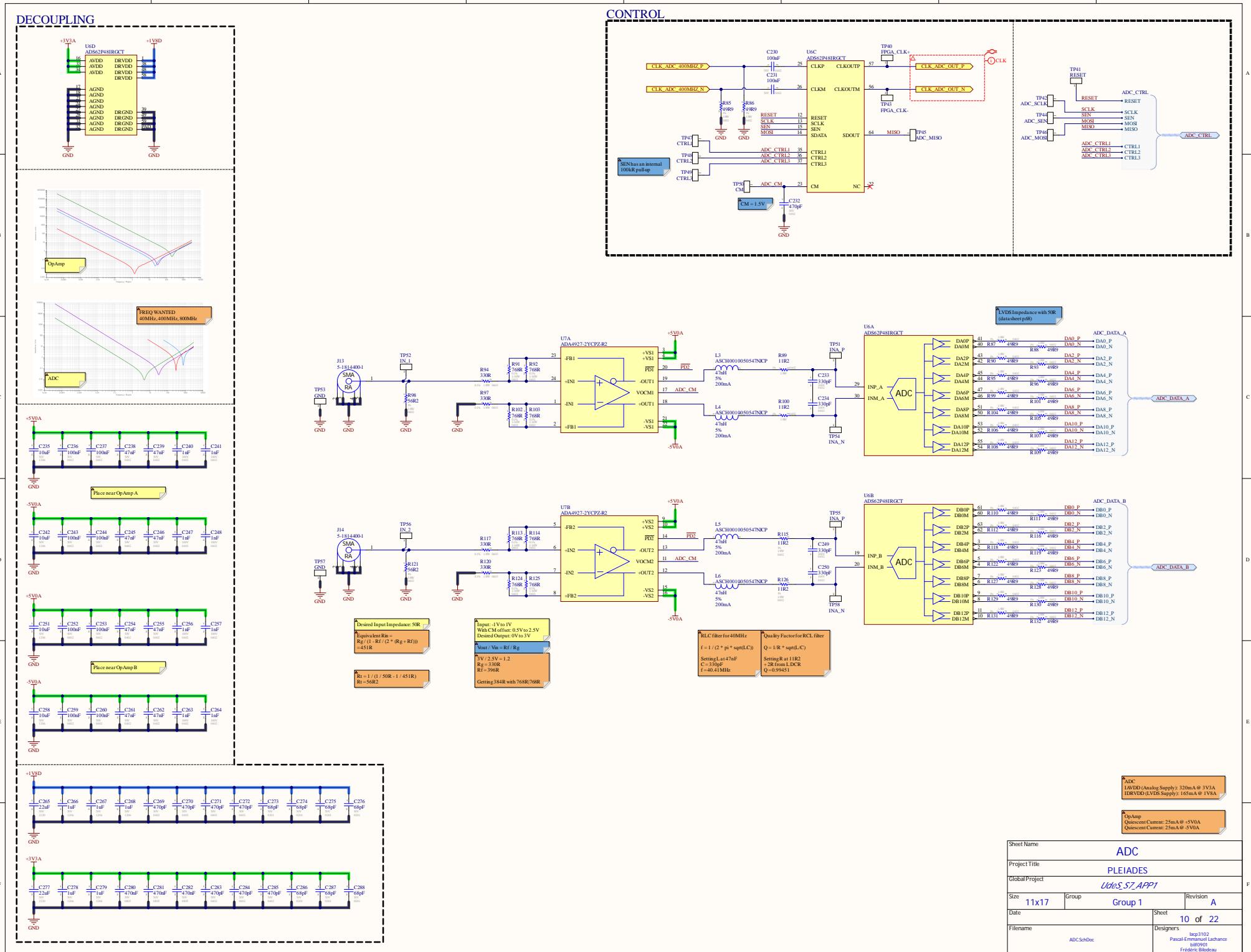


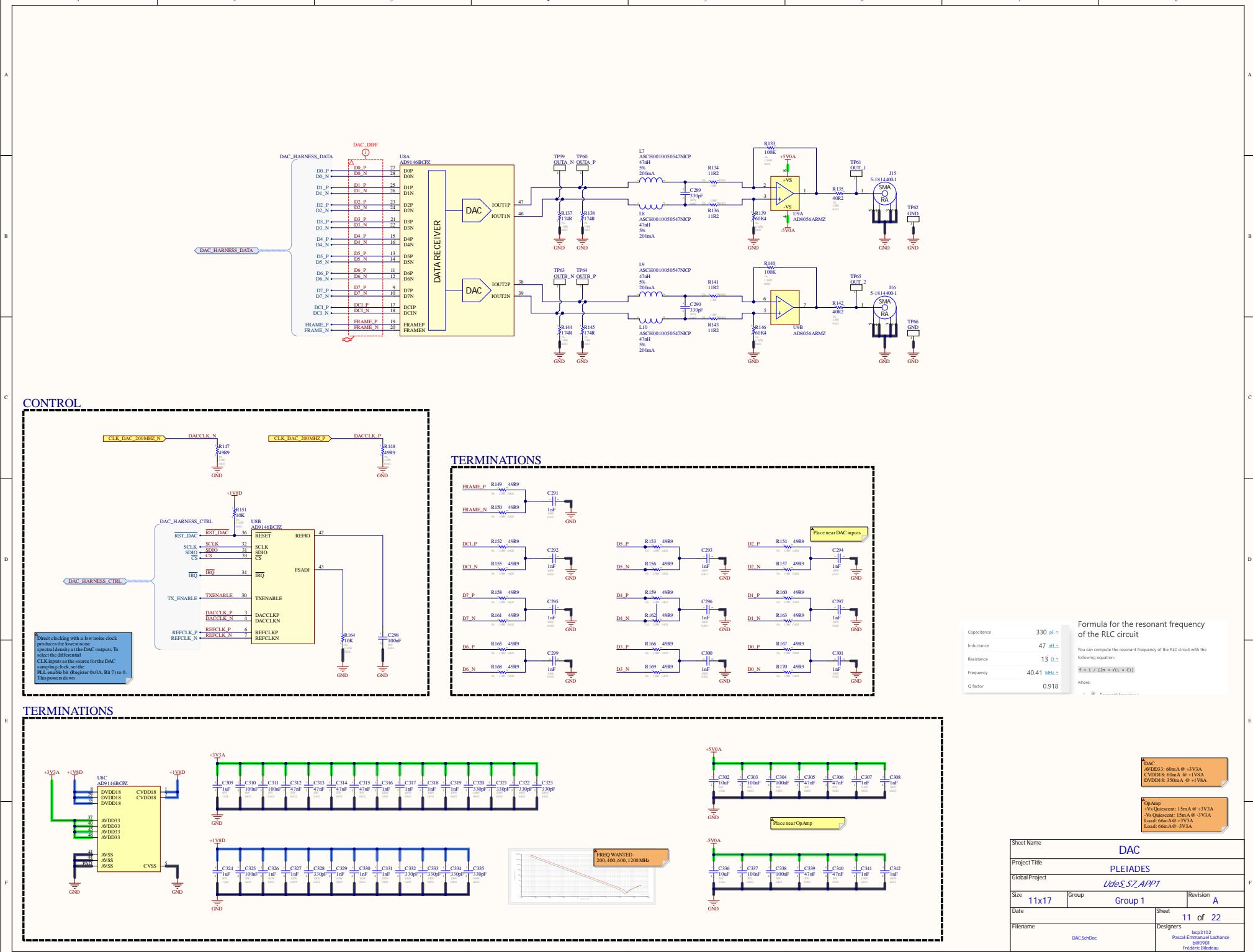
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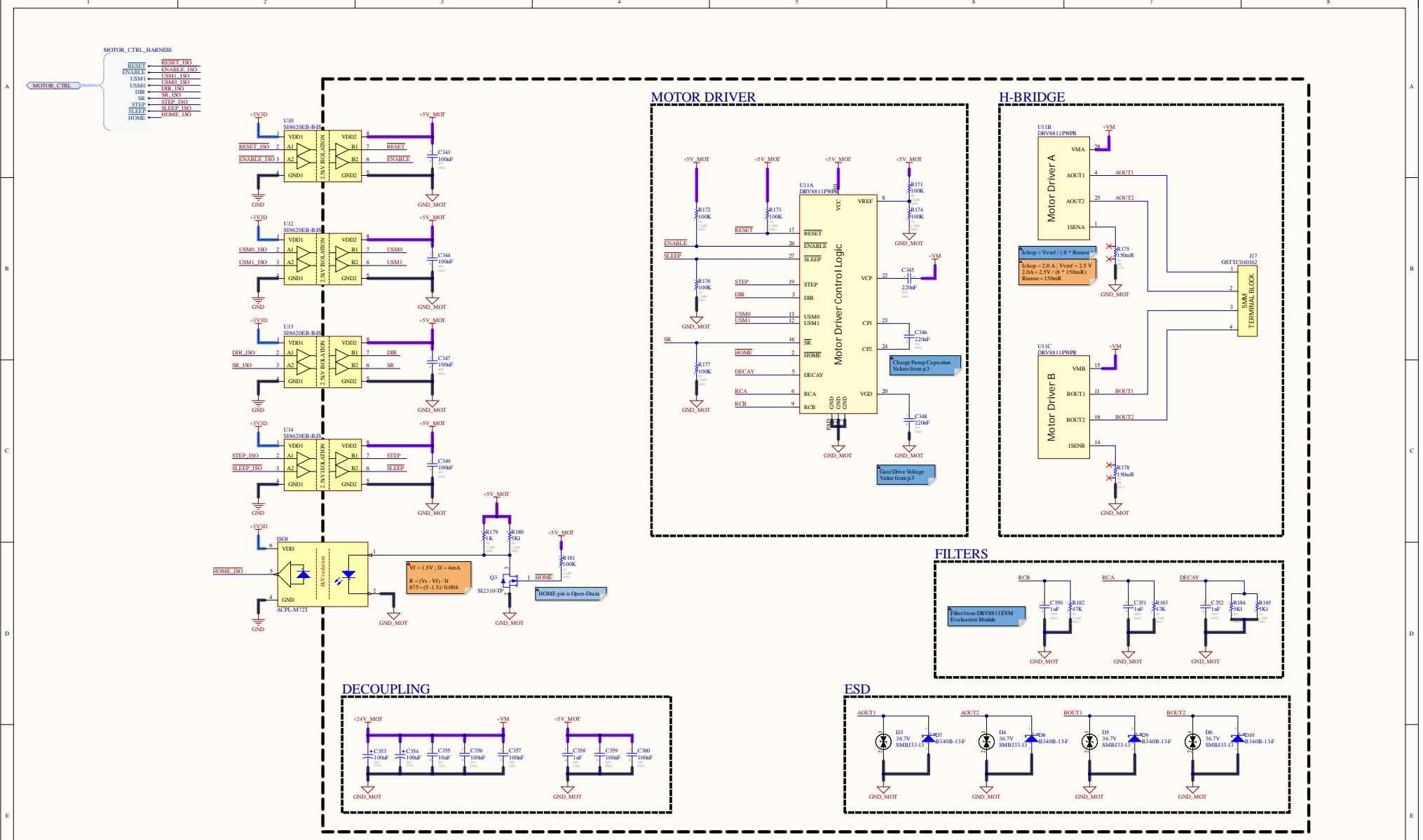
DECOUPLING

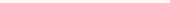


Sheet Name		PROM	
Project Title		PLEIADES	
Global Project		UdeS SZ APP1	
Size	11x17	Group	Group 1
Date		Revision	A
Filename	PROM.SchDoc	Designers	Iacp102 Pascal-Etienne Lachance bill0901 Frédéric Bilodeau
Sheet		9	of 22

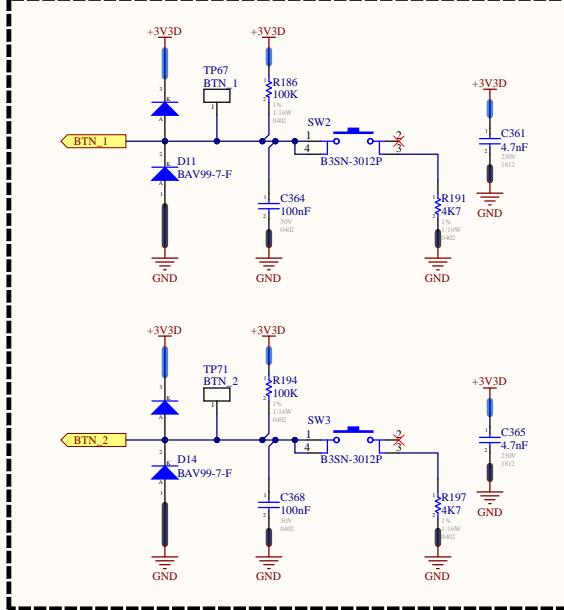
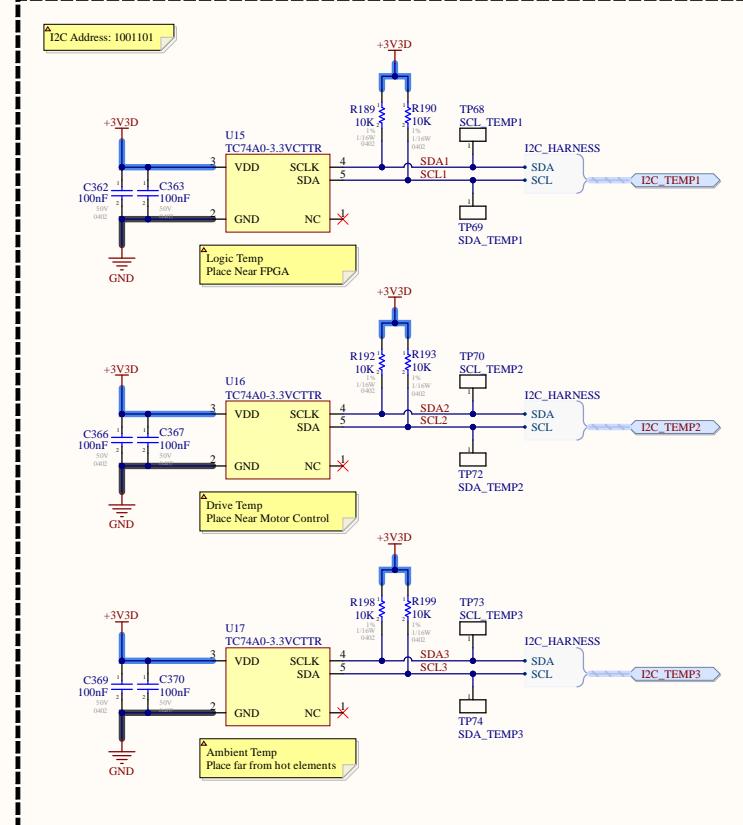
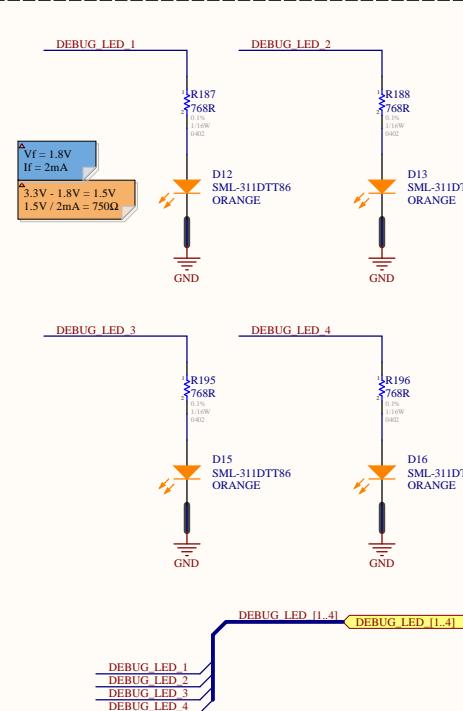






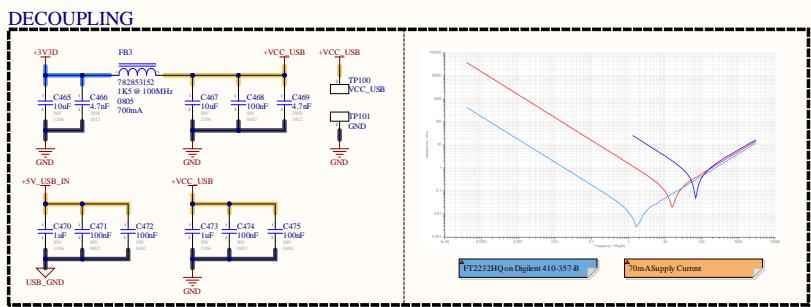
THERMAL MANAGEMENT		4 mA for the home channel 4 mA for the DRVS8	
 datasheet p23 104 $P = 4 \times Rds \times I_{DS(on)}^2$			
Junction-to-case: 19.3°C/W Junction-to-board: 115°C/W			
Power Dissipation: < 100°C & 0.25°C amb. $\Delta T = 77^\circ\text{C}$ $75^\circ\text{C} / 8.4\text{W} = 8.9^\circ\text{C/W}$			
$8.4\text{W} / 11.5^\circ\text{C/W} = 0.73^\circ\text{C/W}$ Heat sink max: 30°CW			
			
HEAT3 ATS-CPX2025025015-166-CL-R0 $12.12^\circ\text{C/CW} @ 100\text{LFM}$			
			
Project Title: PLEIADES Global Project: UteS57_APP1			
Size: 11x17 Group: Group 1 Revision: A			
Date: Sheet 12 of 22			
Filename: MOTOR_CONTROL.SchDoc		Designers: lap3102 Pascal-Emanuel Lachance bill902 Bleuet	

1 2 3 4 5 6

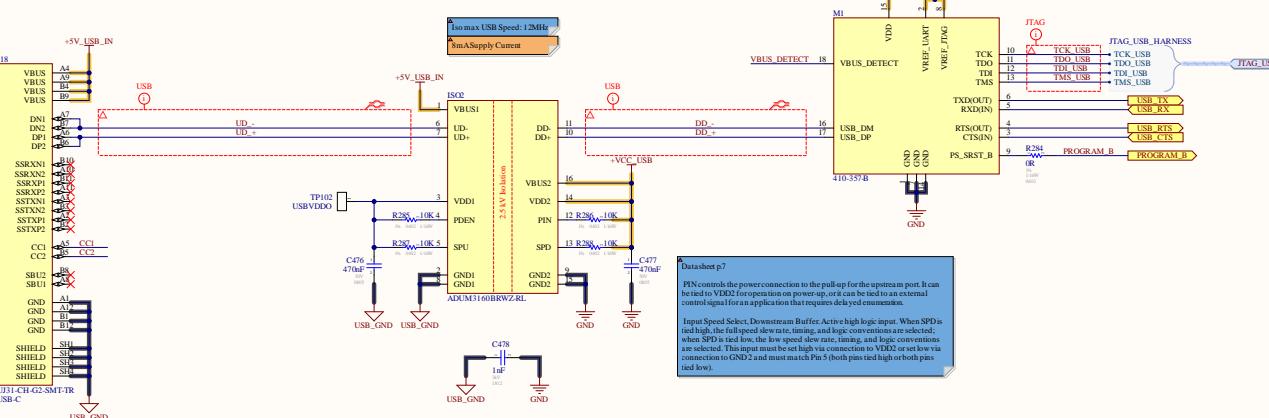
BUTTONS**TEMPERATURE SENSORS****DEBUG LEDS**

Sheet Name		
MECHANICAL		
Project Title		
PLEIADES		
Global Project	Group	Revision
<i>UdeS.S7_APP1</i>	Group 1	A
Date	Sheet	13 of 22
File name	Designers	<i>Iacp3102 Pascal-Etienne Lachance bilf0901 Frédéric Bilodeau</i>
USER_IO.SchDoc		

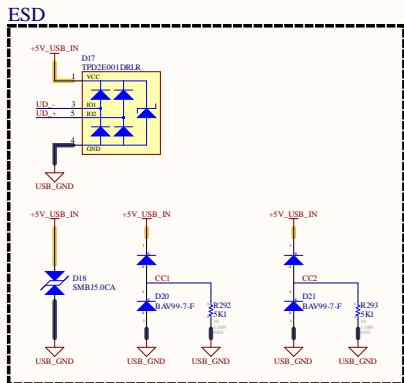
1 2 3 4 5 6



B

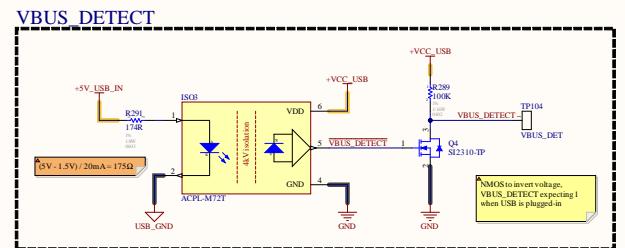


D



1

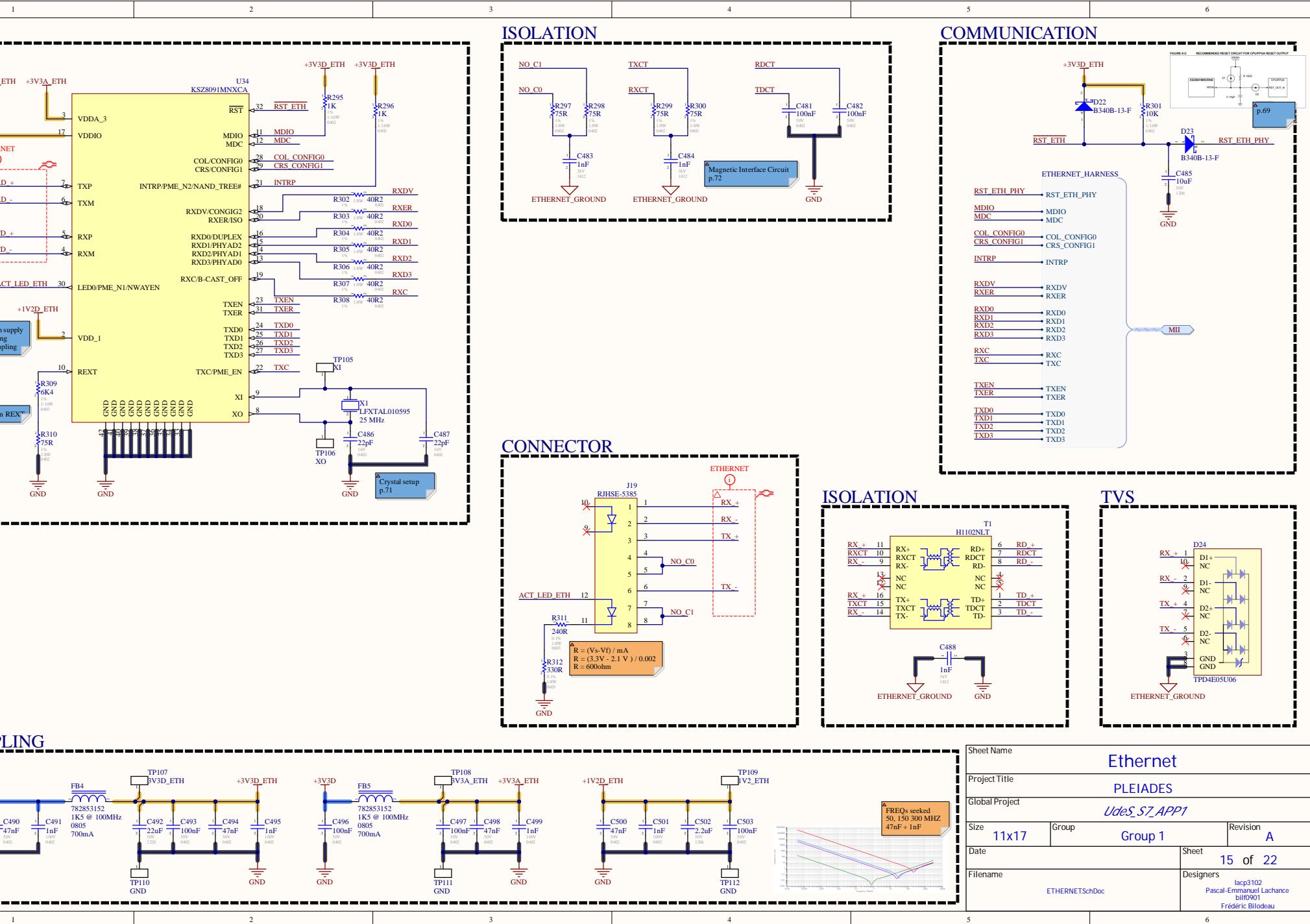
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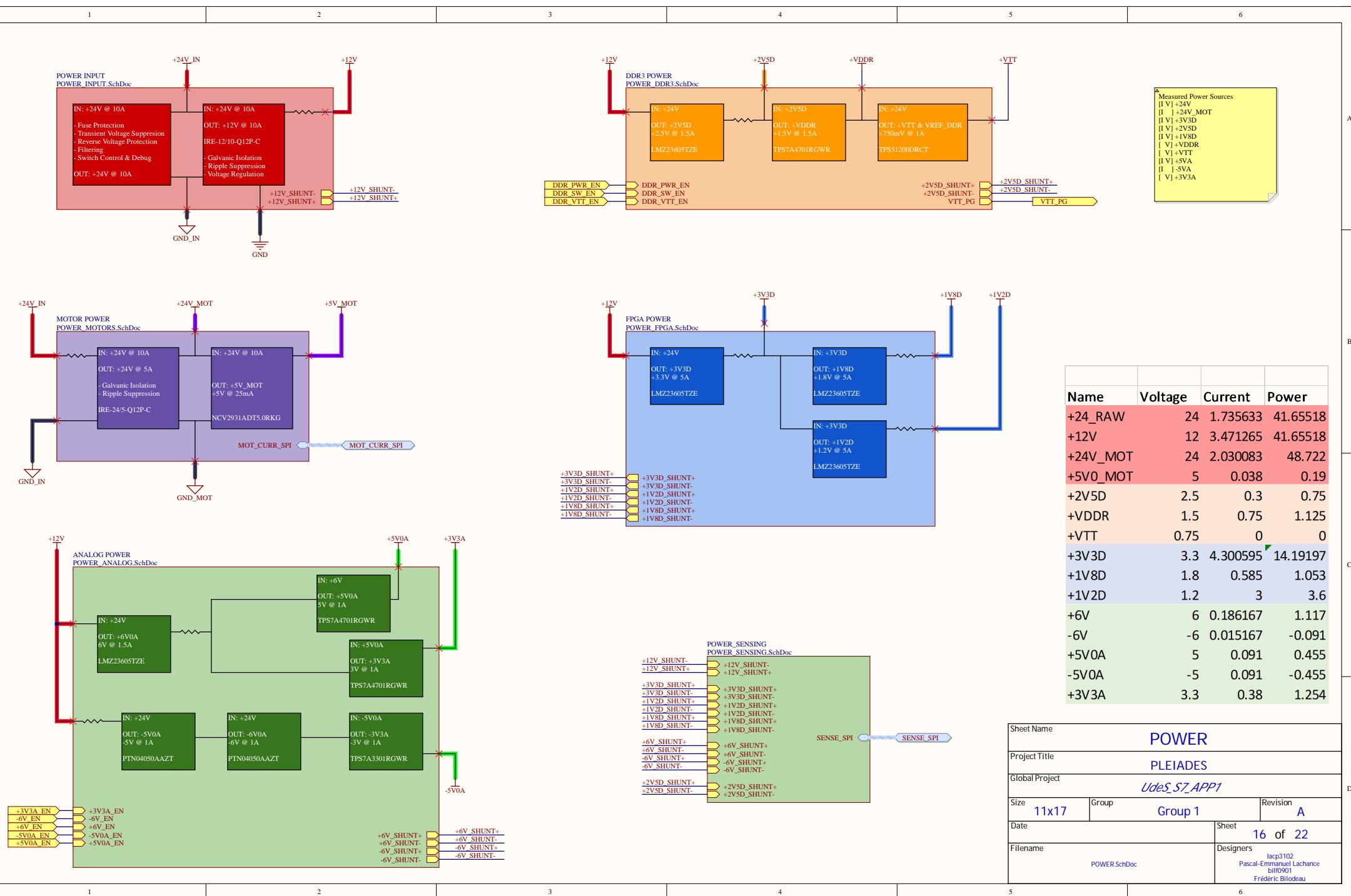


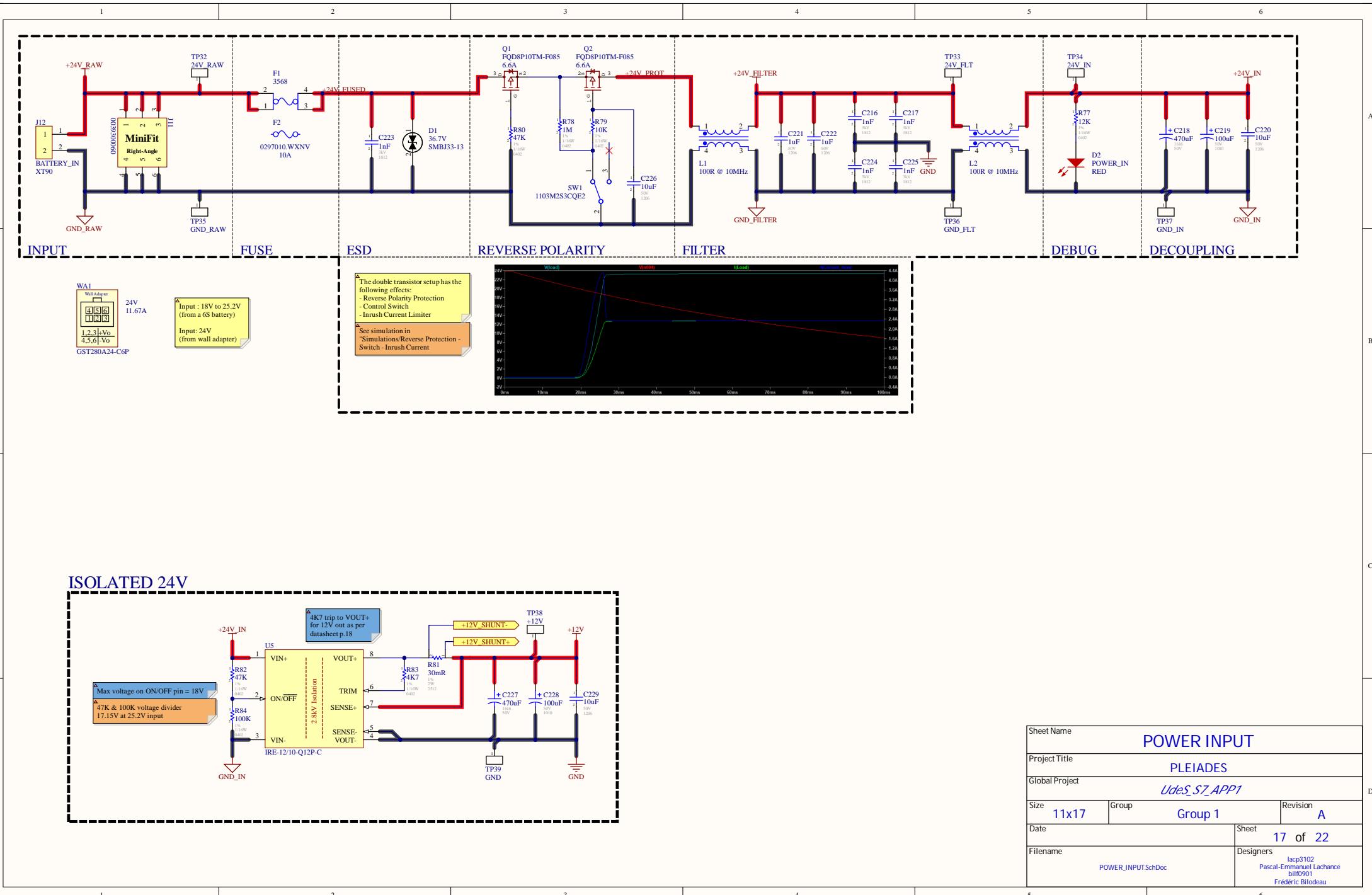
The diagram shows the connection between the main board and the BAV99-7F module for PROGRAM_B. The connections are as follows:

- Power:** +VCC_USB is connected to the BAV99-7F module.
- Reset:** TPH3 RESET is connected to the BAV99-7F module.
- Switches:** SW4 is connected to the BAV99-7F module.
- Capacitors:** C49 (4.7uF) is connected to ground.
- Diodes:** D19 (BAV99-7-F) is connected between the main board and the BAV99-7F module.
- Resistors:** R250 (100K), R294 (4.7K), and R295 (1M) are connected to ground.
- Capacitors:** C48 (100uF) is connected to ground.

Sheet Name	USB		
Project Title	PLEIADES		
Global Project	<i>UdeS.S7_APP1</i>		
Size 11x17	Group	Group 1	Revision A
Date	Sheet 14 of 22		
Filename	Designers tcp13102 Pascal-Emmanuel Lachance Dalleau Frédéric Blaisseau		
USBSchDoc			







1

2

3

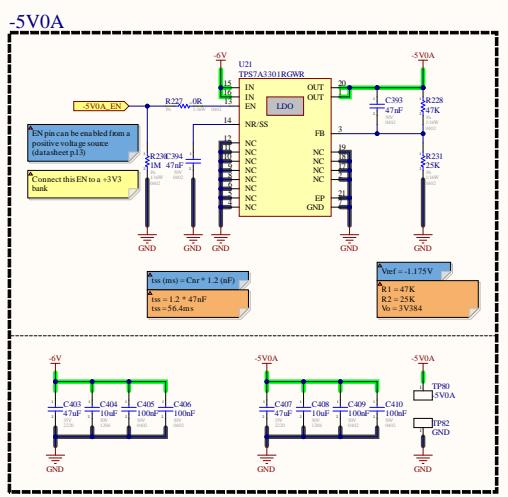
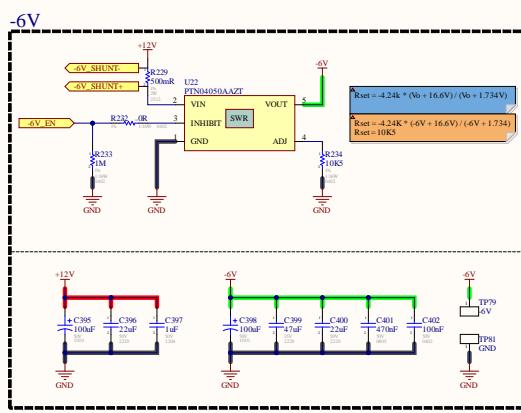
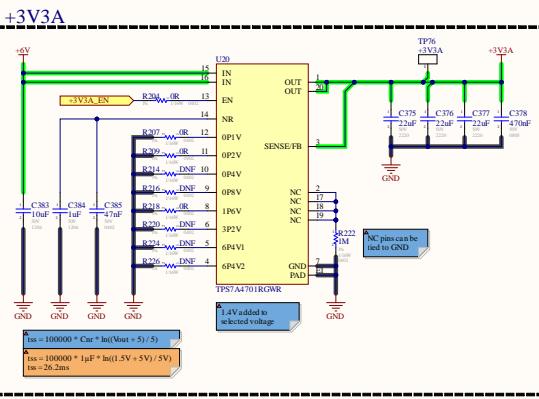
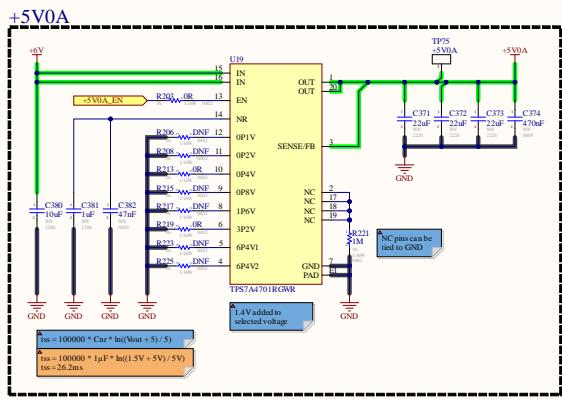
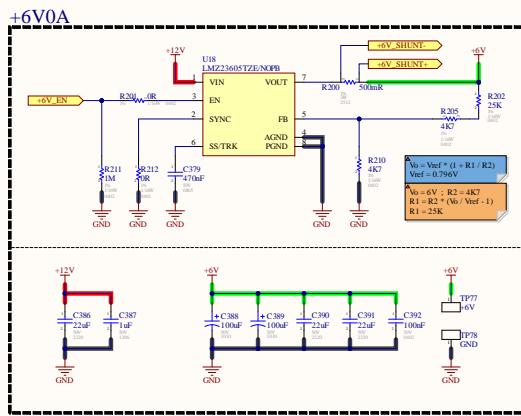
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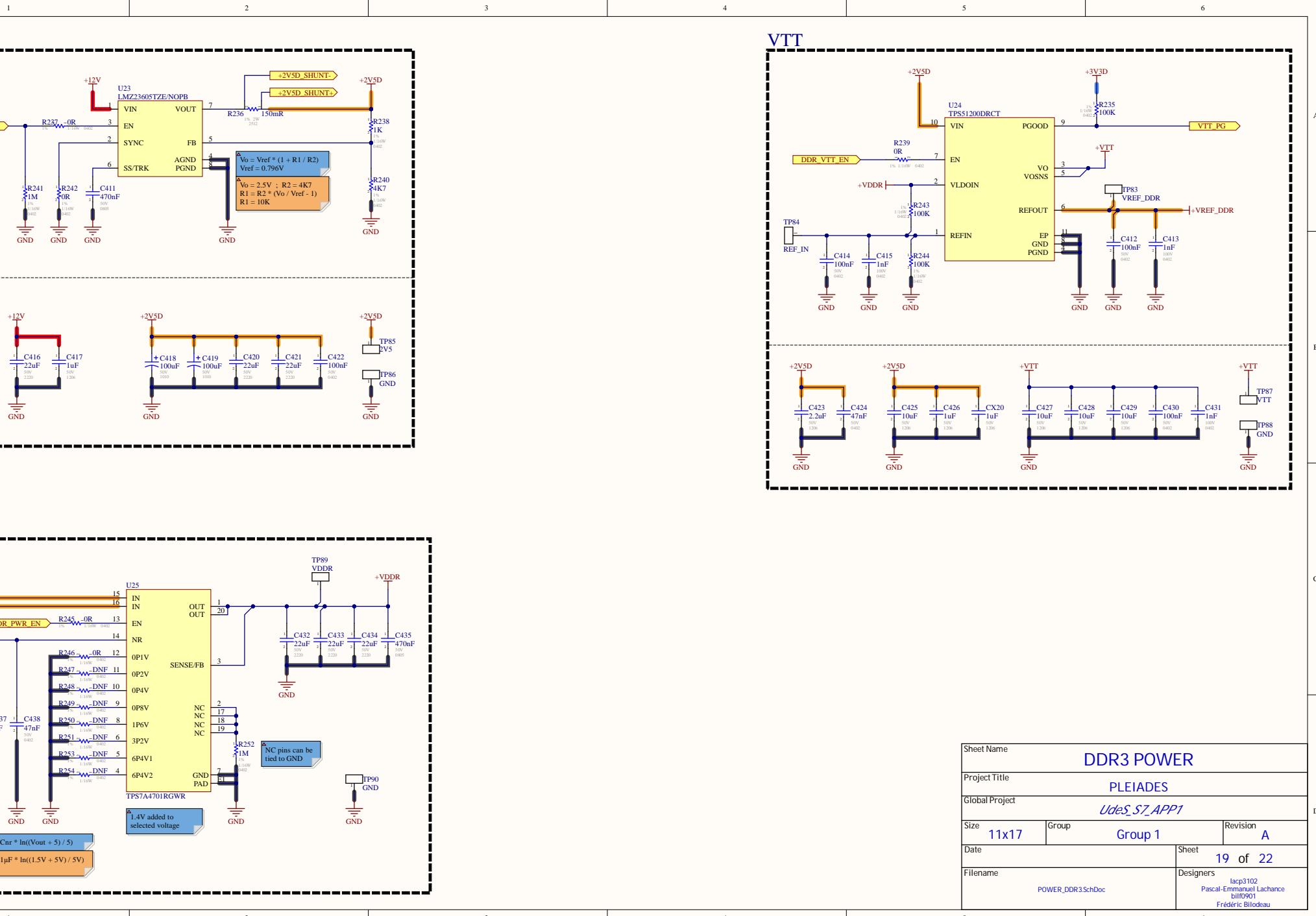
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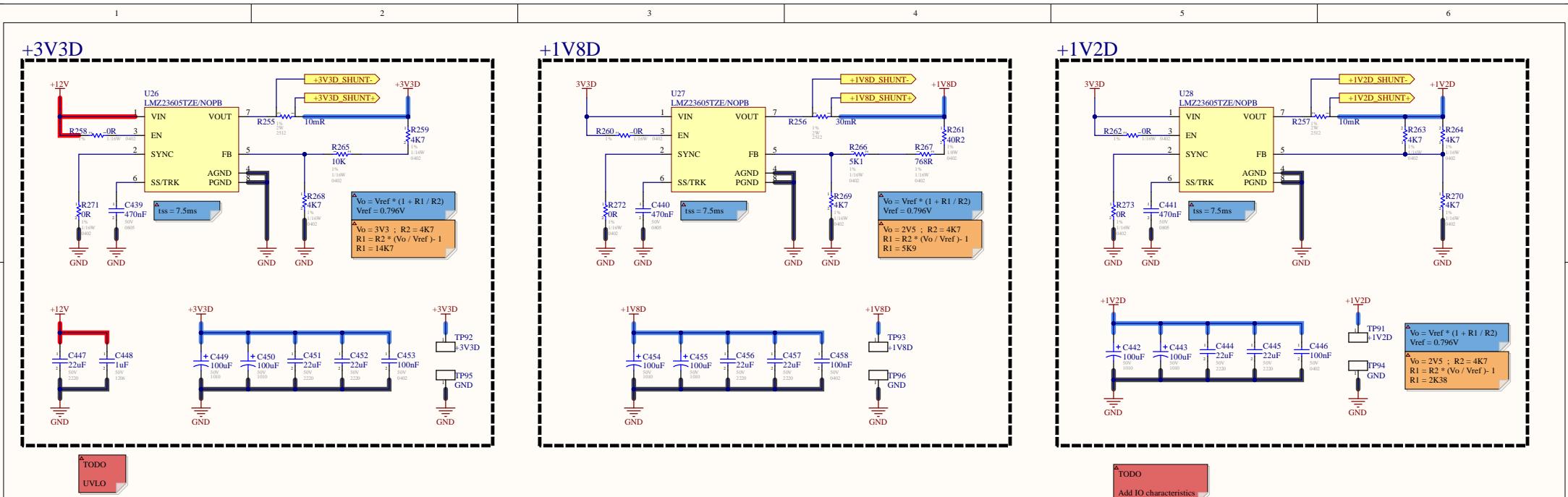
7

8



Sheet Name	POWER				
Project Title	PLEIADES				
Global Project	UdoEs_S7_APP1				
Size	11x17	Group	Group 1	Revision	A
Date	Sheet		18	of	22
Filename	POWER_ANALOGSchDoc		Designers	lasp3102 Pascal Lachance bill0901 Frédéric Blouin	





[△] UG394 p.32
The Spartan-6 FPGA can be powered up and powered down in any sequence. Because the three FPGA supply inputs must be valid to release the POR and can be supplied in any order, there is no FPGA-specific voltage sequencing requirement.

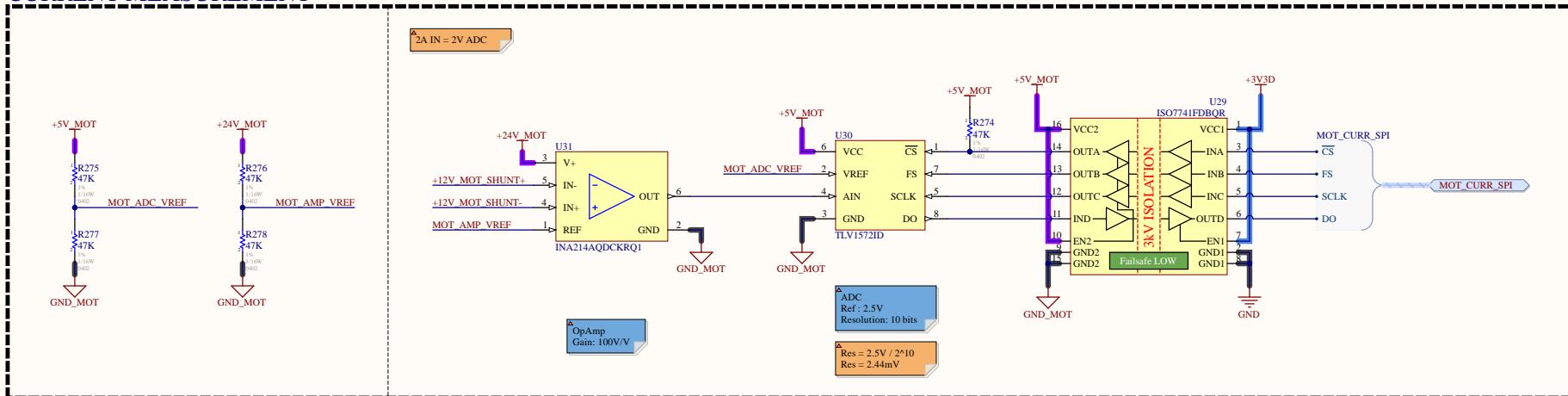
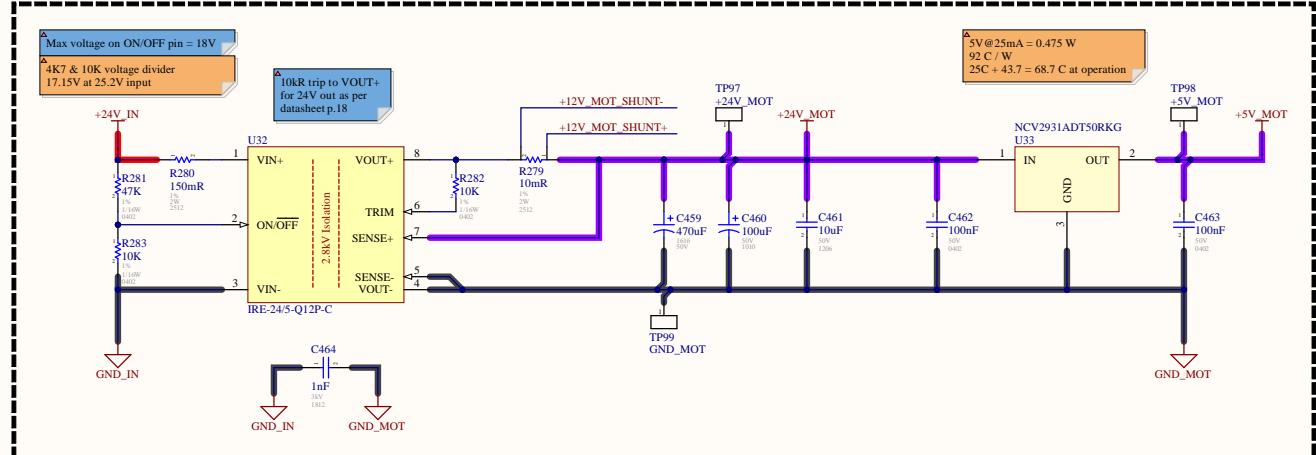
Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V _{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V _{CCO2} ⁽¹⁾	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V _{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

[△] DS162 p.7

V_{CCINT}: 3A @ 1V2D
V_{CCAUX}: 250mA @ 3V3D
V_{CCIO}: 6x 100mA @ 3V3D
6.405W

Sheet Name		POWER				
Project Title		PLEIADES				
Global Project		UdeS_S7_APP1				
Size	11x17	Group	Group 1	Revision	A	
Date					Sheet	20 of 22
Filename					Designers	Iacp3102 Pascal-Etienne Lachance bilf0901 Frédéric Bilodeau

CURRENT MEASUREMENT**ISOLATED 24V****ISOLATED 5V**

Sheet Name	POWER		
Project Title	PLEIADES		
Global Project	UdeS_S7_APP1		
Size	11x17	Group	Group 1
Date		Sheet	21 of 22
Filename	POWER_MOTORS.SchDoc		
Designers	Iacp3102 Pascal-Etienne Lachance bif0901 Frédéric Bilodeau		

