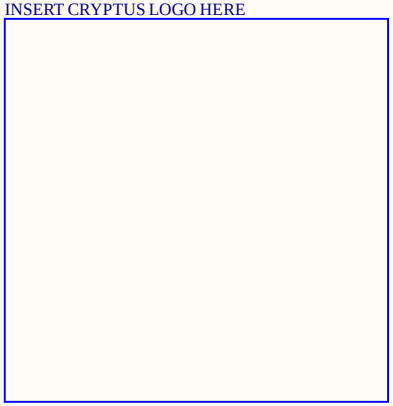
CRYPTUS

REV B

INSERT CRYPTUS LOGO HERE



PAGE	TITLE	DESCRIPTION
[1]	TITLE	COVER PAGE
[2]	INFO	DESIGN RULES, COLOR CODES, COMPONENTS USED
[3]	OVERVIEW	HIERARCHICAL VIEW
[4]	MECHANICAL	FIDUCIALS, SCREW HOLES, HEATSINKS
[5]	POWER INPUT	+24V TERMINAL BLOCK, FILTERING, REGULATION [+12V, +5V & +3.3V]
[6]	FPGA	HIERARCHICAL VIEW OF ALL FPGA PAGES
[7]	FPGA - REGULATORS	REGULATING FROM +5V to [+3.3V, +2.5V, +1.8V & +1.2V]
[8]	FPGA - POWER	CONNECTION OF POWER NETS TO FPGA, DECOUPLING AND FILTERING
[9]	FPGA - PERIPHERALS	JTAG, OSCILLATOR, FLASH & WATCHDOG
[10]	FPGA - IO	INPUTS AND OUTPUTS OF THE DIFFERENT FPGA BANKS
[11]	DDR3	HIERARCHICAL VIEW OF ALL DDR3 PAGES
[12]	DDR3 - REGULATORS	REGULATING FROM +5V to [+1.35V & +680mV]
[13]	DDR3 - POWER	CONNECTION OF POWER NETS TO DDR3, DECOUPLING AND FILTERING
[14]	DDR3 - IO	INPUTS AND OUTPUTS OF DDR3, TERMINATION
[15]	TELEMETRY	ADC MEASURE OF VOLTAGES AND CURRENTS, TEMPERATURE PROBES
[16]	QRNG	QUANTUM RANDOM NUMBER GENERATOR
[17]	SATA	SATA AND SATA POWER CONNECTORS
[18]	USB	USB-C CONNECTOR
[19]	DEBUG	LEDS, DEBUG PORT, 100dB BUZZER

INFO

COMMENT LEGEND

General Notes

Assembly, Part Locations, Fabrication, Debug Information etc.

Revisions

With author and date
To be kept on schematic for a single revision

Datasheet info

Part information, addresses, registers, pull-up/pull-downs, exerpts & tables etc.

Calculations

Values, tensions & currents, passives, etc.

TODO

Things that are left to be done, and who should do it

COLOR CODE

MECHANICAL & INFO

FPGA

DDR3

POWER

ANALOG

MISC

These components should not appear on the PCB or on the BOM.

Specified power, package and tolerances are the same for all components of the same value.

RESISTORS

DNF

	RX1	RX19	RX2	RX20	RX3	RX4	RX5	RX6	RX7	RX8	RX9	RX10	RX11	RX12	RX13	RX14	RX15	RX16	RX17	RX18
	1M	500K	100K	75K	47K	13K	10K	[Value]	3K24	2K2	1K	499R	300R	240R	100R	80R6	49R9	10R	10mR	0R
	0402	0402	0603	0402	0603	0603	0603	0603	0603	0603	0603	0402	0603	0402	0402	0402	0402	0402	2512	0603
	1/16W	1/10W	1/16W	1/10W	1/16W	1/16W	1/16W	1/16W	1/16W	1/16W	1/8W	1/8W	1/8W	1/8W	1/8W	1/8W	1/8W	1/8W	2W	1/8W
	10%	10%	10%	10%	5%	5%	10%	10%	2%	2%	5%	1%	2%	1%	10%	0.5%	0.5%	10%	1%	10%

CAPACITORS

DNF

	CX1	CX2	CX3	CX4	CX5	CX6	CX7	CX8	CX9	CX10
	47uF	47uF	4.7uF	470nF	220nF	100nF	47nF	470pF	220pF	2.2pF
	35V	1206 50V	0805 50V	0402 50V	1812 200V	0402 25V	0201 25V	0402 25V	0402 25V	0402 25V
	2917									
	T498X476K035ATE500	1206	0805	0402	1812	0402	0201	0402	0402	0402
	399-11397-1-ND	50V	50V	50V	200V	25V	25V	25V	25V	25V

OVERVIEW

POWER IN
POWER INPUT.SchDoc

TELEMTRY
TELEMETRY.SchDoc

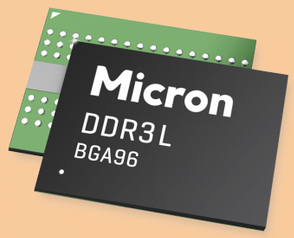
QUANTUM FUCKERY
QRNG.SchDoc

DEBUG
DEBUG.SchDoc

LATTICE ECP5 FPGA
FPGA.SchDoc

LFE5UM-45F-8BG381C

8GB DDR3
DDR3.SchDoc



MT41K512M16HA-125:A

SATA1
SATA.SchDoc

SATA2
SATA.SchDoc

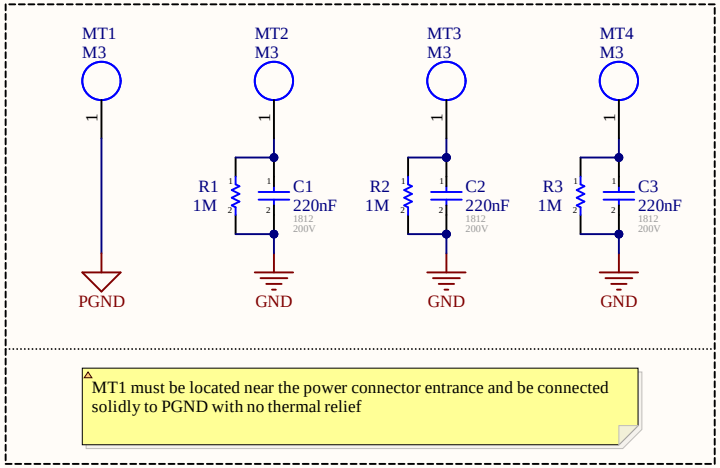
USB1
USB.SchDoc

USB2
USB.SchDoc

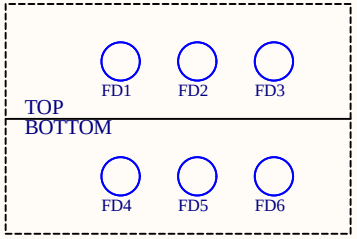
MECHANICAL
MECHANICAL.SchDoc

MECHANICAL

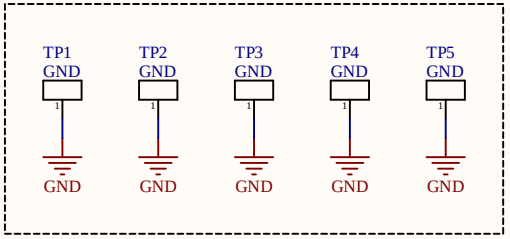
MOUNTING HOLES



FIDUCIALS

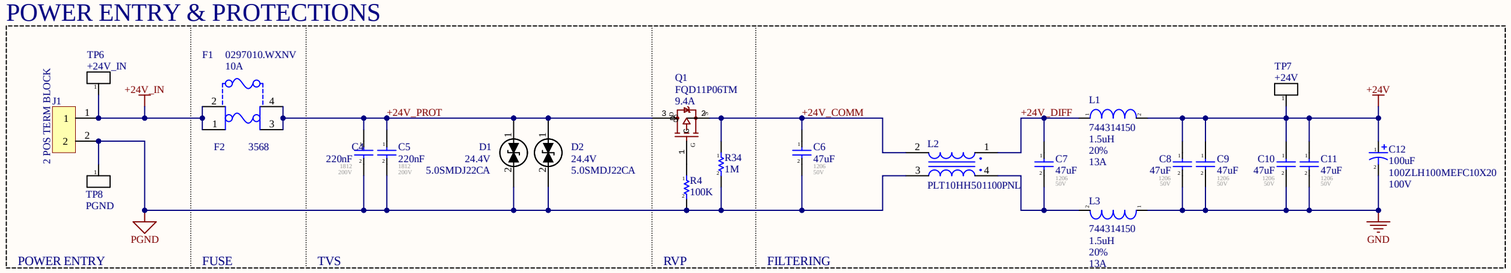


GND TESTPOINTS



POWER INPUT

POWER ENTRY & PROTECTIONS

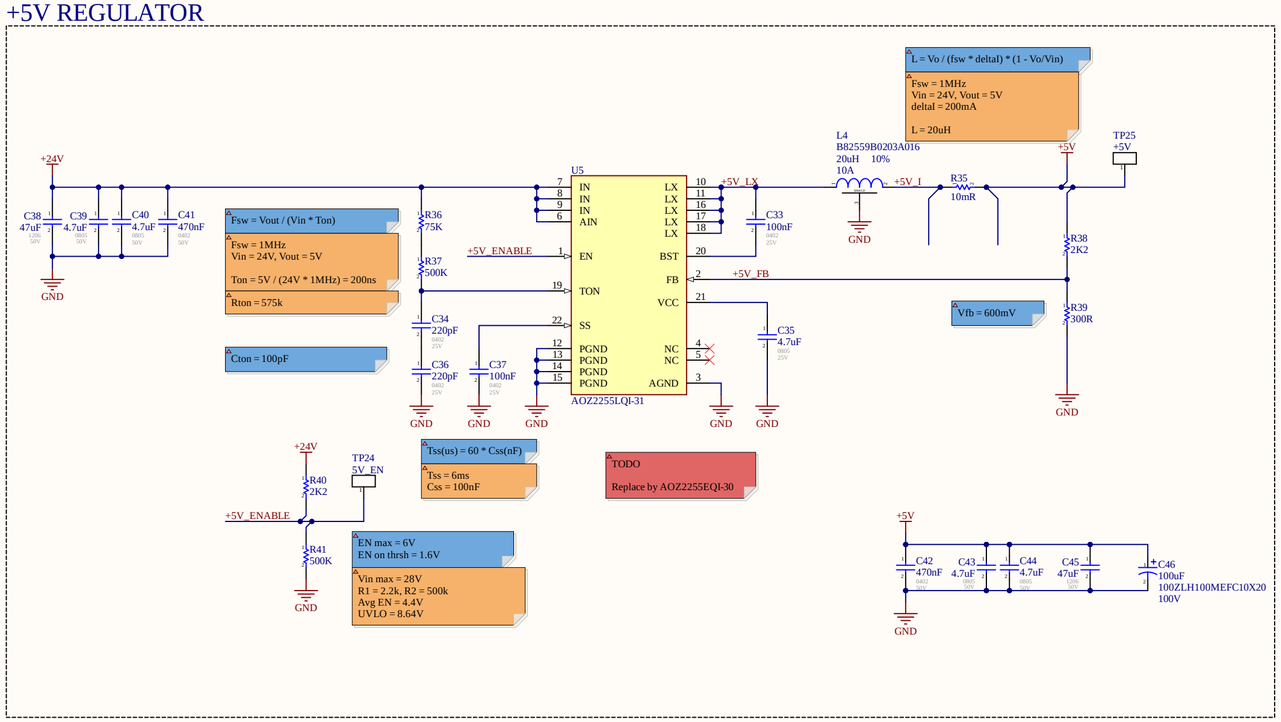


TODO

Add Zener to RVP

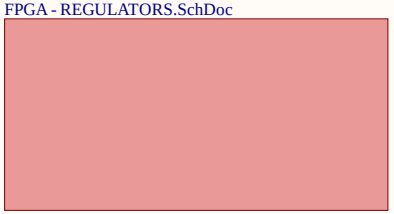
+12V REGULATOR

+5V REGULATOR

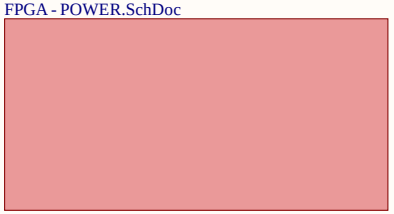


FPGA

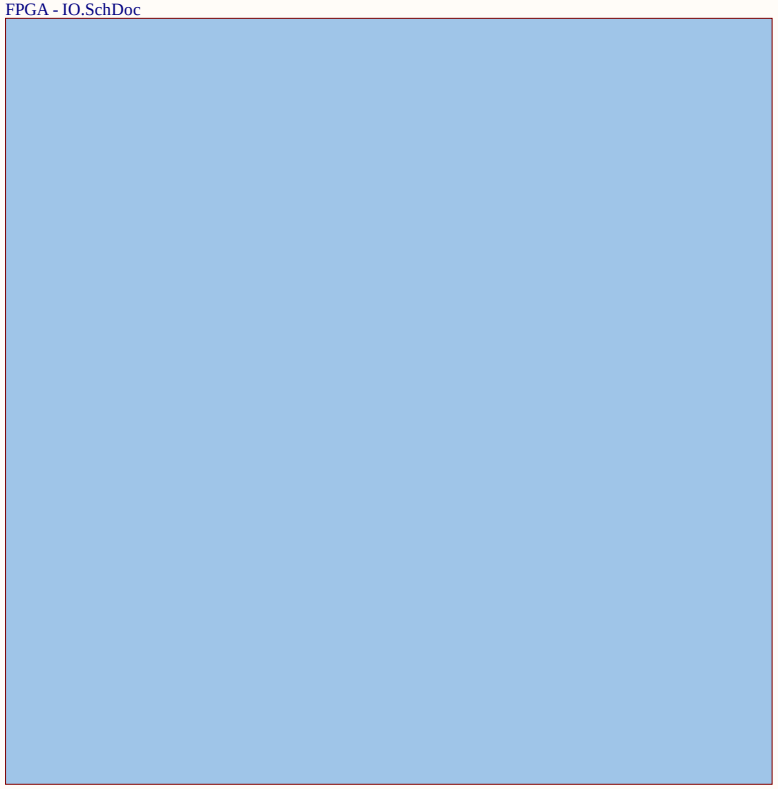
[+5V] => [+3V3, +2V5, +1V8, +1V2]
FPGA - REGULATORS.SchDoc



FPGA POWER INPUTS
FPGA - POWER.SchDoc



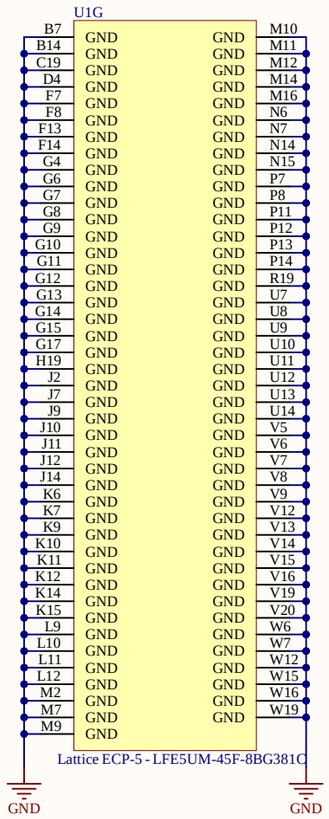
FPGA IO BANKS
FPGA - IO.SchDoc

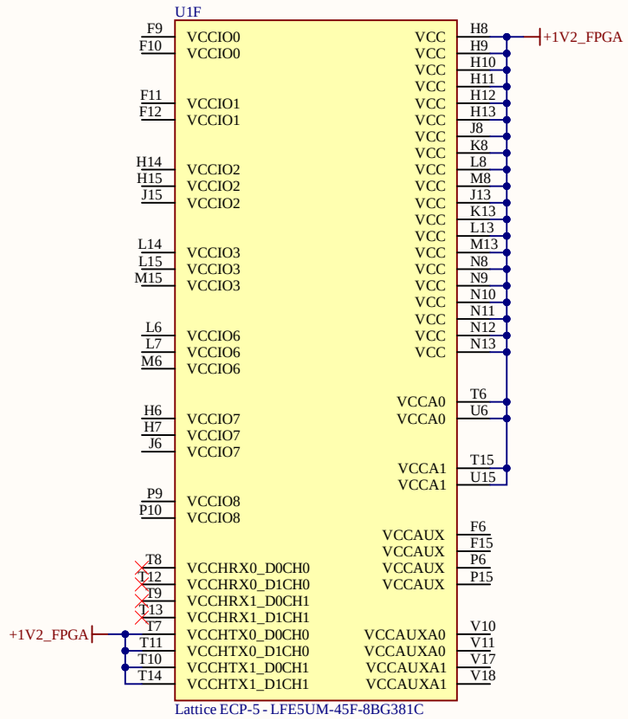


JTAG, OSCILLATOR, FLASH & WATCHDOG
FPGA - PERIPHERALS.SchDoc

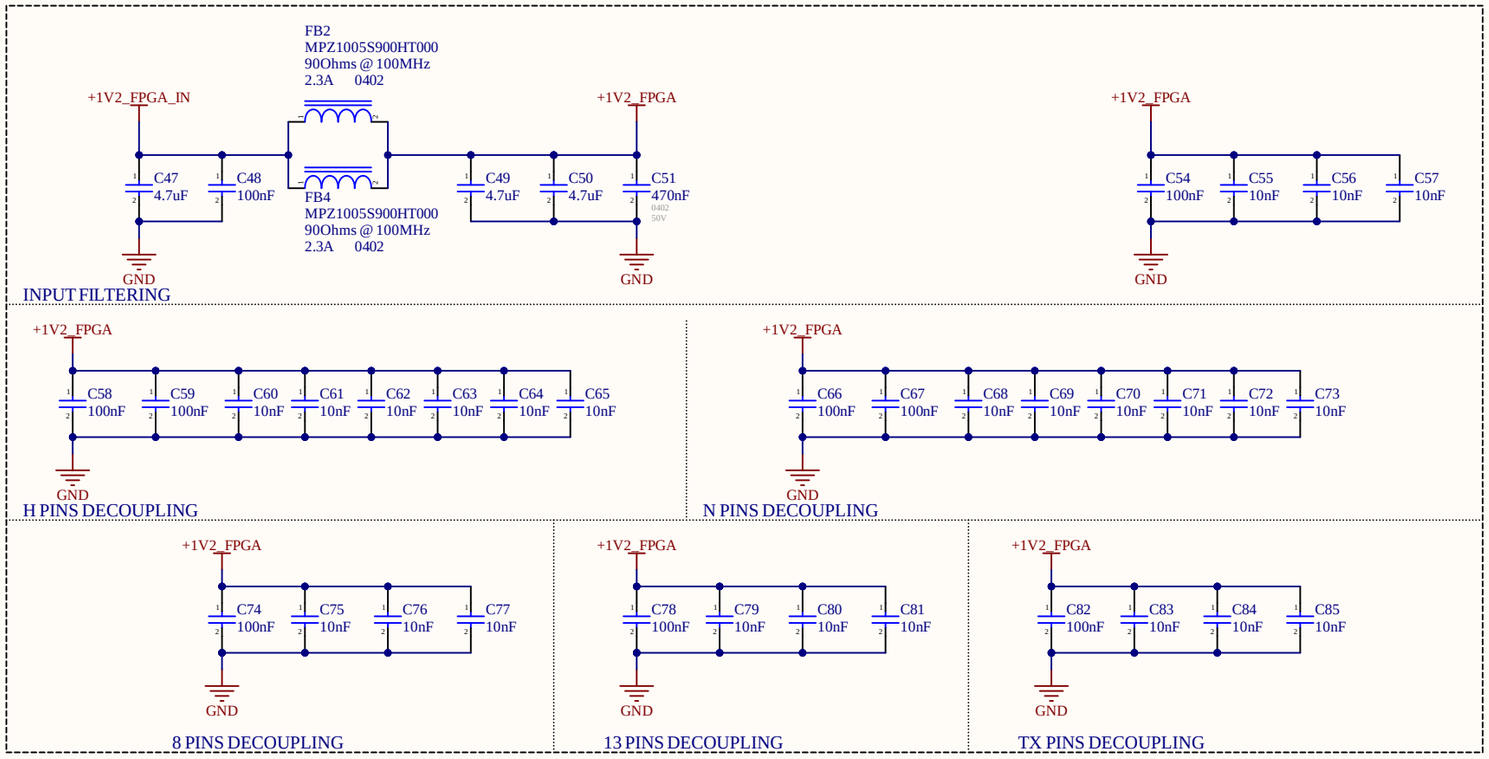
FPGA - REGULATORS

FPGA - POWER



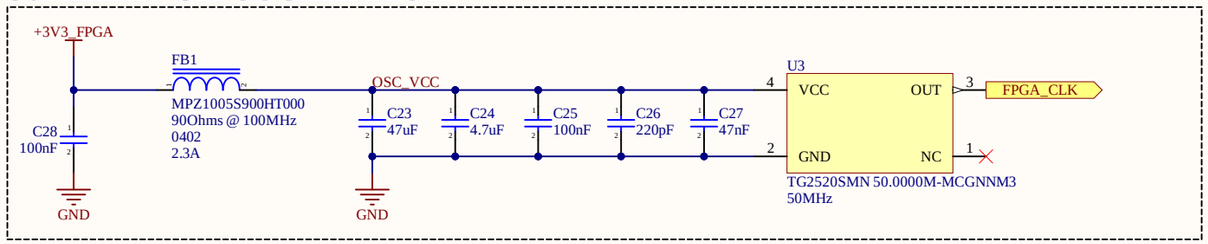


+1.2V CORE

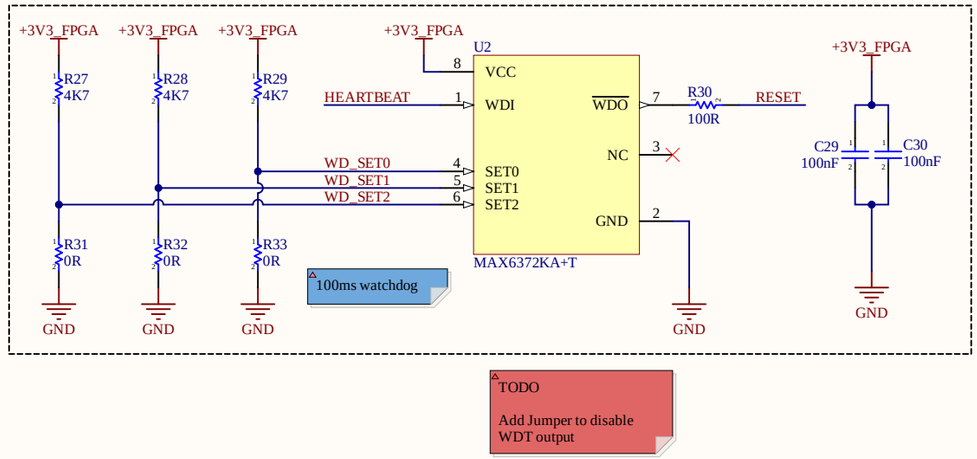


FPGA - PERIPHERALS

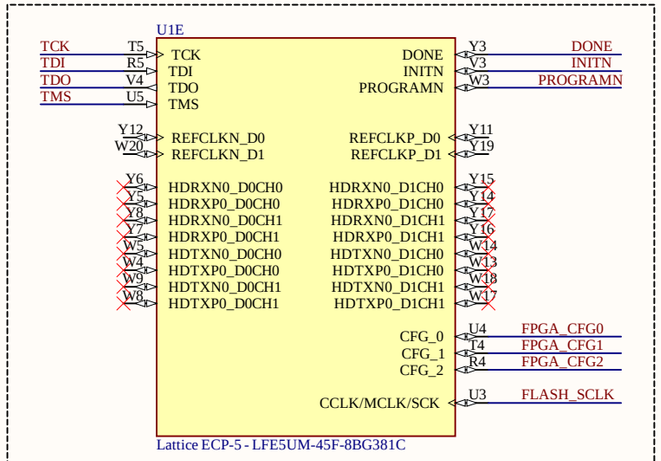
50MHZ FPGA OSCILLATOR



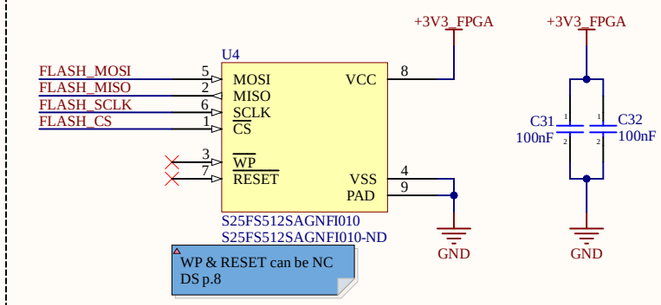
WATCHDOG TIMER



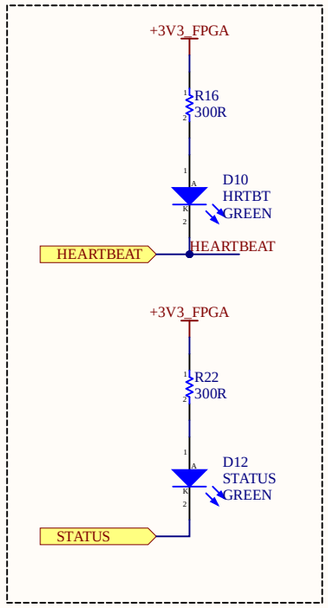
FPGA JTAG



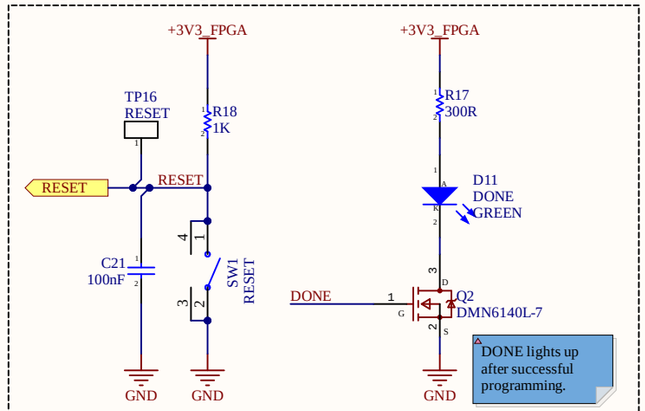
FLASH MEMORY



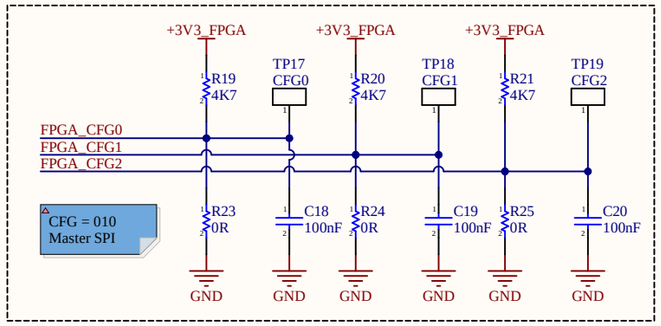
STATUS LED



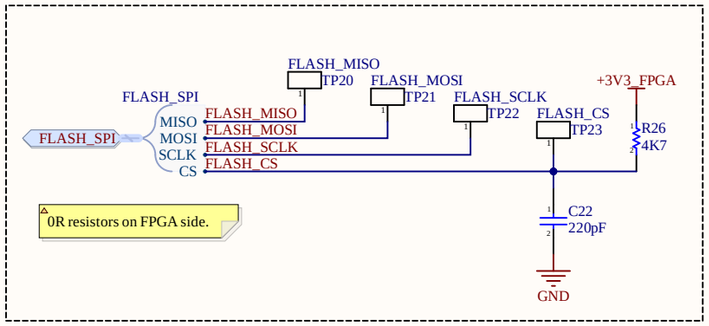
RESET & DONE



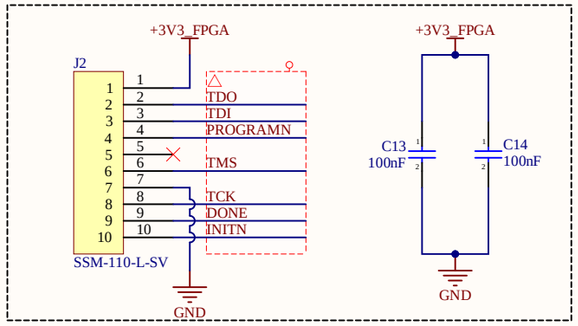
FPGA CONFIG



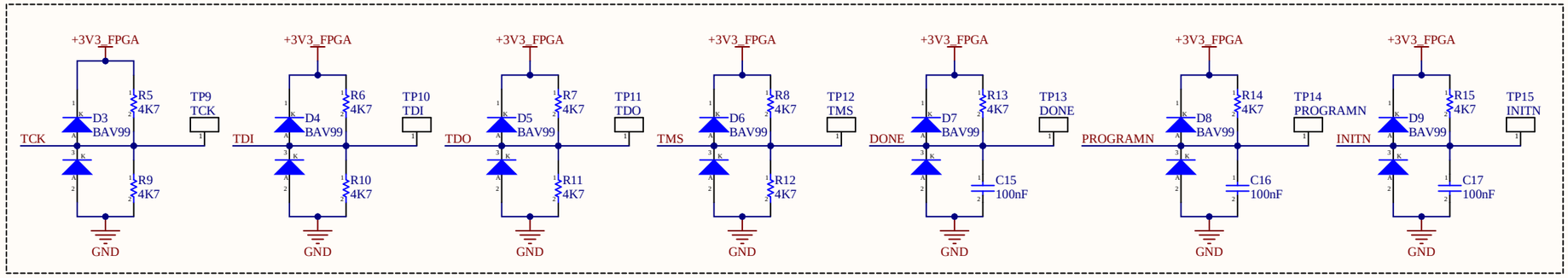
FLASH SPI HARNESS



JTAG CONNECTOR



JTAG PROTECTIONS & PULL-UP



FPGA - IO

U1A

BANK 0

A6	PT4A/ULC_GPLL1T_IN	PT47A/GR_PCLK1_0	D12
B6	PT4B/ULC_GPLL1C_IN	PT47B/GR_PCLK1_1	E12
E6	PT6A	PT49A	A12
D6	PT6B	PT49B	A13
E7	PT9A	PT51A	B13
D7	PT9B	PT51B	C13
C6	PT11A	PT53A	D13
C7	PT11B	PT53B	E13
E8	PT13A	PT56A	A14
D8	PT13B	PT56B	C14
C8	PT15A	PT58A	D14
B8	PT15B	PT58B	E14
A7	PT18A	PT67A	A15
A8	PT18B	PT69A	B15
D9	PT20A	PT69B	C15
E9	PT20B	PT71A	D15
C9	PT27A	PT71B	E15
D10	PT29A	PT74A	A16
E10	PT29B	PT74B	B16
B9	PT31A	PT76A	C16
C10	PT31B	PT76B	D16
A9	PT33A/GR_PCLK0_1	PT78A	B17
B10	PT33B/GR_PCLK0_0	PT78B	C17
A10	PT36A/PCLKT0_1	PT80A	A17
A11	PT36B/PCLKC0_1	PT80B	B18
B11	PT38A/PCLKT0_0	PT83A	A18
C11	PT38B/PCLKC0_0	PT83B	B19
D11	PT42A/PCLKT1_1	PT85A/URC_GPLL1T_IN	A19
E11	PT42B/PCLKC1_1	PT85B/URC_GPLL1C_IN	B20
B12	PT44A/PCLKT1_0		
C12	PT44B/PCLKC1_0		

Lattice ECP-5 - LFE5UM-45F-8BG381C

U1B

BANK 7

A4	PL11A/ULC_GPLL0T_IN	PL35A/PCLKT6_1	G2
A5	PL11B/ULC_GPLL0C_IN	PL35B/PCLKC6_1	F1
B5	PL11C	PL35C/PCLKT6_0	H2
C5	PL11D	PL35D/PCLKC6_0	G1
C4	PL14A	PL38A/GR_PCLK6_0	J4
B4	PL14B	PL38B	J5
A3	PL14C	PL38C/GR_PCLK6_1	J3
B3	PL14D	PL38D	G3
E4	PL17A	PL41A	K2
D5	PL17B	PL41B	J1
C3	PL17C	PL41C	H1
D3	PL17D	PL41D	K1
E4	PL20A	PL44A	K4
E5	PL20B	PL44B/VREF1_6	K5
E5	PL20C	PL44C	L4
F5	PL20D	PL44D	L5
A2	PL23A	PL53A	M5
B1	PL23B	PL59A	M4
B2	PL23C/VREF1_7	PL59B	L6
C2	PL23D	PL59C	M4
C1	PL26A	PL59D	P5
D1	PL26B	PL62A	N3
D2	PL26C	PL62B	M3
E1	PL26D	PL62C	P6
H4	PL29A/GR_PCLK7_1	PL62D	N2
G5	PL29B	PL65A	N1
H5	PL29C/GR_PCLK7_0	PL65B	M1
H3	PL29D	PL65C	L1
G3	PL32A/PCLKT7_1	PL65D	M1
F3	PL32B/PCLKC7_1	PL68A	P1
F2	PL32C/PCLKT7_0	PL68B	P2
E2	PL32D/PCLKC7_0	PL68C/LLC_GPLL0T_IN	P3
		PL68D/LLC_GPLL0C_IN	P4

Lattice ECP-5 - LFE5UM-45F-8BG381C

U1C

BANK 2

C18	PR11A/URC_GPLL0T_IN	PR35A/PCLKT3_1	L20
D17	PR11B/URC_GPLL0C_IN	PR35B/PCLKC3_1	M20
E16	PR11C	PR35C/PCLKT3_0	L19
F16	PR11D	PR35D/PCLKC3_0	M19
D18	PR14A	PR38A/GR_PCLK3_0	L16
E17	PR14B	PR38B	L17
E18	PR14C	PR38C/GR_PCLK3_1	L18
F18	PR14D	PR38D	M18
F17	PR17A	PR41A	N16
G18	PR17B	PR41B	M17
G16	PR17C	PR41C	N18
H16	PR17D	PR41D	P17
H18	PR20A	PR44A	N17
H17	PR20B	PR44B/VREF1_3	P16
J17	PR20C	PR44C	R16
J16	PR20D	PR44D	R17
C20	PR23A	PR53A	L16
D19	PR23B	PR59A	N19
D20	PR23C/VREF1_2	PR59B	N20
E19	PR23D	PR59C	P19
E20	PR26A	PR59D	P18
F19	PR26B	PR62A	P20
F20	PR26C	PR62B	R20
G20	PR26D	PR62C	T20
G19	PR29A/GR_PCLK2_1	PR62D	U20
H20	PR29B	PR65A	T19
J18	PR29C/GR_PCLK2_0	PR65B	R18
K18	PR29D	PR65C	U19
J19	PR32A/PCLKT2_1	PR65D	T18
K19	PR32B/PCLKC2_1	PR68A	U18
J20	PR32C/PCLKT2_0	PR68B	U17
K20	PR32D/PCLKC2_0	PR68C/LRC_GPLL0T_IN	U16
		PR68D/LRC_GPLL0C_IN	T17

Lattice ECP-5 - LFE5UM-45F-8BG381C

U1D

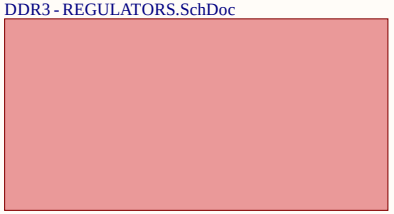
BANK 8

R1	PB4A/D7/IO7
T1	PB4B/D6/IO6
U1	PB6A/D5/MISO2/IO5
V1	PB6B/D4/MOSI2/IO4
W1	PB9A/D3/IO3
Y2	PB9B/D2/IO2
V2	PB11A/D1/MISO/IO1
W2	PB11B/D0/MOSI/IO0
T2	PB13A/SN/CSN
U2	PB13B/CS1N
R2	PB15A/HOLDN/DI/BUSY/CSSPIN/CEN
R3	PB15B/DOUT/CSON
T3	PB18A/WRITEN

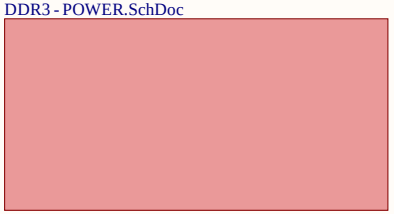
Lattice ECP-5 - LFE5UM-45F-8BG381C

DDR3

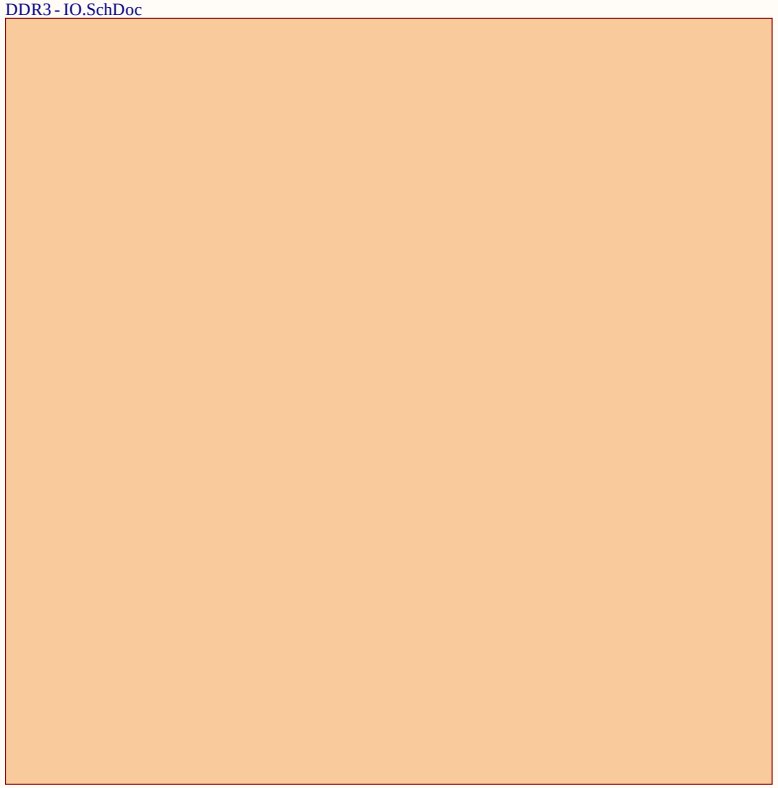
[+5V] => [+1V35, +VTT, +VREF]
DDR3 - REGULATORS.SchDoc



DDR3 POWER INPUTS
DDR3 - POWER.SchDoc



DDR3 IO & TERMINATIONS
DDR3 - IO.SchDoc

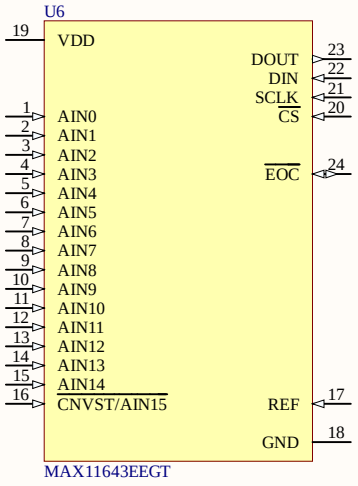


DDR3 - REGULATORS

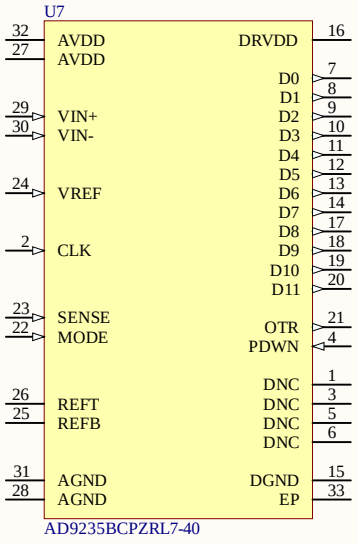
DDR3 - POWER

DDR3 - IO

TELEMETRY


U6
19
VDD
1
AIN0
2
AIN1
3
AIN2
4
AIN3
5
AIN4
6
AIN5
7
AIN6
8
AIN7
9
AIN8
10
AIN9
11
AIN10
12
AIN11
13
AIN12
14
AIN13
15
AIN14
16
CNVST/AIN15
DOUT
23
DIN
22
SCLK
21
CS
20
EOC
24
REF
17
GND
18
MAX11643EEGT

QRNG


U7
32
27
AVDD
AVDD
29
30
VIN+
VIN-
24
VREF
2
CLK
23
22
SENSE
MODE
26
25
REFT
REFB
31
28
AGND
AGND
DRVDD
16
D0
D1
D2
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PDWN
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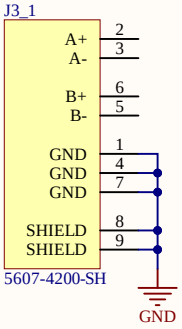
SATA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A+
A-
B+
B-
GND
GND
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SHIELD
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3
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7
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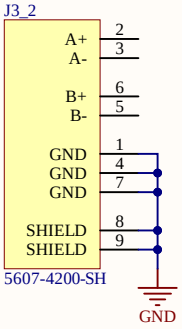
9
5607-4200-SH
GND

SATA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A-
B+
B-
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SHIELD
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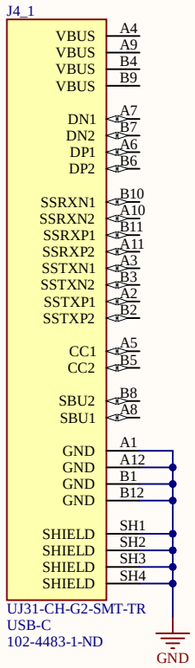
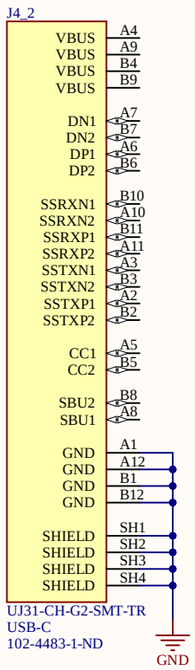
1
4
7
8
9
5607-4200-SH
GND

USB


J4_1
VBUS
VBUS
VBUS
VBUS
DN1
DN2
DP1
DP2
SSRXN1
SSRXN2
SSRXP1
SSRXP2
SSTXN1
SSTXN2
SSTXP1
SSTXP2
CC1
CC2
SBU2
SBU1
GND
GND
GND
GND
SHIELD
SHIELD
SHIELD
SHIELD
A4
A9
B4
B9
A7
B7
A6
B6
B10
A10
B11
A11
A3
B3
A2
B2
A5
B5
B8
A8
A1
A12
B1
B12
SH1
SH2
SH3
SH4
UJ31-CH-G2-SMT-TR
USB-C
102-4483-1-ND
GND

USB


J4_2
VBUS
VBUS
VBUS
VBUS
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DN2
DP1
DP2
SSRXN1
SSRXN2
SSRXP1
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SSTXN1
SSTXN2
SSTXP1
SSTXP2
CC1
CC2
SBU2
SBU1
GND
GND
GND
GND
SHIELD
SHIELD
SHIELD
SHIELD
A4
A9
B4
B9
A7
B7
A6
B6
B10
A10
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A11
A3
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A2
B2
A5
B5
B8
A8
A1
A12
B1
B12
SH1
SH2
SH3
SH4
UJ31-CH-G2-SMT-TR
USB-C
102-4483-1-ND
GND

DEBUG