

123456

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CRYPTUS

MOTHERBOARD

REV. 1-A

COMMENT LEGEND

- General Notes

Assembly, Part Locations, Fabrication, Debug Information etc.
- Revisions

With author and date  
To be kept on schematic for a single revision
- Datasheet info

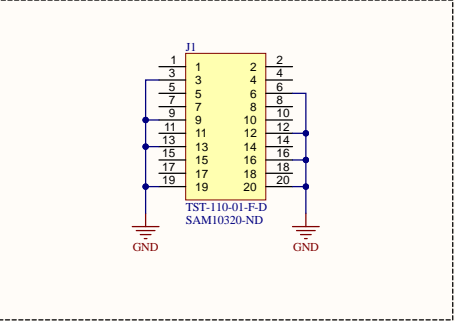
Part information, addresses, registers, pull-up/pull-downs, excerpts & tables etc.
- Calculations

Values, tensions & currents, passives, etc.

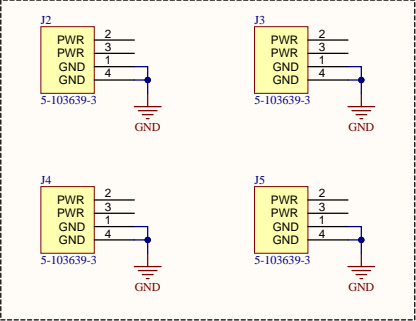
		PROJECT		CryptUS_Motherboard	
		TITLE		★	
*					
*					
*	SIZE	DWG NO.		REV	
*	A3				
		FILE NAME		SHEET	1 OF 7
		Title.SchDoc			

56

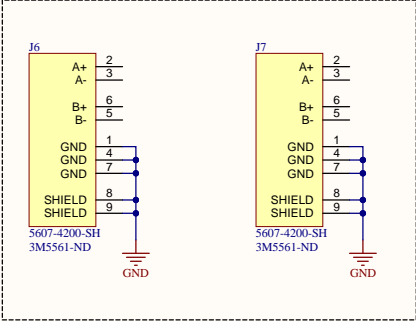
MAIN 20-PIN CONNECTOR



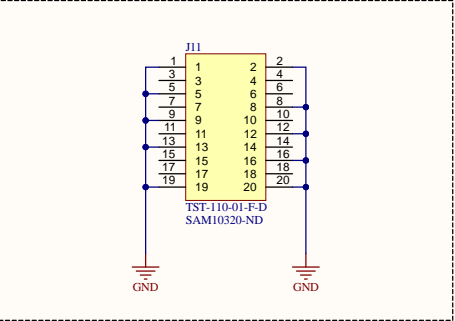
4-PIN POWER CONNECTORS



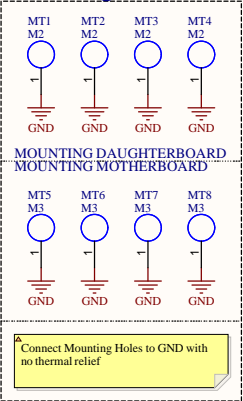
SATA CONNECTORS



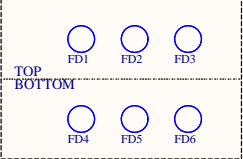
ADC 20-PIN CONNECTOR



Mounting Holes

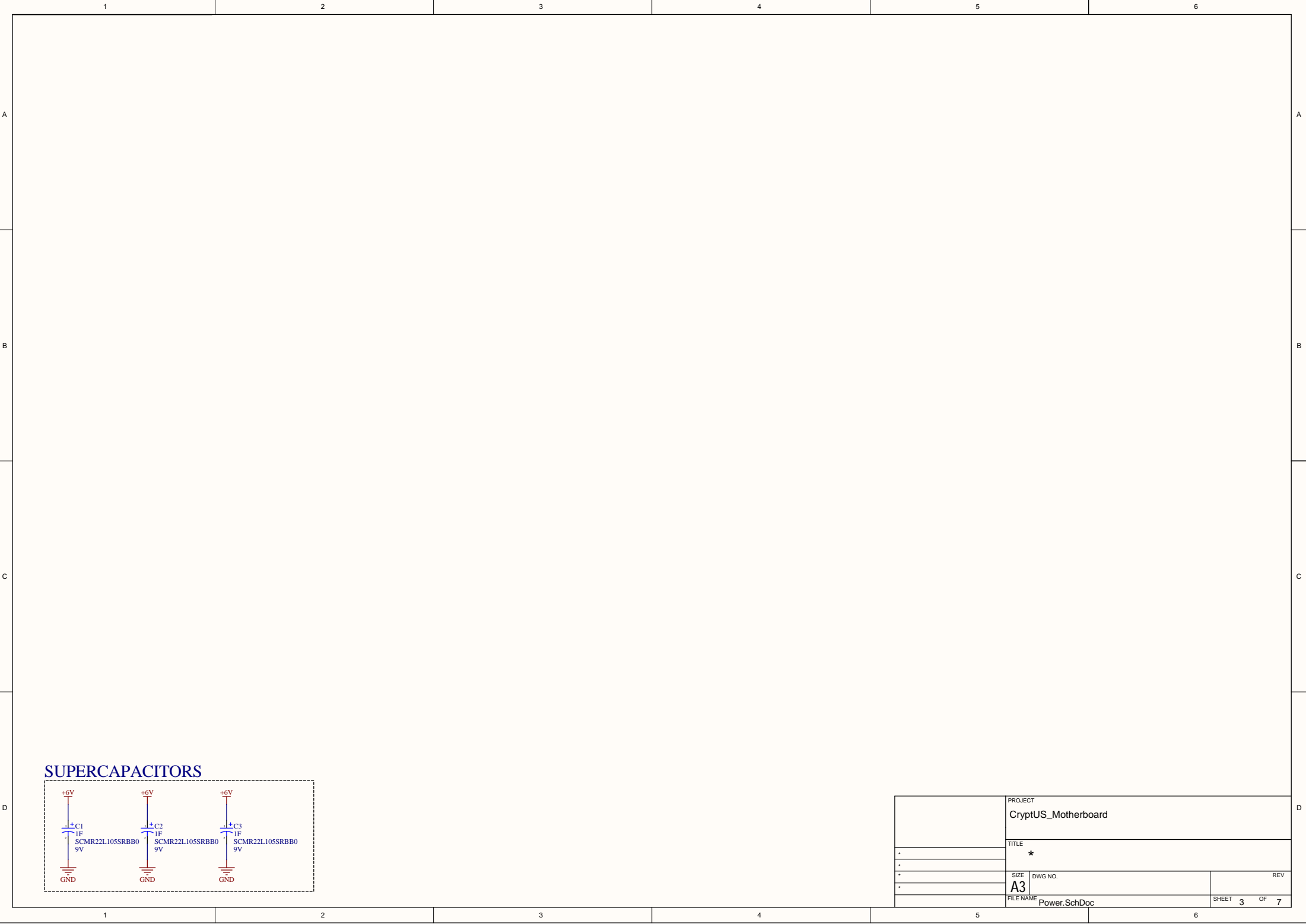


Fiducials

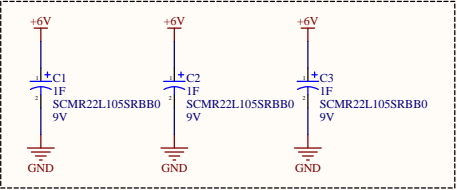


Connect Mounting Holes to GND with no thermal relief

PROJECT		CryptUS_Motherboard	
TITLE		Mechanical and Interconnect	
CryptUS	SIZE	DWG NO.	REV
Pascal-Emmanuel Lachance	A3		
Benjamin Gélinas	FILE NAME	Mechanical and Interconnect.SchDoc	SHEET 2 OF 7



SUPERCAPACITORS



		PROJECT		CryptUS_Motherboard		
		TITLE		★		
		SIZE	DWG NO.		REV	
		A3				
		FILE NAME		Power.SchDoc		
				SHEET 3 OF 7		

A

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C

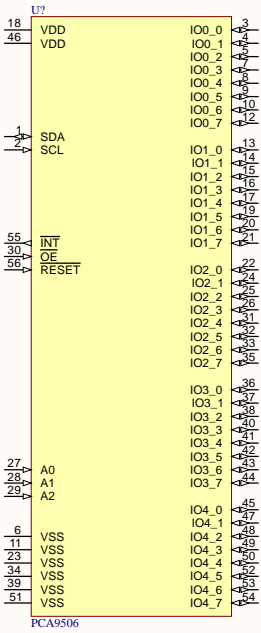
D

A

B

C

D



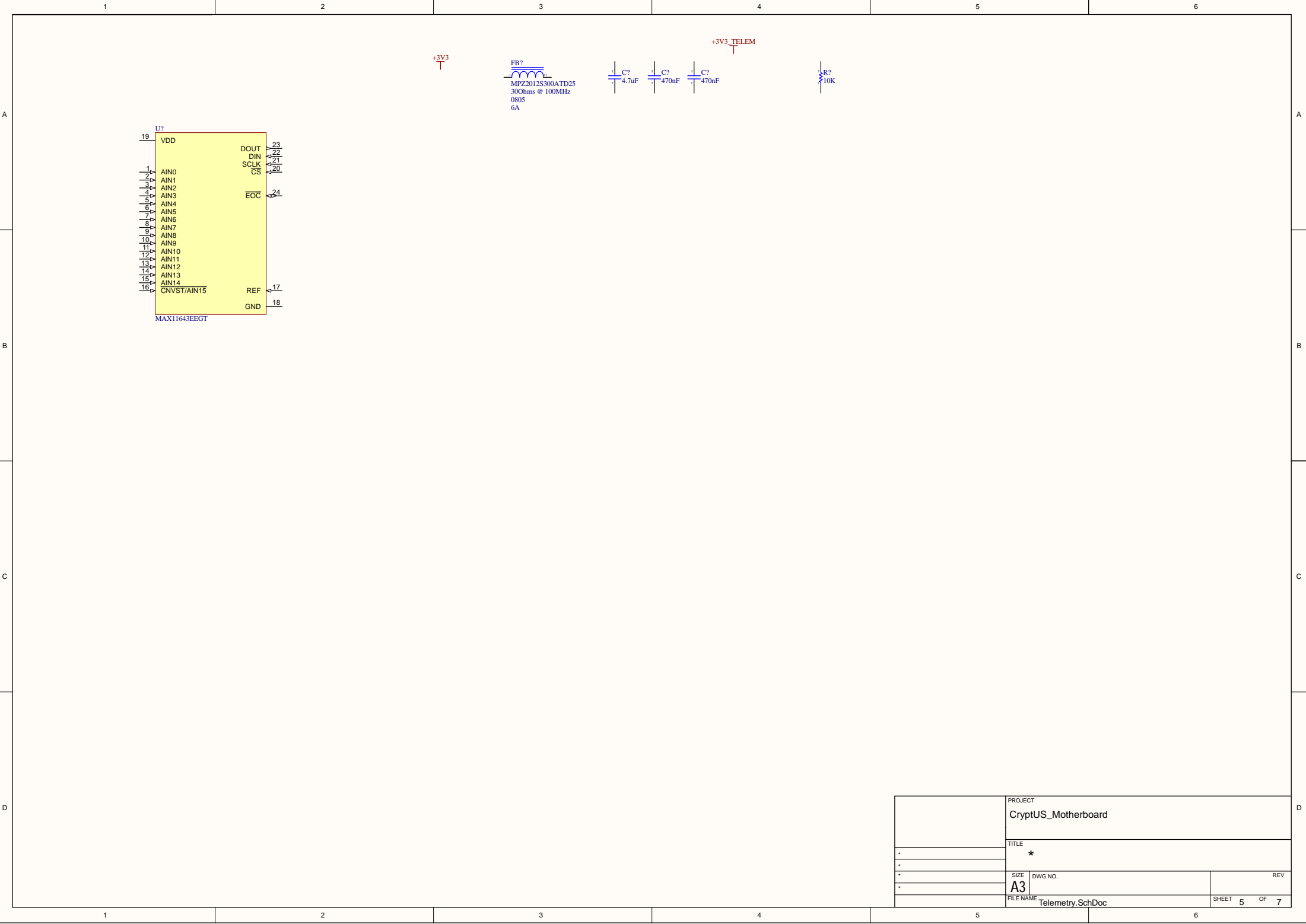
+3V3



+3V3\_IO



PROJECT		CryptUS_Motherboard	
TITLE		★	
SIZE	DWG NO.	REV	
A3			
FILE NAME	IO Extender.SchDoc		SHEET 4 OF 7



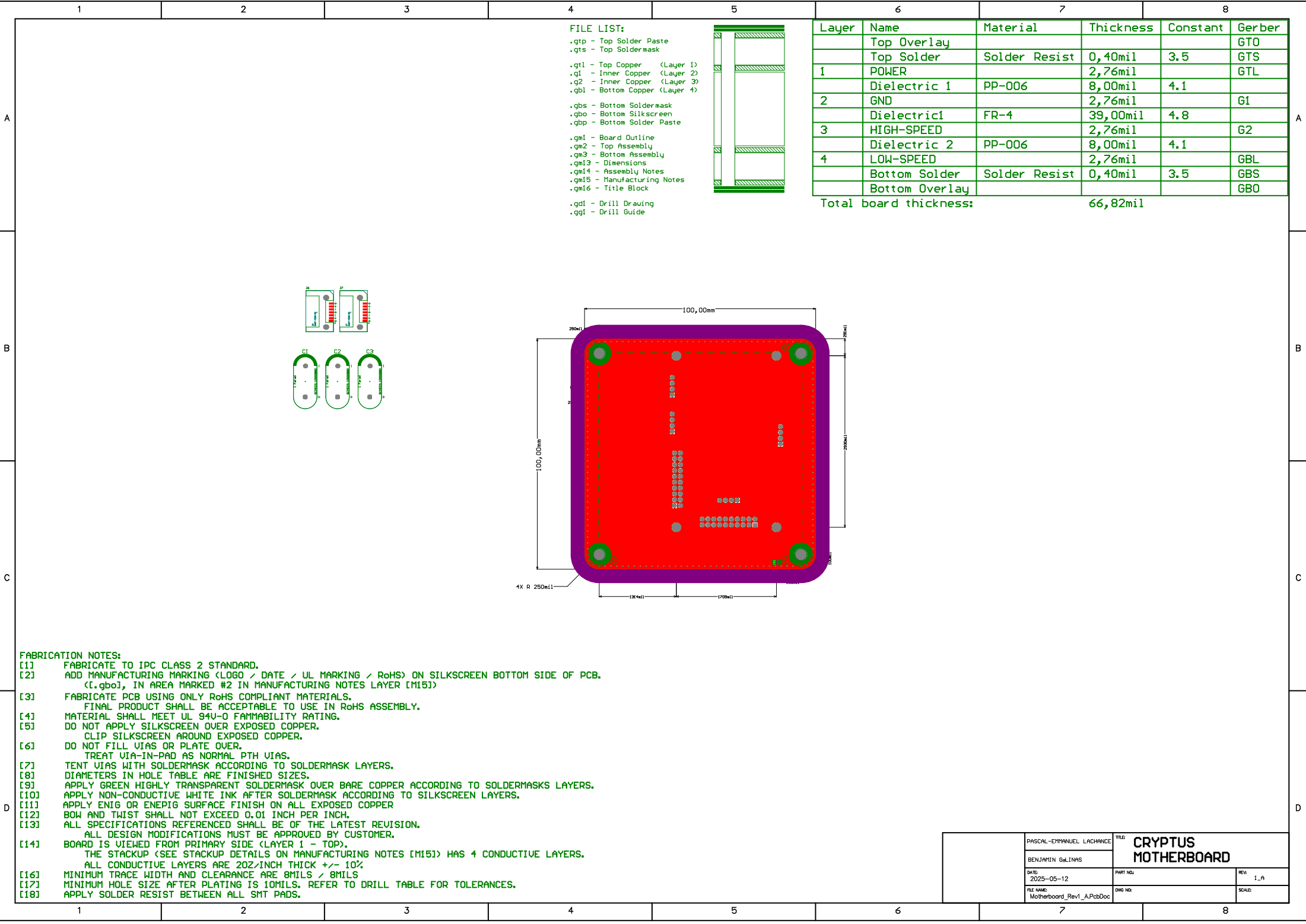
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		CryptUS_Motherboard		
		TITLE		
		★		
*		SIZE	DWG NO.	
*				
*		REV		
*				
FILE NAME		SHEET 5 OF 7		
Telemetry.SchDoc				

1	2	3	4	5	6
A					A
B					B
C					C
D					D
1	2	3	4	5	6

		PROJECT	
		CryptUS_Motherboard	
TITLE		★	
*			
*			
*			
*			
SIZE		DWG NO.	REV
A3			
FILE NAME		QRNG.SchDoc	SHEET 6 OF 7

1	2	3	4	5	6
A					A
B					B
C					C
D					D
1	2	3	4	5	6

		PROJECT CryptUS_Motherboard	
		TITLE ★	
*			
*			
*			
*		SIZE A3	DWG NO.
		REV	
		FILE NAME Debug.SchDoc	SHEET 7 OF 7



FILE LIST:

- .gtp - Top Solder Paste
- .gts - Top Soldermask
- .gtl - Top Copper (Layer 1)
- .q1 - Inner Copper (Layer 2)
- .q2 - Inner Copper (Layer 3)
- .qbl - Bottom Copper (Layer 4)
- .gbs - Bottom Soldermask
- .gbo - Bottom Silkscreen
- .gbp - Bottom Solder Paste
- .qml - Board Outline
- .qm2 - Top Assembly
- .qm3 - Bottom Assembly
- .qml3 - Dimensions
- .qml4 - Assembly Notes
- .qml5 - Manufacturing Notes
- .qml6 - Title Block
- .qdt - Drill Drawing
- .qgl - Drill Guide

Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	Solder Resist	0,40mil	3.5	GTS
1	POWER		2,76mil		GTL
	Dielectric 1	PP-006	8,00mil	4.1	
2	GND		2,76mil		G1
	Dielectric1	FR-4	39,00mil	4.8	
3	HIGH-SPEED		2,76mil		G2
	Dielectric 2	PP-006	8,00mil	4.1	
4	LOW-SPEED		2,76mil		GBL
	Bottom Solder	Solder Resist	0,40mil	3.5	GBS
	Bottom Overlay				GBO

Total board thickness: 66,82mil

FABRICATION NOTES:

- [1] FABRICATE TO IPC CLASS 2 STANDARD.
- [2] ADD MANUFACTURING MARKING (LOGO / DATE / UL MARKING / RoHS) ON SILKSCREEN BOTTOM SIDE OF PCB. ([.gbo], IN AREA MARKED #2 IN MANUFACTURING NOTES LAYER [M15])
- [3] FABRICATE PCB USING ONLY RoHS COMPLIANT MATERIALS. FINAL PRODUCT SHALL BE ACCEPTABLE TO USE IN RoHS ASSEMBLY.
- [4] MATERIAL SHALL MEET UL 94V-0 FMMABILITY RATING.
- [5] DO NOT APPLY SILKSCREEN OVER EXPOSED COPPER. CLIP SILKSCREEN AROUND EXPOSED COPPER.
- [6] DO NOT FILL VIAS OR PLATE OVER. TREAT VIA-IN-PAD AS NORMAL PTH VIAS.
- [7] TENT VIAS WITH SOLDERMASK ACCORDING TO SOLDERMASK LAYERS.
- [8] DIAMETERS IN HOLE TABLE ARE FINISHED SIZES.
- [9] APPLY GREEN HIGHLY TRANSPARENT SOLDERMASK OVER BARE COPPER ACCORDING TO SOLDERMASKS LAYERS.
- [10] APPLY NON-CONDUCTIVE WHITE INK AFTER SOLDERMASK ACCORDING TO SILKSCREEN LAYERS.
- [11] APPLY ENIG OR ENEPIG SURFACE FINISH ON ALL EXPOSED COPPER
- [12] BOW AND TWIST SHALL NOT EXCEED 0.01 INCH PER INCH.
- [13] ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION. ALL DESIGN MODIFICATIONS MUST BE APPROVED BY CUSTOMER.
- [14] BOARD IS VIEWED FROM PRIMARY SIDE (LAYER 1 - TOP). THE STACKUP (SEE STACKUP DETAILS ON MANUFACTURING NOTES [M15]) HAS 4 CONDUCTIVE LAYERS. ALL CONDUCTIVE LAYERS ARE 20Z/INCH THICK +/- 10%
- [16] MINIMUM TRACE WIDTH AND CLEARANCE ARE 8MILS / 8MILS
- [17] MINIMUM HOLE SIZE AFTER PLATING IS 10MILS. REFER TO DRILL TABLE FOR TOLERANCES.
- [18] APPLY SOLDER RESIST BETWEEN ALL SMT PADS.

PASCAL-EMMANUEL LACHANCE		TITLE: CRYPTUS MOTHERBOARD	
BENJAMIN GALINAS		PART NO:	
DATE: 2025-05-12		REV: 1_A	
FILE NAME: Motherboard_Rev1_A.PcbDoc		SCALE:	



Comment	Description	Designator	Footprint	LibRef	Quantity
1F	CAP 1F -10%+30%9V T/H	C1, C2, C3	SCMR22L105SRBB0	CAP_SCMR22L105SRB B0	3
4.7uF	Generic SMT Ceramic Capacitor	C?	CAP_0805	CAP_CER	2
100nF	Generic SMT Ceramic Capacitor	C?	CAP_0402	CAP_CER	1
470nF	Generic SMT Ceramic Capacitor	C?	CAP_0402	CAP_CER	4
MPZ2012S300ATD25	30 Ohms @ 100 MHz 1 Power Line Ferrite Bead 0805 (2012 Metric) 6A 10mOhm	FB?	IND_0805	IND_MPZ2012S300ATD 25	2
FIDUCIAL		FD1, FD2, FD3, FD4, FD5, FD6	FIDUCIAL	FIDUCIAL	6
TST-110-01-F-D	CONN HEADER VERT 20POS2.54MM	J1, J11	TST-110-01-F-D	CONN_TST-100-01-F- D	2
5-103639-3	CONN HEADER VERT 4POS2.54MM	J2, J3, J4, J5	5-103639-3	CONN_5-103639-3	4
5607-4200-SH	7 Position SATA Plug Connector Solder Surface Mount, Right Angle	J6, J7	5607-4200-SH	CONN_5607-4200-SH	2
M2		MT1, MT2, MT3, MT4	MTH_M2	MOUNTING_HOLE	4
M3		MT5, MT6, MT7, MT8	MTH_M3	MOUNTING_HOLE	4
0R	Resistor	R?	RES_0603	RESISTOR	3
10K	Resistor	R?	RES_0603	RESISTOR	3
MAX11643EEGT	8 Bit Analog to Digital Converter 16 Input 1 SAR24-QSOP	U?	MAX11643EEG+	IC_MAX11643EEGT	1
PCA9506	I/O Expander 40 pins I2CTSSOP-56	U?	PCA9506	IC_PCA9506	1