

CRYPTUS

DAUGHTERBOARD

REV. 1-A

RESISTORS

DNF

RX1 100K	RX2 47K	RX3 13K	RX4 10K	RX5 [Value]	RX6 3K24	RX7 2K2	RX8 1K	RX9 499R	RX10 300R	RX11 240R	RX12 100R	RX13 80R6	RX14 49R9	RX15 10R	RX16 15mR	RX17 0R
0603 1/16W 10%	0603 1/16W 5%	0603 1/16W 10%	0603 1/16W 10%	0603 1/16W 2%	0603 1/16W 2%	0603 1/16W 5%	0402 1/8W 1%	0603 1/8W 2%	0402 1/8W 1%	0402 1/8W 10%	0402 1/8W 0.5%	0402 1/8W 0.5%	0402 1/8W 10%	0402 1/8W 2%	1206 1/2W 10%	0603 1/8W 10%

These components should not appear on the PCB or on the BOM.

Specified power, package and tolerances are the same for all components of the same value.

CAPACITORS

DNF

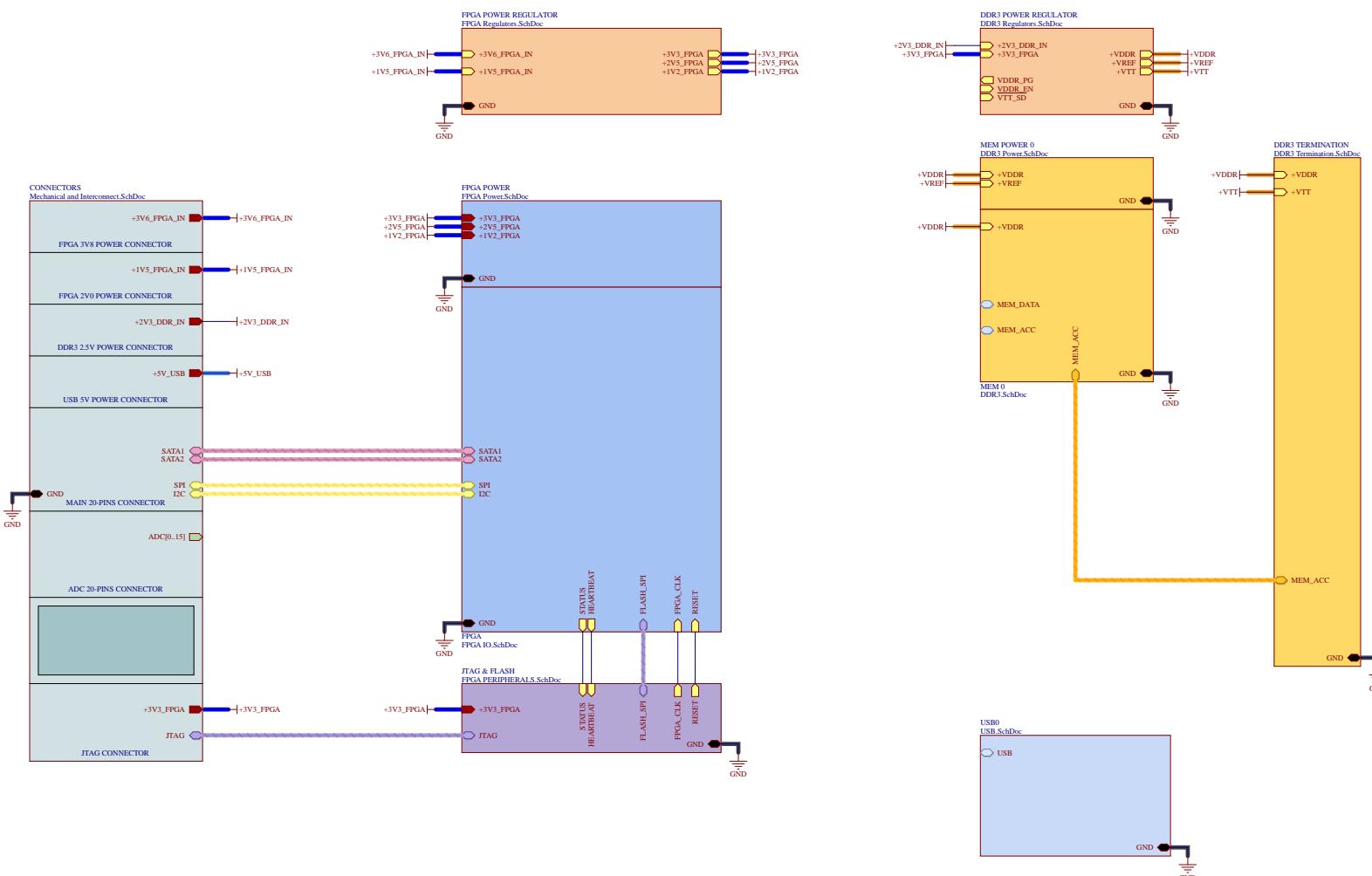
CX1 47uF 35V 2917 T498X476K035ATE500 399-11397-1-ND	CX2 47uF	CX3 4.7uF	CX4 470nF	CX5 100nF	CX6 47nF	CX7 10nF	CX8 470pF	CX9 220pF	CX10 2.2pF
1206 25V	0805 25V	0402 25V	0402 25V	0201 25V	0201 25V	0402 25V	0402 25V	0402 25V	0402 25V

These components should not appear on the PCB or on the BOM.

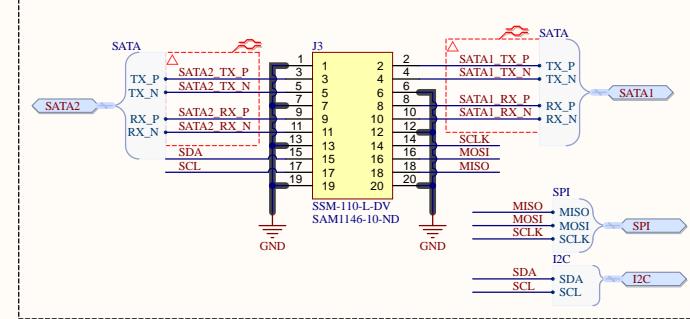
COMMENT LEGEND

General Notes Assembly, Part Locations, Fabrication, Debug Information etc.
Revisions With author and date To be kept on schematic for a single revision
Datasheet info Part information, addresses, registers, pull-up/pull-downs, excerpts & tables etc.
Calculations Values, tensions & currents, passives, etc.
TODO Things that are left to be done, with who should do it

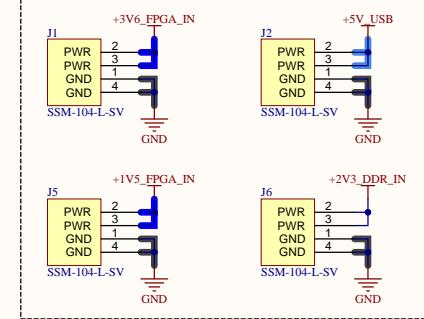
PROJECT	TITLE		REV
	CryptUS	Pascal-Emmanuel Lachance	
	SHEET 1 OF 12	FILE NAME Title.SchDoc	DWG NO. A3



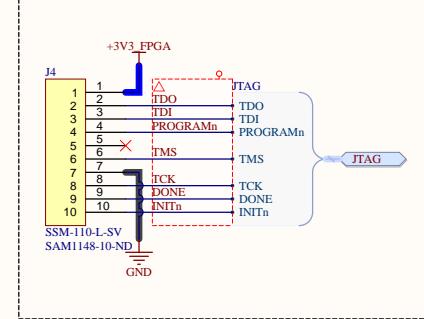
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Size	Number	Revision
A2		
Date: 5.12.2025	Sheet of	
File: Usgithubb_Overview.SchDoc		Drawn By:



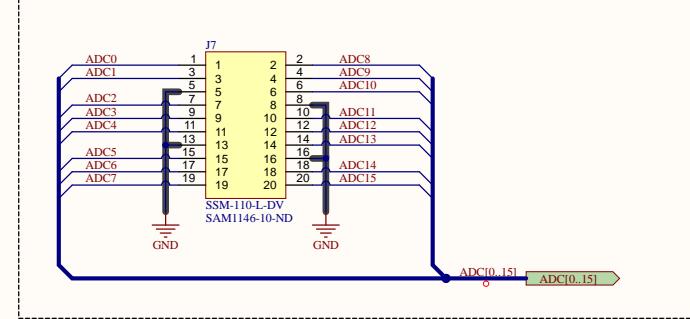
4-PIN POWER CONNECTORS



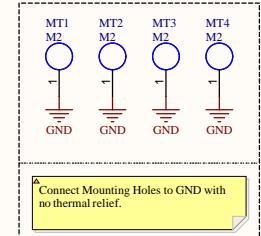
JTAG CONNECTOR



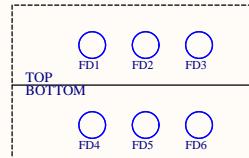
ADC 20-PIN CONNECTOR



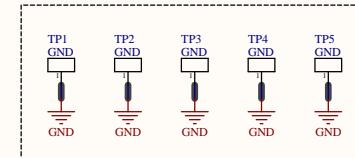
MOUTING HOLES



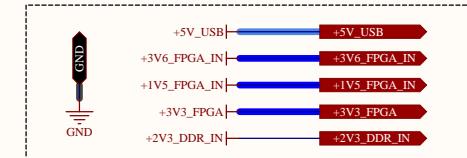
FIDUCIALS



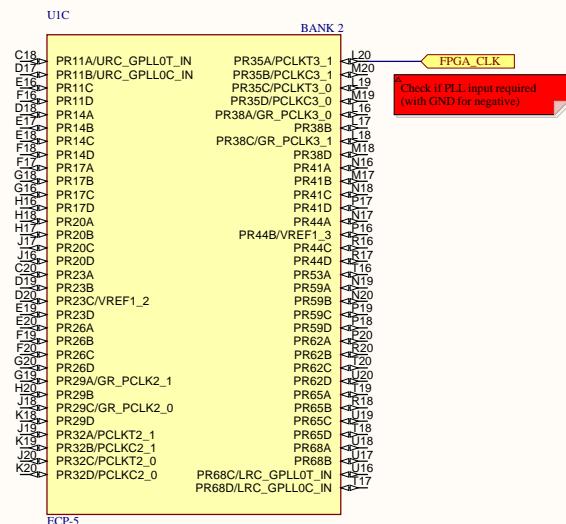
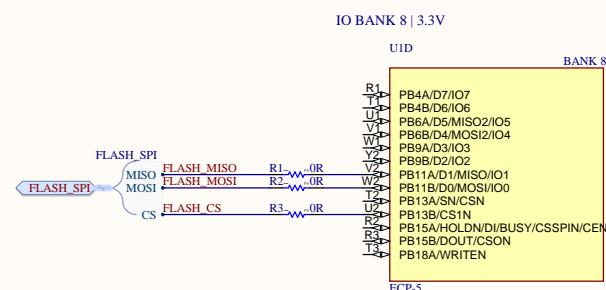
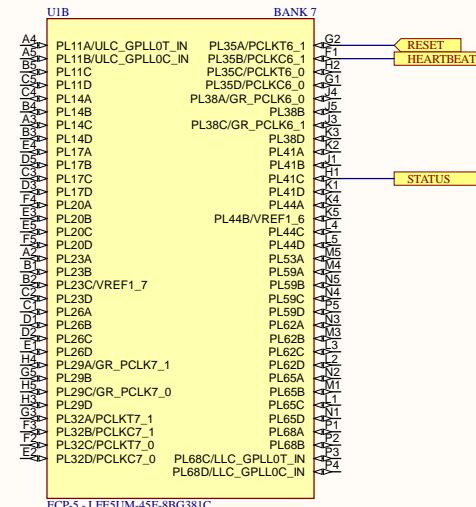
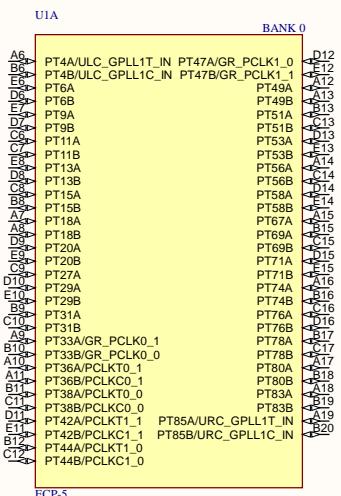
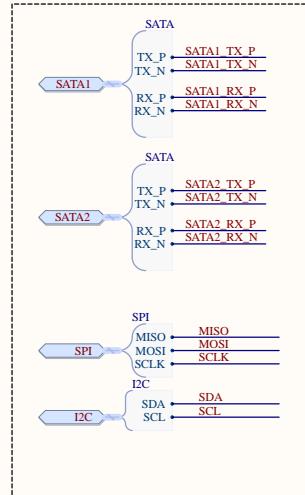
GND TESTPOINTS



PWR PORTS

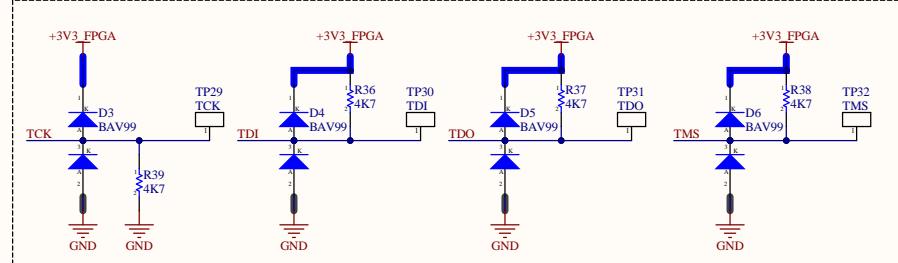
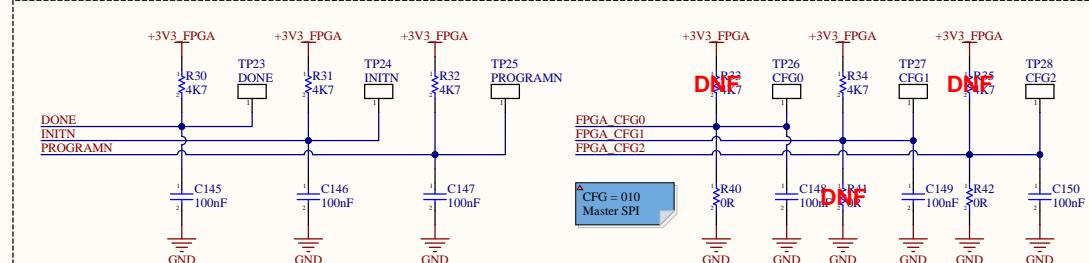
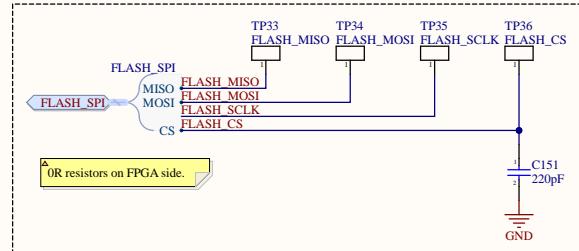
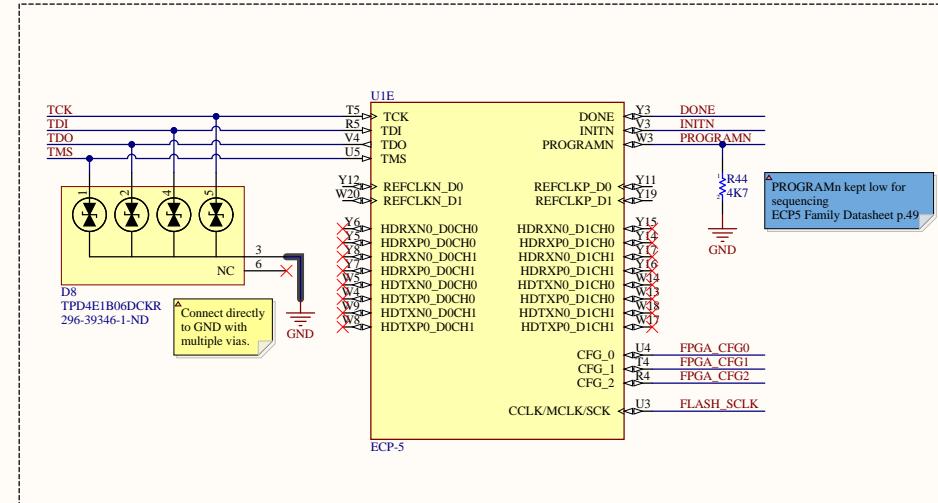
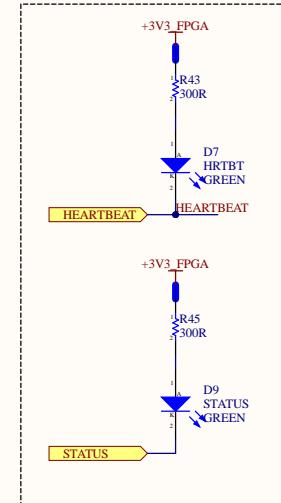
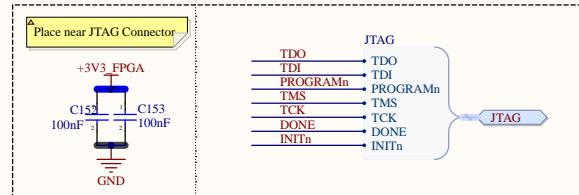
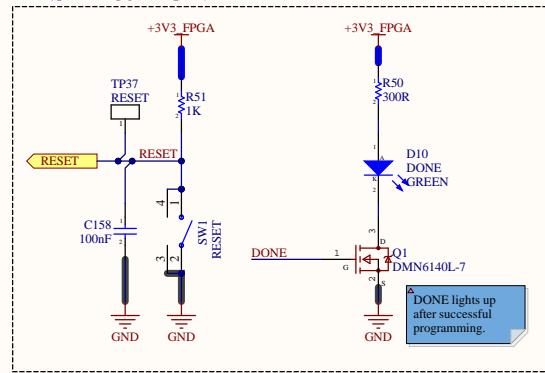
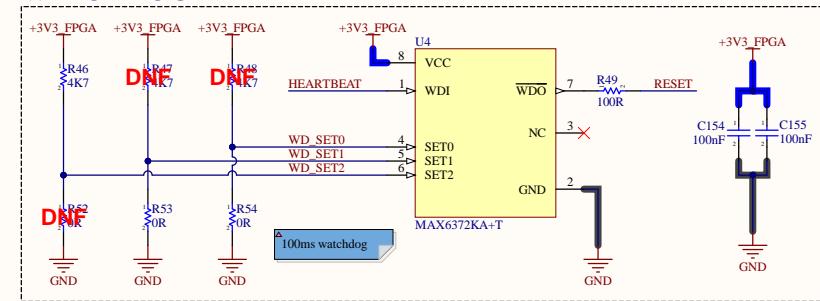
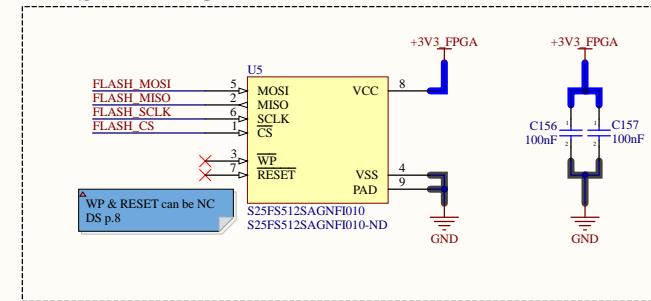
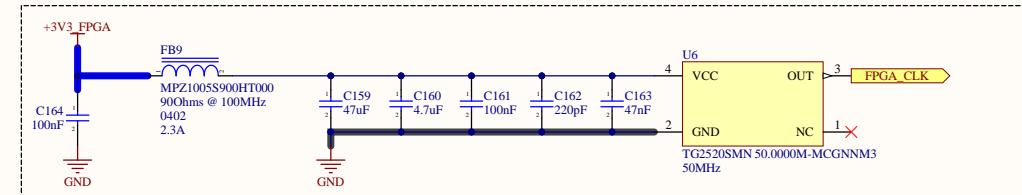


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	TITLE	Mechanical & Interconnect	
CryptUS	SIZE	DWG NO.	REV
Pascal-Emmanuel Lachance	A3		
FILE NAME	Mechanical and Interconnect.SchDoc		SHEET 3 OF 12

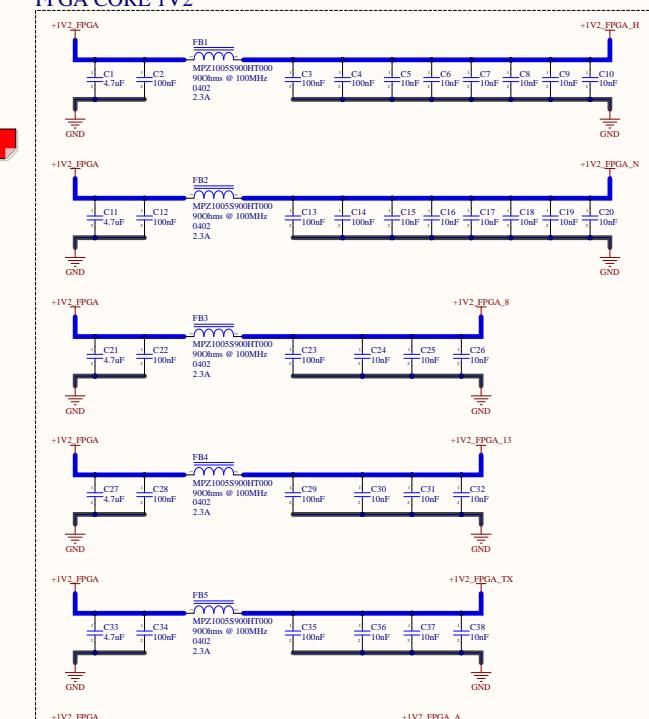
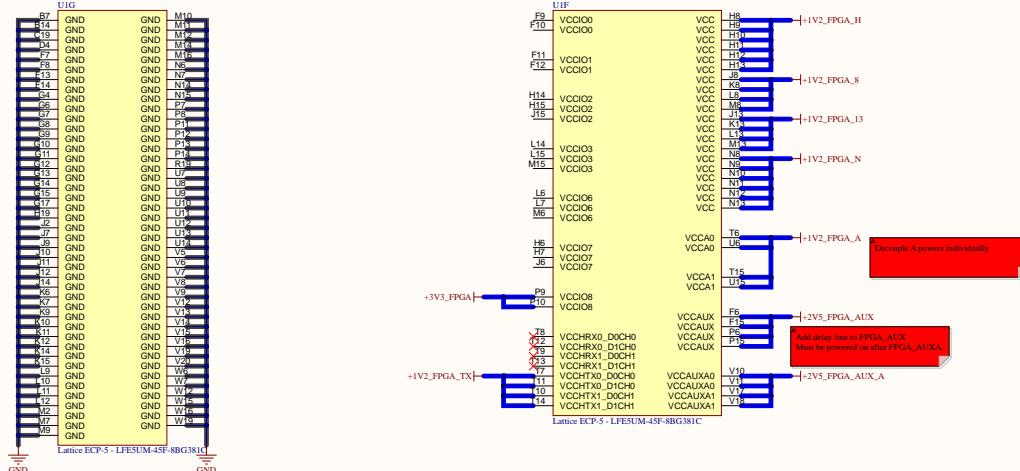
HARNESSES

PROJECT		CryptUS_Daughterboard	
TITLE		*	
SIZE		DWG NO.	REV
A3			
FILE NAME		FPGAIO.SchDoc	SHEET 4 OF 12



JTAG PROTECTIONS & PULL-UP**FPGA CONFIG & PROG SIGNALS****FLASH SPI HARNESS****FPGA JTAG****STATUS LED****JTAG HARNESS****RESET & DONE****WATCHDOG TIMER****FLASH MEMORY****50MHZ FPGA OSCILLATOR**

Title		
Size	Number	Revision
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Date:	5-12-2025	Sheet of
File:	U:\github\...\FPGA PERIPHERALS.SchDoc	Drawn By:



1

2

3

4

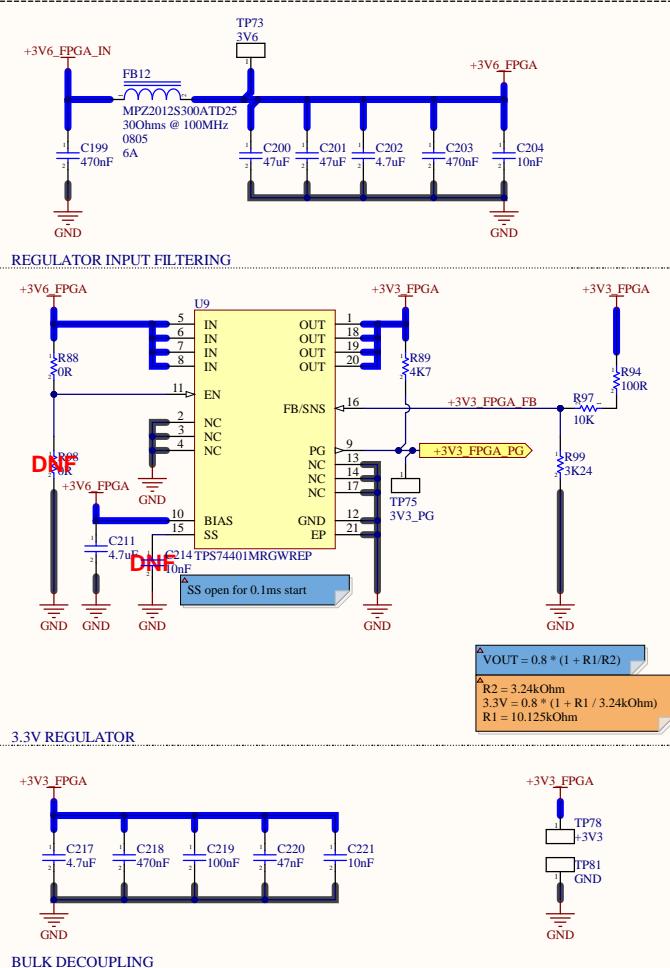
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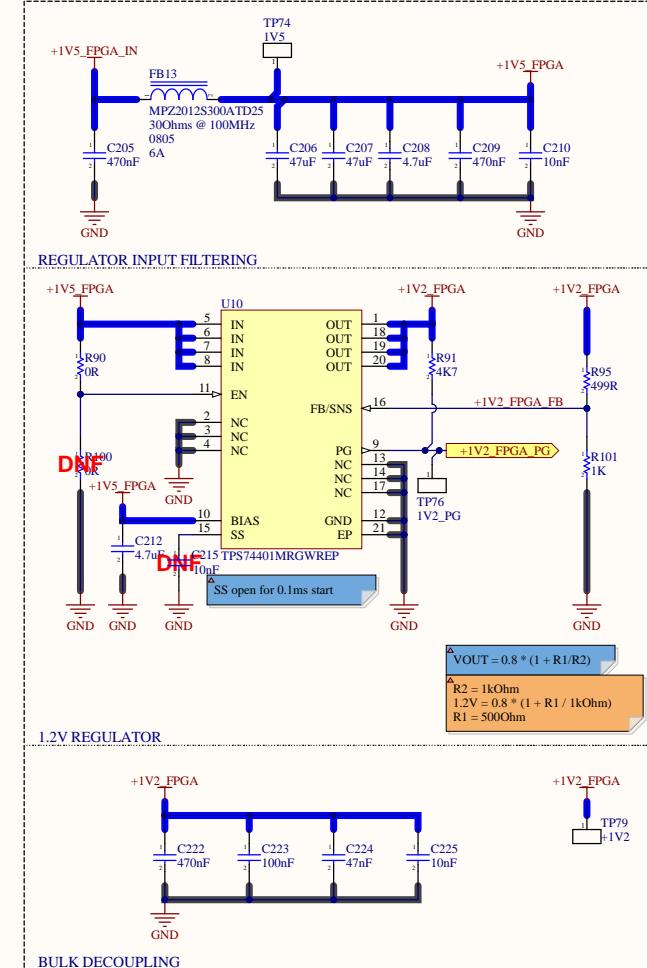
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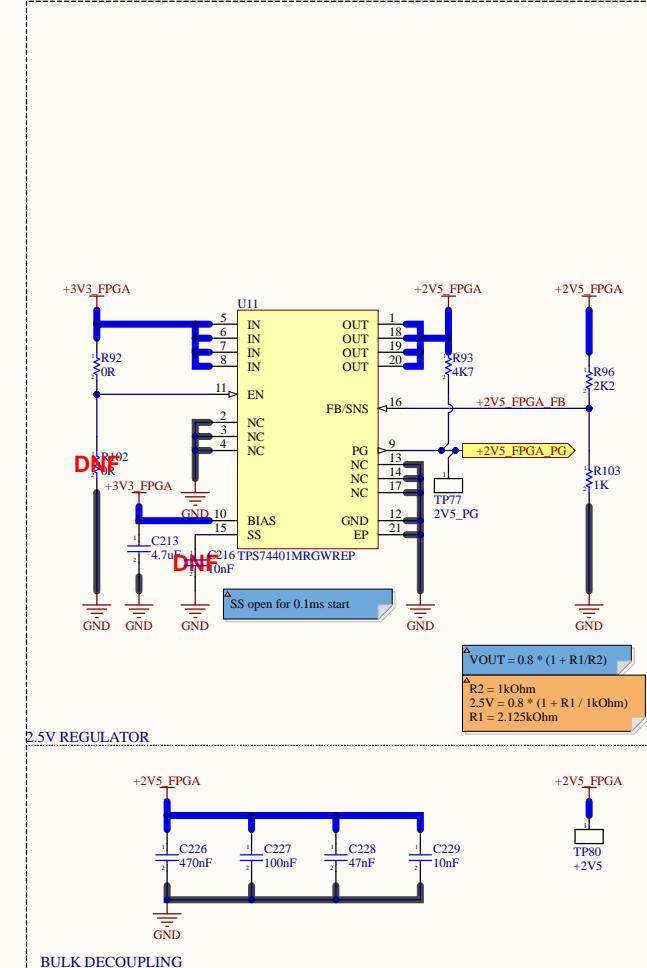
3.3V @ 3A REGULATOR



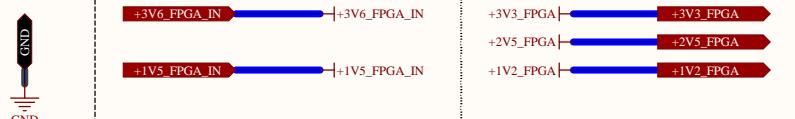
1.2V @ 3A REGULATOR



2.5V @ 3A REGULATOR



PWR PORTS



Title		
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File: U:\github\...\FPGA Regulators.SchDoc	Drawn By:	

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2

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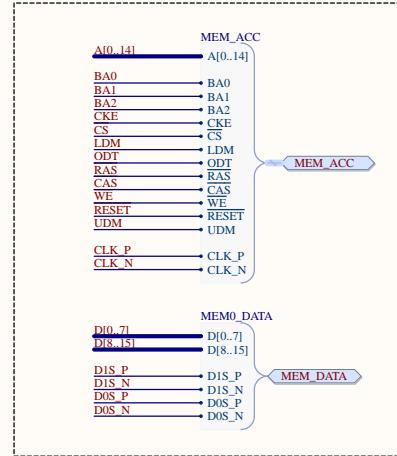
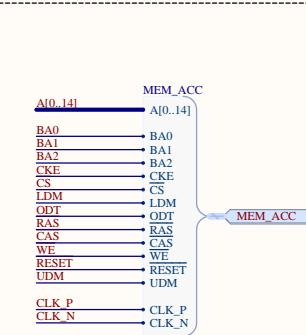
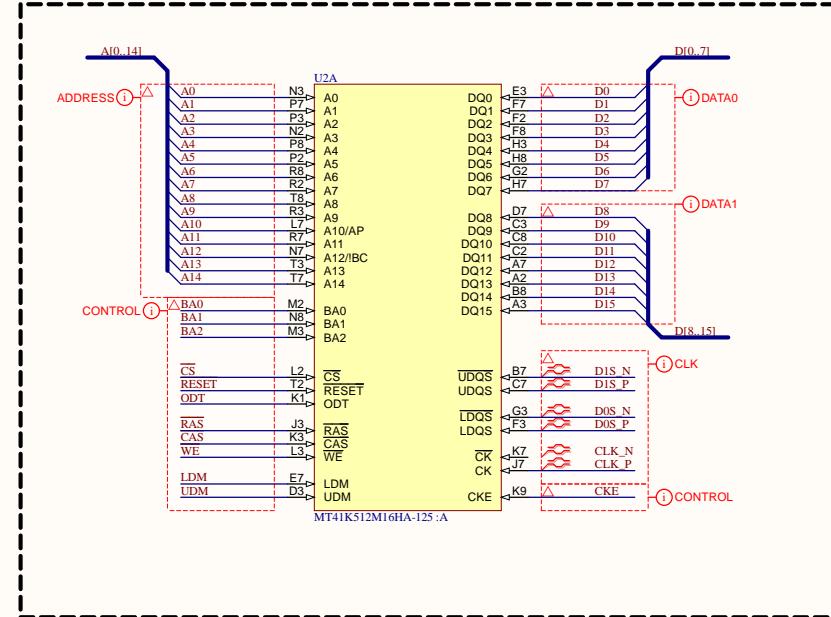
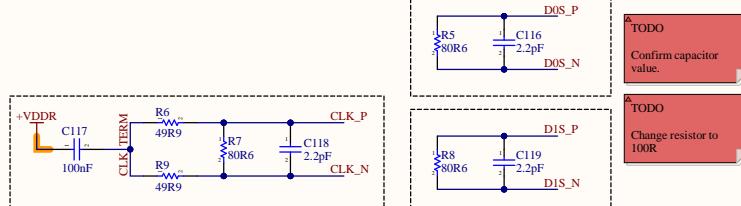
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5

6

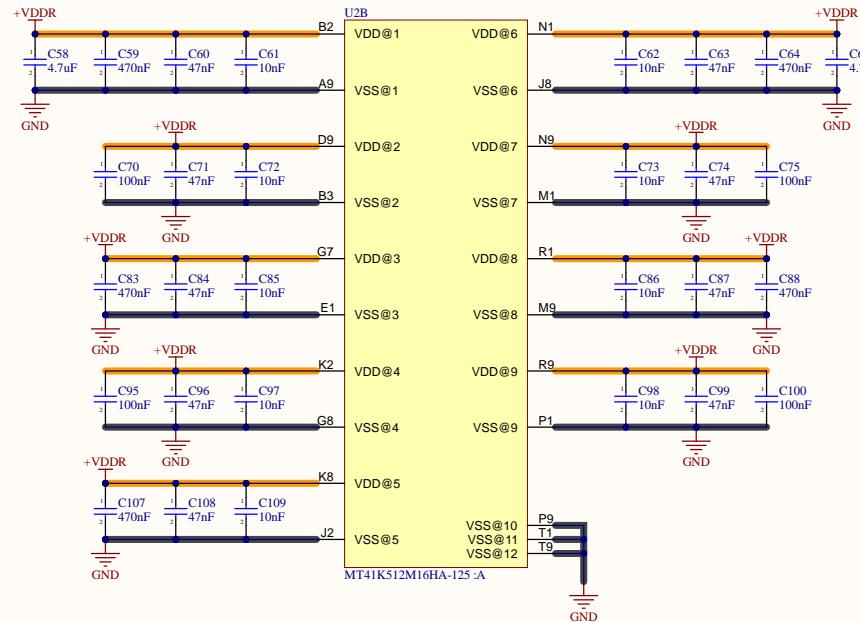
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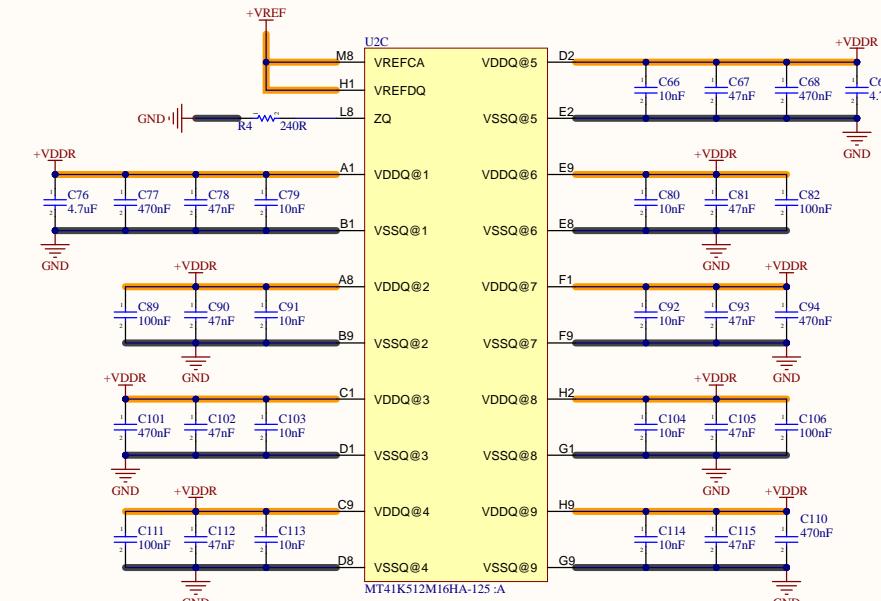
INPUT SHEET ENTRY

OUTPUT SHEET ENTRY

DDR3
**B****B****C****C****D****D**

PROJECT	CryptUS_Daughterboard	
TITLE	*	
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A3		
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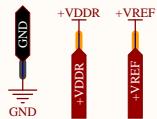
A



B

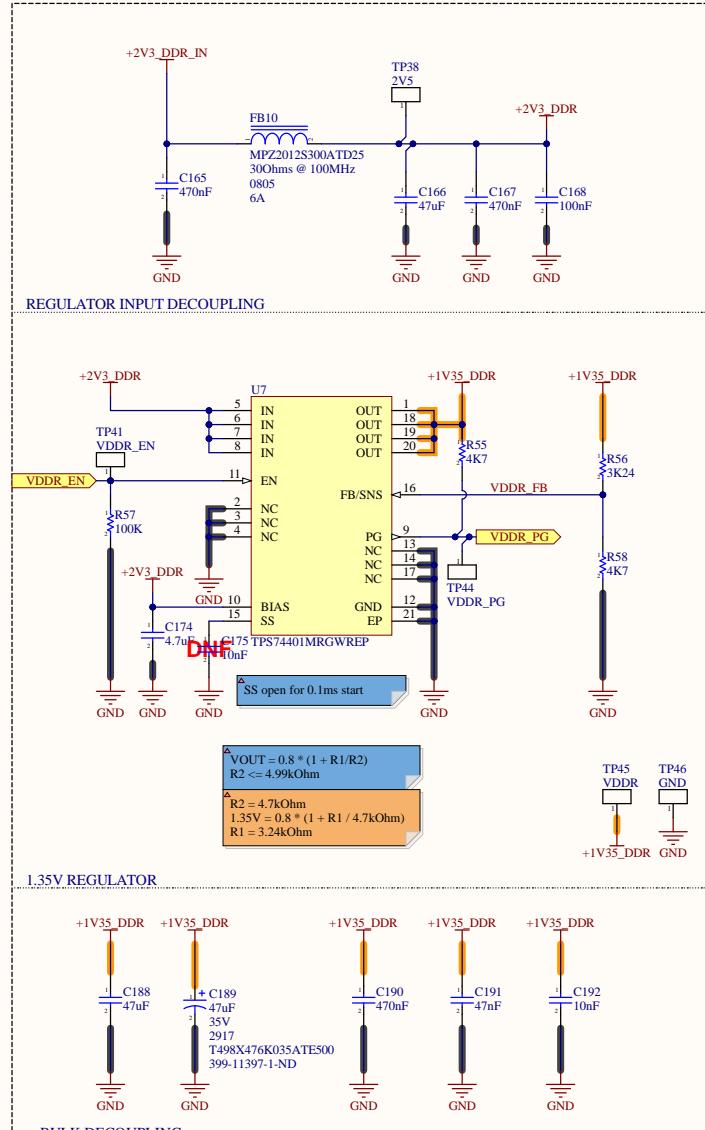


C

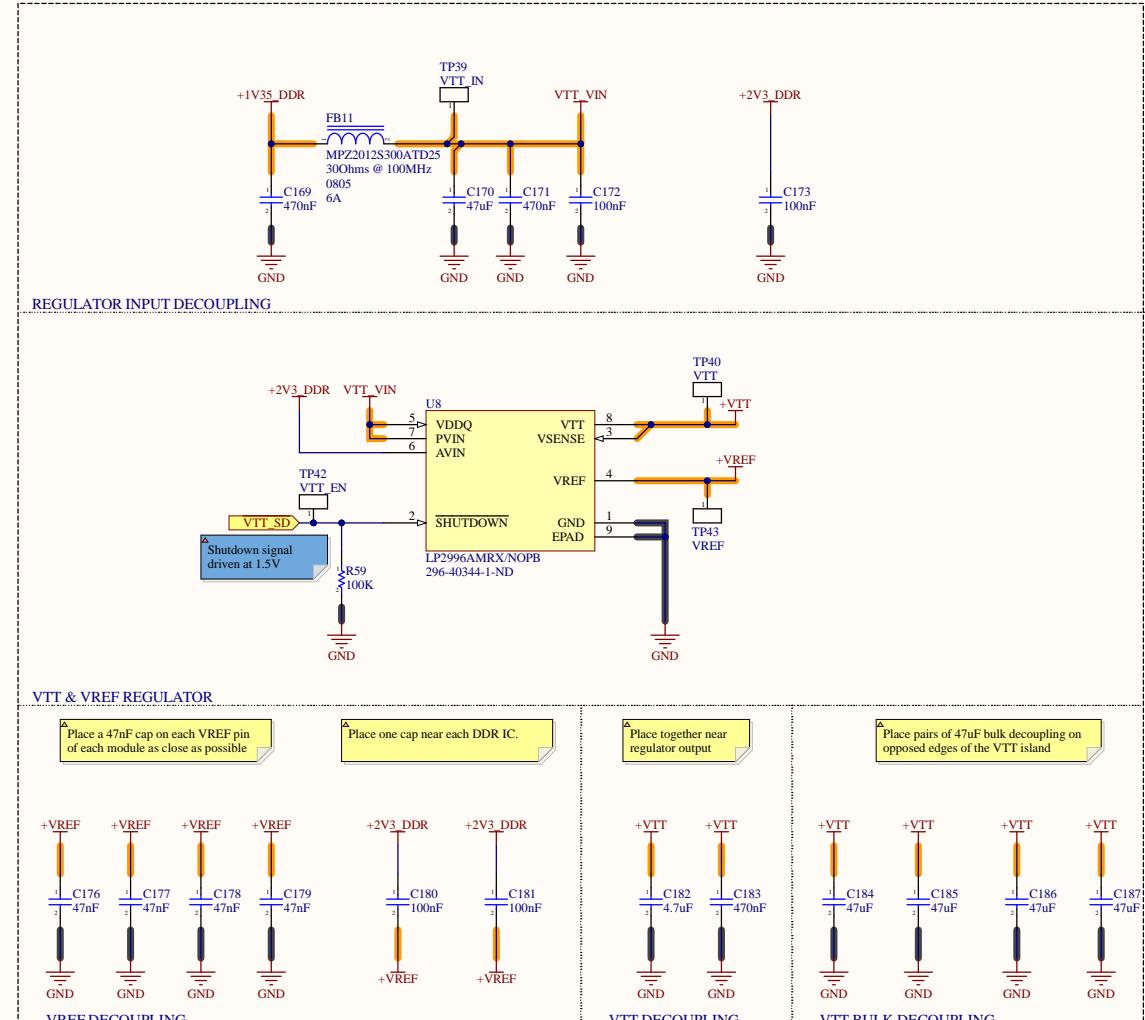


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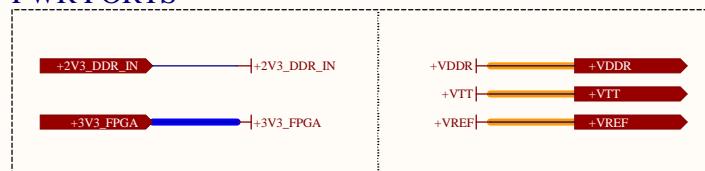
1.35V @ 3A VDDR REGULATOR



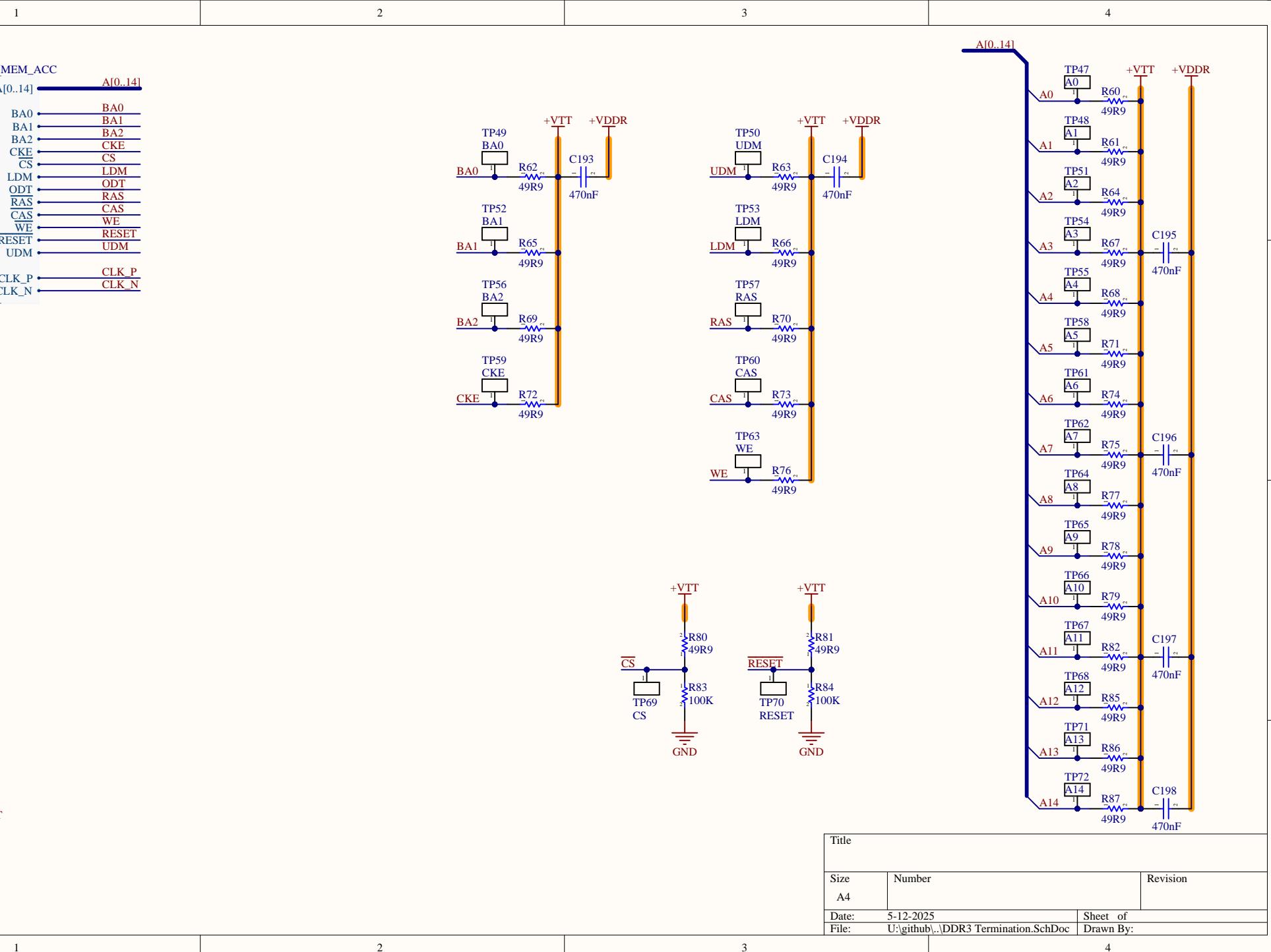
VTT & VREF REGULATOR



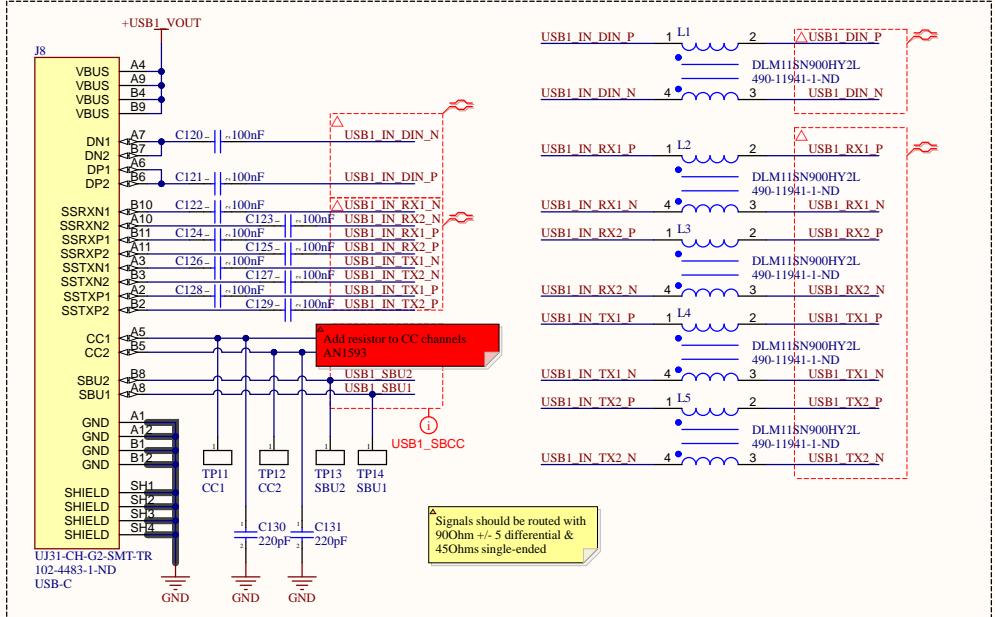
PWR PORTS



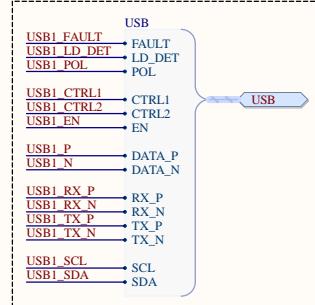
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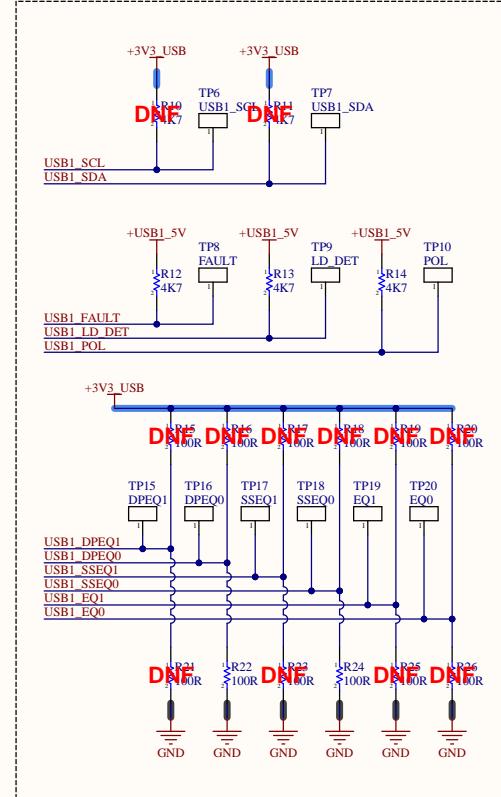
USB-C CONNECTOR



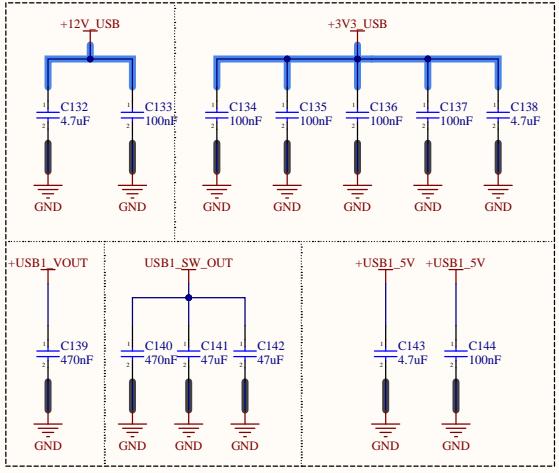
SIGNAL HARNESS



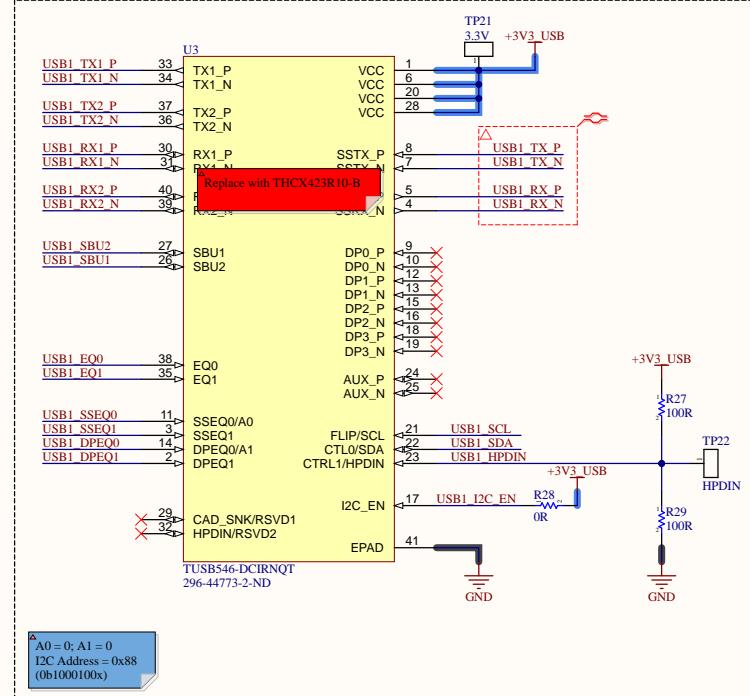
RESISTORS & TESTPOINTS



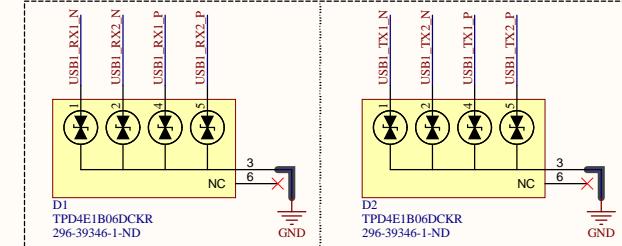
DECOUPLING



USB HIGHSPEED MUX



PROTECTIONS



Title		
Size	Number	Revision
A3		
Date:	5-12-2025	Sheet of
File:	U:\git\hub\.\USB.SchDoc	Drawn By:

