

Simulador Amnesia: Um estudo sobre o impacto de diferentes técnicas e políticas em um computador

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Introdução à nossa Arquitetura-Base

```
5 <AmnesiaConfiguration>
6   <Processor>
7     <processorContains>0</processorContains>
8     <createTraceFile>0</createTraceFile>
9   </Processor>
10   <Trace>
11     <wordSize>4</wordSize>
12   </Trace>
13   <CPU>
14     <wordSize>4</wordSize>
15   </CPU>
16   <MainMemory>
17     <blockSize>2</blockSize>
18     <memorySize>16</memorySize>
19     <cyclesPerAccessRead>1</cyclesPerAccessRead>
20     <cyclesPerAccessWrite>2</cyclesPerAccessWrite>
21     <timeCicle>10</timeCicle>
22   </MainMemory>
23   <Cache>
24     <cacheType>Unified</cacheType>
25     <unifiedCache>
26       <lineSize>2</lineSize>
27       <cyclesPerAccessRead>1</cyclesPerAccessRead>
28       <cyclesPerAccessWrite>2</cyclesPerAccessWrite>
29       <timeCicle>1</timeCicle>
30       <memorySize>8</memorySize>
31       <associativityLevel>2</associativityLevel>
32       <writePolicy>WriteThrough</writePolicy>
33       <replacementAlgorithm>FIFO</replacementAlgorithm>
34     </unifiedCache>
35   </Cache>
36   <VirtualMemory>
37     <pageSize>4</pageSize>
38     <diskMemorySize>16</diskMemorySize>
39     <diskCyclesPerAccessRead>1</diskCyclesPerAccessRead>
40     <diskCyclesPerAccessWrite>2</diskCyclesPerAccessWrite>
41     <timeCicle>100</timeCicle>
42     <pageTableReplacementAlgorithm>FIFO</pageTableReplacementAlgorithm>
43   </VirtualMemory>
44   <TLBType>unified</TLBType>
45   <unifiedTLB>
46     <memorySize>2</memorySize>
47     <cyclesPerAccessRead>1</cyclesPerAccessRead>
48     <cyclesPerAccessWrite>2</cyclesPerAccessWrite>
49     <timeCicle>1</timeCicle>
50     <replacementAlgorithm>FIFO</replacementAlgorithm>
51   </unifiedTLB>
52 </AmnesiaConfiguration>
```

File View Simulate Window Help Exit

RAM

PAGE	BLOCK	WORD	DATA
PAGE0	BLOCK0	0	0x00000000
		1	0x00000000
	BLOCK1	2	0x00000000
		3	0x00000000
PAGE1	BLOCK2	4	0x00000000
		5	0x00000000
	BLOCK3	6	0x00000000
		7	0x00000000
PAGE2	BLOCK4	8	0x00000000
		9	0x00000000
	BLOCK5	10	0x00000000
		11	0x00000000
PAGE3	BLOCK6	12	0x00000000

Page Table

Virtual Page	V	R	M	REP	Frame Page
0x00000000	0	0	0	0x0000	0x00000000d
0x00000001	0	0	0	0x0000	0x00000000
0x00000002	0	0	0	0x0000	0x00000000
0x00000003	0	0	0	0x0000	0x00000000
0x00000004	0	0	0	0x0000	0x00000000
0x00000005	0	0	0	0x0000	0x00000000
0x00000006	0	0	0	0x0000	0x00000000
0x00000007	0	0	0	0x0000	0x00000000

Disk

PAGE	WORD	DATA
PAGE0	0	0x00000000
	1	0x00000000
	2	0x00000000
	3	0x00000000
PAGE1	4	0x00000000
	5	0x00000000
	6	0x00000000
	7	0x00000000
PAGE2	8	0x00000000
	9	0x00000000
	10	0x00000000
	11	0x00000000
PAGE3	12	0x00000000

Caches

Unified - Level 1

SET	TAG	FLAGS	WORD0	WORD1	TAG	FLAGS	WORD0
0x0000	0xffffffff	0x00000000	0x00000000	0x00000000	0xffffffff	0x00000000	0x0000
0x0001	0xffffffff	0x00000000	0x00000000	0x00000000	0xffffffff	0x00000000	0x0000

Trace: TR_6_read...

211
214
215
0 c
0 d
210
211
214
215
0 c
0 d

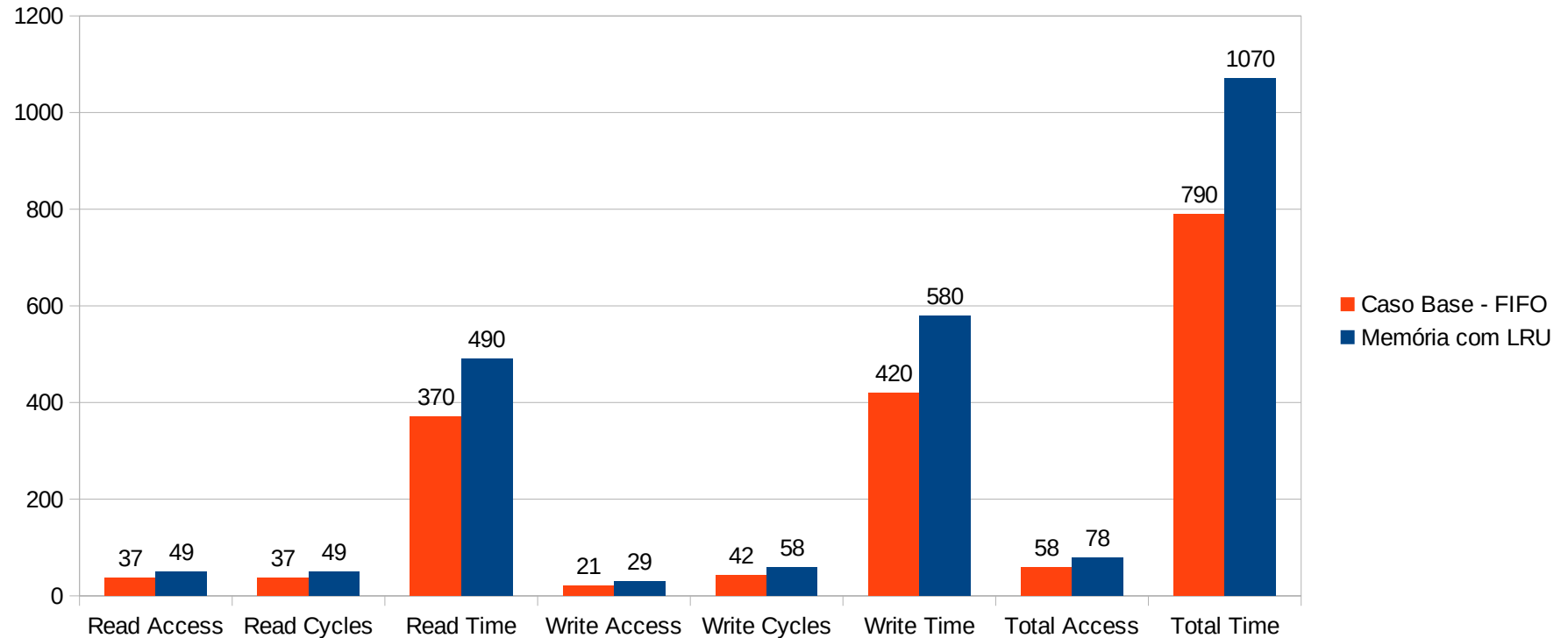
TLB

Data

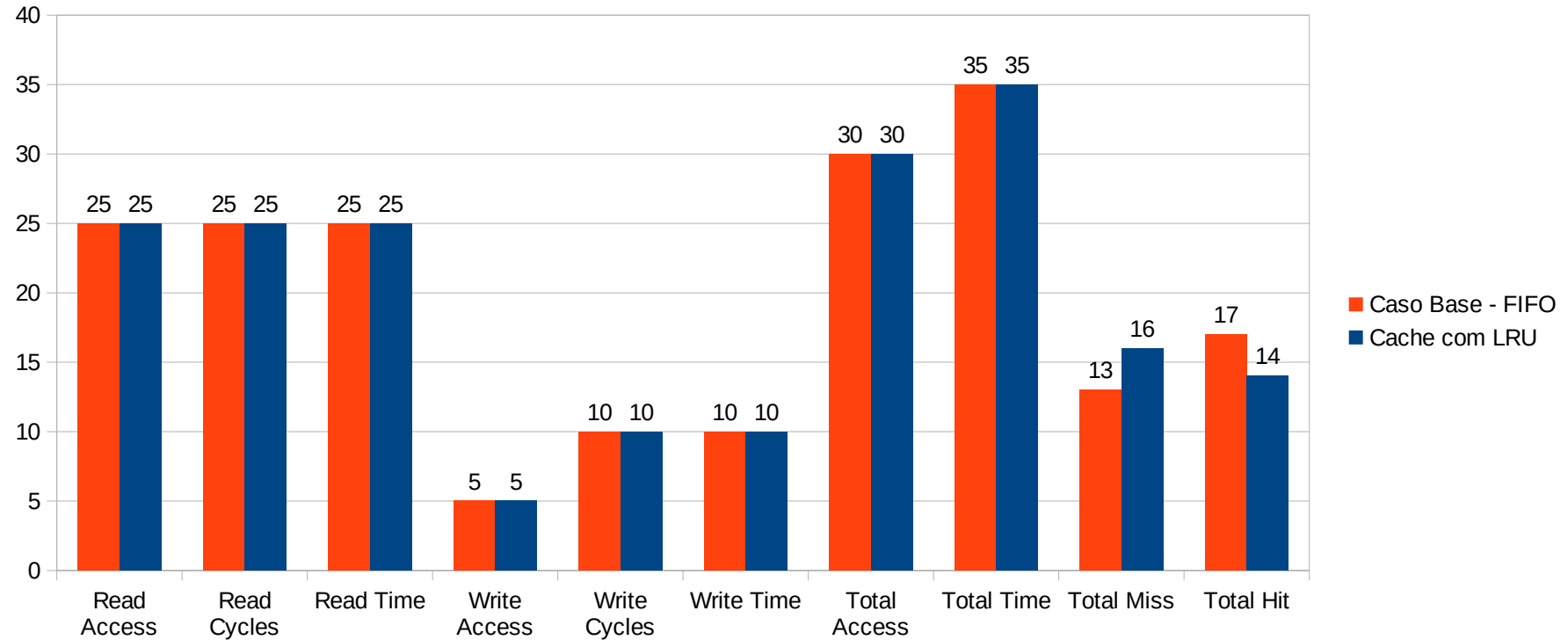
SET	TAG	FLAGS	V	R	M	WORD0	TAG	FLAGS	V	R	M	WORD0
0x0000	0xffffffff	0xffffffff	0	0	0	0x00000000	0xffffffff	0xffffffff	0	0	0	0x00000000

Teste 1: Políticas de Substituição FIFO e LRU

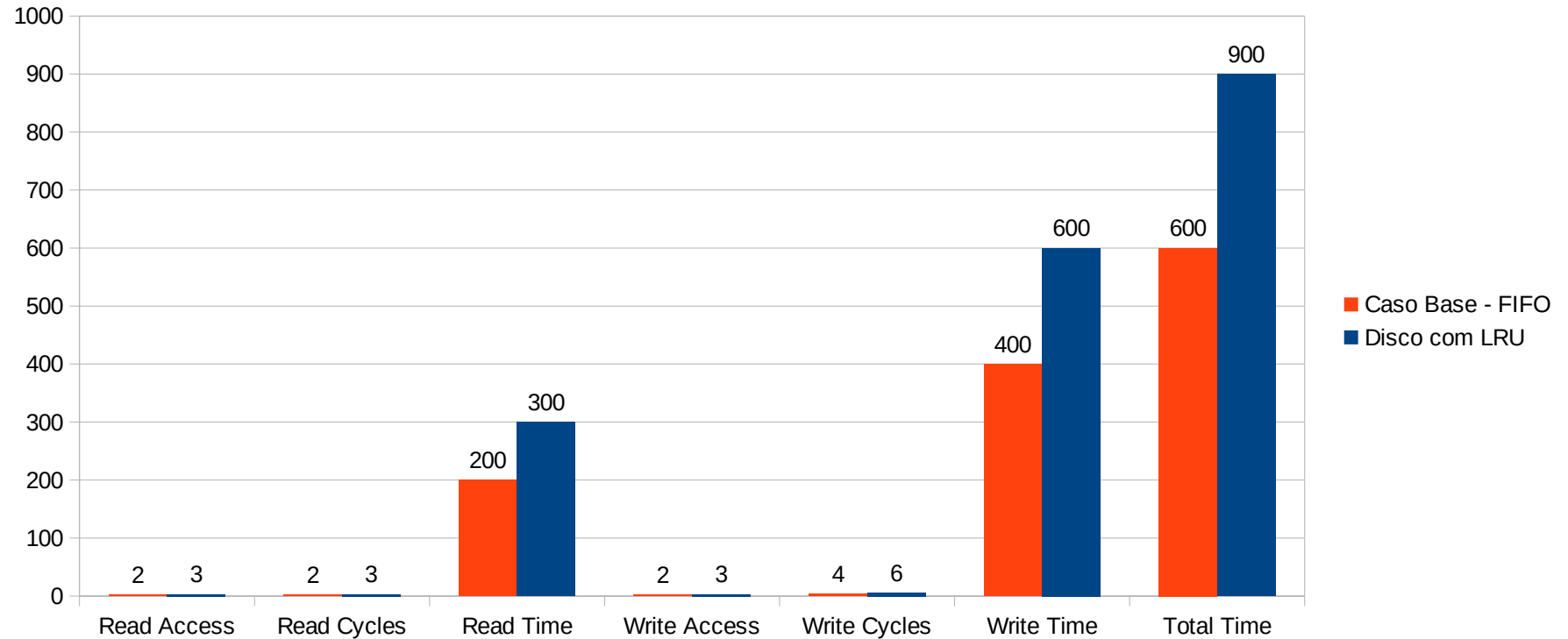
Impacto da política LRU na Memória Principal



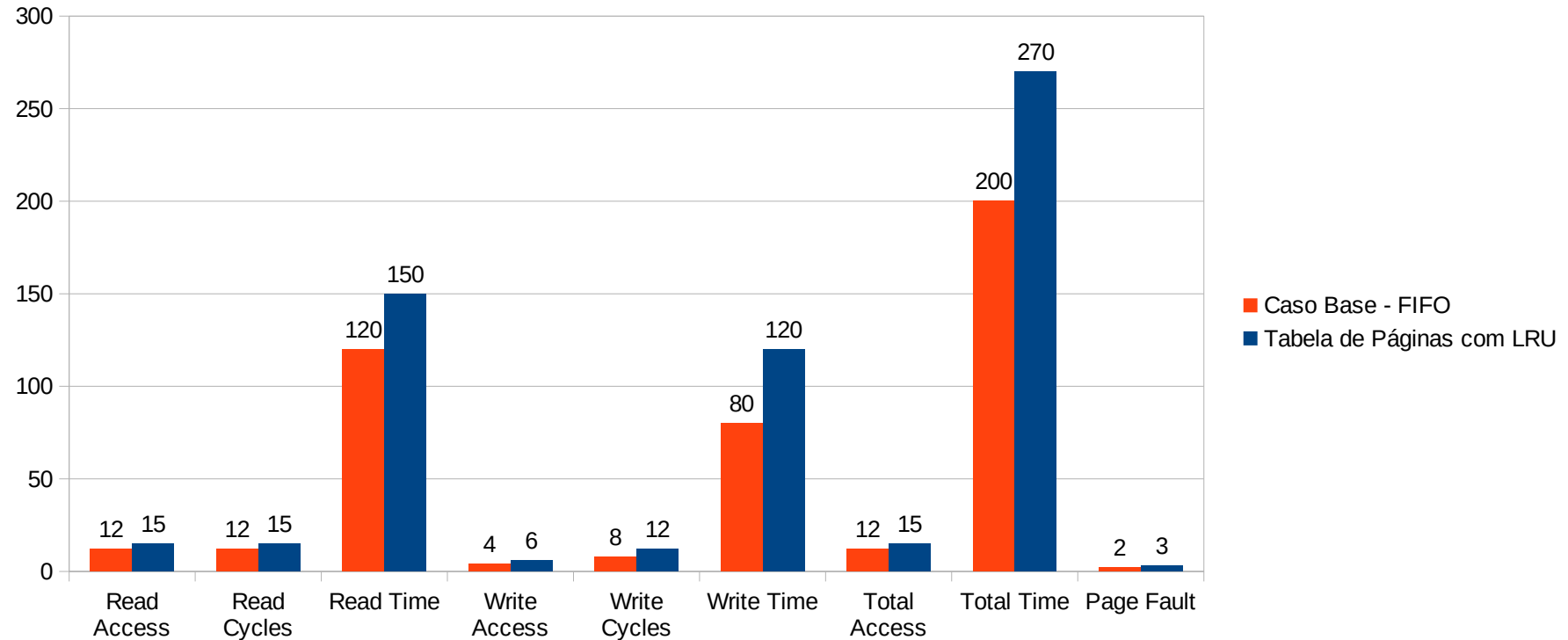
Impacto da política LRU na Cache



Impacto da política LRU no disco

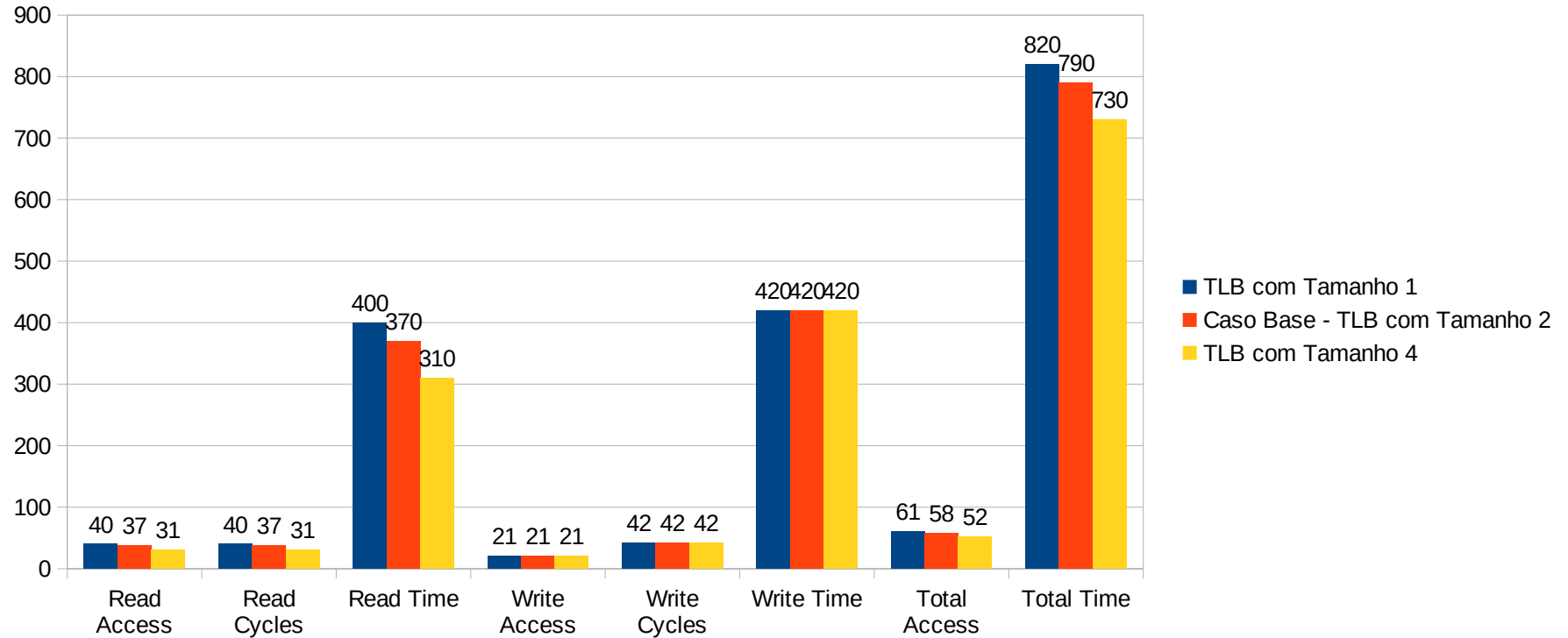


Impacto da política LRU na tabela de páginas

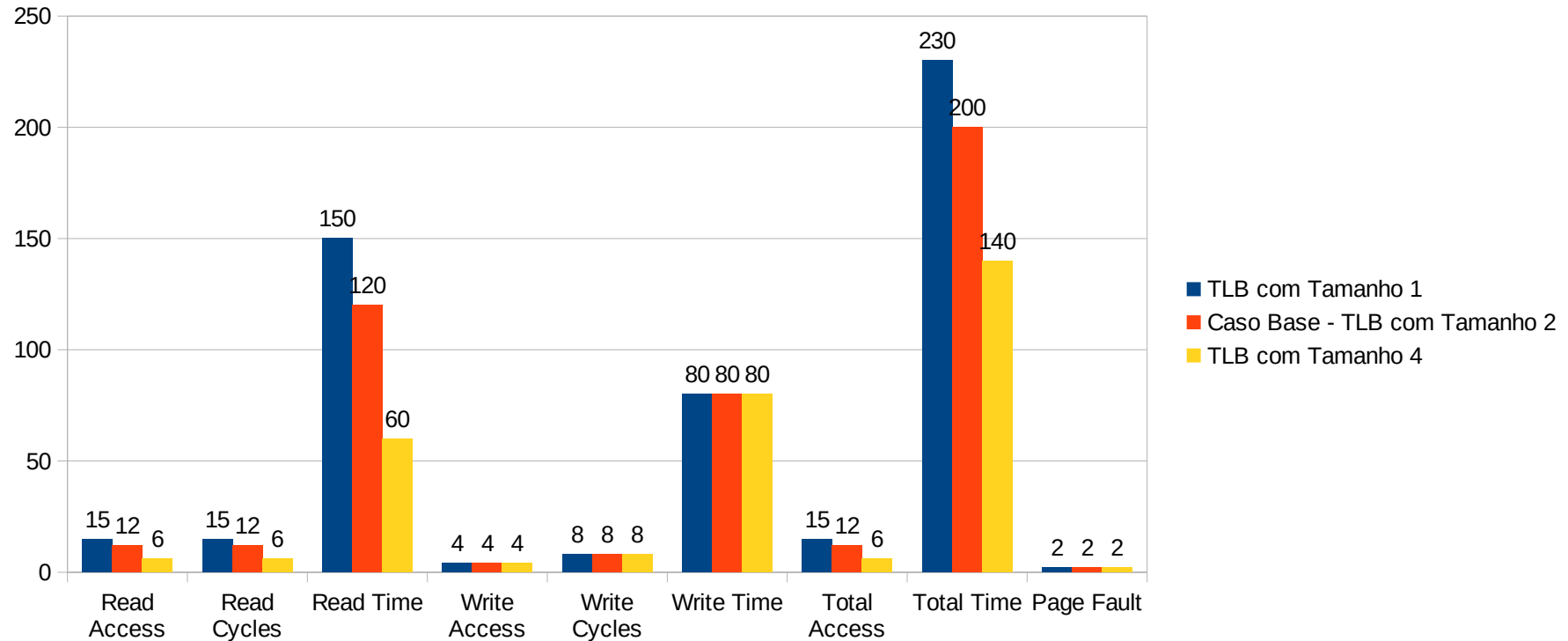


Teste 2: Alteração do tamanho da TLB

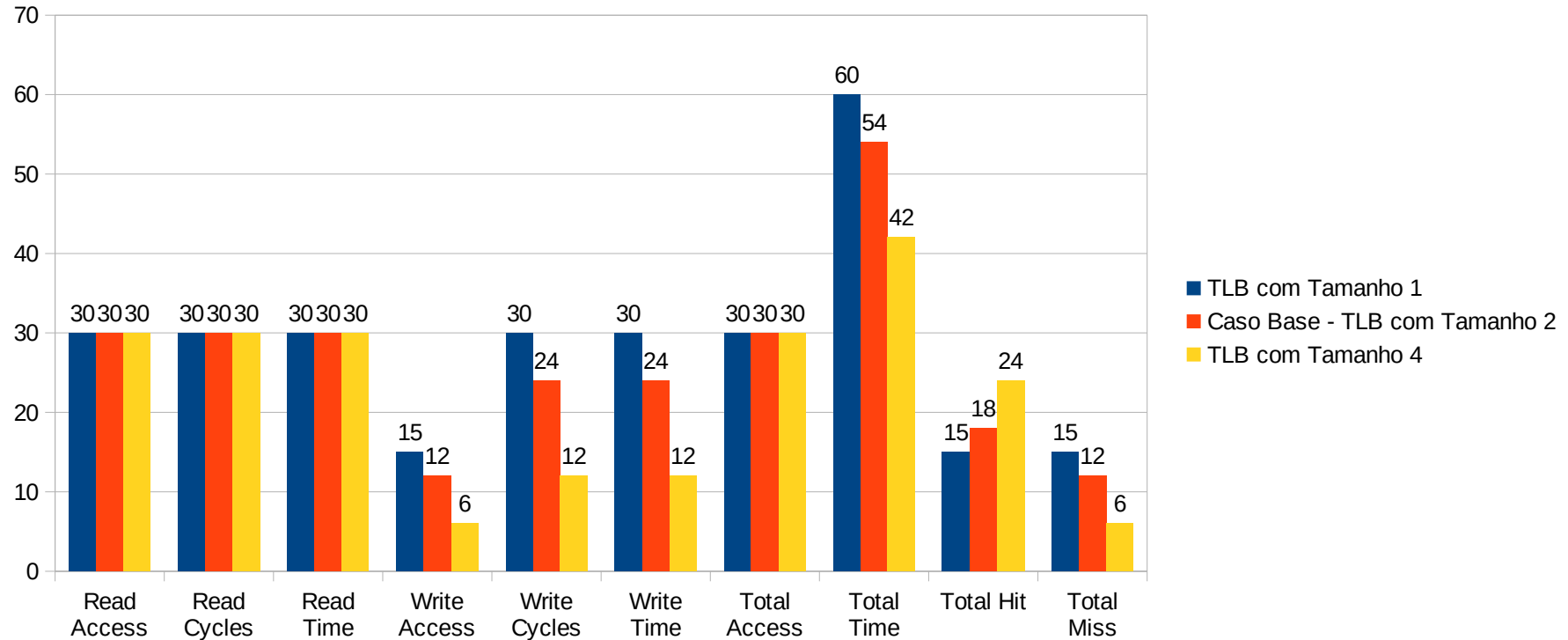
Impacto da alteração do tamanho da TLB na memória principal



Impacto da alteração do tamanho da TLB na tabela de páginas

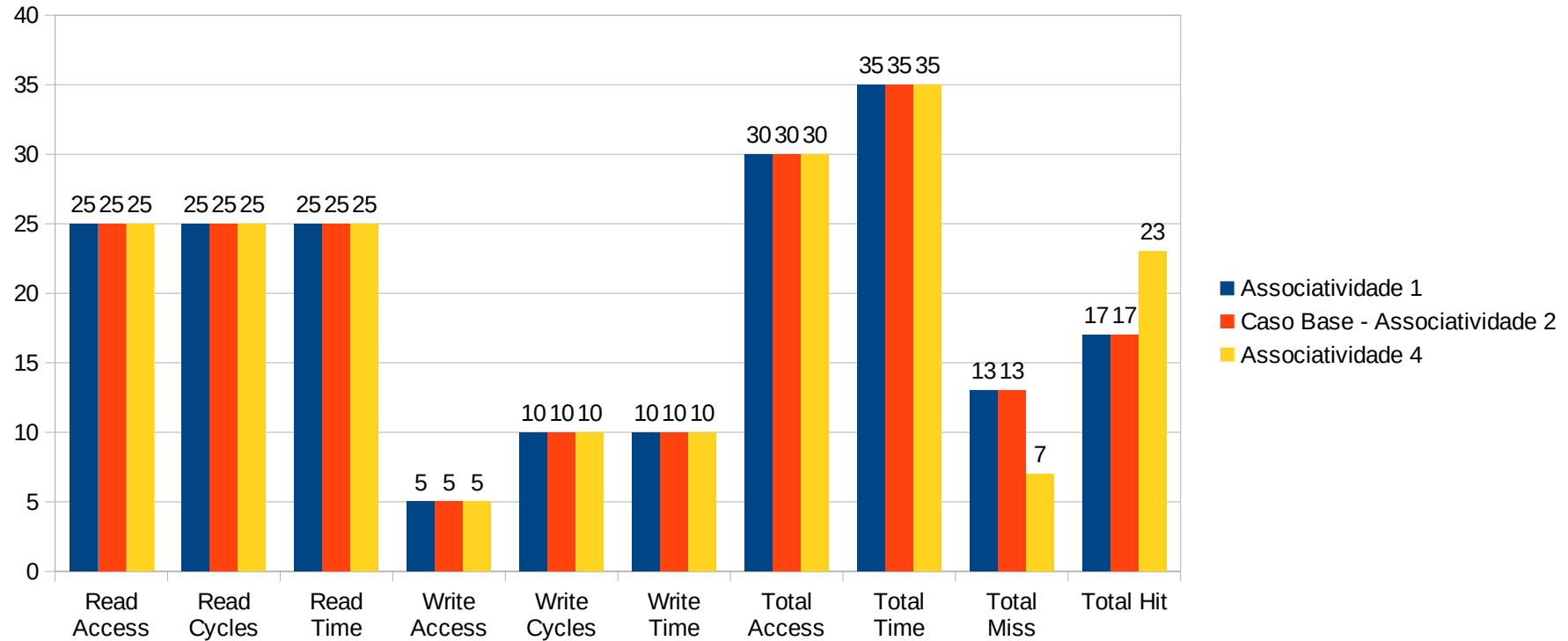


Impacto da alteração do tamanho da TLB na TLB

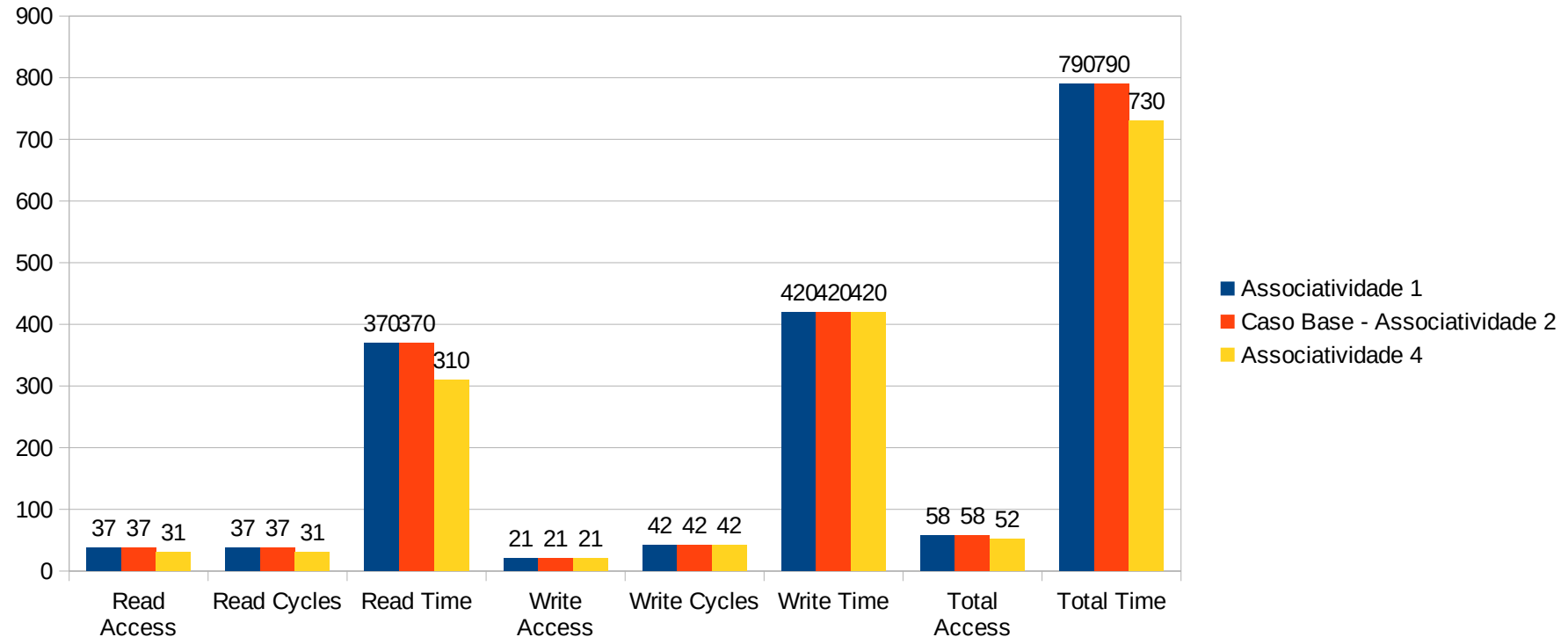


Teste 3: Associatividade de uma, duas e quatro vias

Impacto da alteração da associatividade na cache

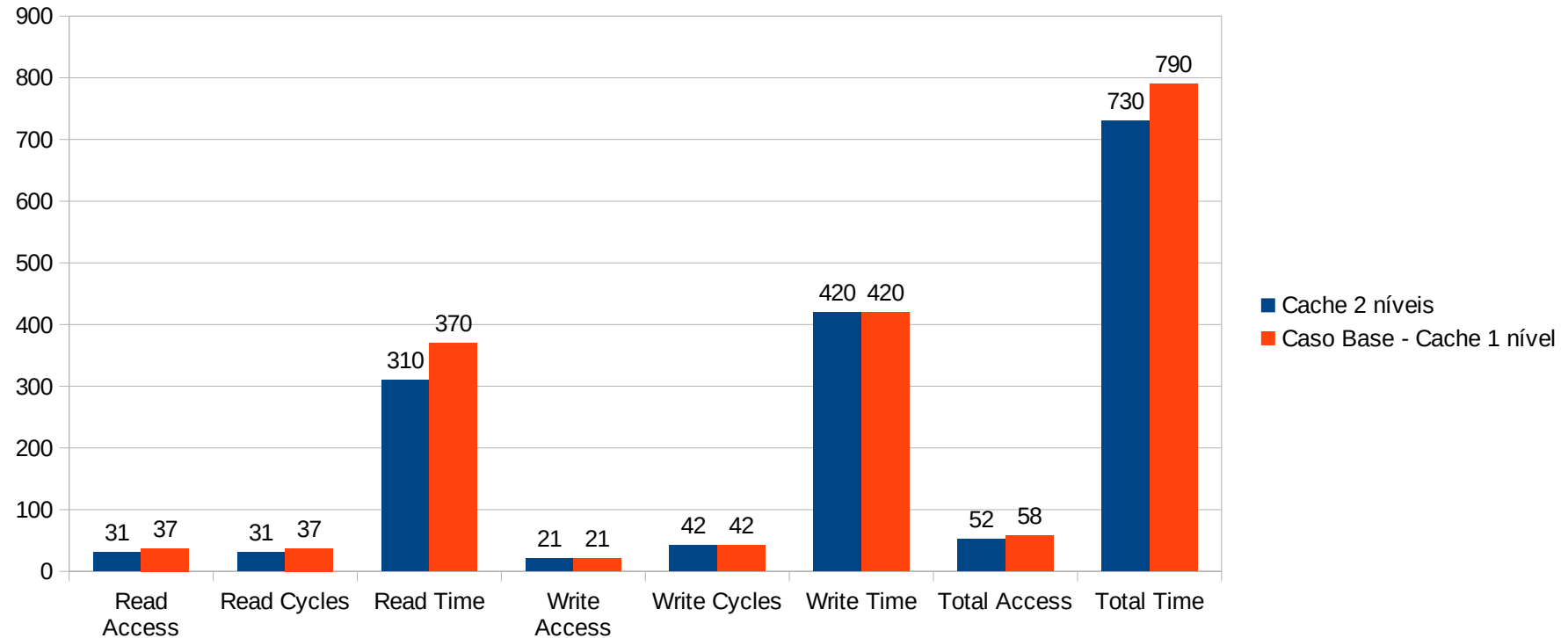


Impacto da alteração da associatividade na memória principal



Teste 4: Cache Unificada e Cache Multinível

Impacto de uma cache multinível na memória principal



Teste 5: Tudo junto?

Tempos de acesso totais com Cache Multinível, TLB maior e associatividade 4 vias

