

IRLZ24N

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

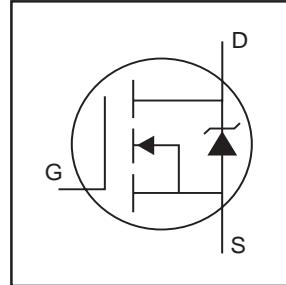
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

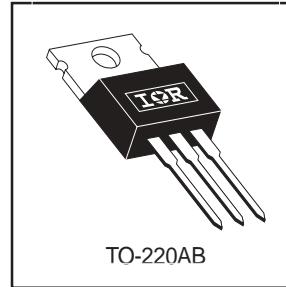
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	18	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	13	
I_{DM}	Pulsed Drain Current ①	72	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	45	W
	Linear Derating Factor	0.30	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②	68	mJ
I_{AR}	Avalanche Current ①	11	A
E_{AR}	Repetitive Avalanche Energy ①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	



$V_{DSS} = 55\text{V}$
 $R_{DS(on)} = 0.06\Omega$
 $I_D = 18\text{A}$

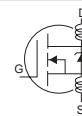


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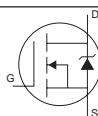
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.061	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.060	Ω	$V_{GS} = 10\text{V}, I_D = 11\text{A}$ ④
		—	—	0.075		$V_{GS} = 5.0\text{V}, I_D = 11\text{A}$ ④
		—	—	0.105		$V_{GS} = 4.0\text{V}, I_D = 9.0\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	8.3	—	—	S	$V_{DS} = 25\text{V}, I_D = 11\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 44\text{V}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16\text{V}$
Q_g	Total Gate Charge	—	—	15	nC	$I_D = 11\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	3.7		$V_{DS} = 44\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.5		$V_{GS} = 5.0\text{V}$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	—	7.1		$V_{DD} = 28\text{V}$
t_r	Rise Time	—	—	74	ns	$I_D = 11\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	—	20		$R_G = 12\Omega, V_{GS} = 5.0\text{V}$
t_f	Fall Time	—	—	29		$R_D = 2.4\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	480	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	130	—		$V_{DS} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	61	—		$f = 1.0\text{MHz}$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 11\text{A}, V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	60	90	ns	$T_J = 25^\circ\text{C}, I_F = 11\text{A}$
Q_{rr}	Reverse Recovery Charge	—	130	200	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 790\mu\text{H}$
 $R_G = 25\Omega, I_{AS} = 11\text{A}$. (See Figure 12)

③ $I_{SD} \leq 11\text{A}, dI/dt \leq 290\text{A}/\mu\text{s}, V_{DD} \leq V_{(\text{BR})\text{DSS}}, T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

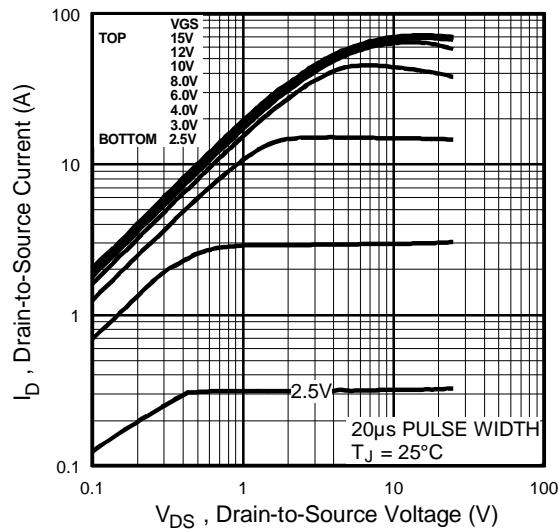


Fig 1. Typical Output Characteristics

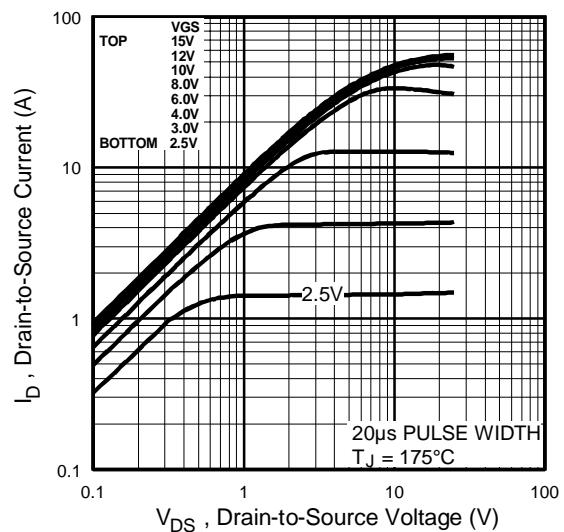


Fig 2. Typical Output Characteristics

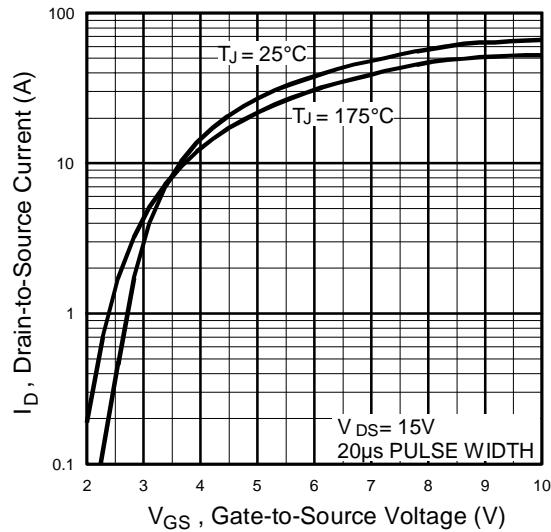


Fig 3. Typical Transfer Characteristics

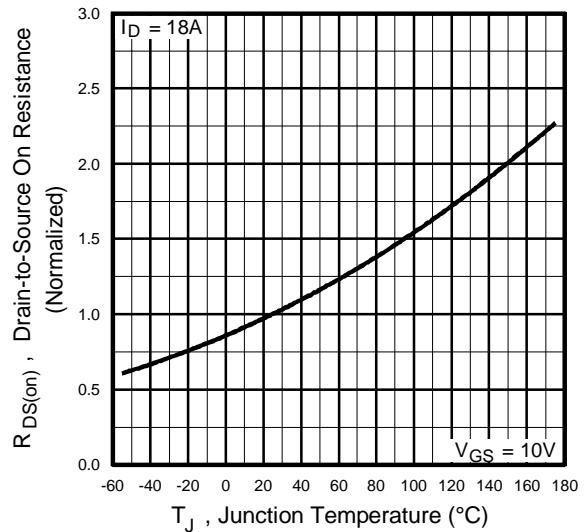


Fig 4. Normalized On-Resistance
Vs. Temperature

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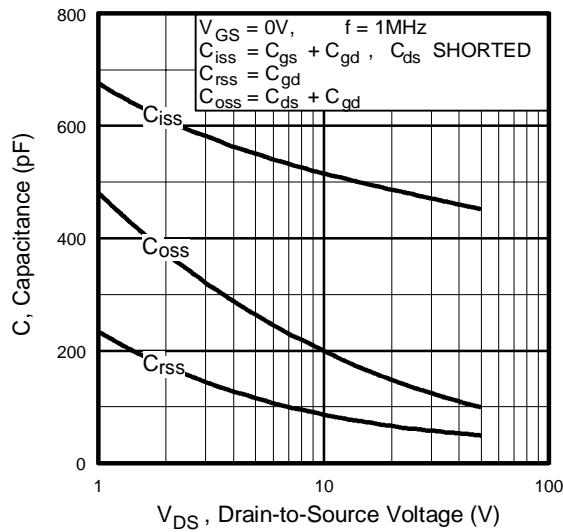


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

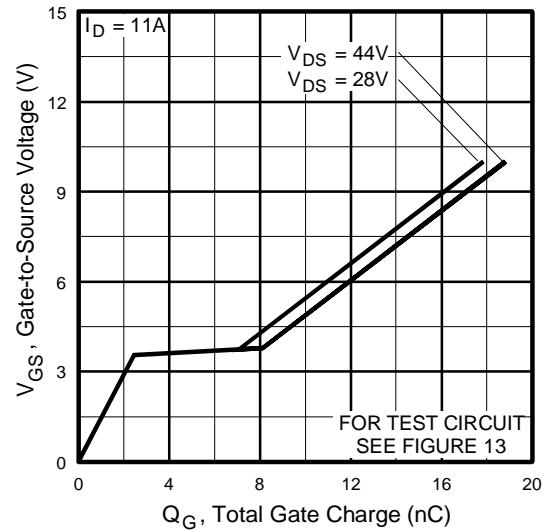


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

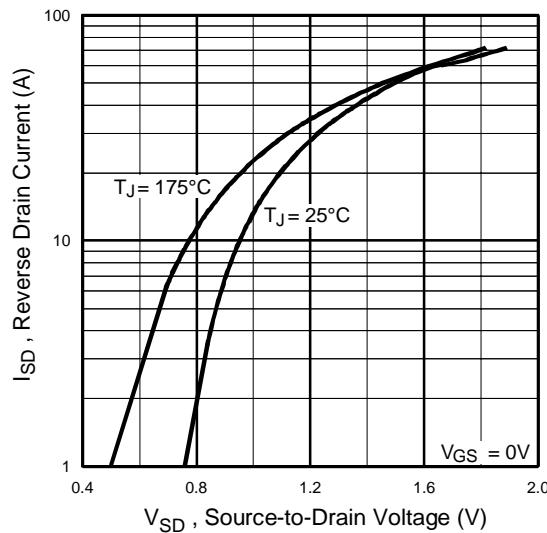


Fig 7. Typical Source-Drain Diode
Forward Voltage

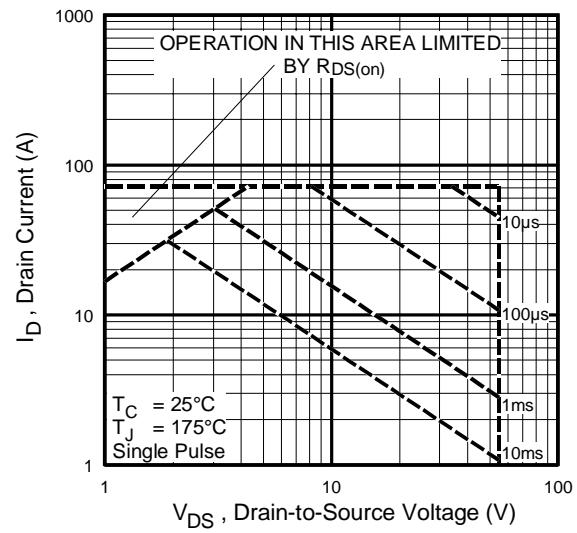


Fig 8. Maximum Safe Operating Area

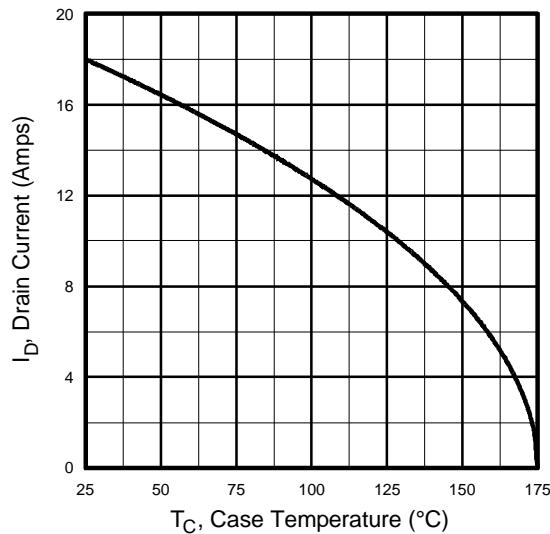


Fig 9. Maximum Drain Current Vs.
Case Temperature

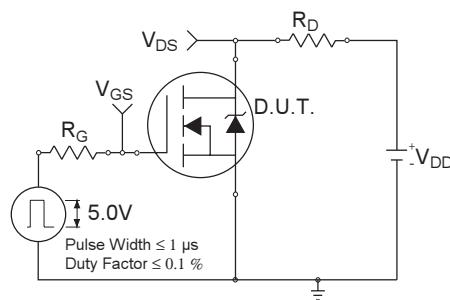


Fig 10a. Switching Time Test Circuit

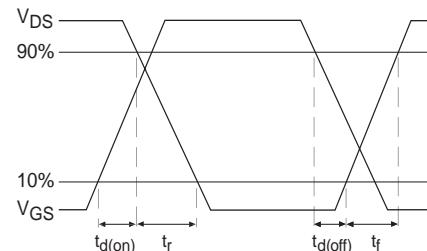


Fig 10b. Switching Time Waveforms

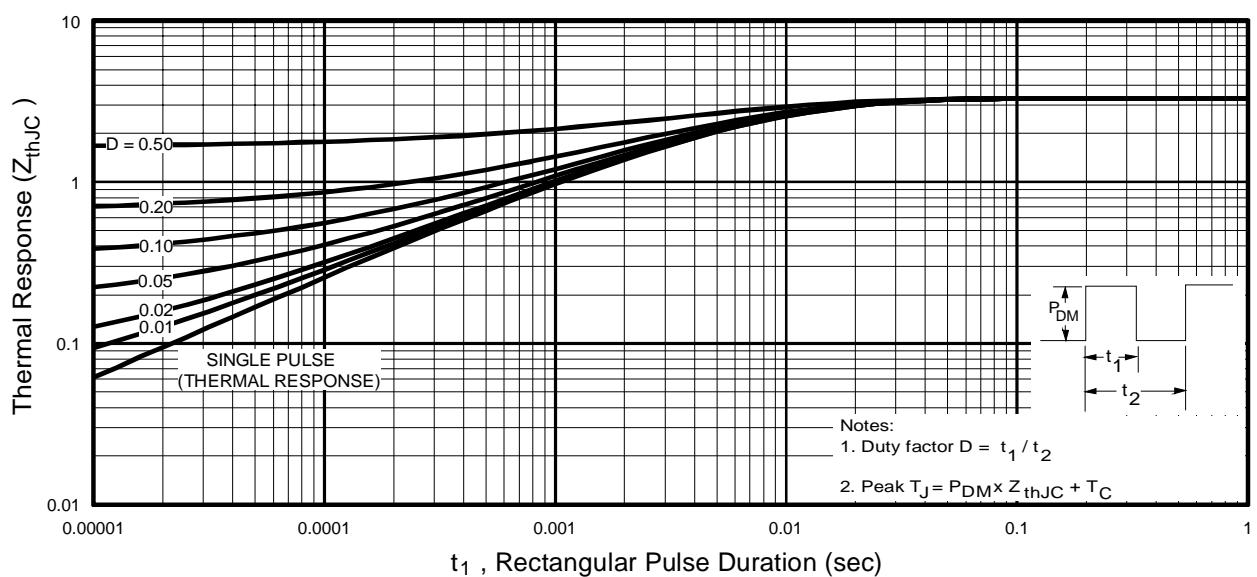


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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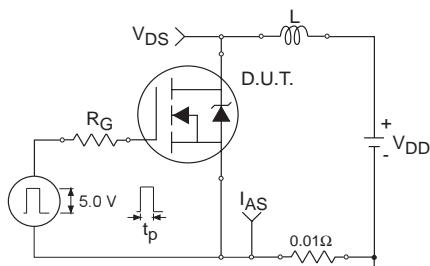


Fig 12a. Unclamped Inductive Test Circuit

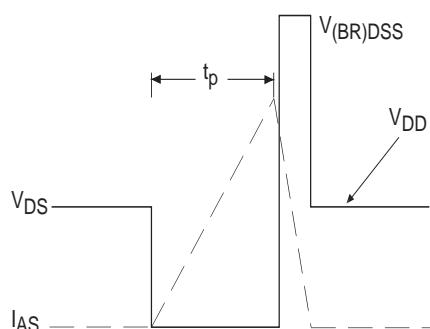


Fig 12b. Unclamped Inductive Waveforms

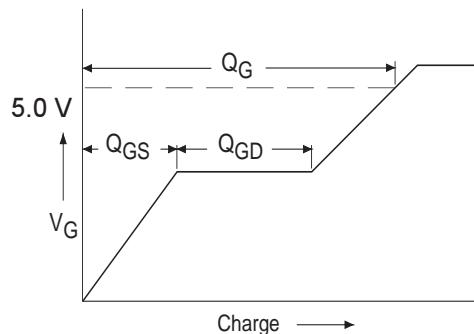


Fig 13a. Basic Gate Charge Waveform

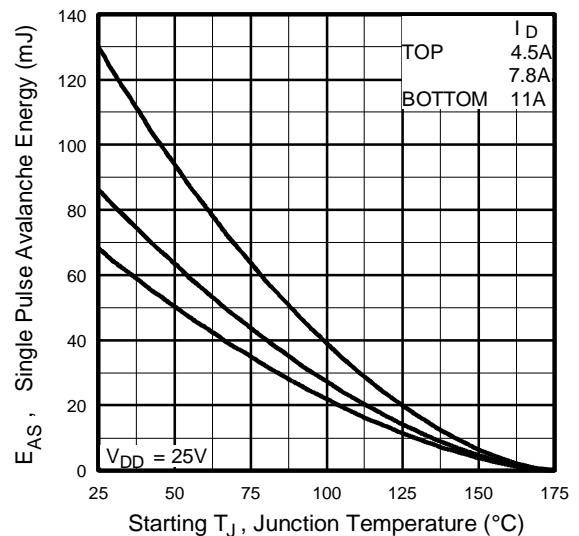


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

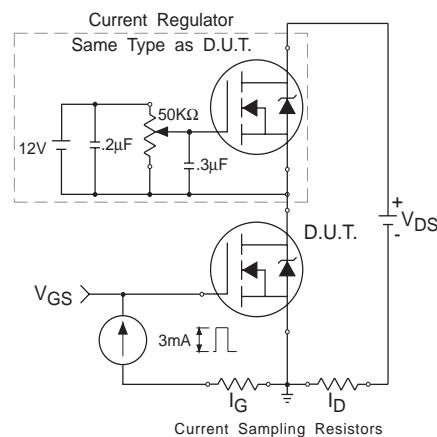
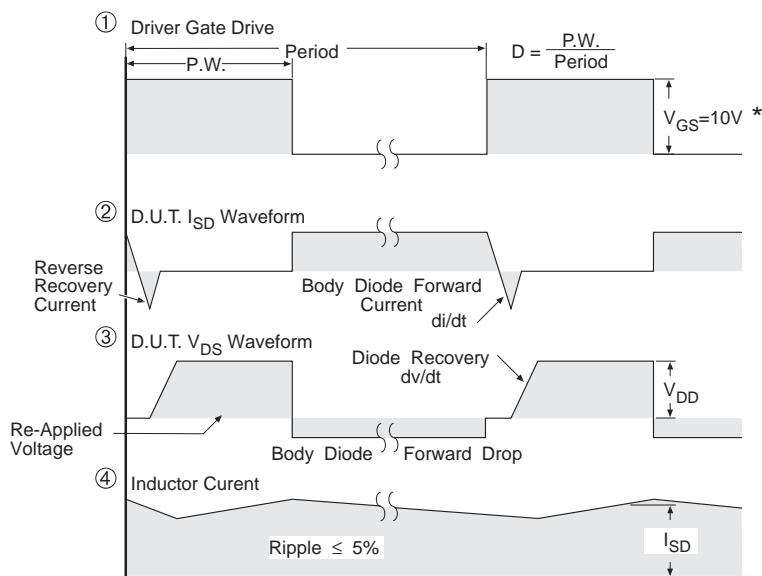
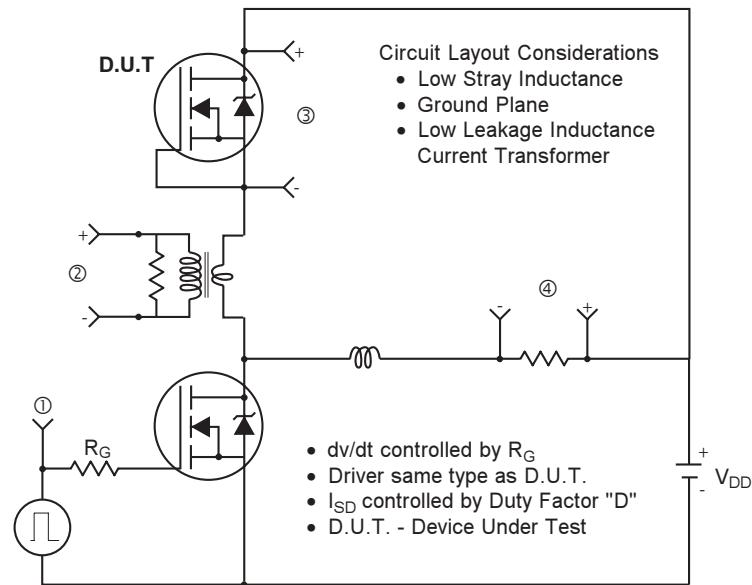


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETs

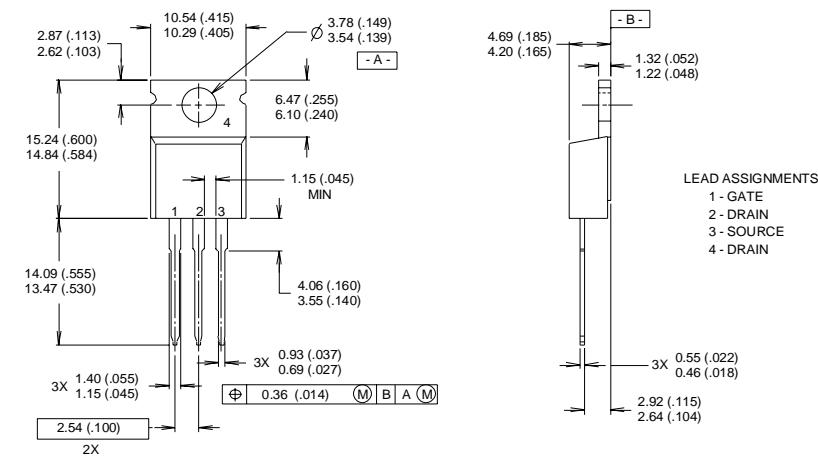
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Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES:

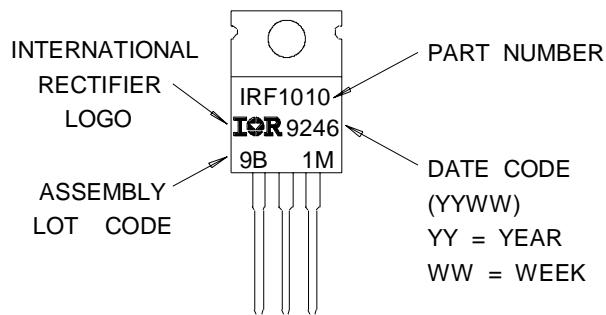
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.

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