

Table 3-2. Data Movement Operation Format

Instruction	Operand Syntax	Operand Size	Operation
EXG	Rn, Rn	32	$Rn \leftarrow \rightarrow Rn$
FMOVE	FPm,FPn <ea>,FPn FPm,<ea> <ea>,FPcr FPcr,<ea>	X B, W, L, S, D, X, P B, W, L, S, D, X, P 32 32	Source \rightarrow Destination
FSMOVE, FDMOVE	FPm,FPn <ea>,FPn	X B, W, L, S, D, X	Source \rightarrow Destination; round destination to single or double precision.
FMOVEM	<ea>,<list> ¹ <ea>,Dn <list> ¹ ,<ea> Dn,<ea>	32, X X 32, X X	Listed Registers \rightarrow Destination Source \rightarrow Listed Registers
LEA	<ea>,An	32	<ea> \rightarrow An
LINK	An,#<d>	16, 32	$SP - 4 \rightarrow SP$; $An \rightarrow (SP)$; $SP \rightarrow An$, $SP + D \rightarrow SP$
MOVE MOVE16 MOVEA	<ea>,<ea> <ea>,<ea> <ea>,An	8, 16, 32 16 bytes 16, 32 \rightarrow 32	Source \rightarrow Destination Aligned 16-Byte Block \rightarrow Destination
MOVEM	list,<ea> <ea>,list	16, 32 16, 32 \rightarrow 32	Listed Registers \rightarrow Destination Source \rightarrow Listed Registers
MOVEP	Dn, (d ₁₆ ,An) (d ₁₆ ,An),Dn	16, 32	Dn 31–24 \rightarrow (An + d _n); Dn 23–16 \rightarrow (An + d _n + 2); Dn 15–8 \rightarrow (An + d _n + 4); Dn 7–0 \rightarrow (An + d _n + 6) (An + d _n) \rightarrow Dn 31–24; (An + d _n + 2) \rightarrow Dn 23–16; (An + d _n + 4) \rightarrow Dn 15–8; (An + d _n + 6) \rightarrow Dn 7–0
MOVEQ	#<data>,Dn	8 \rightarrow 32	Immediate Data \rightarrow Destination
PEA	<ea>	32	$SP - 4 \rightarrow SP$; <ea> \rightarrow (SP)
UNLK	An	32	$An \rightarrow SP$; (SP) \rightarrow An; $SP + 4 \rightarrow SP$

NOTE: A register list includes any combination of the eight floating-point data registers or any combination of three control registers (FPCR, FPSR, and FPIAR). If a register list mask resides in a data register, only floating-point data registers may be specified.

3.1.2 Integer Arithmetic Instructions

The integer arithmetic operations include four basic operations: ADD, SUB, MUL, and DIV. They also include CMP, CMPM, CMP2, CLR, and NEG. The instruction set includes ADD, CMP, and SUB instructions for both address and data operations with all operand sizes valid for data operations. Address operands consist of 16 or 32 bits. The CLR and NEG instructions apply to all sizes of data operands. Signed and unsigned MUL and DIV instructions include:

- Word multiply to produce a long-word product.
- Long-word multiply to produce a long-word or quad-word product.
- Long word divided by a word divisor (word quotient and word remainder).
- Long word or quad word divided by a long-word divisor (long-word quotient and long-word remainder).