Design Portfolio

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Submitted in pursuit of the degree

BACHELOR OF ENGINEERING

In

COMPUTER AND ELECTRONIC ENGINEERING

North-West -University Potchefstroom Campus

Supervisor: Prof J. Holm

Potchefstroom

2017

It all starts here ™

NORTH-WEST UNIVERSITY
YUNIBESITI YA BOKONE-BOPHIRIMA
NOORDWES-UNIVERSITEIT
POTCHEFSTROOM CAMPUS

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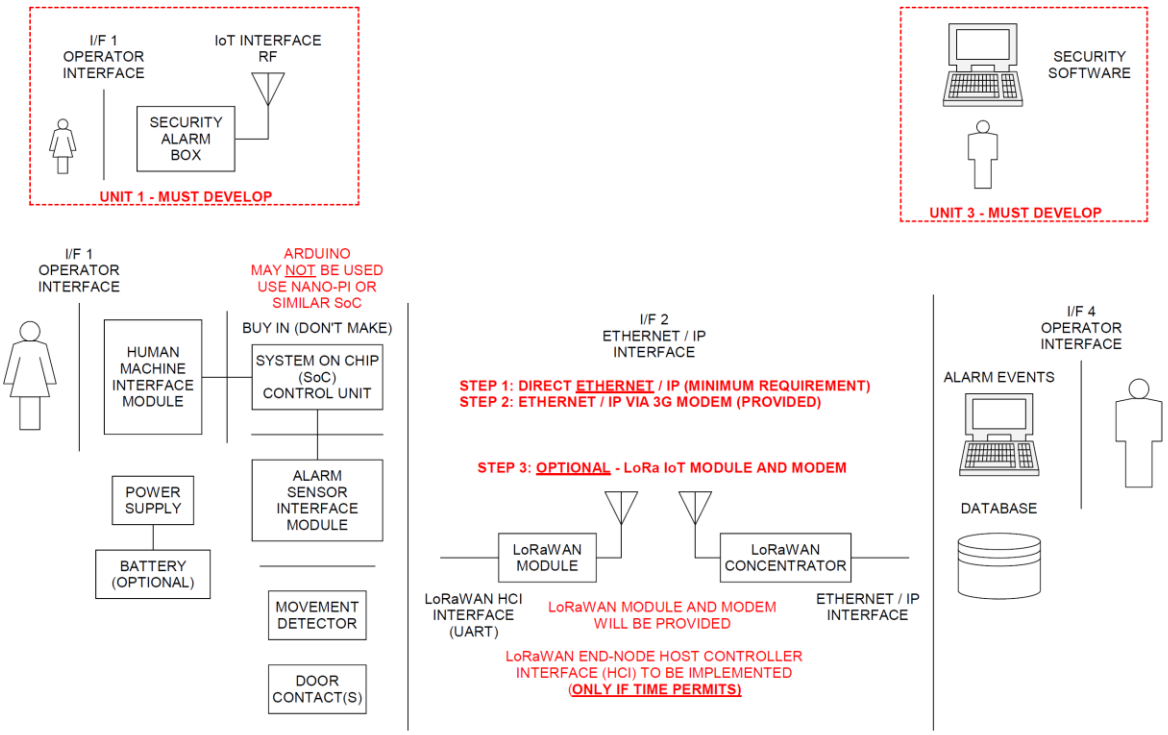
List of abbreviations:

- FSM – Finite State Machine
- UDP – User Datagram Protocol
- OS – Operating System
- SoC – System on Chip
- SBC – Single Board Computer.
- DCS – Door Contact Switch

1 SYSTEM OPERATIONAL REQUIREMENTS

1.1 FUNCTIONAL ANALYSIS – OPERATIONAL LEVEL ARCHITECTURE AND BEHAVIOUR

1.1.1 System Operational Architecture:



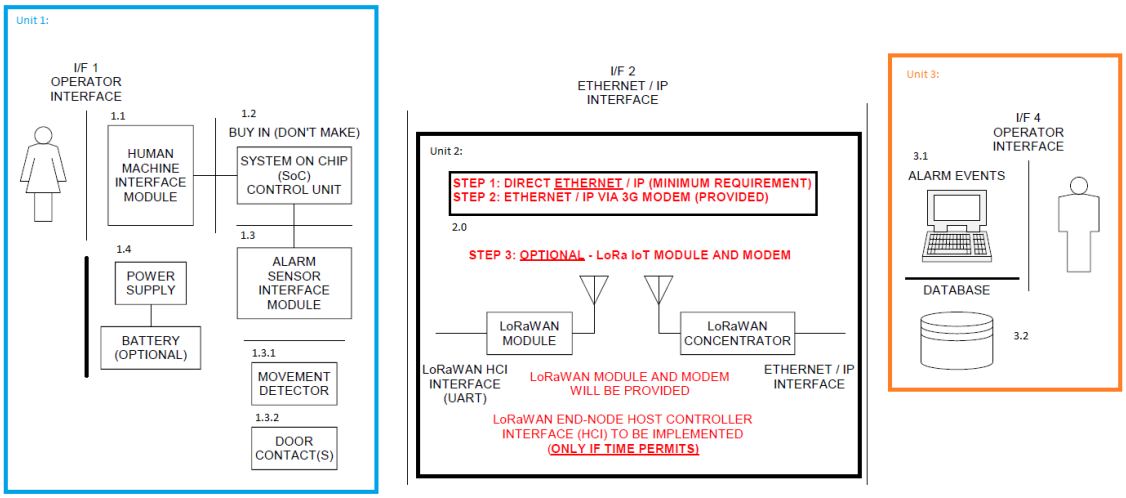


Figure 1: System Operational Architecture

1.1.2 System Operational Flow:

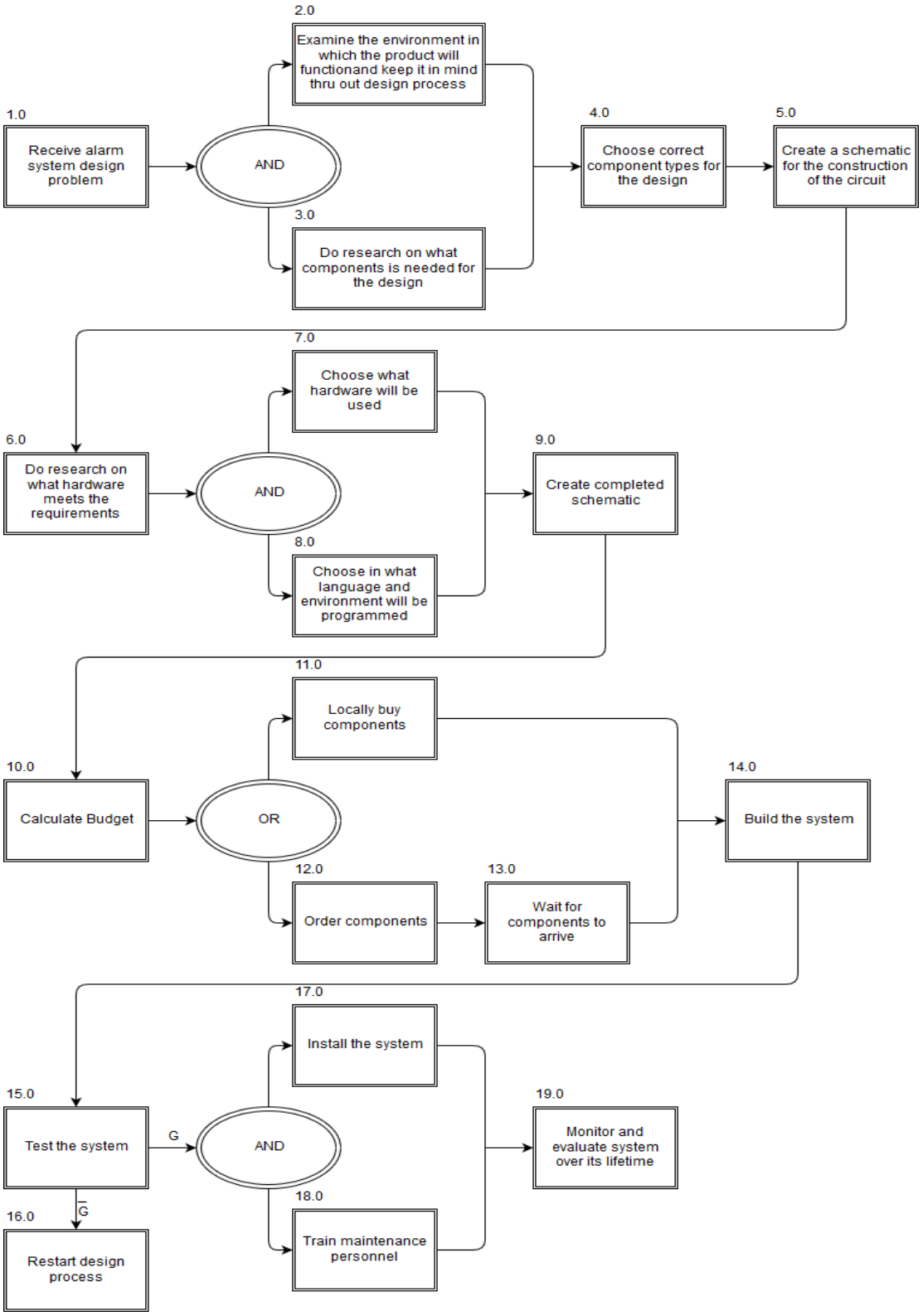


Figure 2: System Operational Flow

1.2 PHYSICAL REQUIREMENTS (FORM):

- The alarm panel as well as any sensors of the system must be IP54 rated.
- The alarm panel must be wall mountable
    - The Design must not exceed 0.5Kg as to be easily wall mountable
- Unit should not protrude at strange angles that will cause harm to people passing by. All edges must be smooth to the touch, with no sharp object on the unit to cut/hurt.
- Functional shape that will fit into any home without inconvenience
- Size of unit must not be to large
    - 1m x 1m x 0,5m size constraint
- The alarm panel must allow for wires to enter the panel without damaging the wires. A rubber grommet is used to protect wires extruding from the unit.
- The placement on the wall cannot be too high as it will make it difficult for users to access the panels 1.6 meter from floor level is recommended, this can be varied for specific user use.
- The placement cannot be to low either as it may become a risk for small children, placement must be more than 1 meter from floor level
- The placement should not be over pre-existing water pipes or wiring in the wall

1.3 INTERFACE REQUIREMENTS(FIT):

- The interface between the end user and the alarm will be both audio and visual, and be easily understandable (I/F 1.1)
- All items on the functional architecture must be developed, apart from PIR and other sensors (I/F 1.4)
- The single board computer (SBC) will be a Raspberry Pi
- An output will be provided to the Power Block to show that motion has been detected on an “outdoor sensor”
- The input power to the Alarm Panel will be provided from the Power Block and will be 12V at a maximum of 6W (I/F 1.5)
- The interface between the incoming power and the internal power supply of the system will be a two-wire interface, positive and negative wire, to be connected to the system with screw in wire terminals. (I/F 1.5)

- The Alarm Panel will provide its own internal voltages for the SBC and other components (Unit 1.4)
- The network communication between the Alarm panel and the backend-server is to be done with a direct ethernet connection or a WIFI connection (I/F 2)
- The database server will initially be hosted on a laptop or PC.

1.4 ADDITIONAL REQUIREMENTS:

1.4.1 Environmental Requirements:

- The alarm panel as well as any sensors of the system must be IP54 rated
- Dust proof rating of 5, Limited protection against dust ingress. (no harmful deposit)
- Water resistant rating of 4, Protected against splash water from any direction.
- Temperature requirement of -5°C to 40°C
- Will be made reasonably tamper proof. Wires are tied down internally to prevent the destruction of internal component when the extruded wires are being tampered with.
- The Alarm panel is to be serviceable with the use of a key to open the unit. Key will only be available to trained technicians.
- Will be made from strong material to endure some wear a metal chassis is to be used for the alarm panel
- The system must be protected against Electro Static Discharges, ESD.

1.4.2 Safety requirements

- The system will be grounded to ensure no electrical shocks can occur to an end user
- No open wires
- Not accessible to children
- Closed box so that people who do not understand the device cannot tamper with it
- Reasonably tamper proof

1.43 Legislative Requirements (SAIDSA bylaw 25)

- Control equipment
  - Control panel installed min of 1.5 m form ceiling
  - Digital keypads must be of the data transfer technology type
  - Disarming delay no more than 30 seconds
- Signalling equipment
  - Signalling equipment will be positioned within the protected area
  - Not placed where telephone lines are vulnerable

- Maintenance
  - Inspect and test each detection device back to control panel
  - Inspecting alarm panel and transmitter
  - Inspect cables for visible damage

1.4.4 Usability Requirements:

- System must be easily operated with minimal training required to operate the system
- Compensation for mounting will be made for the control box

2 EXCEL PROJECT MANAGEMENT

2.1 COMBINED PROJECT DOCUMENTS

The following documentation has been taken and adapted from the project management excel document.

2.1.1 WORK BREAKDOWN ALLOCATION

In the following Table 1 the work allocation for each member is documented. This work allocation was done at the start of the project and as new work may arise or some work may prove to be more difficult than thought or some work may be found to be very easy this list will be adjusted accordingly.

Table 1: Work Breakdown and Allocation

Member	Work allocation
Randolph Bock	• Design circuit for security inputs (Including Door switches and PIR's) • Design circuit for output siren (to be run on 12v) • Design and implement a user interface • Design and code the SoC to handle all inputs and outputs • Order parts • Trade-off decisions • Assemble the final unit 1 as a whole • Design and implement a Direct Ethernet / IP connection between SoC and Pc • Design and implement an Ethernet / IP connection via 3g between SoC and Pc
FJ Fourie	• Design database for information of users and alarm systems • Design backend operator interface • Write program for backend of system to manage alarms going off and instruct operators on what to do • Integrate backend program with database

	• Ensure operator interface works correctly with signals received from web • Assemble the final complete project • Designing and implementing the backend communications to the SoC

2.1.2 PROJECT SCHEDULE

Below in Table 2 the timeline for the project is documented as decided upon at the start of the project.

Table 2: Project Schedule

Date	Description
17-Jul-17	**Project Initiation**
10-Aug-17	**Functional Analysis Test**
14-Aug-17	**Preliminary Design Complete**
31-Aug-17	**30% Completion Milestone**
30-Sep-17	**50% Completion Milestone**
27-Oct-17	**80% Completion Milestone**
10-Nov-17	**100% Completion Milestone**
16-Nov-17 to 17-Nov-17	**Demonstration**

2.1.3 PROGRESS TRACKING

We use a RAG status to track the progress of the project each week with descriptions for when the project falls into the amber or red regions. This is all shown below in Table 3.

Table 3: Progress tracking

Progress Tracking					
		Project Status			
	% Complete	Green	Amber	Red	Description
Week 1	100%				
Week 2	100%				
Week 3	100%				
Week 4	100%				
Week 5	100%				
Week 6	100%				
Week 7	100%				
Week 8	100%				
Week 9	100%				
Week 10	100%				
Week 11	100%				
Week 12	100%				
Week 13	100%				
Week 14					
Etc					

2.2 RISK / MITIGATION REGISTER

Table 4: Risks and Mitigations

Risk No	Date	Description of Issue / Risk	Severity	Impact	Mitigation / Action	Responsible person	Status
	Date when risk was identified	*Description of issue / risk*	*(1-5)*	*What will happen when this risk event happens?*	*What needs to be done to reduce this risk.*	*Who will work on this risk.*	
1	28-Aug-17	*Availability of PIR running on 5/3.3V*	*1*	*Circuit will need to change to use 12V PIR's correctly*	*Order PIR using 5/3.3 Volt as soon as possible,*	*Randolph Bock*	
				not to overvolt the control unit	*Or change circuit to use 12V PIR's*		
2	21-Aug-17	*Time Manegment*	*5*	*If time is not managed correctly the project will be*	*Work with the schedule provided*	*All members*	
				rushed, affecting quality of the project			
3	08-Aug-17	*Groupwork not yet distributed*	*5*	*Members will not be able to work as they don't*	*Assigning and documenting groupwork*	*Randolph Bock*	
				know what they should be working on	*to each member*		
4	11-Sep-17	*Database Design*	*3*	*Database nor working or working incorrectly,*	*Work with Database design software and*	*FJ Fourie*	
				resulting in a fail of unit 3	*familiarize with the language of databases*		
5	04-Sep-17	*Power distribution*	*4*	*Under or over power of project, ultimately leading*	*Do power management calculations*	*Randolph Bock*	
				to the project not working			
6	18-Sep-17	*Subject know how*	*5*	*If one or more members do not have the necessary*	*Tell other members if you do not have the*	*All members*	
				knowledge to complete their unit	*knowledge and seek help*		
7	24-Aug-17	*Uncertainty about 30% deadline*	*3*	*We cannot complete work satisfactory and all the*	*Find out by asking fellow class members*	*Anton Duronat*	
				necessary work if we do not know what it is	*and talking to the lecturer*		
8	18-Sep-17	*Uncertainty about 50% deadline*	*5*	*We cannot complete work satisfactory and all the*	*Find out by asking fellow class members*	*FJ Fourie*	
				necessary work if we do not know what it is	*and talking to the lecturer*		
9	05-Oct-17	*Non-participating Member*	*5*	*A non-participating member, Anton Durant, results*	*Reallocating the work of Anton to*	*Randolph Bock & FJ Fourie*	
				in a critical aspect of the project not working.	*Randolph and FJ*		
				Ultimately resulting in failure of the project.			

2.3 MINUTES OF MEETINGS

The following are the minutes of all the meetings held by the group.

Meeting 1:			
Date	08-Aug-17		
Time	14:00		
Chairman	***Randolph Bock***		
Attendance list	***Randolph Bock***		
	FJ Fourie		
	Anton Durandt		
Agenda			
Progress Tracking	***Progress on schedule***		
Issues / Risks and Mitigations	*Groupwork not yet distrobuted*		
Decisions	Functional Flow Diagram		
	Functional Architecture Design		
	Specification of interfaces		
Actions	Allocated work	***Randolph Bock***	Specification of interfaces
		FJ Fourie	Functional Flow Diagram
		Anton Durandt	Functional Architecture Design

Meeting 2:			
Date	21-Aug-17		
Time	8:00		
Chairman	***FJ Fourie***		
Attendance list	***Randolph Bock***		
	FJ Fourie		
	Anton Durandt		
Agenda			
Progress Tracking	15% complete		
Issues / Risks and Mitigations	*Time Manegment*		
Decisions	Members work allocation		
Actions	Allocated work	***Randolph Bock***	User end
			Unit 1
		FJ Fourie	Back end
			Unit 3
		Anton Durandt	Communications link
			Unit 2

Meeting 3:		
Date	24-Aug-17	
Time	15:30	
Chairman	***Anton Durandt***	
Attendance list	***Randolph Bock***	
	FJ Fourie	
	Anton Durandt	
Agenda		
Progress Tracking	20% complete	
Issues / Risks and Mitigations	Uncertainty about 30% deadline	
Decisions	Portfolio	ELO 8
		ELO 5
Actions	Allocate individual and group work between members	

Meeting 4:	
Date	28-Aug-17
Time	8:00
Chairman	***Randolph Bock***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	25% complete
Issues / Risks and Mitigations	Availability of PIR running on 5/3,3V
Decisions	Responsibilitys
Actions	Find out about prices and availibility of components

Meeting 5:	
Date	04-Sep-17
Time	8:00
Chairman	***FJ Fourie***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	30% complete
Issues / Risks and Mitigations	*Power distrobution*
Decisions	Finilize what components are necesarry
	and create Bill of materials (BOM)
Actions	Get quotes for items in the BOM

Meeting 6:	
Date	11-Sep-17
Time	8:00
Chairman	***Anton Durandt***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	35% complete
Issues / Risks and Mitigations	*Database Design*
Decisions	Code structure
Actions	Order components

Meeting 7:	
Date	18-Sep-17
Time	8:00
Chairman	***Randolph Bock***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	40% complete
Issues / Risks and Mitigations	*Subject know how*
Decisions	Decides who is responsible for what for 50% deadline
Actions	Start work on 50% deadline

Meeting 8:	
Date	23-Sep-17
Time	11:30
Chairman	***FJ Fourie***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	40% complete
Issues / Risks and Mitigations	*Uncertainty about 50% deadline*
Decisions	We are behind on work for 50% deadline
Actions	Work harder to complete work by 50% deadline

Meeting 9:	
Date	09-Oct-17
Time	8:00
Chairman	***Randolph Bock***
Attendance list	***Randolph Bock***
	FJ Fourie
Agenda	
Progress Tracking	45% complete
Issues / Risks and Mitigations	*50% deadline completion was not perfect*
Decisions	Everyone needs to work on there
	paperwork to complete 50%
	Need to start building and coding
	Need to report inactive member
Actions	Plan for the rest of the semester
	File a change request with prof Holm
	for inactive member
	Speak to Prof Holm on the state of member Anton

Meeting 10:	
Date	16-Oct-17
Time	8:00
Chairman	***FJ Fourie***
Attendance list	***Randolph Bock***
	FJ Fourie
Agenda	
Progress Tracking	60% complete
Issues / Risks and Mitigations	*Non- Participating member*
Decisions	Complete all documentation for next Monday
	Need to take case of inactive member further
Actions	Speak to Holm and report state of inactive member
	Arange meeting with inactive member Anton

Meeting 11:	
Date	17-Oct-17
Time	9:00
Chairman	***Randolph Bock***
Attendance list	***Randolph Bock***
	FJ Fourie
	Anton Durandt
Agenda	
Progress Tracking	60% complete
Issues / Risks and Mitigations	*Non- Participating member*
Decisions	Allow member chance to catch up with the
	work, Finish documentation for 80% completion
Actions	Work allocated for the 80% deadline
	deadline set for non-participating member Anton

2.4 RANDOLPH BOCK

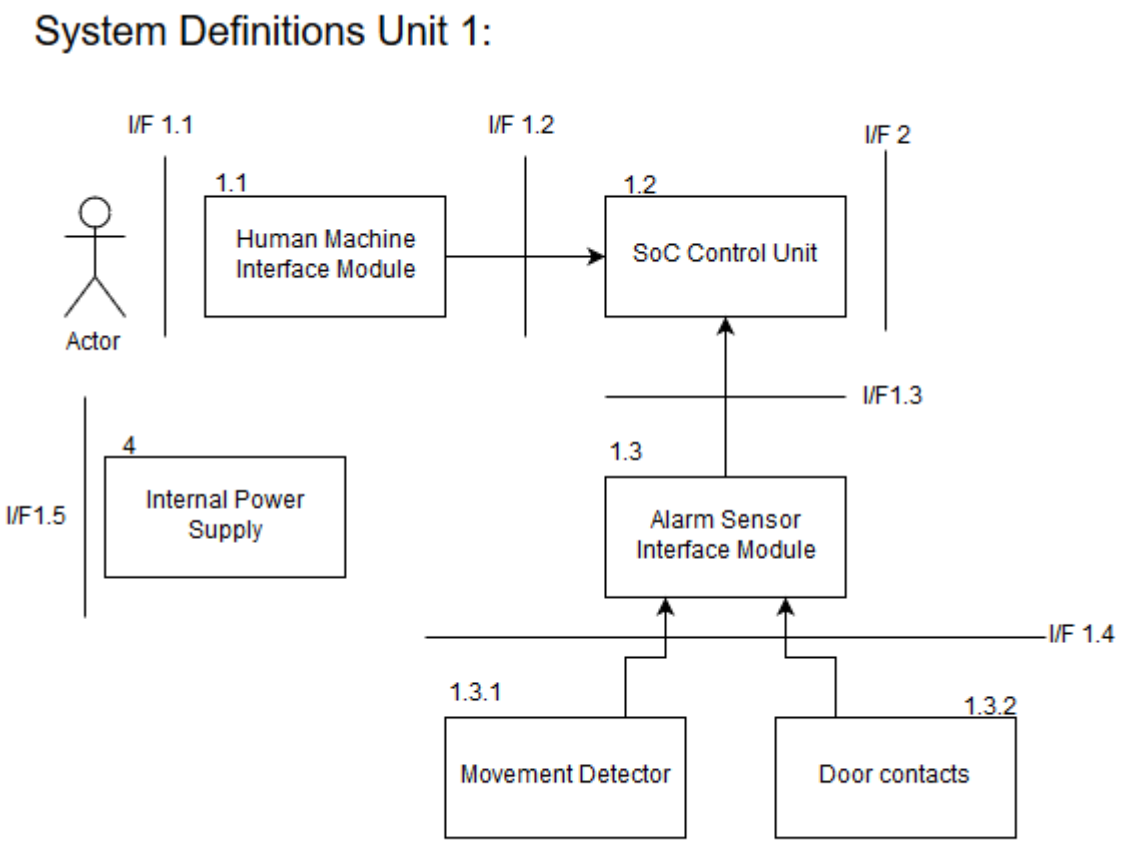
2.4.1 EXCEL PROJECT MANAGEMENT DOCUMENTS

2.4.1.1 EXPERTISE

- Software
- Hardware
- Documentation

2.4.1.2 PARTS OF THE PROJECT THE MEMBER IS RESPONSIBLE FOR

2.4.1.3 UNIT BREAKDOWN:



2.4.1.4 WORK BREAKDOWN

- Design circuit for security inputs (Including Door switches and PIR's)
- Design circuit for output siren (to be run on 12v)
- Design and implement a user interface
- Design and code the SoC to handle all inputs and outputs
- Order parts
- Trade-off decisions

- Assemble the final unit as a whole

2.4.1.5 TIMELINE

Table 5: Timeline of Randolph Bock

Date	Description
17-Jul-17	Project Initiation
10-Aug-17	Functional Analysis Test
14-Aug-17	Preliminary Design Complete
31-Aug-17	30% Completion Milestone
30-Sep-17	50% Completion Milestone
7-Oct-17	Design of inputs and outputs Unit 1
14-Oct-17	Code and implementation on SoC
20-Oct-17	Final assembly of Unit 1
27-Oct-17	80% Completion Milestone
10-Nov-17	100% Completion Milestone
16-Nov-17 to 17-Nov-17	Demonstration

2.4.1.6 PROGRESS TRACKING

Progress Tracking					
		Project Status			
	% Complete	Green	Amber	Red	Description
Week 1	100%				
Week 2	100%				
Week 3	100%				
Week 4	100%				
Week 5	100%				
Week 6	100%				
Week 7	100%				
Week 8	100%				
Week 9	100%				
Week 10	100%				
Week 11	100%				
Week 12	100%				
Week 13	100%				
Week 14					
Etc					

2.4.2 EXPERIENCE REPORT

Myself and two other members has been tasked to design and implement an alarm system for our third years project. The project was divided into 3 units, each member will be responsible for their own unit. The units consist of the physical Alarm Panel, communications, and back-end server. Unit 1 has been allocated to me as I had the most experience in hardware solutions.

The task was daunting at first, but after doing research and determining the requirement, the task then seemed doable within the given timeframe.

Skills required for the task of design Unit 1 the alarm panel is electronic knowledge for the electrical connection required. Programming knowledge to write the embedded system program, as well as knowledge of the Linux operating system distribution, “Raspbian”.

2.5 ANTON DURANDT

Member missing in action.

2.6 FJ FOURIE

2.6.1 EXCEL PROJECT MANAGEMENT DOCUMENTS

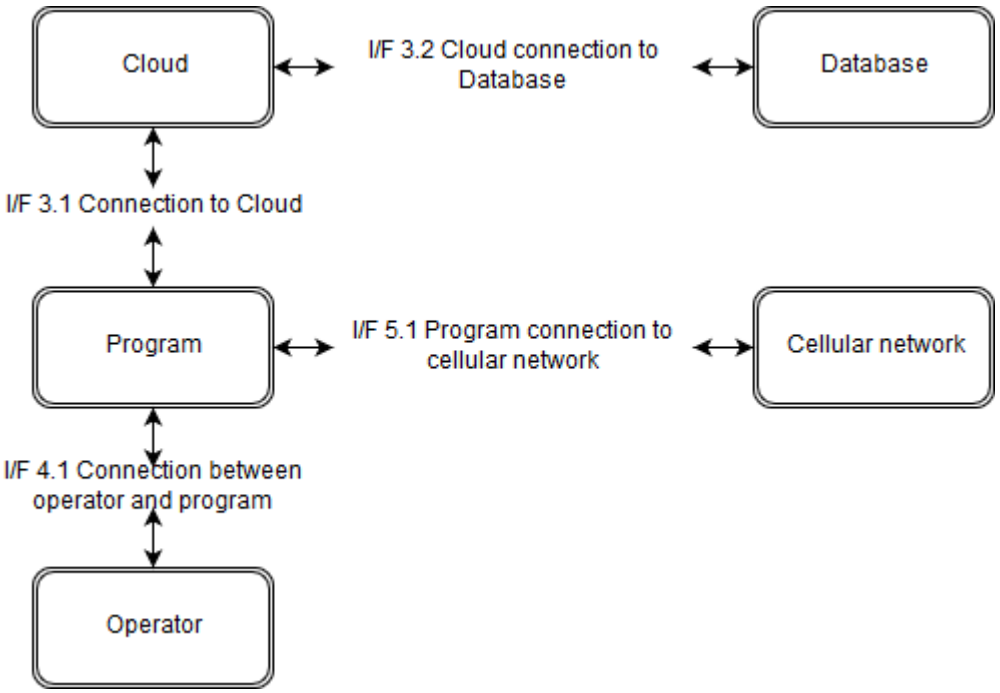
2.6.1.1 EXPERTISE

- Software
- Documentation
- Databases

2.6.1.2 PARTS OF THE PROJECT THE MEMBER IS RESPONSIBLE FOR

- I/F 4 Operator Interface
- I/F 3 Cloud Interface
- I/F 5 Cellular Network

2.6.1.3 UNIT BREAKDOWN



2.6.1.4 WORK BREAKDOWN

- Design database for information of users and alarm systems
- Design backend operator interface
- Write program for backend of system to manage alarms going off and instruct operators on what to do
- Integrate backend program with database
- Ensure operator interface works correctly with signals received from web
- Assemble the final complete project

2.6.1.5 TIMELINE

Table 6: Timeline of FJ Fourie

Date	Description
17-Jul-17	Project Initiation
10-Aug-17	Functional Analysis Test
14-Aug-17	Preliminary Design Complete
31-Aug-17	30% Completion Milestone
30-Sep-17	50% Completion Milestone
7-Oct-17	Design database and program for Unit 3
14-Oct-17	Write program and integrate program with database
20-Oct-17	Final assembly of Unit 3
27-Oct-17	80% Completion Milestone
10-Nov-17	100% Completion Milestone
16-Nov-17 to 17-Nov-17	Demonstration

2.6.1.6 PROGRESS TRACKING

Progress Tracking					
		Project Status			
	% Complete	Green	Amber	Red	Description
Week 1	100%				
Week 2	100%				
Week 3	100%				
Week 4	100%				
Week 5	100%				
Week 6	100%				
Week 7	100%				
Week 8	100%				
Week 9	100%				
Week 10	100%				
Week 11	100%				
Week 12	100%				
Week 13	100%				
Week 14					
Etc					

2.6.2 EXPERIENCE REPORT

In 2017 which is my 3rd year of studying I have been put into a team of 3 students to complete a project. The project that has been allocated to us is that of an alarm security system we must design and construct the entire system. The project was divided into 3 major units with each member being tasked with completing a unit. The first unit is the alarm panel and user end of the system, the second unit is the communication of the first unit with third unit over the cellular network. The third unit of this project is the backend program that will be connected to a database in the cloud and will be manned by an operator, this is the unit I have been given and tasked with completing. I went about completing this task by firstly identifying all the requirements and individual parts of my unit after which I started researching each component in an attempt to find the best possible solution for each requirement. Through my research and eventual completion of the unit have I broaden my knowledge of the fields of telecommunication, databases, programming and cloud hosting. This has also been a great opportunity for me to have grown as an engineer and thru this process I have grown my skills and abilities in these fields, my knowledge and abilities with the QT programming environment

have increased drastically as well as my capabilities in the C++ programming language. I have also learnt a lot about Databases learning to use the program and tools provided by MYSQL to create and host databases. This was also a great opportunity to increase my understanding and abilities with transmission of data over a wireless network using different protocols some of which are existing protocols and others which we designed ourselves. I have also gotten a much broader understanding of the engineering process and all the documentation involved with it as well as all the additional tools used before starting the actual building or programming of the project such as using functional analysis. I have also increased my abilities to work in a team and have learned a lot of important team skills that will be necessary in the work place one day.

3 ENGINEERING METHODS/SKILLS/TOOLS:

3.1 RANDOLPH BOCK

See additional Document: Design 2017 - Randolph ELO5 - Net1Bier.docx

3.2 ANTON DURANDT

Member missing in action.

3.3 FJ FOURIE

See additional Document: Design 2017 - FJ ELO5 - Net1Bier.docx

4 SUB-SYSTEM SPECIFICATION DOCUMENTS:

4.1 RANDOLPH BOCK

See additional Document: Design 2017 - Randolph Sub-System-specification-Document-Net1Bier.docx

4.2 ANTON DURANDT

Member missing in action.

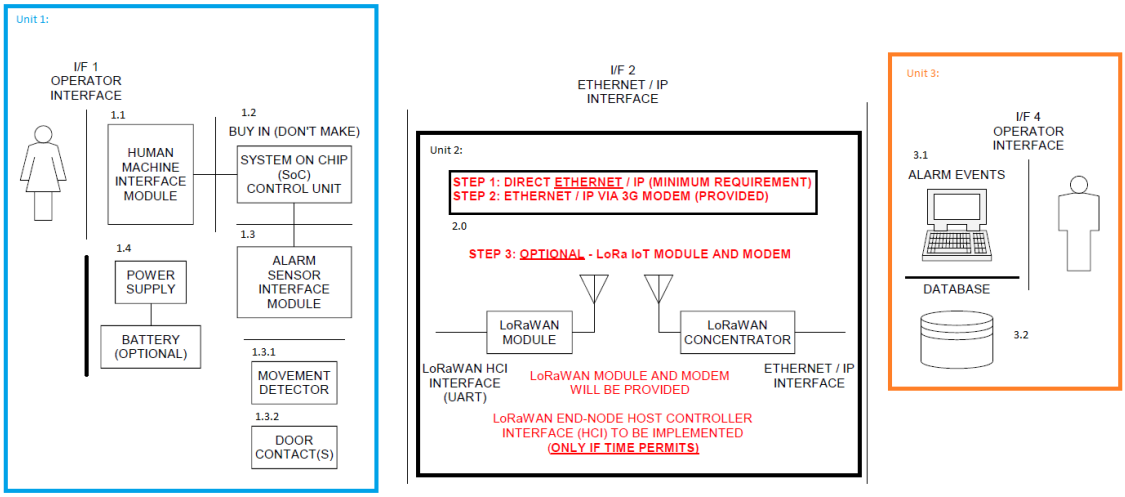
4.3 FJ FOURIE

See additional Document: Design 2017 - FJ Sub-System-specification-Document-Net1Bier.docx

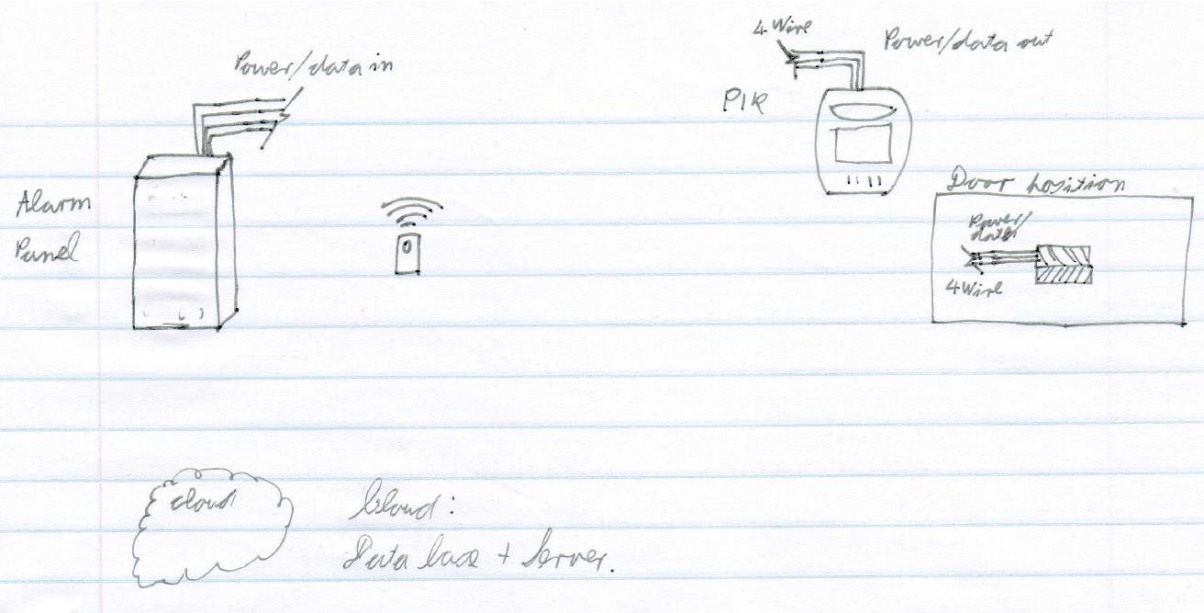
5 DESIGN DOCUMENTATION:

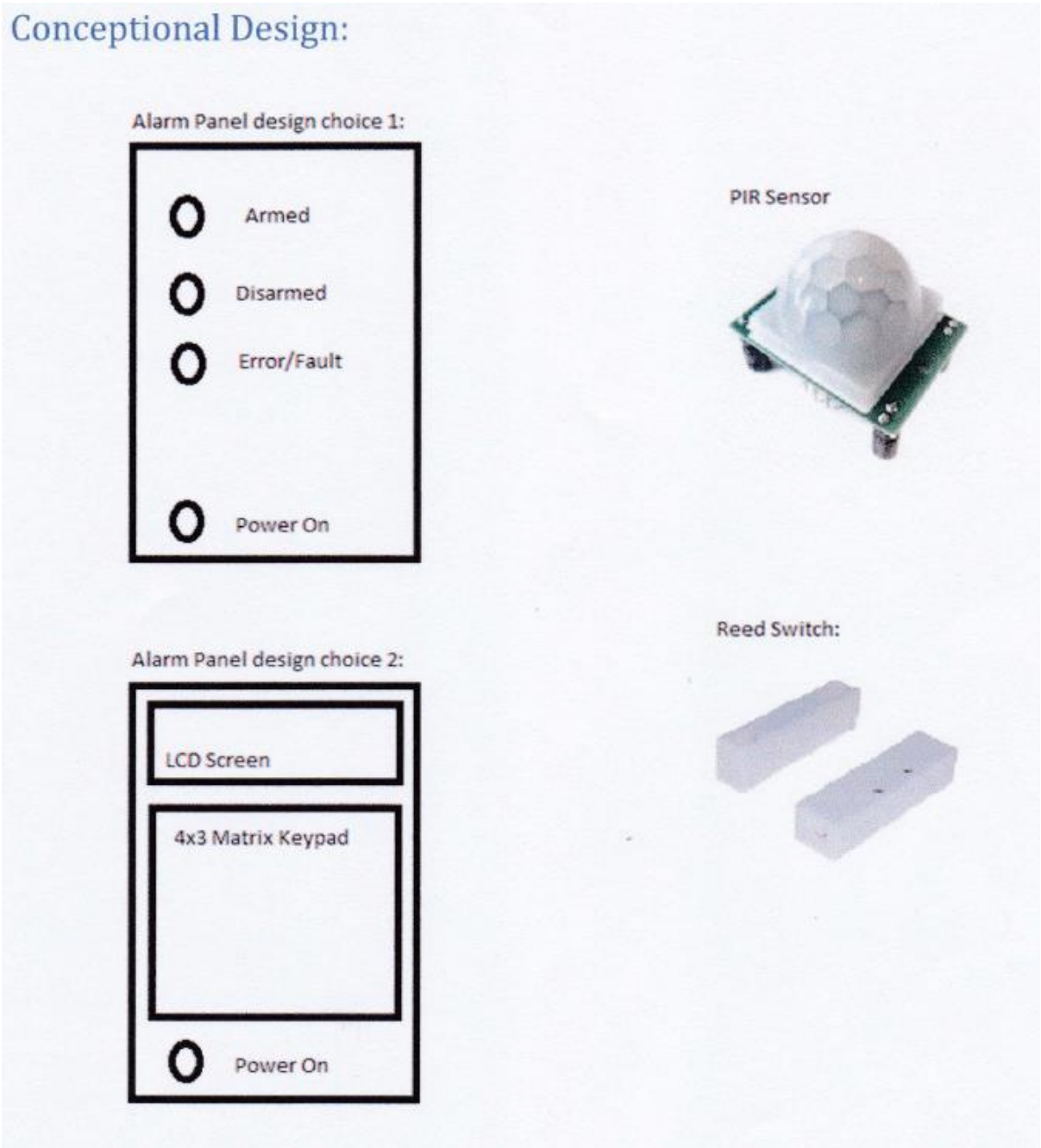
5.1 SYSTEM DESIGN DOCUMAENTATION

5.1.1 FINAL SYSTEM FUNCTIONAL DEFINITION:



5.1.2 SYSTEM CONCEPT DRAWINGS:



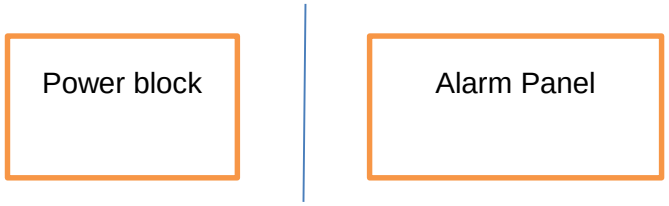


5.1.3 SYSTEM INTERFACE DEFINITIONS:

Interface control document (I/F 1.5)

This interface control document is the interaction between the power block and the alarm.

I/F 1.5



Electrical requirements

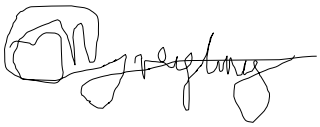
The power block will provide 12 V and 6 W power to the alarm panel.

Mechanical requirements:

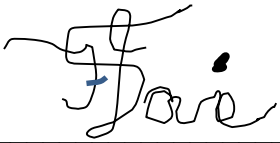
The mechanical interface will be a two-point screw terminal for both sides so that a wire can be connected between the two.

This document was signed in Potchefstroom on the date 2017/09/4 as an agreement between the EERI327/ INEM327 and REII327 students regarding the power supply to the alarm panel. This document is binding until the end of the 3rd year design module 2017.

Representatives



C.F. Greyling

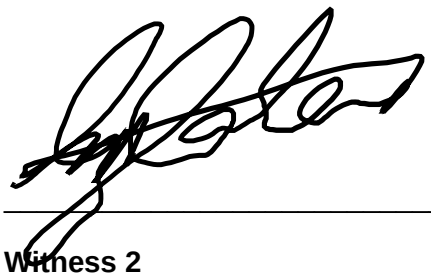


FJ Fourie

Witnesses

Net1Bier

Witness 1



Witness 2

Interface control document (I/F 2):

This interface control document is the network interaction between the Alarm panel and the Back-end security software.

Network requirements:

Transmission Control Protocol, TCP, to be used to send data from Panel to backend services.

For network connection:

1. The Alarm panel will send out a broadcast command over User Datagram Protocol, UDP. (Port 7000)
2. The Back-end server will then send it's IP over UDP to the alarm panel
3. A TCP Connection will be set-up between the server and the alarm panel. (Port 7000)
4. Communications will then take place according to the protocol requirements below

Protocol requirements:

Protocol payload fields:

Protocol ID ('1B')	Client ID	Date	Time	Section code	Parity

The payload fields will be "#" separated.

5.1.4 SYSTEM INTEGRATION TESTING:

Action	Expected Results	✓/✗
Trigger Alarm	Message sent through network to PC	
Read from Database	Read specific data from database to PC	

5.2 SUB-SYSTEM DESIGN DOCUMENTATION RANDOLPH BOCK:

5.2.1 TECHNOLOGY SURVEY/DATASHEETS

2N2222

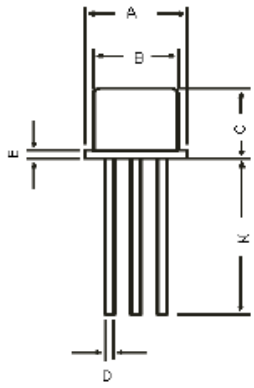
Low Power Bipolar Transistors

multicomp

Features:

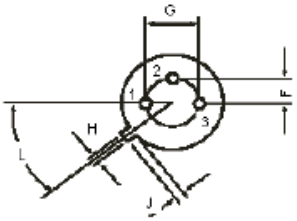
- NPN Silicon Planar Switching Transistors.
- Switching and Linear application DC and VHF Amplifier applications.

TO-18 Metal Can Package



Dimensions	Minimum	Maximum
A	5.24	5.84
B	4.52	4.97
C	4.31	5.33
D	0.40	0.53
E	-	0.76
F	-	1.27
G	-	2.97
H	0.91	1.17
J	0.71	1.21
K	12.70	-
L	45°	

Dimensions : Millimetres



Pin Configuration:
1. Emitter
2. Base
3. Collector

multicomp

Page 1 06/04/06 V1.0

2N2222

Low Power Bipolar Transistors

multicomp

Absolute Maximum Ratings (T_a = 25°C unless specified otherwise)

Description	Symbol	2N2222	Unit
Collector Emitter Voltage	V_{CEO}	30	V
Collector Base Voltage	V_{CBO}	60	
Emitter Base Voltage	V_{EBO}	5	
Collector Current Continuous	I_C	800	mA
Power Dissipation at T_a = 25°C Derate above 25°C	P_D	500 2.28	mW mW/°C
Power Dissipation at T_C = 25°C Derate above 25°C		1.2 6.85	W mW/°C
Operating and Storage Junction Temperature Range	T_J, Tstg	-65 to +200	°C

Electrical Characteristics (T_a = 25°C unless specified otherwise)

Description	Symbol	Test Condition	Value		Unit
			Minimum	Maximum	
Collector Emitter Breakdown Voltage	BV_{CEO}	I_C = 10mA, I_B = 0	30	-	V
Collector Base Breakdown Voltage	BV_{CBO}	I_C = 10µA, I_E = 0	60	-	
Emitter Base Breakdown Voltage	V_{EBOf}	I_E = 10µA, I_C = 0	5	-	
Collector Leakage Current	I_{CBO}	V_{CB} = 50V, I_E = 0 V_{CB} = 50V, I_E = 0 T_a = 150°C	-	10 10	nA µA
Collector Emitter Saturation Voltage	*$V_{CE\ (Sat)}$	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA	-	0.4 1.6	V
Base Emitter Saturation Voltage	*$V_{BE\ (Sat)}$	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA	0.6	1.3 2.6	

2N2222

Low Power Bipolar Transistors

multicomp

Electrical Characteristics (T_a = 25°C unless specified otherwise)

Parameter	Symbol	Test Condition	2N2222		Unit
			Minimum	Maximum	
DC Current Gain	h_{FE}	I_C = 0.1mA, V_{CE} = 10V* I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V* I_C = 150mA, V_{CE} = 1V* I_C = 150mA, V_{CE} = 1V* I_C = 500mA, V_{CE} = 10V*	35 50 75 50 100 30	300	-
Dynamic Characteristics					
Transition Frequency	f_t	I_C = 20mA, V_{CE} = 20V f = 100MHz	250	-	MHz
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0 f = 100kHz	-	8	pF
Input Capacitance	C_{ib}	V_{EB} = 0.5V, I_C = 0 f = 100kHz	-	30	
Switching Characteristics					
Delay Time	t_d	I_C = 150mA, I_{B1} = 15mA	-	10	ns
Rise Time	t_r	V_{CC} = 30V, $V_{BE\ (off)}$ = 0.5V	-	25	
Storage Time	t_s	I_C = 150mA, I_{B1} = 15mA	-	225	
Fall Time	t_f	I_{B2} = 15mA, V_{CC} = 30V	-	60	

*Pulse Condition: Pulse Width ≤300µs, Duty Cycle ≤2%.

Part Number Table

Package	Part Number
TO-18	2N2222

VISHAY
www.vishay.com

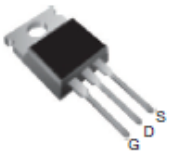
IRF9530, SiHF9530

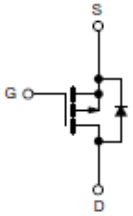
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	0.30
Q_g max. (nC)	38	
Q_{gs} (nC)	6.8	
Q_{gd} (nC)	21	
Configuration	Single	

TO-220AB





P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available
RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF9530PbF
	SiHF9530-E3
SnPb	IRF9530
	SiHF9530

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	-100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 12	A
		T_C = 100 °C		-8.2	
Pulsed Drain Current [a]			I_{DM}	-48	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	400	mJ
Repetitive Avalanche Current [a]			I_{AR}	-12	A
Repetitive Avalanche Energy [a]			E_{AR}	8.8	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	88	W
Peak Diode Recovery dV/dt [c]			dV/dt	- 5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) [d]	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = -25 V, starting T_J = 25 °C, L = 4.2 mH, R_g = 25 Ω, I_{AS} = -12 A (see fig. 12).
c. $I_{SD} \leq$ -12 A, dI/dt ≤ 140 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C.
d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = -1 mA	-	-0.10	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-	-	-100	µA
		V_{DS} = -80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10 V; I_D = -7.2 A [b]	-	-	0.30	Ω
Forward Transconductance	g_{fs}	V_{DS} = -50 V, I_D = -7.2 A [b]	3.7	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5	-	860	-	pF
Output Capacitance	C_{oss}		-	340	-	
Reverse Transfer Capacitance	C_{rss}		-	93	-	
Total Gate Charge	Q_g	V_{GS} = -10 V; I_D = -12 A, V_{DS} = -80 V, see fig. 6 and 13 [b]	-	-	38	nC
Gate-Source Charge	Q_{gs}		-	-	6.8	
Gate-Drain Charge	Q_{gd}		-	-	21	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -50 V, I_D = -12 A, R_g = 12 Ω, R_D = 3.9 Ω, see fig. 10 [b]	-	12	-	ns
Rise Time	t_r		-	52	-	
Turn-Off Delay Time	$t_{d(off)}$		-	31	-	
Fall Time	t_f		-	39	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.4	-	3.3	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p -n junction diode 	-	-	-12	A
Pulsed Diode Forward Current [a]	I_{SM}		-	-	-48	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = -12 A, V_{GS} = 0 V [b]	-	-	-6.3	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = -12 A, dI/dt = 100 A/µs [b]	-	120	240	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.46	0.92	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

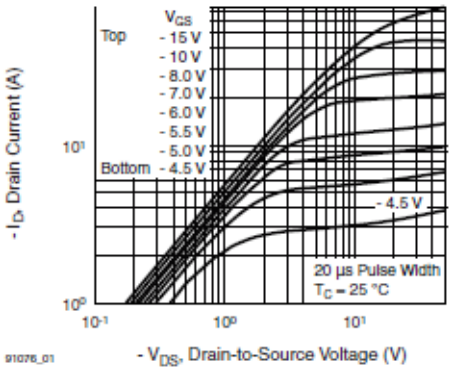


Fig. 1 -Typical Output Characteristics, T_C = 25 °C

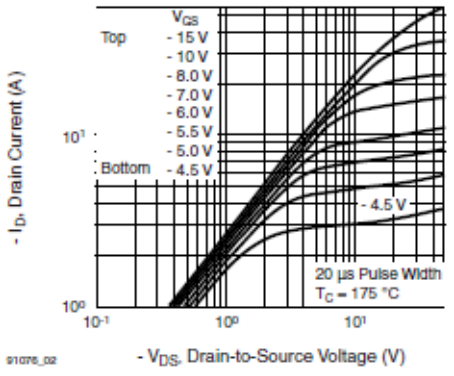


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

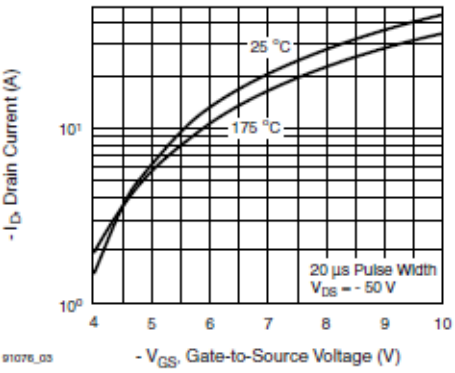


Fig. 3 -Typical Transfer Characteristics

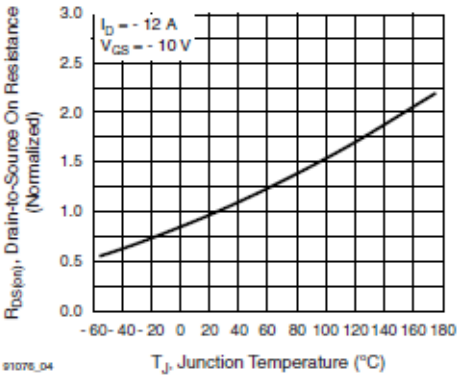


Fig. 4 -Normalized On-Resistance vs. Temperature

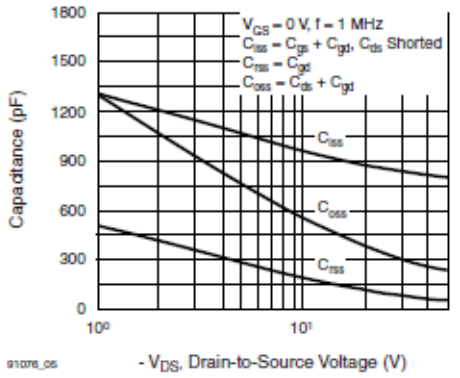


Fig. 5 -Typical Capacitance vs. Drain-to-Source Voltage

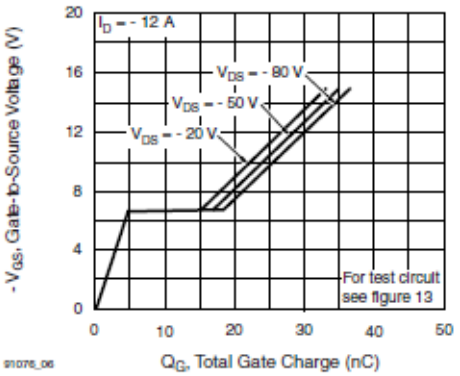


Fig. 6 -Typical Gate Charge vs. Gate-to-Source Voltage

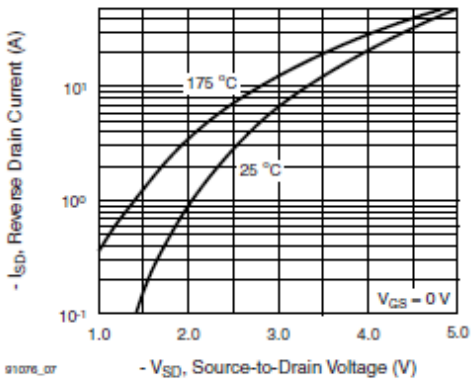


Fig. 7 -Typical Source-Drain Diode Forward Voltage

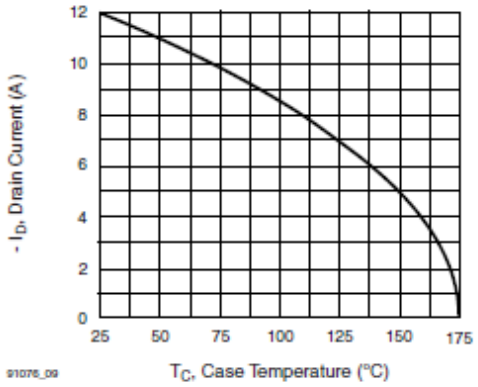


Fig. 9 -Maximum Drain Current vs. Case Temperature

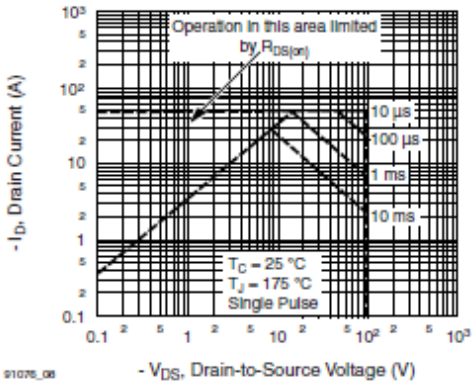


Fig. 8 -Maximum Safe Operating Area

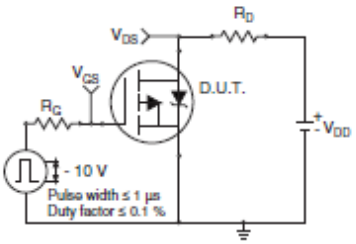


Fig. 10a - Switching Time Test Circuit

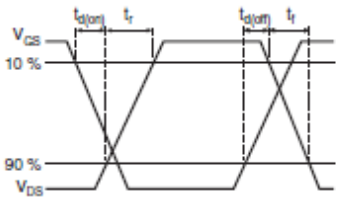


Fig. 10b - Switching Time Waveforms

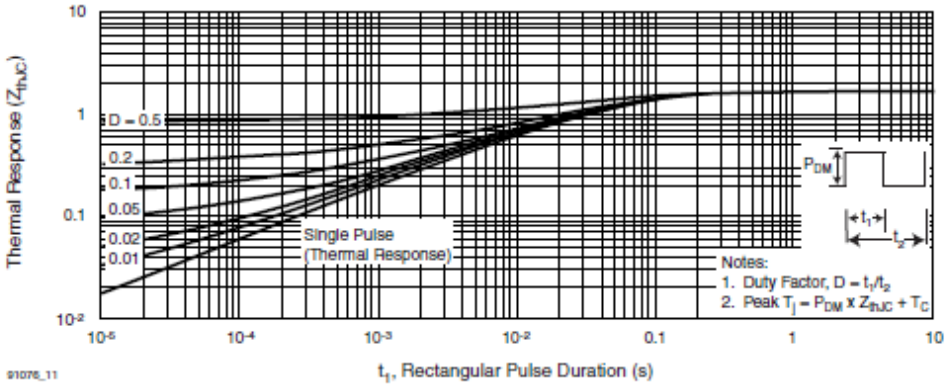


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

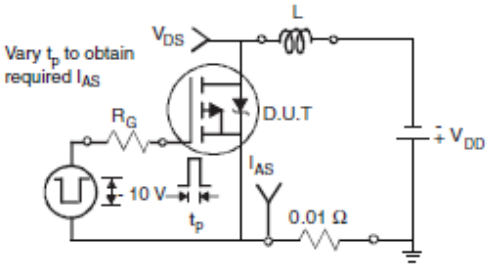


Fig. 12a - Unclamped Inductive Test Circuit

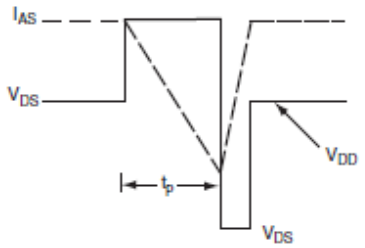


Fig. 12b - Unclamped Inductive Waveforms

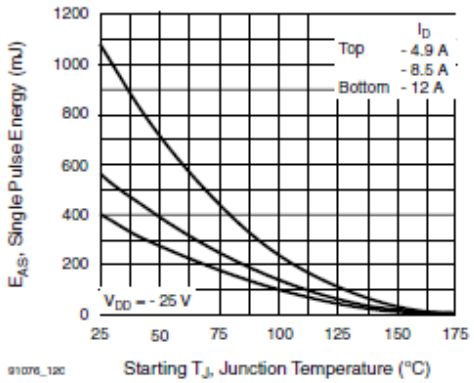


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

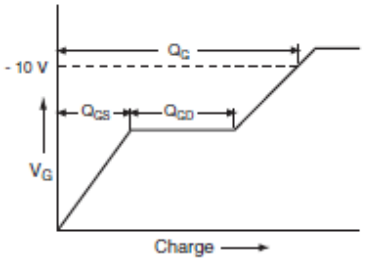


Fig. 13a - Basic Gate Charge Waveform

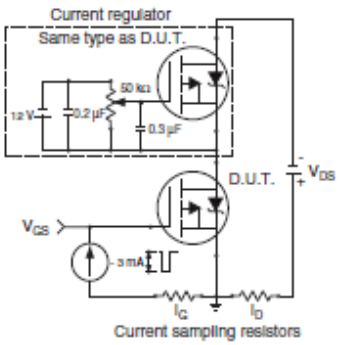
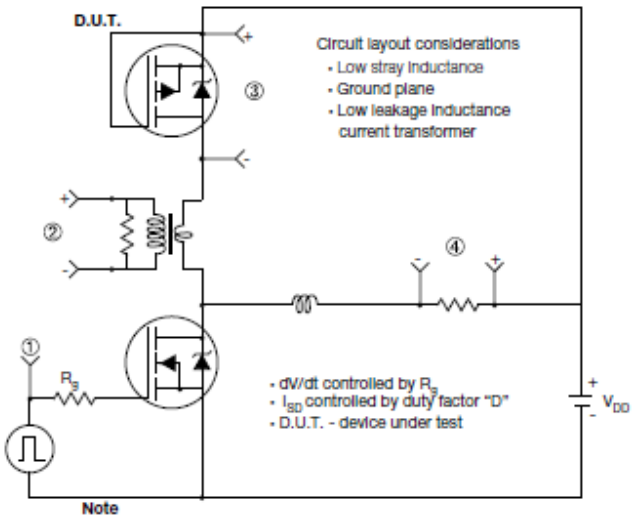
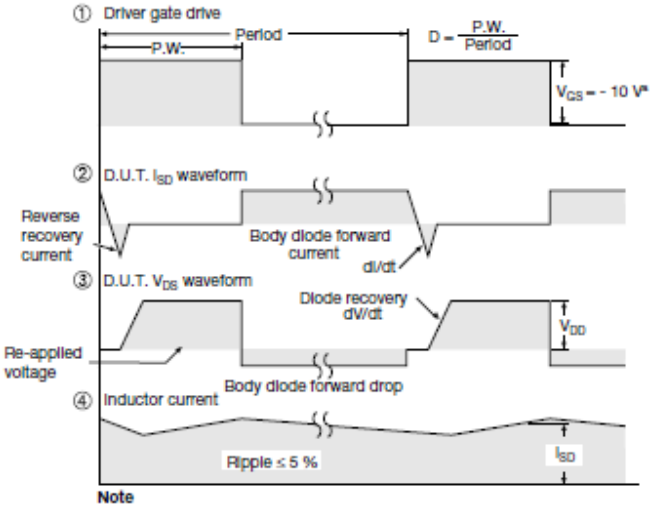


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

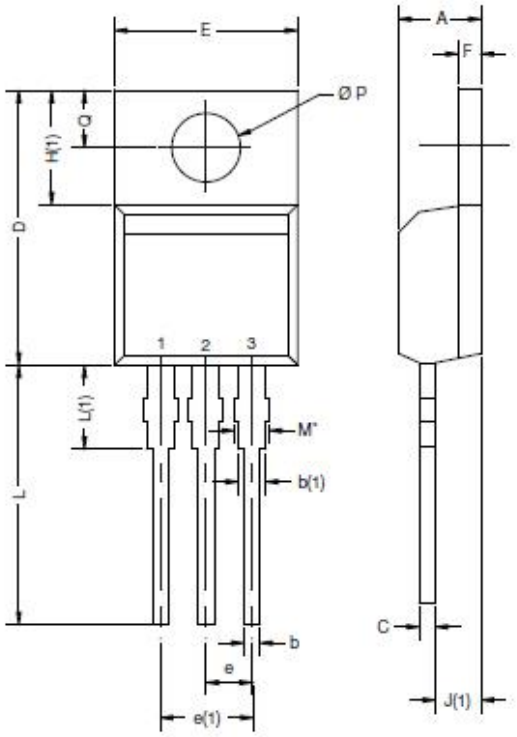
Fig. 14 -For P-Channel

VISHAY
www.vishay.com

Package Information

Vishay Siliconix

TO-220-1

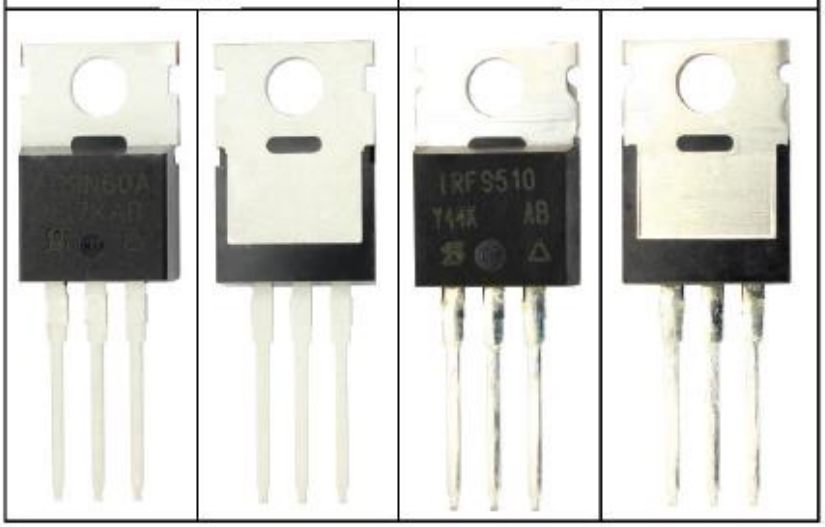


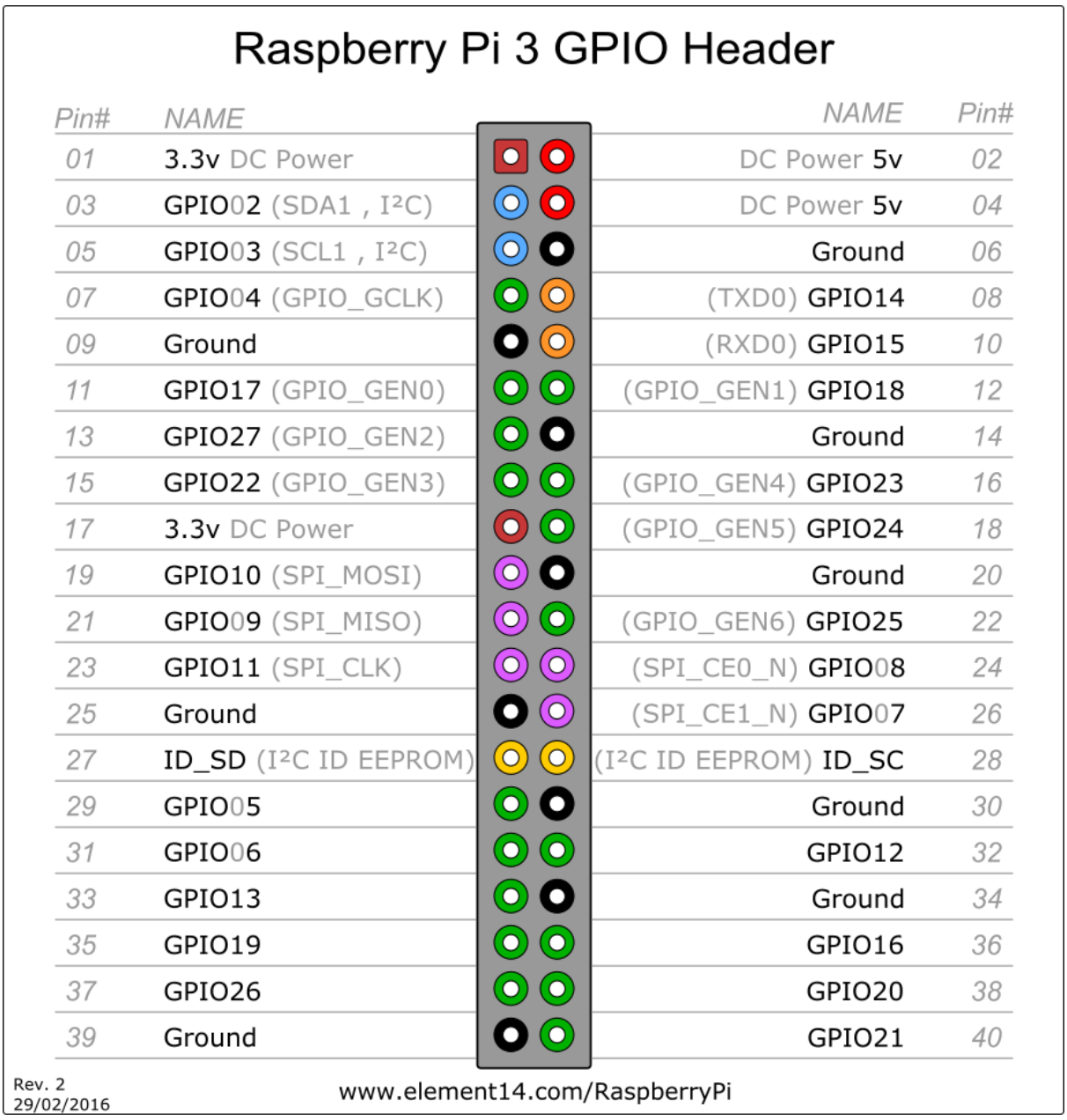
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture	
ASE	Xi'an





5.2.2 APPLICATION NOTES

GPIO pins can be configured as either general-purpose input, general-purpose output or as one of up to 6 special alternate settings, the functions of which are pin-dependant.

There are 3 GPIO banks on BCM2835.

Each of the 3 banks has its own VDD input pin. On Raspberry Pi, all GPIO banks are supplied from 3.3V. **Connection of a GPIO to a voltage higher than 3.3V will likely destroy the GPIO block within the SoC.**

A selection of pins from Bank 0 is available on the P1 header on Raspberry Pi.

GPIO Pads

The GPIO connections on the BCM2835 package are sometimes referred to in the peripherals datasheet as "pads" - a semiconductor design term meaning "chip connection to outside world".

The pads are configurable CMOS push-pull output drivers/input buffers. Register-based control settings are available for

- Internal pull-up / pull-down enable/disable
- Output drive strength
- Input Schmitt-trigger filtering

Power-On States

All GPIOs revert to general-purpose inputs on power-on reset. The default pull states are also applied, which are detailed in the alternate function table in the ARM peripherals datasheet. Most GPIOs have a default pull applied.

Interrupts

Each GPIO pin, when configured as a general-purpose input, can be configured as an interrupt source to the ARM. Several interrupt generation sources are configurable:

- Level-sensitive (high/low)
- Rising/falling edge
- Asynchronous rising/falling edge

Level interrupts maintain the interrupt status until the level has been cleared by system software (e.g. by servicing the attached peripheral generating the interrupt).

The normal rising/falling edge detection has a small amount of synchronisation built into the detection. At the system clock frequency, the pin is sampled with the criteria for generation of an interrupt being a stable transition within a 3-cycle window, i.e. a record of "1 0 0" or "0 1 1". Asynchronous detection bypasses this synchronisation to enable the detection of very narrow events.

Alternative Functions

Almost all the GPIO pins have alternative functions. Peripheral blocks internal to BCM2835 can be selected to appear on one or more of a set of GPIO pins, for example the I2C busses can be configured to at least 3 separate locations. Pad control, such as drive strength or Schmitt filtering, still applies when the pin is configured as an alternate function.

5.2.3 TRADE OFF STUDIES

Visual Human Machine interface (I/F 1):

	LCD Screen	LED's	7-Segment		Weight
Cost	3	10	7		0,5
Reliability	6	9	7		0,3
Ease of use	6	7	6		0,2
	4,5	9,1	6,8		

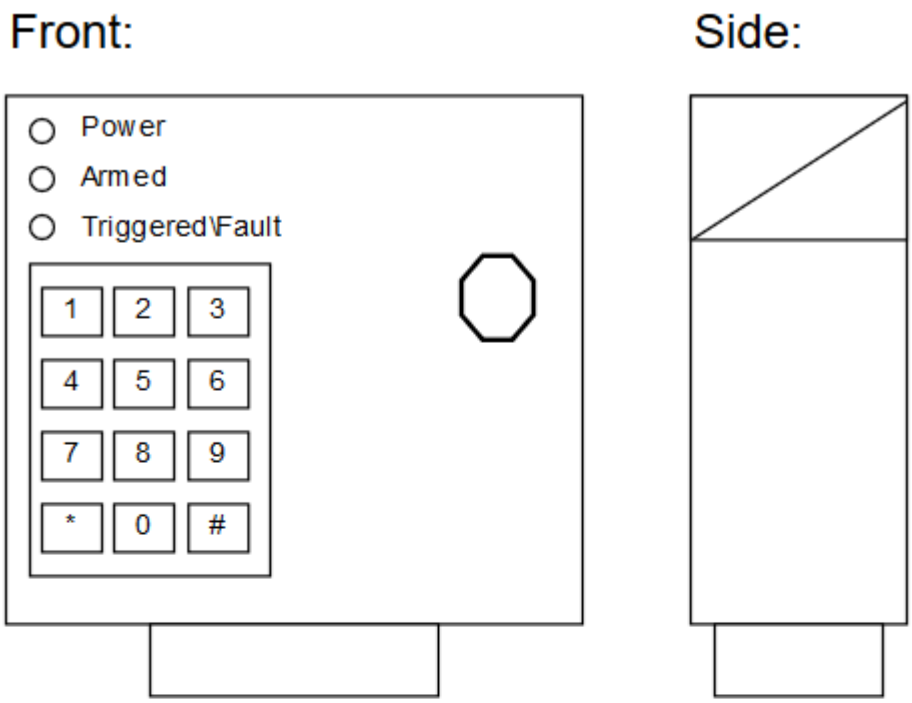
Input Human Machine interface (I/F 1):

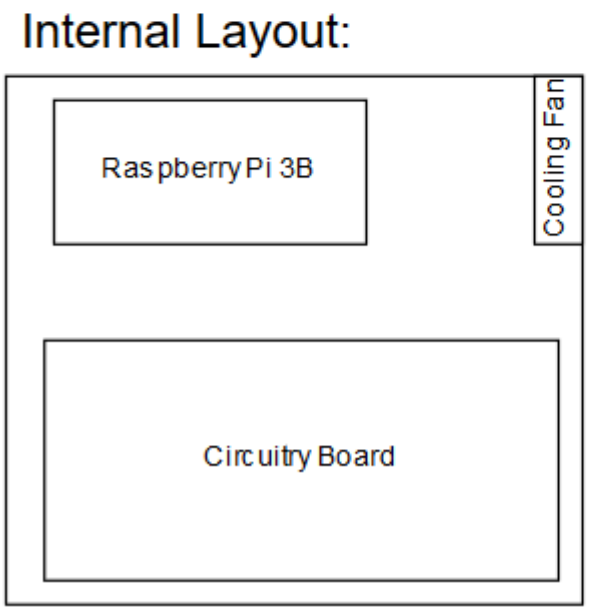
	Remote	Turn key	Keypad		Weight
Cost	1	5	9		0,5
Reliability	2	2	8		0,3
Ease of use	7	9	6		0,2
	2,5	4,9	8,1		

5V Voltage regulator

	LM7805	LM371	usb1002		Weight
Efficiency	3	4	8		0,5
Cost	8	8	7		0,2
Reliability	7	8	9		0,3
	5,2	6	8,1		

5.2.4 DESIGN DRAWINGS:

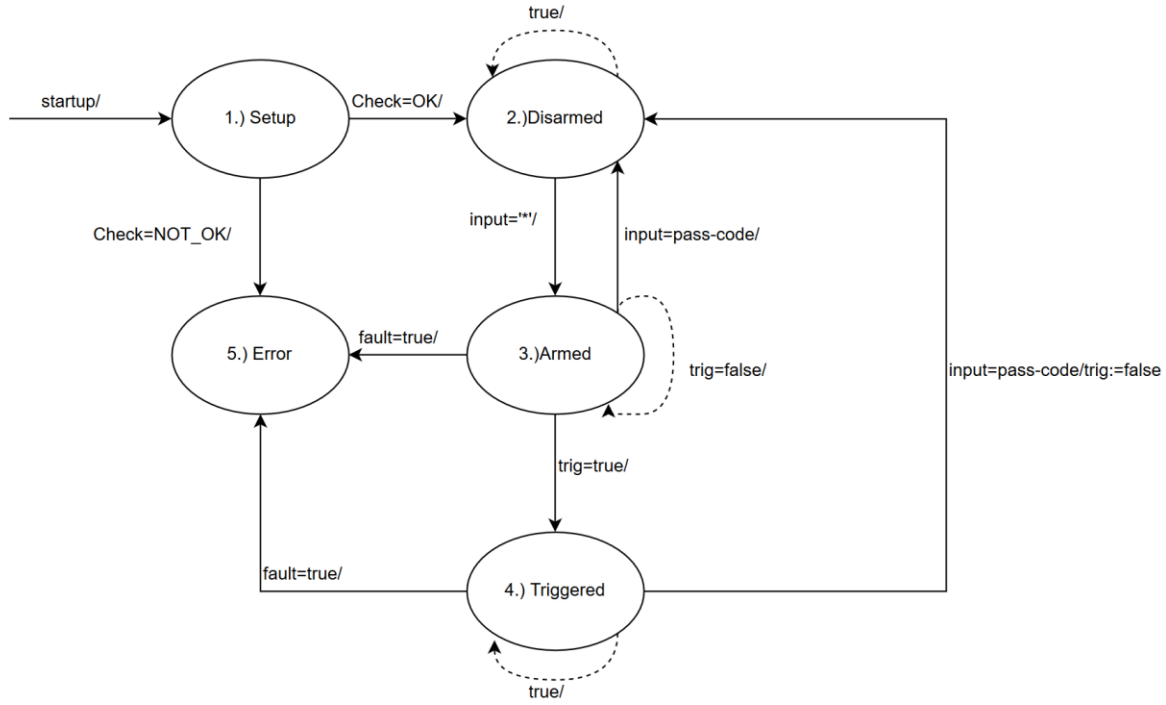


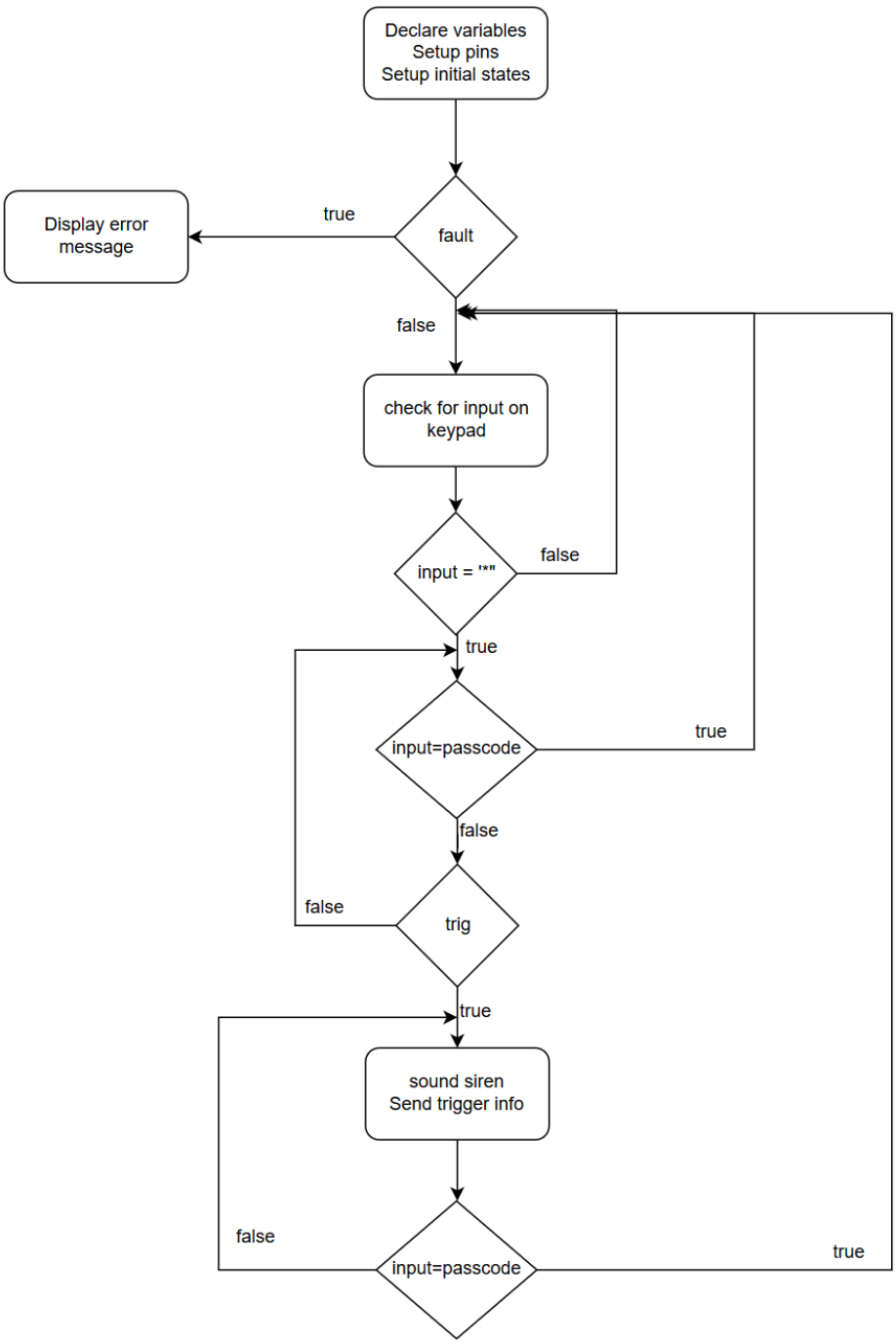


5.2.5 BEHAVIOURAL MODELLING:

Alarm Finite State machine:

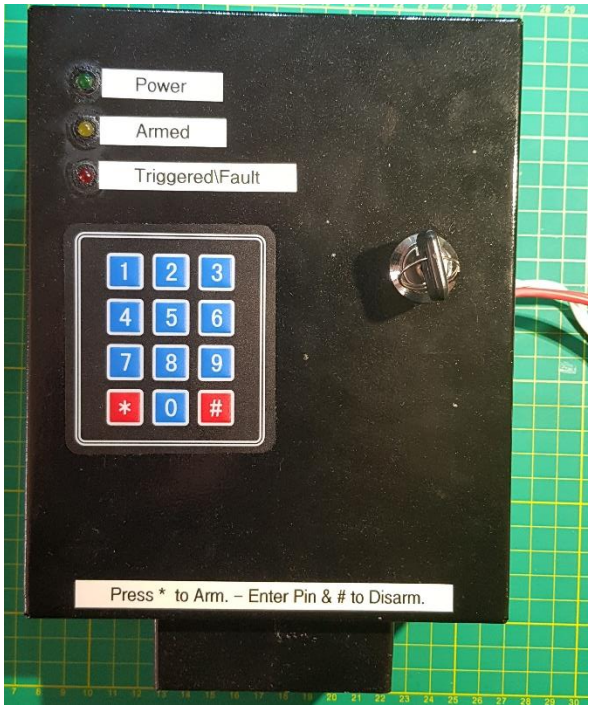
States = {Setup, Idle, Disarmed, Triggered, Error}
Inputs = ({Check, trig, fault} = {absent, present}, {input} = string)
Outputs = ({Siren} = {absent, present}
Initial_State = Setup.

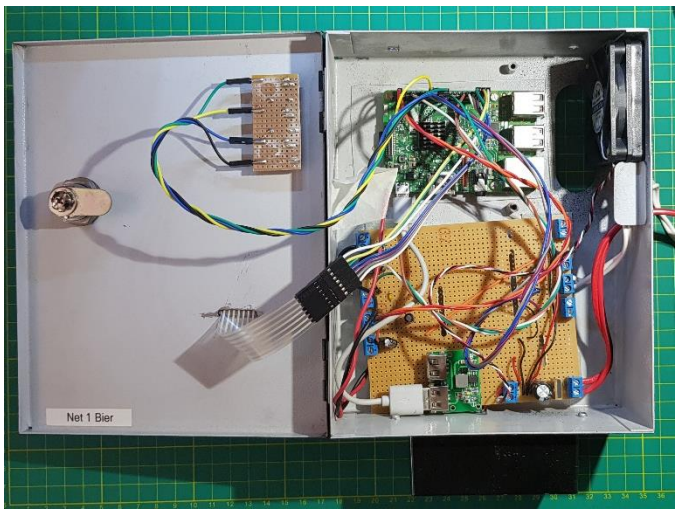



Declare variables
Setup pins
Setup initial states
fault
true
Display error message
false
check for input on keypad
input = '*'
false
true
input=passcode
true
false
trig
false
true
sound siren
Send trigger info
input=passcode
false
true

5.2.6 DESIGN IMPLEMENTATION:

Final construction of Alarm Panel:





5.2.7 SUB-SYSTEM TEST AND EVALUATION:

Action	Expected Results	✓/✗
Program started	Terminal shows program has started and heartbeat signal is shown on the power status LED	✓
Buttons are Pressed on the Keypad	Terminal shows the button pressed	✓
The "*" button is pressed in idle mode to enter armed Mode	The terminal displays that the system is arming, when the system is armed the terminal will display armed, and a heartbeat signal will show on the Armed status LED	✓
Moving the reed switch while in armed mode	The siren starts ringing. The terminal displays a trigger on the Reed sensor. The Triggered status LED starts flashing	✓
Moving the PIR sensor while in armed mode	The siren starts ringing. The terminal displays a trigger on the PIR sensor. The Triggered status LED starts flashing	✓

Action	Expected Results	✓/✗
Power up	The system run through the setup phase and the heartbeat signal is shown on the power status LED. The system is then in the idle state.	
The "*" button is pressed in idle mode to enter armed Mode	A buzzer will start sounding and after 5 second the system will enter the armed state. A heartbeat signal will show on the Armed status LED	
Moving the reed switch (DCS) while in armed mode	The Triggered status LED starts flashing. The user is then given time to disarm the system. After the time has elapsed (20 seconds) and no passcode has been entered or the incorrect passcode has been entered. The siren starts ringing. A UDP message is sent showing a Door switch trigger has occurred	
Disarming the system when the Reed Switch (DCS) has been triggered	The system turns of the armed status LED, and the Triggered status LED. Thereafter the system returns to the idle state	
Triggering the PIR sensor while in armed mode	The siren starts ringing. The Triggered status LED starts flashing. A UDP message is sent showing a PIR sensor trigger has occurred	
Enter the passcode + "#" while in armed state	The system turns of the armed status LED and returns to the idle state	
Enter the passcode + "#" while in triggered state	The system turns of the triggered status LED and returns to the idle state	

5.3 SUB-SYSTEM DESIGN DOCUMENTATION FJ FOURIE:

5.3.1 TECHNOLOGY SURVEY/DATASHEETS

Datasheets in separate PDF

5.3.2 APPLICATION NOTES

Application notes in separate PDF

5.3.3 TRADE OFF STUDIES

Programming Language

	QT	IDLE	Matlab		Weight
Ease of use	8	6	7		0,2
Available information	8	9	10		0,3
Functionality	10	7	8		0,5
	9	7,4	8,9		

Database program bundles

	Oracle Database	XAMPP	MYSQL		Weight
Ease of use	7	10	9		0,2
Available information	6	8	9		0,3
Functionality	8	9	10		0,5
	7,2	8,9	9,5		

5.2.4 DESIGN DRAWINGS:

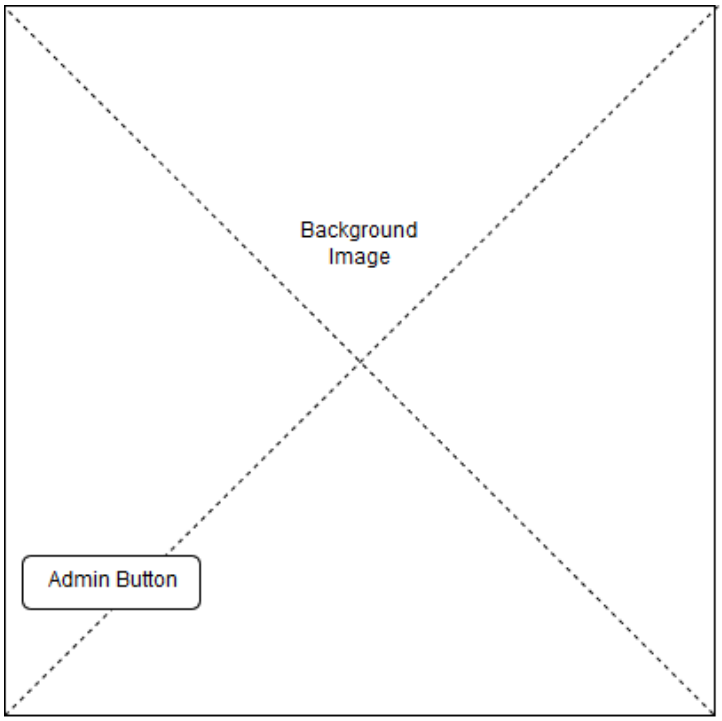


Figure 3: Back end initial screen concept

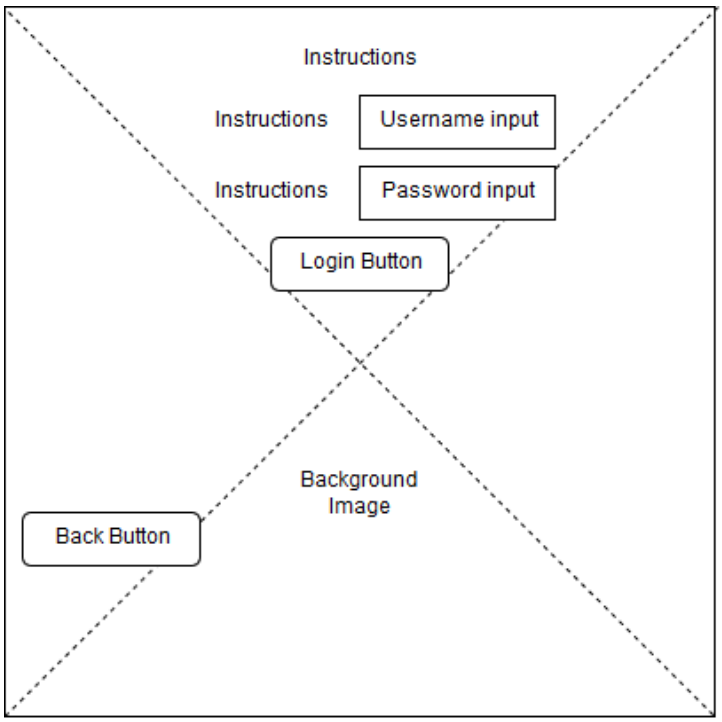


Figure 4: Admin login screen concept

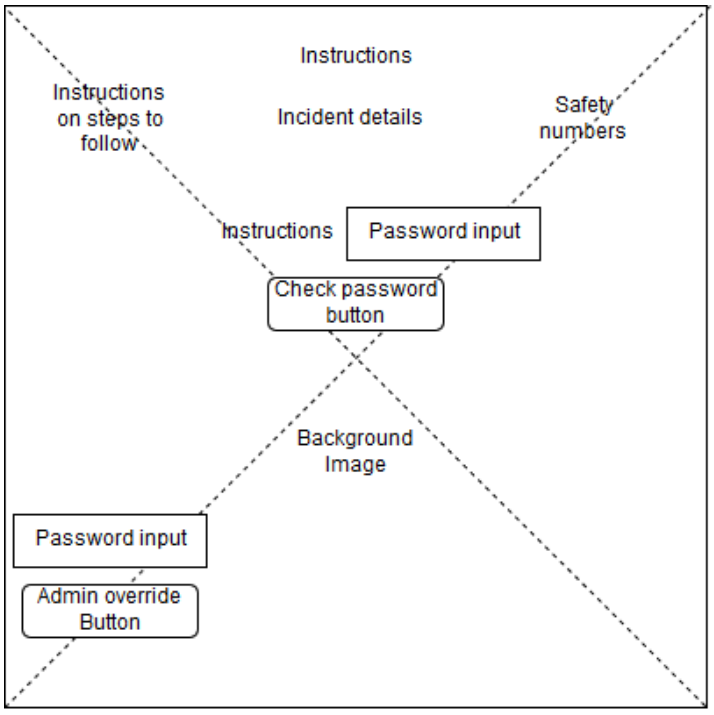
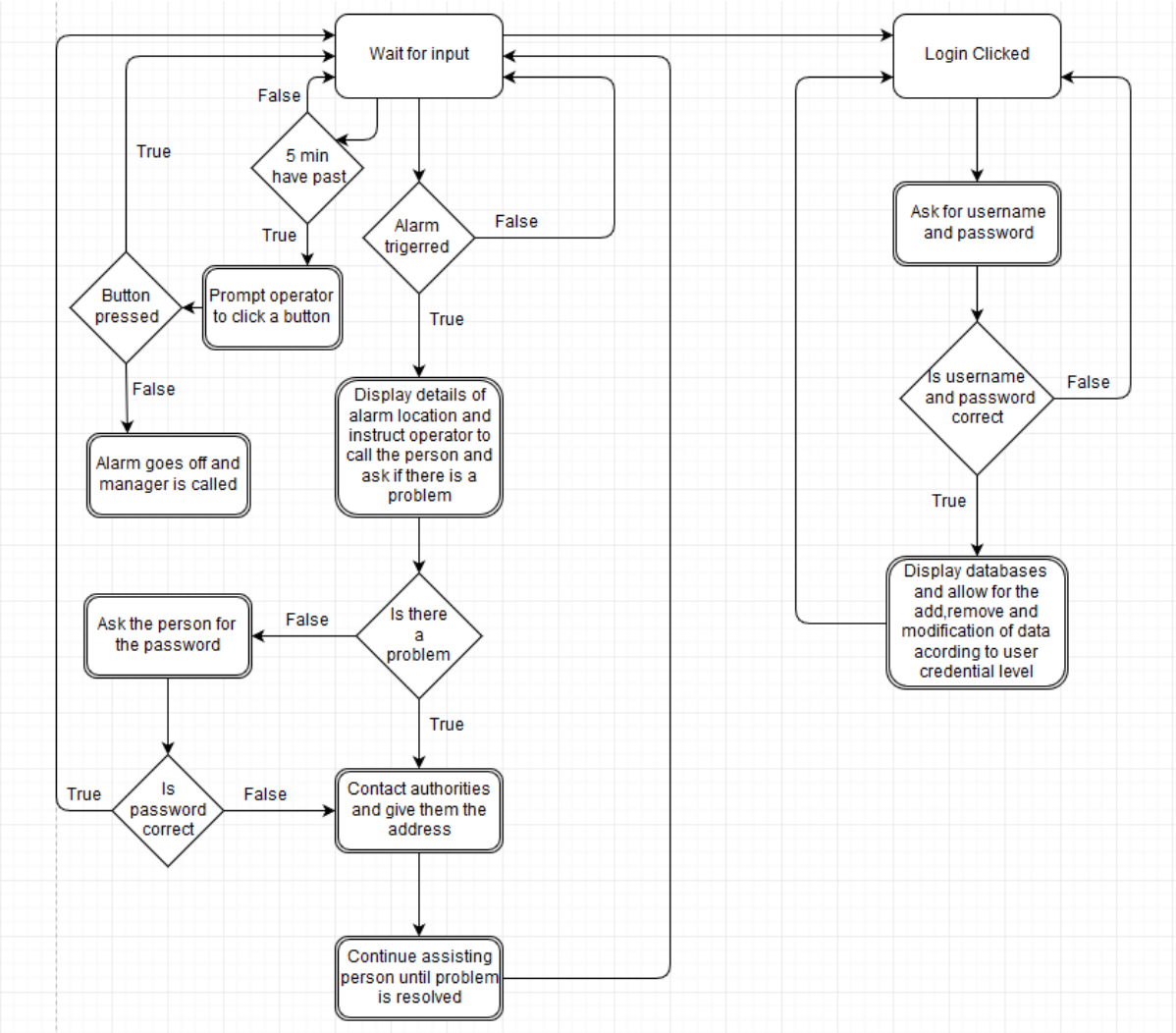


Figure 5: Incident display screen concept

5.2.5 BEHAVIOURAL MODELLING:



5.2.6 DESIGN IMPLEMENTATION:

Screenshots from backend program that has been made from the design drawings above.

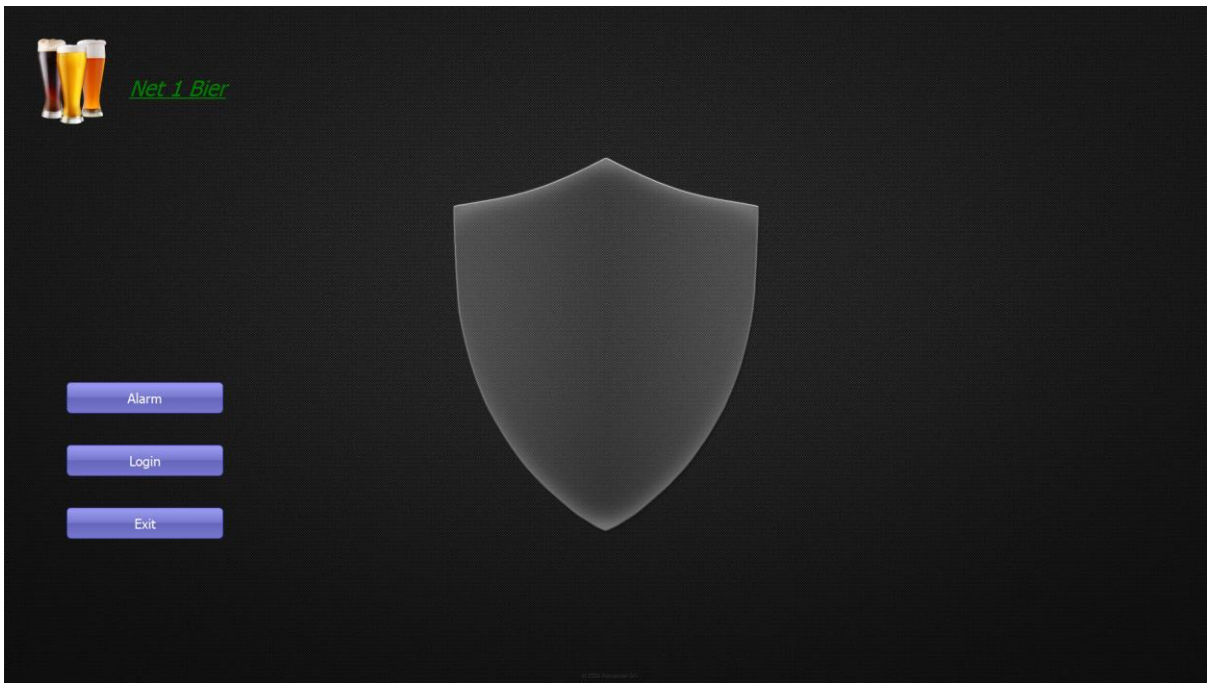


Figure 6: Back end initial screen

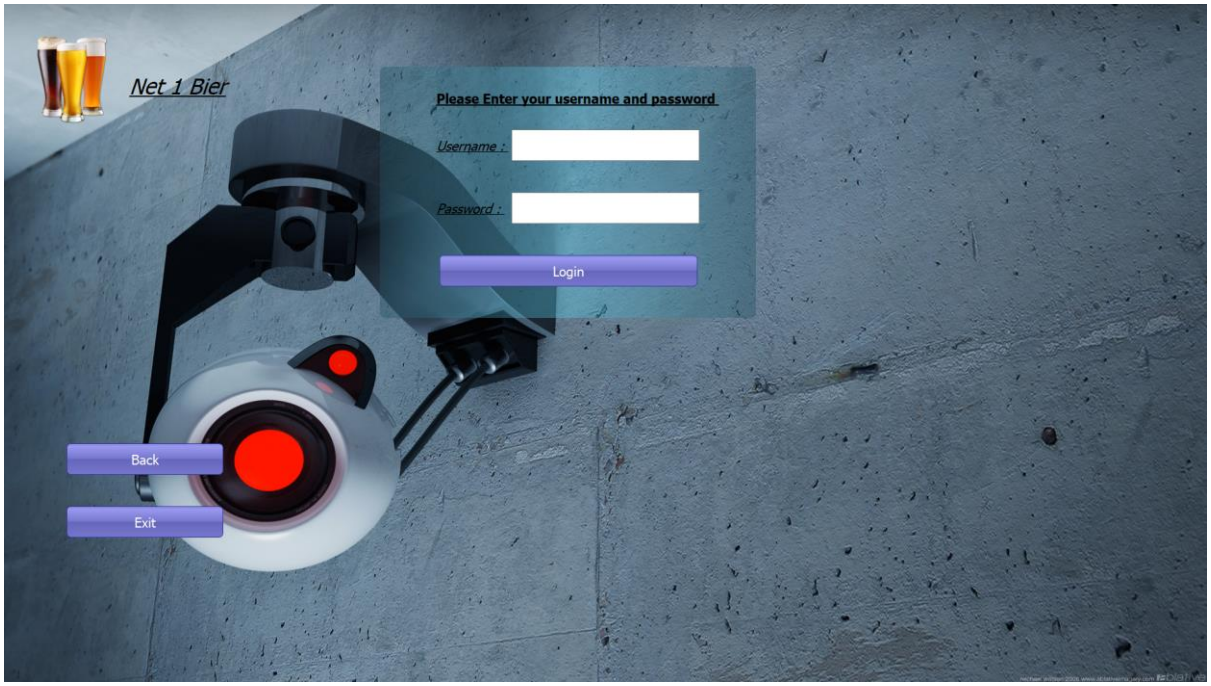


Figure 7: Admin login screen

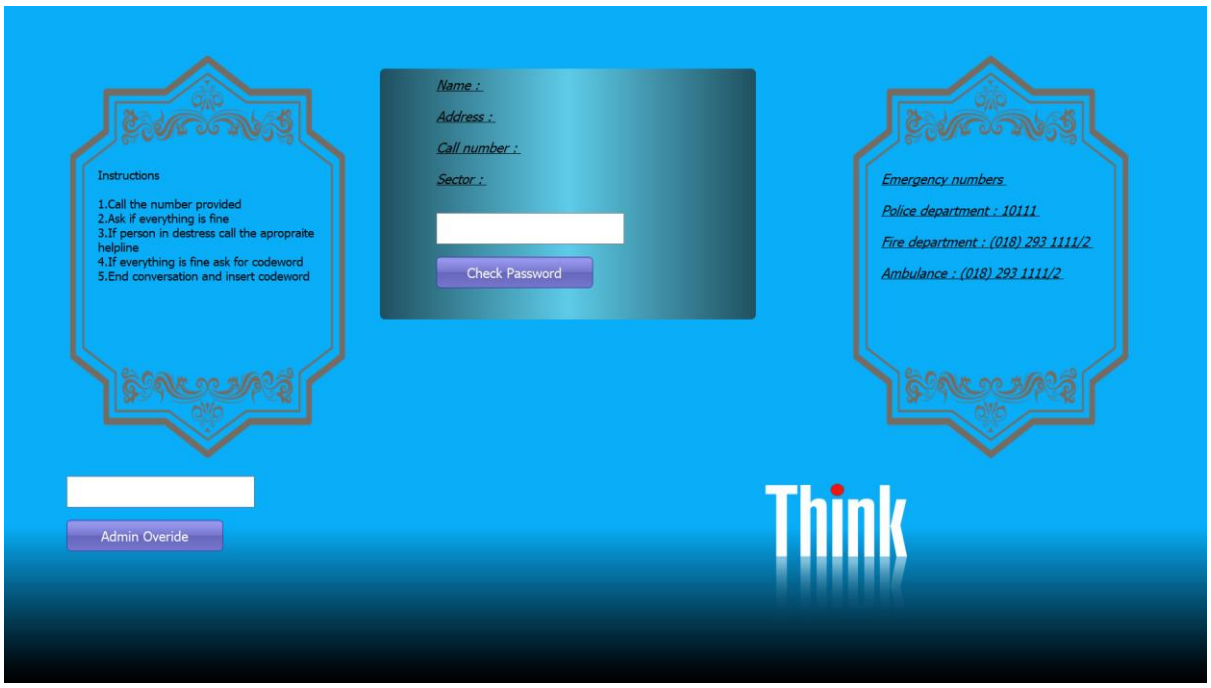


Figure 8: Incident display screen

5.2.7 SUB-SYSTEM TEST AND EVALUATION:

Action	Expected Results	✓/✖
Program started	Displays screen that cannot be exited can only navigate to admin login screen	✓
Login Pressed	When button is pressed navigate to admin login screen	✓
Incident occurs	If an incident occurs immediately open the incident window with no possibilities of closing it or going back	✓
Admin check login button pressed	Checks if admin user credentials are correct before giving him access to the database	✓
Admin Override pressed	Checks if admins override password is correct and if correct close incident	✓
Password check pressed	If the password typed in is the users correct passcode close the incident	✓