Chapter 5

Interference coupling mechanisms

5.1 Source and victim

Situations in which the question of electromagnetic compatibility arises invariably have two complementary aspects. Any such situation must have a source of interference emissions and a victim which is susceptible to this interference. If either of these is not present, there is no EMC problem. If both source and victim are within the same piece of equipment we have an "intrasystem" EMC situation; if they are two different items, such as a computer monitor and a radio receiver, it is said to be an "inter-system" situation. The standards which were discussed in Chapter 2 were all related to controlling inter-system EMC. The same equipment may be a source in one situation and a victim in another.

Knowledge of how the source emissions are coupled to the victim is essential, since a reduction in the coupling factor is often the only way to reduce interference effects, if a product is to continue to meet its performance specification. The two aspects are frequently reciprocal, that is measures taken to improve emissions will also improve the susceptibility, though this is not invariably so. For analysis, they are more easily considered separately.

Systems EMC

Putting source and victim together shows the potential interference routes that exist from one to the other (Figure 5.1). When systems are being built, you need to know the emissions signature and susceptibility of the component equipment, to determine whether problems are likely to be experienced with close coupling. Adherence to published emission and susceptibility standards does not guarantee freedom from systems EMC problems. Standards are written from the point of view of protecting a particular service – in the case of emissions standards, this is radio broadcast and telecommunications – and they have to assume a minimum separation between source and victim.

Most electronic hardware contains elements which are capable of antenna-like behaviour, such as cables, pcb tracks, internal wiring and mechanical structures. These elements can unintentionally transfer energy via electric, magnetic or electromagnetic fields which couple with the circuits. In practical situations, intra-system and external coupling between equipment is modified by the presence of screening and dielectric materials, and by the layout and proximity of interfering and victim equipment and especially their respective cables. Ground or screening planes will enhance an interfering signal by reflection or attenuate it by absorption. Cable-to-cable coupling can be either capacitive or inductive and depends on orientation, length and proximity. Dielectric materials may also reduce the field by absorption, though this is negligible compared with the effects of conductors in most practical situations.

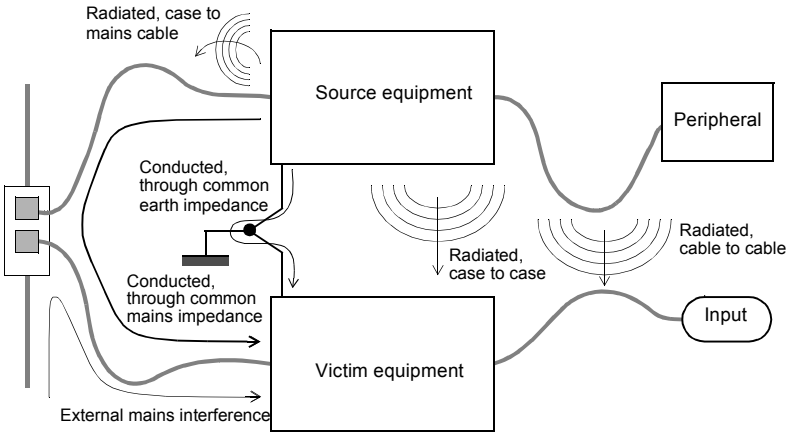


Figure 5.1 Coupling paths

5.1.1 Common impedance coupling

Common impedance coupling routes are those which are due to a circuit impedance which the source shares with the victim. The most obvious common impedances are those in which the impedance is physically present, as with a shared conductor; but the common impedance may also be due to mutual inductive coupling between two current loops, or to mutual capacitive coupling between two voltage nodes. Philosophically speaking, every node and every loop is coupled to all others throughout the universe. Practically, the strength of coupling falls off very rapidly with distance. Figure 5.4 shows the variation of mutual capacitance and inductance of a pair of parallel wires versus their separation, and the field equations in Appendix C (section C.3) give the precise expressions for the field at any point due to a radiating element.

5.1.1.1 Conductive connection

When an interference source (output of system A in Figure 5.2) shares a ground connection with a victim (input of system B) then any current due to A's output flowing through the common impedance section X-X develops a voltage in series with B's input. The common impedance need be no more than a length of wire or pcb track. High frequency or high di/dt components in the output will couple more efficiently because of the inductive nature of the impedance (see appendix C section C.5 for the inductance of various conductor configurations). The voltage developed across an inductor as a result of current flow through it is given by equation (5.1). The output and input may be part of the same system, in which case there is a spurious feedback path through the common impedance which can cause oscillation.

$$V_N = -L \cdot dI_L/dt \qquad (5.1)$$

where L is the self inductance in henries

The solution as shown in Figure 5.2 is to separate the connections so that there is no common current path, and hence no common impedance, between the two circuits. The

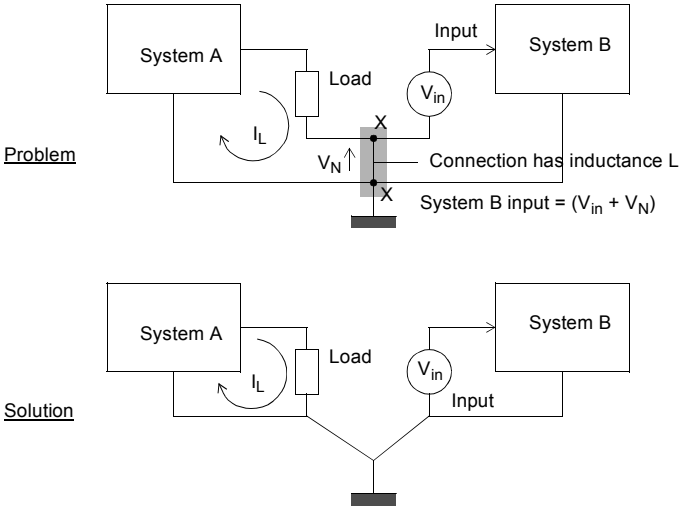


Figure 5.2 Conducted common impedance coupling

only "penalty" for doing this is the need for extra wiring or track to define the separate circuits. This applies to any circuit which may include a common impedance, such as power rail connections. Grounds are the most usual source of common impedance because the ground connection, often not shown on circuit diagrams, is taken for granted.

5.1.1.2 Magnetic induction

Alternating current flowing in a conductor creates a magnetic field which will couple with a nearby conductor and induce a voltage in it (Figure 5.3(a)). The voltage induced in the victim conductor is now given by equation (5.2):

$$V_N = -M \cdot dI_L/dt \qquad (5.2)$$

where M is the mutual inductance in henries

Notice the similarity between this and equation (5.1). M depends on the areas of the source and victim current loops, their orientation and separation distance, and the presence of any magnetic screening. Appendix C (section C.5) gives mutual inductance formulae, but typical values for short lengths of cable loomed together lie in the range 0.1 to 3μH. The equivalent circuit for magnetic coupling is a voltage generator in series with the victim circuit. The coupling is unaffected by whether or not there is a direct connection between the two circuits; the induced voltage would be the same if the circuits were isolated or connected to ground.

5.1.1.3 Electric induction

Changing voltage on one conductor creates an electric field which may couple with a nearby conductor and induce a voltage on it (Figure 5.3(b)). The voltage induced on the victim conductor in this manner is:

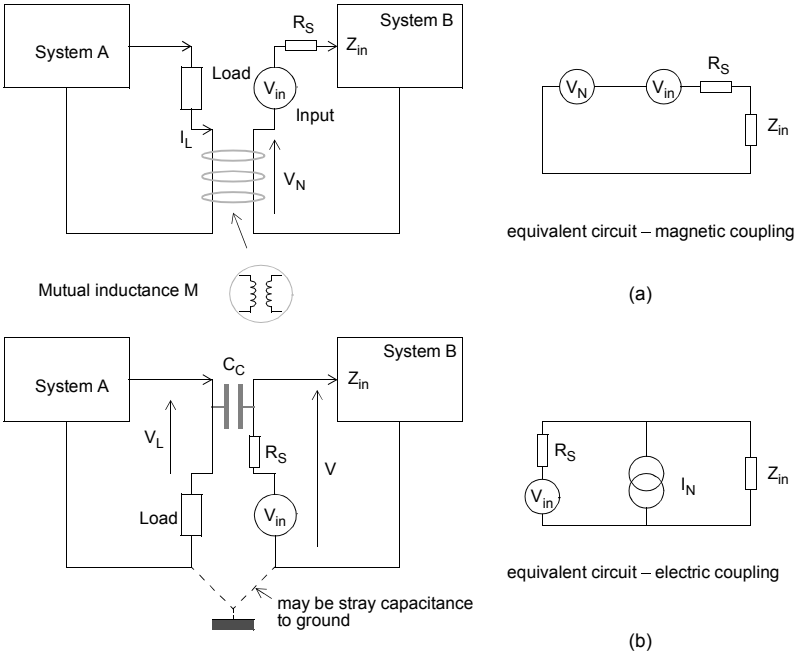


Figure 5.3 Magnetic and electric induction

$$V_N = C_C \cdot dV_L/dt \cdot Z_{in}//R_S, \quad (5.3)$$

where C_C is the coupling capacitance and
$Z_{in}//R_S$ is the impedance to ground of the victim circuit

This assumes that the impedance of the coupling capacitance is much higher than that of the circuit impedances. The noise is injected as if from a current source with a value of $C_C \cdot dV_L/dt$. The value of C_C is a function of the distance between the conductors, their effective areas and the presence of any electric screening material. Typically, two parallel insulated wires 0.1" apart show a coupling capacitance of about 50pF per metre; the primary-to-secondary capacitance of an unscreened medium power mains transformer is 100–1000pF.

Floating circuits

In this case, both circuits need to be referenced to ground for the coupling path to be complete. But if either is floating, this does *not* mean that there is no coupling path: the floating circuit will exhibit a stray capacitance to ground and this is in series with the direct coupling capacitance. Alternatively, there will be stray capacitance direct from the circuit nodes of system A to B even in the absence of any ground node. The noise current will still be injected across R_L but its value will be determined by the series combination of C_C and the other stray capacitance.

5.1.1.4 Effect of input impedance

Note that the difference in equivalent circuits for magnetic and electric coupling means that their behaviour with a varying circuit input impedance is different. Electric field coupling *increases* with an increasing Z_{IN} while magnetic field coupling *decreases* with an increasing Z_{IN}. This property can be useful for diagnostic purposes; if you are able to vary Z_{IN} while observing the coupled voltage, you can deduce which mode of coupling predominates. For the same reason, magnetic coupling is more of a problem for low-impedance circuits while electric coupling applies to high impedance circuits.

5.1.1.5 Spacing

Both mutual capacitance and mutual inductance are affected by the physical separation of source and victim conductors. Figure 5.4 shows the effect of spacing on mutual capacitance of two parallel wires in free space, and on mutual inductance of two conductors over a ground plane (the ground plane provides a return path for the current). Appendix C includes the equations from which this graph derives.

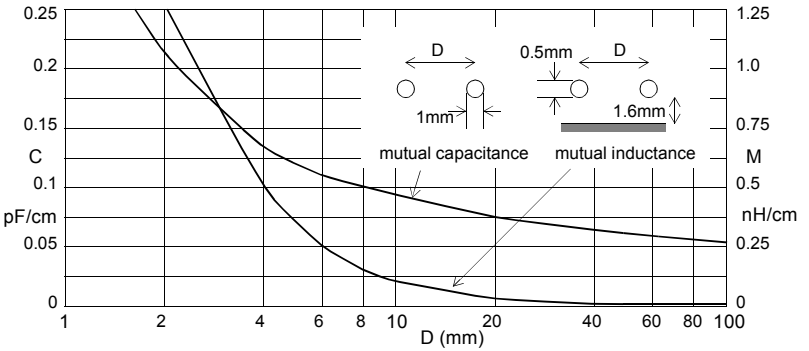


Figure 5.4 Mutual capacitance and inductance versus spacing

5.1.2 Distributed near field coupling

5.1.2.1 Low frequency model

The discussion in 5.1.1.2 and 5.1.1.3 assumes that the coupling mechanism – inductive or capacitive – occurs at a single point in the circuit, or at least can be approximated to such a point. It also assumes that inductive and capacitive coupling can be treated quite separately. In reality, and particularly in cables and on PCB tracks, neither assumption is justifiable. When near-field coupling between circuits is distributed over an appreciable length then the two mechanisms interact and the circuit must be analysed in more detail.

Consider the equivalent circuit of two conductors in a cable as shown in Figure 5.5. For the purposes of the analysis we can assume that the current return paths are both via a remote ground plane. The interference is induced in the second circuit magnetically, in series with the conductor (V_M) and capacitively in parallel with it (I_C). Then the sum total of the interference at each end is given by the superposition of the two sources. But since the magnetically induced voltage is in series with the conductor it appears with

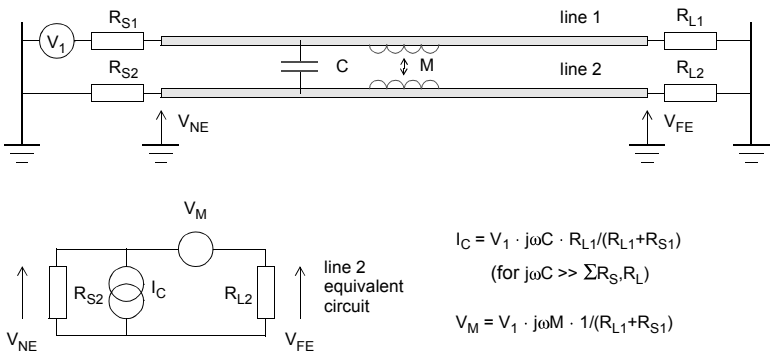


Figure 5.5 Superposition of inductive and capacitive coupling

one sign at one end but the opposite sign at the far end:

$$V_{NE}(C) = I_C \cdot R_{S2}//R_{L2} = V_{FE}(C) \quad \text{(Capacitive coupling)} \tag{5.4}$$

$$V_{NE}(L) = V_M \cdot R_{S2}/(R_{S2}+R_{L2}) = -V_{FE}(L) \quad \text{(Inductive coupling)} \tag{5.5}$$

So

$$V_{NE}(C) = V_{NE}(C) + V_{NE}(L) = (I_C \cdot R_{L2} + V_M) \cdot (R_{S2}/(R_{S2}+R_{L2})) \tag{5.6}$$

$$V_{FE}(C) = V_{FE}(C) + V_{FE}(L) = (I_C \cdot R_{L2} - V_M) \cdot (R_{S2}/(R_{S2}+R_{L2})) \tag{5.7}$$

Since this is a crosstalk phenomenon it gives rise to the terms "near-end crosstalk" (NEXT) and "far-end crosstalk" (FEXT).

5.1.2.2 High frequency model

The above model is only valid at low frequencies, that is if the length of the coupled lines is much less than a wavelength. A more general approach treats the two conductors as transmission lines with lumped L and C parameters, and integrates the coupling contributions along the length of the line. These parameters together with the source and load terminating impedances then determine the coupling time constants. Appendix C section C.5 gives the full coupling equations, and Figure 5.6 shows their effect: at frequencies below the breakpoint determined by the terminated line's time constant, the LF model applies and the coupling increases monotonically with frequency. At higher frequencies the lines become resonant and a maximum coupling is reached, followed by a series of nulls and peaks at integer multiples of a half wavelength.

5.1.3 Mains coupling

Interference can propagate from a source to a victim via the mains distribution network to which both are connected. This is not well characterized at high frequencies, especially since connected electrical loads can present virtually any RF impedance at their point of connection. We have already seen that the RF impedance presented by the

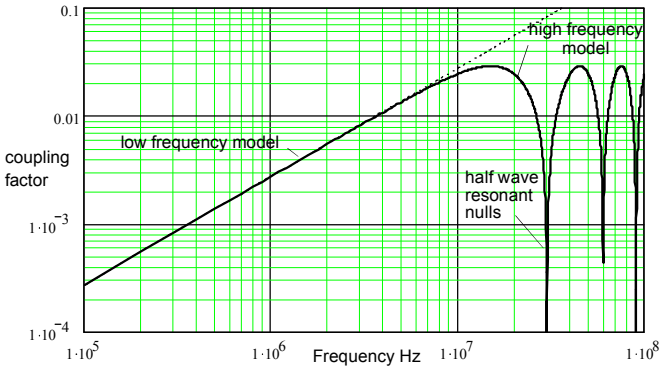


Figure 5.6 High frequency line coupling, line length 5m

mains can on the average be approximated by a network of 50Ω in parallel with 50µH (section 3.1.2.3). For short distances such as between adjacent outlets on the same ring, coupling via the mains connection of two items of equipment can be represented by the equivalent circuit of Figure 5.7.

Over longer distances, power cables are fairly low loss transmission lines of around 150–200Ω characteristic impedance up to about 10MHz. However, in any local power distribution system the disturbances and discontinuities introduced by load connections, cable junctions and distribution components will dominate the RF transmission characteristic. These all tend to increase the attenuation.

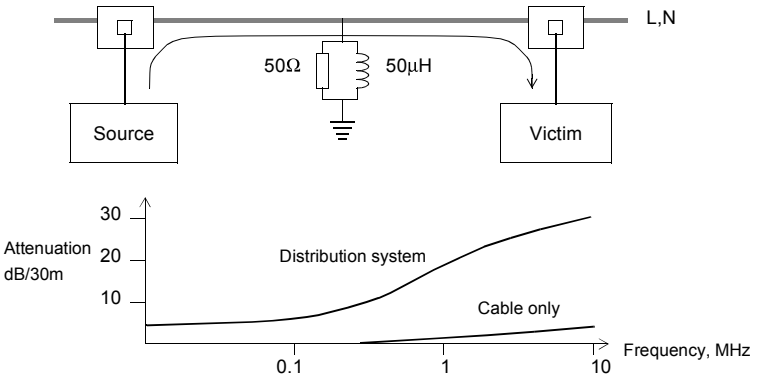


Figure 5.7 Coupling via the mains network

5.1.4 Radiated coupling

To understand how energy is coupled from a source to a victim at a distance with no intervening connecting path, you need to have a basic understanding of electromagnetic

wave propagation. This section will do no more than introduce the necessary concepts. The theory of EM waves has been well covered in many other works [3][7][14].

5.1.4.1 Field generation

An electric field (E field) is generated between two conductors at different potentials. The field is measured in volts per metre and is proportional to the applied voltage divided by the distance between the conductors.

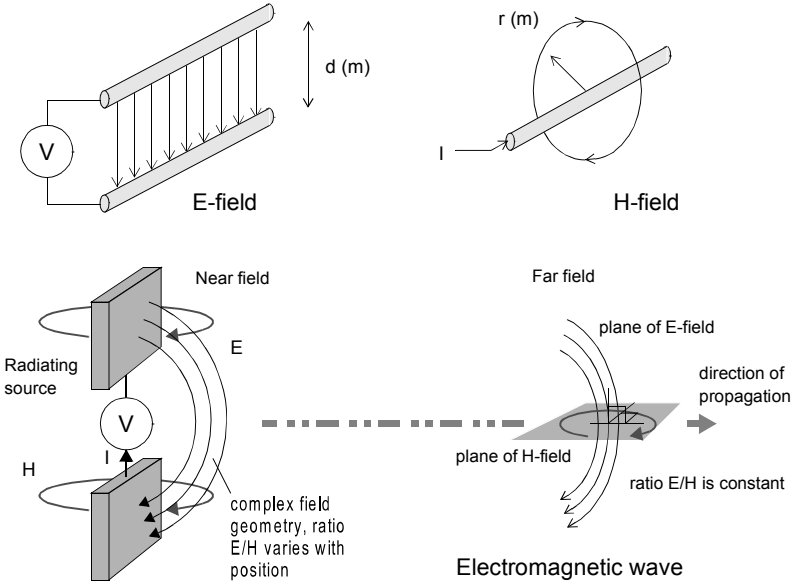


Figure 5.8 Electromagnetic fields

A magnetic field (H field) is generated around a conductor carrying a current, is measured in amps per metre and is proportional to the current divided by the distance from the conductor.

When an alternating voltage generates an alternating current through a network of conductors – a description which applies to any electronic circuit – an electromagnetic (EM) wave is generated which propagates as a combination of E and H fields. The speed of propagation is determined by the medium; in free space it is equal to the speed of light, $3 \cdot 10^8$m/s. Near to the radiating source the geometry and strength of the fields depend on the characteristics of the source. A conductor carrying a significant di/dt will generate mostly a magnetic field; a circuit node carrying a significant dv/dt will generate mostly an electric field. The structure of these fields will be determined by the physical layout of the source conductors, as well as by other conductors, dielectrics and permeable materials nearby. Further away from the source, the complex three-dimensional field structure decays and only the components which are orthogonal to each other and to the direction of propagation remain. Figure 5.8 demonstrates these concepts graphically.

5.1.4.2 Wave impedance

The ratio of the electric to magnetic field strengths (E/H) is called the wave impedance (Figure 5.9). The wave impedance is a key parameter of any given wave as it determines the efficiency of coupling with another conducting structure, and also the effectiveness of any conducting screen which is used to block it. In the far field, that is for $d > \lambda/2\pi$, the wave is known as a plane wave and the E and H fields decay with distance at the same rate. Therefore its impedance is constant, and is equal to the impedance of free space given by equation (5.8):

$$Z_o = \sqrt{(\mu_o/\varepsilon_o)} = 120\pi = 377\Omega \quad (5.8)$$

where μ_o is $4\pi \cdot 10^{-7}$ H/m (the permeability of free space)
and ε_o is $8.85 \cdot 10^{-12}$ F/m (the permittivity of free space)

In the near field, $d < \lambda/2\pi$, the wave impedance is determined by the characteristics of the source. A low current, high voltage radiator (such as a rod) will generate mainly an electric field of high impedance, while a high current, low voltage radiator (such as a loop) will generate mainly a magnetic field of low impedance. If (as a special case) the radiating structure happens to have an impedance around 377Ω, then a plane wave can in fact be generated in the near field, depending on geometry.

The region around $\lambda/2\pi$, or approximately one sixth of a wavelength, is the transition region between near and far fields. This is not a precise criterion, rather it indicates the region within which the field structure changes from complex to simple. Plane waves are always assumed to be in the far field, while if you are looking at the near field it is necessary to consider individual electric or magnetic fields separately. Appendix C presents the formulae (Maxwell's field equations) that underpin this description.

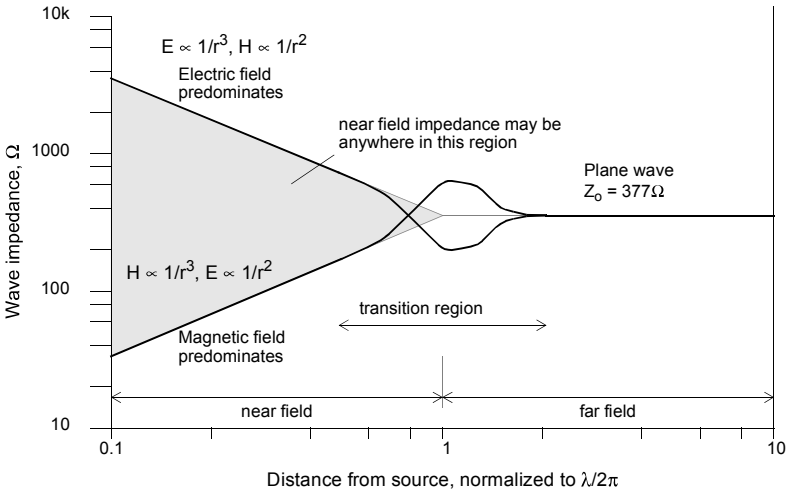


Figure 5.9 The wave impedance

5.1.4.3 The Rayleigh criterion

There is another definition of the transition between near and far fields, determined by the Rayleigh range. This has to do not with the field structure according to Maxwell's equations, but with the nature of the radiation pattern from any physical antenna (or equipment under test) which is too large to be a point source. For the far field assumption to hold, the phase difference between the field components radiated from the extremities of the antenna must be small and therefore the path differences to these extremities must also be small in comparison to a wavelength. This produces a criterion that relates the wavelength and the maximum dimension of the antenna (or EUT) to the distance from it. Using the Rayleigh criterion, the far field is defined as beyond a distance:

$$d > 2D^2/\lambda \quad (5.9)$$

where D is the maximum dimension of the antenna

Table 5.1 shows a comparison of the distances for the two criteria for the near field/far field transition for various frequencies and EUT dimensions. Note how for typical EUT dimensions the Rayleigh range determines the far field condition above 100–200MHz.

Table 5.1 Rayleigh and Maxwell distances for transition to far field

Frequency	Maximum dimension D (m)	Rayleigh $d = 2D^2/\lambda$ (m)	Maxwell $d = \lambda/2\pi$ (m)
10MHz	1	0.067	4.77
	3	0.6	
30MHz	1	0.2	1.59
	3	0.6	
100MHz	0.3	0.06	0.477
	1	0.67	
	3	6.0	
300MHz	0.3	0.18	0.159
	1	2.0	
1GHz	0.3	0.6	0.0477
	1	6.67	

5.1.5 Coupling modes

The concepts of differential mode, common mode and antenna mode radiated field coupling are fundamental to an understanding of EMC and will crop up in a variety of guises throughout this book. They apply to coupling of both emissions and incoming interference.

5.1.5.1 Differential mode

Consider two items of equipment interconnected by a cable (Figure 5.10). The cable carries signal currents in ***differential*** mode (go and return) down the two wires in close

proximity. A radiated field can couple to this system and induce differential mode interference between the two wires; similarly, the differential current will induce a radiated field of its own. The ground reference plane (which may be external to the equipment or may be formed by its supporting structure) plays no part in the coupling.

5.1.5.2 Common mode

The cable also carries currents in ***common*** mode, that is, all flowing in the same direction on each wire. These currents very often *have nothing at all to do with the signal currents*. They may be induced by an external field coupling to the loop formed by the cable, the ground plane and the various impedances connecting the equipment to ground, and may then cause internal differential currents to which the equipment is susceptible. Alternatively, they may be generated by internal noise voltages between the ground reference point and the cable connection, and be responsible for radiated emissions. The existence of RF common mode currents means that *no* cable, whatever signal it may be intended to carry – even a single wire – can be viewed as safe from the EMC point of view.

Notice that the stray capacitances and inductances associated with the wiring and enclosure of each unit are an integral part of the common mode coupling circuit, and play a large part in determining the amplitude and spectral distribution of the common mode currents. These stray impedances are incidental rather than designed in to the equipment. They don't appear on any circuit diagram, and are much harder to control or predict than those parameters such as cable spacing and filtering which determine differential mode coupling.

5.1.5.3 Antenna mode

Antenna mode currents are carried in the same direction by the cable and the ground reference plane. They should not arise as a result of internally-generated noise, but they will flow when the whole system, ground plane included, is exposed to an external field. An example would be when an aircraft flies through the beam of a radar transmission; the aircraft structure, which serves as the ground plane for its internal equipment, carries the same currents as the internal wiring. Antenna mode currents only become a problem for the radiated field susceptibility of self-contained systems when they are converted to differential or common mode by varying impedances in the different current paths.

5.1.5.4 Conversion between differential and common mode

Although it was said above that common mode currents may be unrelated to the intended signal currents, there may also be a component of common mode current which *is* due to the signal current. Conversion occurs when the two signal conductors present differing impedances to their environment, represented by the external ground. These impedances are dominated at RF by stray capacitance and inductance related to physical layout, and are only under the circuit designer's control if that person is also responsible for physical layout.

In Figure 5.11 the differential mode current I_{DM} produces the desired signal voltage across load R_L. The common mode current I_{CM} does not flow through R_L directly but through impedances Z_A, Z_B and back via the external ground. Z_A, Z_B are not circuit components but distributed stray impedances, typically but not always capacitive, and are determined by such factors as surface area of PCB tracks and components and their proximity to chassis metalwork and other parts of the equipment. If $Z_A = Z_B$ then no

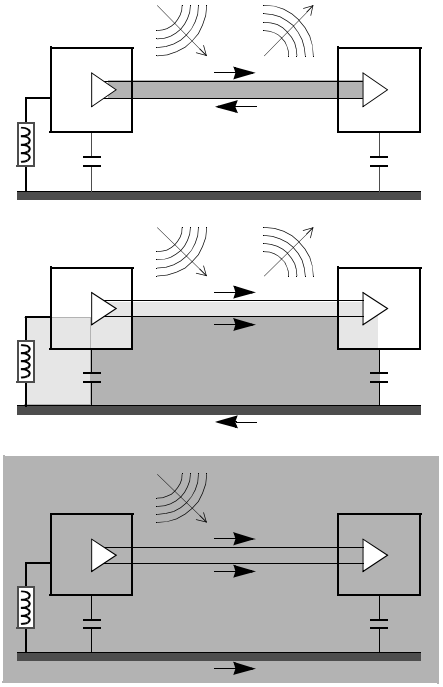


Figure 5.10 Radiated coupling modes

voltage is developed across R_L by the common mode currents I_{CM}. But any inequality results in such a voltage, proportional to the differences in impedance:

$$V_{load(CM)} = I_{CM} \cdot Z_A - I_{CM} \cdot Z_B = I_{CM} \cdot (Z_A - Z_B) \quad (5.10)$$

For this reason, circuits which carry high-frequency interfering signals (such as wideband data or video) or which could be susceptible to RF are best designed in such a way that the stray impedances of each conductor are balanced as nearly as possible. Alternatively, a common-mode choke (section 8.2.4.1) is used which swamps the imbalance of the strays and reduces the magnitude of I_{CM}.

The increasing popularity of wideband data transmission via unscreened cables within and between buildings has sharpened the problem of interference radiated from these cables. As well as the balance of the circuit at either end of the cable, the balance of the cable itself, as it passes near to other conducting structures in its environment, is an important factor. This is largely determined by the quality of the cable construction, and has resulted in a cable parameter known as "longitudinal conversion loss" (LCL) being defined. LCL is treated in more detail in section 8.1.7.1.

5.1.5.5 Generalization

The principles demonstrated in the circuits of Figure 5.10 and Figure 5.11 are not limited to currents propagating down cables between modules. The circuits can be

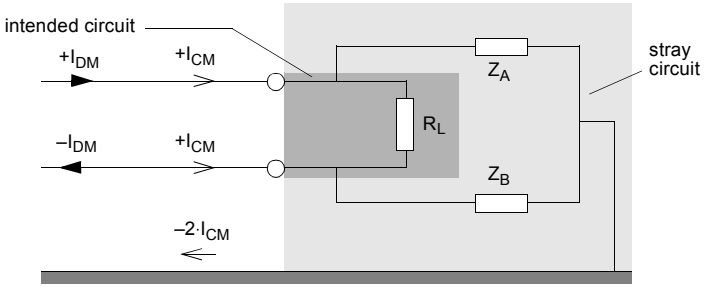


Figure 5.11 Differential to common mode conversion

extended to include currents on interconnections between PCBs in an individual module, or even on tracks between parts of a PCB mounted on a chassis. Many EMC problems of products can be traced to the common mode currents flowing *within* them as well as outside them.

5.2 Emissions

When designing a product to a specification without knowledge of the system or environment in which it will be installed, you will normally separate the two aspects of emissions and susceptibility, and design to meet minimum requirements for each. Limits are laid down in various standards but individual customers or market sectors may have more specific requirements. In those standards which derive from CISPR (see Chapter 2), emissions are subdivided into radiated emissions from the system as a whole, and conducted emissions present on the interface and power cables. Conventionally, the breakpoint between radiated (high frequency) and conducted (low frequency) is set at 30MHz, primarily for convenience of measurement. Radiated emissions can themselves be separated into emissions that derive from differential currents on internal pcbs or other wiring, and emissions from common-mode currents on PCBs or conducting structures, or that find their way onto external cables that are connected to the equipment.

5.2.1 Radiated emissions

5.2.1.1 Radiation from the pcb

In most equipment, the primary sources are currents flowing in circuits (clocks, video and data drivers, and other oscillators) that are mounted on printed circuit boards. Some of the energy is radiated directly from the pcb, which can be modelled as a small loop antenna carrying the interference current (Figure 5.12). A small loop is one whose dimensions are smaller than a quarter wavelength ($\lambda/4$) at the frequency of interest (e.g. 1 metre at 75MHz). Most pcb loops count as "small" at emission frequencies of up to a few hundred MHz. When the dimensions approach $\lambda/4$ the currents at different points on the loop appear out of phase at a distance, so that the effect is to reduce the field strength at any given point. The maximum electric field strength from such a loop over

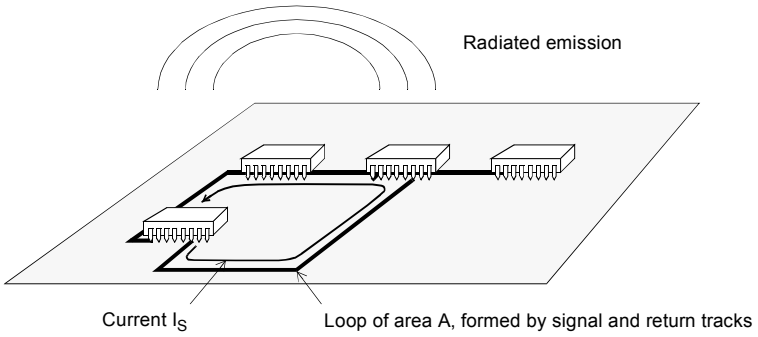


Figure 5.12 PCB radiated emissions

a ground plane at 10 metres distance is proportional to the square of the frequency:

$$E = 263 \cdot 10^{-12} (f^2 \cdot A \cdot I_S) \text{ volts per metre [12]} \quad (5.11)$$

where A is the loop area in cm^2,
f (MHz) is the frequency of I_S the source current in mA.

In free space, the field falls off proportionally to distance from the source. The figure of 10m is used as this is the standard measurement distance for the European radiated emissions standards. A factor of 2 times is allowed for worst case field reinforcement due to reflection from the ground plane, which is also a required feature of testing to standards.

The loop whose area must be known is the overall path taken by the signal current and its return. Equation (5.11) assumes that I_S is at a single frequency. For square waves with many harmonics, the Fourier spectrum must be used for I_S. These points are taken up again in section 7.1.2.

Assessing pcb design

You can use equation (5.11) to indicate roughly whether a given pcb design will need extra screening. For example if A = $10cm^2$, I_S = 20mA, f = 50MHz then the field strength E is 42dBμV/m, which is 12dB over the European Class B limit. Thus if the frequency and operating current are fixed, and the loop area cannot be reduced, screening will be necessary.

But the converse is not true. Differential mode radiation from small loops on pcbs is by no means the only contributor to radiated emissions; common mode currents flowing on the pcb and on attached cables can contribute much more. Paul [106] goes so far as to say:

> "predictions of radiated emissions based solely on differential-mode currents will generally bear no resemblance to measured levels of radiated emissions. Therefore, basing system EMC design on differential-mode currents and the associated prediction models that use them exclusively while neglecting to consider the (usually much larger) emissions due to common-mode currents can lead to a strong 'false sense of security'".

Common mode currents on the pcb itself are not at all easy to predict, in contrast with the differential mode currents which are governed by Kirchoff's current law. The return path for common mode currents is via stray capacitance (displacement current) to other

nearby objects and therefore a full prediction would have to take the detailed mechanical structure of the pcb and its case, as well as its proximity to ground and to other equipment, into account. Except for trivial cases this is to all intents and purposes impossible. It is for this reason more than any other that EMC design has earned itself the distinction of being a "black art".

5.2.1.2 Radiation from cables

Fortunately (from some viewpoints) radiated coupling at VHF tends to be dominated by cable emissions, rather than by direct radiation from the pcb. This is for the simple reason that typical cables resonate in the 30–100MHz region and their radiating efficiency is higher than pcb structures at these frequencies. The interference current is generated in common mode from ground noise developed across the PCB or elsewhere in the equipment and may flow along the conductors, or along the shield of a shielded cable. A model for this effect has been well described in [33]; simplistically, the capacitances between the noise-generating track and external ground, and between the PCB's ground reference and external ground, form a network for return of currents that are injected into cables connected to the PCB. A more detailed model can be generated which includes the inductance of the tracks and plane. Reference [33] describes how it is possible from this model to derive coupling parameters for a PCB which can then be applied to the large-scale system (enclosure and cables) of which the PCB is a part, to predict the common mode radiated emissions.

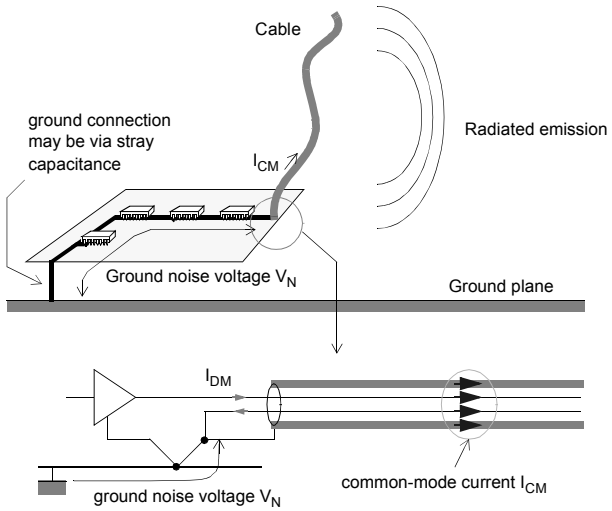


Figure 5.13 Cable radiated emissions

The model for cable radiation at lower frequencies (Figure 5.13) is a short ($L < \lambda/4$) monopole antenna over a ground plane. (When the cable length is resonant the model becomes invalid; see section C.3 in appendix C for an equation describing emissions from resonant cables.) The maximum field strength allowing +6dB for ground plane reflections at 10m due to this radiation is directly proportional to frequency:

$$E = 1.26 \cdot 10^{-4} \cdot (f \cdot L \cdot I_{CM}) \text{ volts per metre [12]} \quad (5.12)$$

where L is the cable length in metres and
I_{CM} is the common-mode current at f MHz in mA flowing in the cable.

For a 1m cable, I_{CM} must be less than 20μA for a 10m-distance field strength at 50MHz of 42dBμV/m – i.e., a thousand times less than the equivalent differential mode current! To meet the 30dBμV/m limit, the current needs to be 12dB or four times less, i.e. 5μA, under these conditions. And indeed, this value of 5μA when measured as a common-mode cable current is regarded as a good indicator of likely compliance with radiated emissions limits [5] – any more than 5μA and the product has a good chance of failing the compliance test. I_{CM} can be easily measured in the development lab using a current probe or absorbing clamp (see section 3.1.2.5) and so this forms a useful diagnostic or pre-compliance check on the prospects for a given item.

Common mode cable noise

At the risk of repetition, it is vital to appreciate the difference between common mode and differential mode cable currents. Differential mode current, I_{DM} in Figure 5.13, is the current which flows in one direction along one cable conductor and in the reverse direction along another. It is normally equal to the signal or power current, and is not present on the shield. It contributes little to the net radiation as long as the total loop area formed by the two conductors is small; the two currents tend to cancel each other. Common mode current I_{CM} flows equally in the same direction along all conductors in the cable, potentially including the shield, and is only related to the (differential) signal currents insofar as these are converted to common mode by unbalanced external impedances, and may be quite *un*related to them. For instance, an RS-232 interface cable will only be carrying data at a rate of perhaps 19.2kbaud, but can also carry common mode noise from the circuit ground which is polluted by a processor clock and its harmonics at hundreds of MHz. It returns via the associated ground network and therefore the radiating loop area is large and uncontrolled. As a result, even a small I_{CM} can result in large emitted signals.

5.2.2 Conducted emissions

Interference sources within the equipment circuit or its power supply are coupled onto the power cable to the equipment. Interference may also be coupled either inductively or capacitively from another cable onto the power cable. Until recently, attention has focussed on the power cable as the prime source of conducted emissions since CISPR-based standards have only specified measurements on this cable. However, signal and control cables can and do also act as coupling paths and the latest versions of the standards apply measurements to these cables as well.

The resulting interference may appear as differential mode (between live and neutral, or between signal wires) or as common mode (between live/neutral/signal and earth) or as a mixture of both. For signal and control lines, only common mode currents are of interest. For the mains port, the voltages between each phase/neutral and earth at the far end of the mains cable are measured. Differential mode emissions are normally associated with low-frequency switching noise from the power supply, while common-mode emissions can be due to the higher frequency switching components, internal circuit sources or inter-cable coupling.

5.2.2.1 Coupling paths

Figure 5.14, showing a typical product with a switched mode supply, gives an idea of

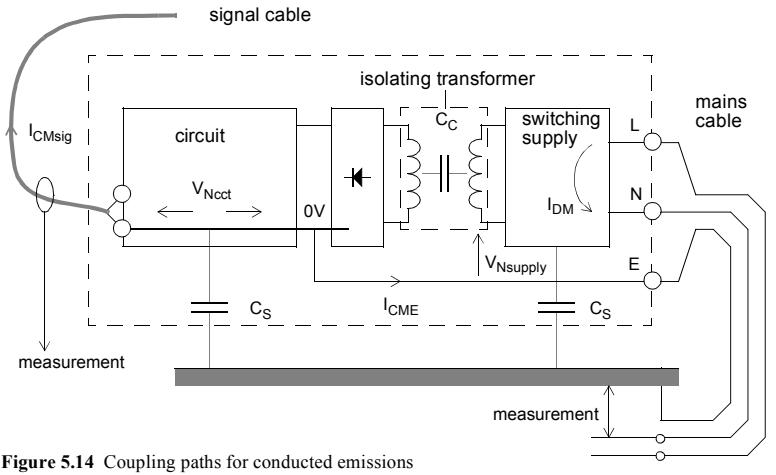


Figure 5.14 Coupling paths for conducted emissions

the various paths these emissions can take. (Section 7.1.5 looks at SMPS emissions in more detail.) Differential mode current I_{DM} generated at the input of the switching supply is measured as an interference voltage across the load impedance of each line with respect to earth at the measurement point. Higher frequency switching noise components $V_{Nsupply}$ are coupled through C_C, the coupling capacitance between primary and secondary of the isolating transformer, to appear between L/N and E on the mains cable, and C_S to appear with respect to the ground plane. Circuit ground noise V_{Ncct} (digital noise and clock harmonics) is referenced to ground by C_S and coupled out via signal cables as I_{CMsig} or via the safety earth as I_{CME}.

The problem in a real situation is that all these mechanisms are operating simultaneously, and the stray capacitances C_S are widely distributed and unpredictable, depending heavily on proximity to other objects if the case is unscreened. A partially-screened enclosure may actually worsen the coupling because of its higher capacitance to the environment.

5.2.2.2 Simplified equivalent circuits

The basic equivalent circuit for conducted emissions testing on the mains port is shown in Figure 5.15(a). The mains connection is represented by the AMN/LISN giving a defined RF impedance between live and earth, and between neutral and earth. The EUT contains both differential and common mode sources, generalized here as appearing in one case between live and neutral, and in the other case between both live and neutral with respect to earth. If the apparatus is Safety Class II there is no earth wire, but common mode signals can still return via the stray capacitance to the ground plane.

Differential mode sources appear between live and neutral connections without reference to the earth connection (Figure 5.15(b)). In circuits with switch-mode power supplies or other power switching circuits the RF emissions are dominated by interference developed across the DC link to the switching devices. Although there will normally be a reservoir capacitor, the high di/dt through this capacitor will generate voltages at the harmonics of the switching frequency across its equivalent series impedance. Diode noise, if it is significant, will also appear in differential mode.

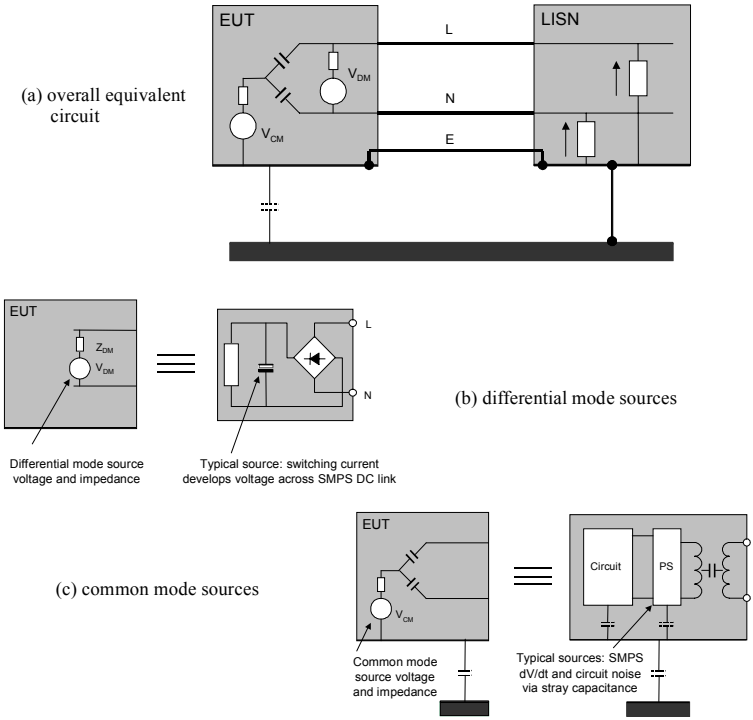


Figure 5.15 Equivalent circuits for conducted emissions tests

Common mode sources (Figure 5.15(c)) are more complex. The common mode voltage appears between both live and neutral with respect to earth. Since the mains input is normally isolated from earth, it is usual for common mode coupling to be capacitive.

The coupling is dominated by the interwinding capacitance of the isolating transformer and the stray capacitances of noise sources, both in the power supply (e.g. from heatsinks) and the operating circuit. These capacitances are referred to earth, either directly or via the enclosure if this is conductive. A well-shielded enclosure will minimise "leakage" of this capacitive coupling and hence reduced conducted emissions. Other impedances may appear in the coupling path: for instance the leakage inductance of the isolating transformer is in series with its interwinding capacitance and may give a series resonant peak in the MHz range.

5.3 Immunity

Electronic equipment will be susceptible to environmental electromagnetic fields and/or to disturbances coupled into its ports via connected cables. An electrostatic discharge may be coupled in via the cables or the equipment case, or a nearby discharge can create a local field which couples directly with the equipment. The potential threats are:

- radiated RF fields
- conducted transients
- electrostatic discharge (ESD)
- magnetic fields
- supply voltage disturbances

Quite apart from legal requirements, equipment that is designed to be immune to these effects – especially ESD and transients – will save its manufacturer considerable expense through improved reliability and reduced field returns. Although many aspects of emission control are also relevant for immunity, in some cases the shielding and circuit suppression measures that are required for protection against ESD or RF interference may be more than you need for simple compliance with emission standards.

5.3.1 Radiated field

An external field can couple either directly with the internal circuitry and wiring in differential mode or with the cables to induce a common mode current (Figure 5.16). Coupling with internal wiring and pcb tracks is most efficient at frequencies above a

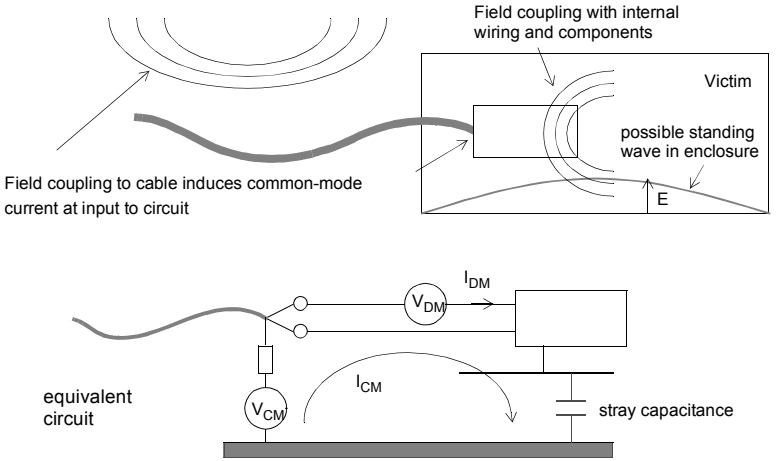


Figure 5.16 Radiated field coupling

few hundred MHz, since wiring lengths of a few inches approach resonance at these frequencies.

RF voltages or currents in analogue circuits can induce nonlinearity, overload or DC bias and in digital circuits can corrupt data transfer [111]. Modulated fields can have greater effect than unmodulated ones. Likely sources of radiated fields are walkie-talkies, cellphones, high-power broadcast transmitters and radars. Field strengths between 1 and 10V/m from 20MHz to 1GHz are typical, and higher field strengths can occur in environments close to such sources.

Reciprocity

Because the coupling mechanisms for immunity are essentially the same as those for emissions, the principle of *reciprocity* has evolved. In essence it states that

> improvements to coupling which reduce emissions over a particular frequency range will also improve immunity over that frequency range

or, on the other hand,

> frequencies at which emissions are particularly troublesome will also be those at which immunity problems occur.

This concept relies on the fact that coupling mechanisms usually show resonant behaviour which maximizes the coupling at certain frequencies. The reciprocity principle should not be accorded too much weight: actual EMC performance depends on the operation of both source and victim circuits as well as on the coupling between them, and these are rarely either reciprocal or linear. Understanding the principle can help in dealing with many coupling-related problems, though.

5.3.1.1 Cable resonance

Cables are most efficient at coupling RF energy into equipment at the lower end of the vhf spectrum (30–100MHz). The external field induces a common mode current on the cable shield or on all the cable conductors together, if it is unshielded. The common mode cable current effects tend to dominate the direct field interactions with the equipment as long as the equipment's dimensions are small compared with half the wavelength of the interfering signal.

A cable connected to a grounded victim equipment can be modelled as a single conductor over a ground plane, which appears as a transmission line (Figure 5.17, and compare this also to Figure 5.6). The current induced in such a transmission line by an external field increases steadily with frequency until the first resonance is reached, after which it exhibits a series of peaks and nulls at higher resonances [20]. The coupling mechanism is enhanced at the resonant frequency of the cable, which depends on its length and on the reactive loading of whatever equipment is attached to its end. A length of 2 metres is quarter-wave resonant at 37.5MHz, half-wave resonant at 75MHz.

Cable loading

The dominant resonant mode depends on the RF impedance (high or low) at the distant end of the cable. If the cable is connected to an ungrounded object such as a hand controller it will have a high RF impedance, which will cause a high coupled current at quarter-wave resonance and high coupled voltage at half-wave. Extra capacitive loading such as body capacitance will lower its apparent resonant frequency.

Conversely, a cable connected to another grounded object such as a separately earthed peripheral will see a low impedance at the far end, which will generate high coupled current at half-wave and high coupled voltage at quarter-wave resonance. Extra inductive loading, such as the inductance of the earth connection, will again tend to lower the resonant frequency.

These effects are summarized in Figure 5.18. The RF common mode impedance of the cable varies from around 35Ω at quarter wave resonance to several hundred ohms maximum. A convenient average figure (and one that is taken in many standards) is 150Ω. Because cable configuration, layout and proximity to grounded objects are outside the designer's control, attempts to predict resonances and impedances accurately are unrewarding.

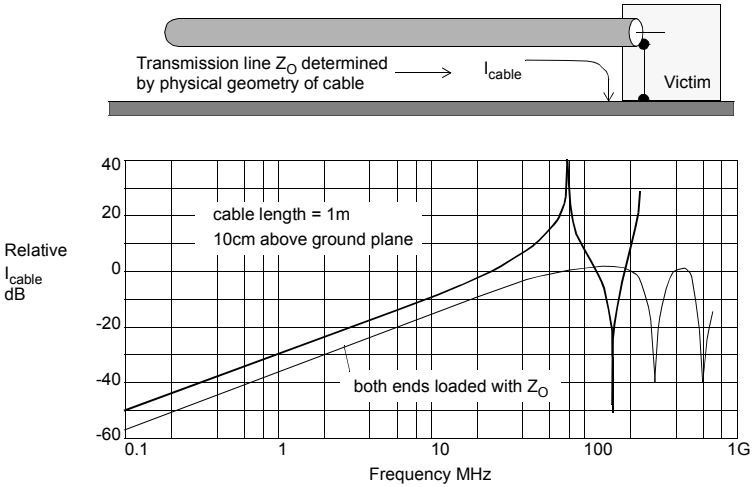


Figure 5.17 Cable coupling to radiated field

5.3.1.2 Current injection

A convenient method for testing the RF susceptibility of equipment without reference to its cable configuration is to inject RF as a common mode current or voltage directly onto the cable port (see also section 4.1.4)[90]. This represents real-life coupling situations at lower frequencies well, until the equipment dimensions approach a half wavelength. It can also reproduce the fields (E_{RF} and H_{RF}) associated with radiated field coupling. The route taken by the interference currents, and hence their effect on the circuitry, depends on the various internal and external RF impedances to earth, as shown in Figure 5.19. Connecting other cables will modify the current flow to a marked extent, especially if the extra cables interface to a physically different location on the pcb or equipment. An applied voltage of 1V, or an injected current of 3–10mA, can be taken to correspond in typical cases to a radiated field strength of 1V/m. However there is considerable disagreement over any single figure for conversion from radiated to injected, and it is generally accepted that conducted tests do not directly represent radiated tests at all [107], because of the variability attributable to multiple cable connections.

5.3.1.3 Cavity resonance

A screened enclosure can form a resonant cavity; standing waves in the field form between opposite sides when the dimension between the sides is a multiple of a half-wavelength. The electric field is enhanced in the middle of this cavity while the magnetic field is enhanced at the sides. This effect is usually responsible for peaks in the susceptibility versus frequency profile in the UHF region, and is also a contributor to the reciprocal nature of susceptibility peaks corresponding with emission peaks. It is discussed further in section 8.3.3.

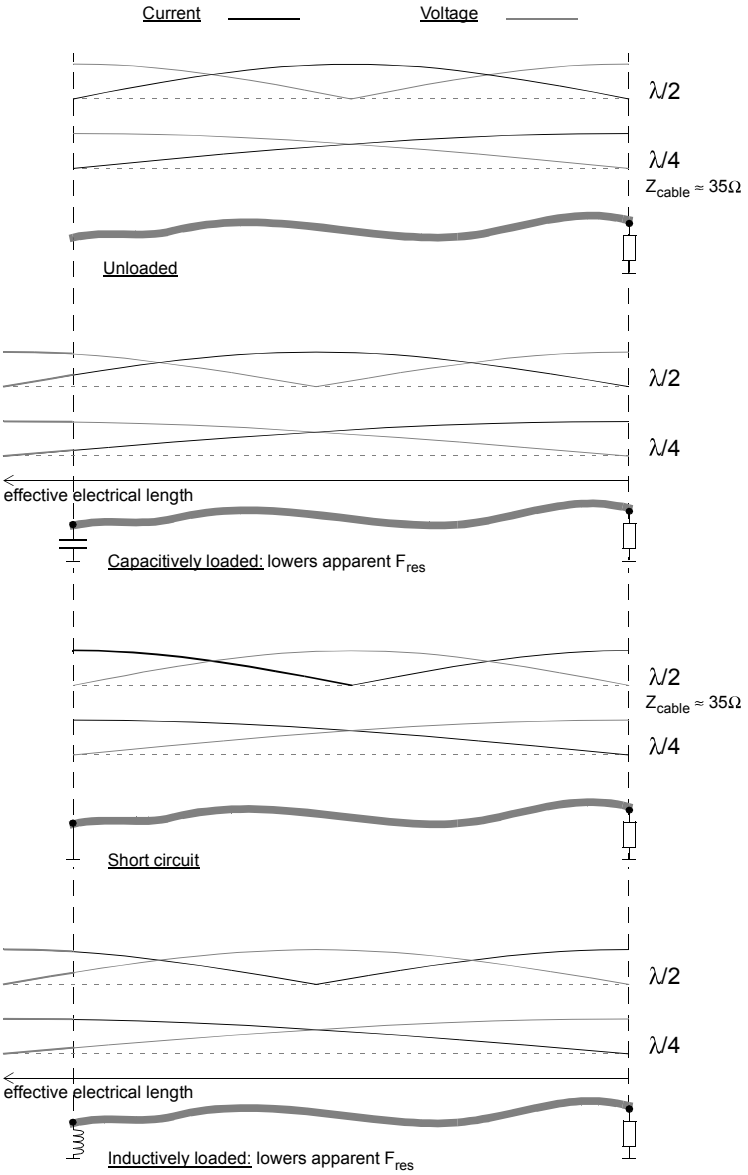


Figure 5.18 Current and voltage distribution along a resonant cable

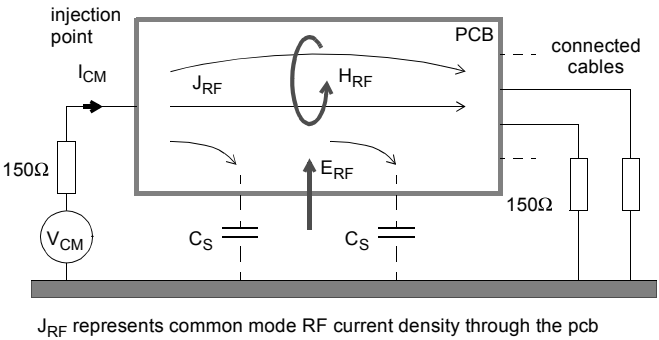


Figure 5.19 Common mode RF injection

5.3.2 Transients

Transient overvoltages occur on the mains supply leads due to switching operations, fault clearance or lightning strikes elsewhere on the network. Transients over 1kV account for about 0.1% of the total number of transients observed. A study by the German ZVEI [67] made a statistical survey of 28,000 live-to-earth transients exceeding 100V, at 40 locations over a total measuring time of about 3,400 hours. Their results were analysed for peak amplitude, rate of rise and energy content. Table 5.2 shows the average rate of occurrence of transients for four classes of location, and Figure 5.20 shows the relative number of transients as a function of maximum transient amplitude. This shows that the number of transients varies roughly in inverse proportion to the cube of peak voltage.

High energy transients may threaten active devices in the equipment power supply. Fast-rising edges are the most disruptive to circuit operation, since they are attenuated least by the coupling paths and they can generate large voltages in inductive ground and signal paths. The ZVEI study found that rate of rise increased roughly in proportion to the square root of peak voltage, being typically 3V/ns for 200V pulses and 10V/ns for 2kV pulses. Other field experience has shown that mechanical switching produces multiple transients (bursts) with risetimes as short as a few nanoseconds and peak amplitudes of several hundred volts. Attenuation through the mains network (see section 5.1.3) restricts fast risetime pulses to those generated locally.

Analogue circuits are almost immune to isolated short transients, whereas digital circuits are easily corrupted by them. As a general guide, microprocessor equipment should be tested to withstand pulses at least up to 2kV peak amplitude. Thresholds below 1kV will give unacceptably frequent corruptions in nearly all environments, while between 1kV–2kV occasional corruption will occur. For a belt-and-braces approach for high reliability equipment, a 4–6kV threshold is recommended.

5.3.2.1 Coupling mode

Mains transients may appear in differential mode (symmetrically between live and neutral) or common mode (asymmetrically between live/neutral and earth). Coupling between the conductors in a supply network tends to mix the two modes. Differential mode spikes are usually associated with relatively slow risetimes and high energy, and

Area Class	Average rate of occurrence (transients/hour)
Industrial	17.5
Business	2.8
Domestic	0.6
Laboratory	2.3

Table 5.2 Average rate of occurrence of mains transients

Sources:
Transients in Low Voltage Supply Networks, J.J. Goedbloed, IEEE Transactions on Electromagnetic Compatibility, Vol EMC-29 No 2, May 1987, p 107
Characterization of Transient and CW Disturbances Induced in Telephone Subscriber Lines, J.J. Goedbloed, W.A. Pasmooij, IEE 7th International Conference on EMC, York 1990

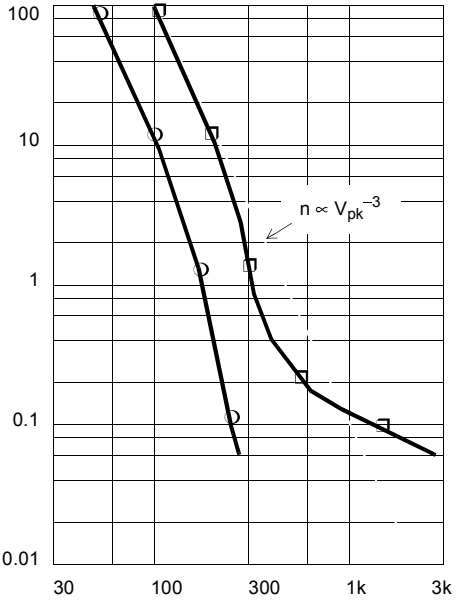


Figure 5.20 Relative number of transients (per cent) vs. maximum transient amplitude (volts)
❒ Mains lines (V_T 100V), ❍ Telecomm lines (V_T 50V)

require suppression to prevent input circuit damage but do not, provided this suppression is incorporated, affect circuit operation significantly. Common mode transients are harder to suppress because they require connection of suppression components between live and earth, or in series with the earth lead, and because stray capacitances to earth are harder to control. Their coupling paths are very similar to those followed by common mode RF signals. Unfortunately, they are also more disruptive because they result in transient current flow in ground traces.

5.3.2.2 Spectral density and energy content

Transient interference is inherently broadband, and its frequency distribution is described by its amplitude spectral density: that is, the amplitude over a defined bandwidth versus frequency, expressed in volts per Hertz or volt-seconds. If the actual waveshape of a transient is known then the spectral density can be derived by taking the Fourier transform of this time domain waveform. In general of course the waveforms of real transients vary widely, but Figure 5.21 shows the spectral densities of the waveforms which have been standardized in the IEC 61000-4 series of immunity tests. If the frequency domain coupling transfer function is known even approximately, then the spectral density can be multiplied by this transfer function to work out the amplitude of an incoming transient at points of interest in the circuit [17].

The energy content of transients and surges is not simple to define. The actual energy available from the source is not all dissipated in the load. That proportion which

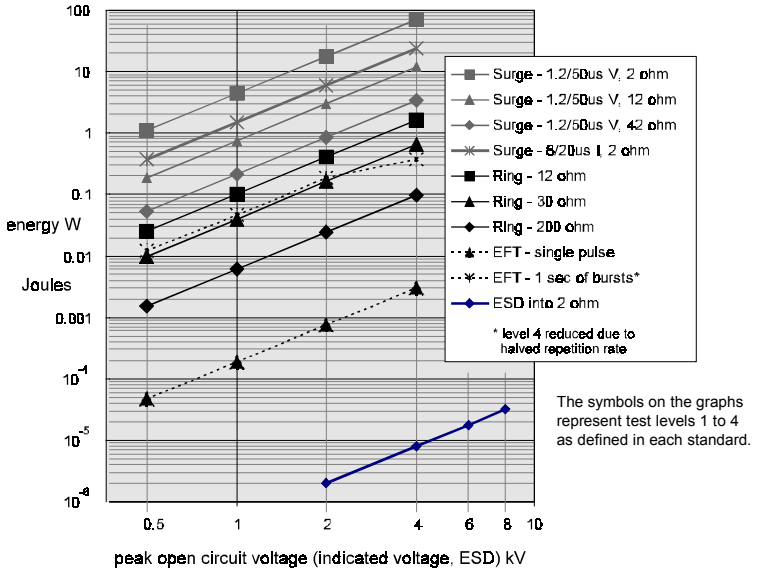


Figure 5.21 Amplitude spectral density and energy content

is, depends on the ratio of the load and source impedances. In general, a load such as a surge suppressor will be non-linear and will also have a time or frequency dependence.

As an approximate indication of the energy content of a particular standard transient, the actual energy delivered by the generator into a defined resistive load can be calculated. For the ESD and EFT waveforms, these can be the calibration loads of 2Ω and 50Ω respectively. For the surge and ring waves, a load which matches the output impedance can be chosen, and the voltage or current waveform is delivered into this resistance with half the open circuit (or short circuit, for current) amplitude. In practice, of course, this doesn't happen since the load is not matched to the output

impedance. In these cases the energy in Joules (watt seconds) is shown in Figure 5.21 and is given by

$$W = \frac{1}{R} \cdot \int_0^T \left(\frac{V(t)}{2}\right)^2 dt \qquad W = R \cdot \int_0^T \left(\frac{I(t)}{2}\right)^2 dt$$

where V(t) and I(t) are the open circuit voltage and short circuit current waveforms, respectively.

These graphs are for comparative purposes only – the real energy delivered to a particular EUT can only be calculated if the load impedance and characteristics, and the actual waveshape applied to this load, are known accurately.

5.3.2.3 Transients on signal lines

Fast transients can be coupled, usually capacitively, onto signal cables in common mode, especially if the cable passes close to or is routed alongside an impulsive interference source. Although such transients are generally lower in amplitude than mains-borne ones, they are coupled directly into the I/O ports of the circuit and will therefore flow in the circuit ground traces, unless the cable is properly screened and terminated or the interface is properly filtered.

Other sources of conducted transients are telecommunication lines and the automotive 12V supply. The automotive environment can regularly experience transients that are many times the nominal supply range. The most serious automotive transients (Figure 5.22) are the load dump, which occurs when the alternator load is suddenly disconnected during heavy charging; switching of inductive loads, such as motors and solenoids; and alternator field decay, which generates a negative voltage spike when the ignition switch is turned off. ISO 7637 specifies transient testing in the automotive field.

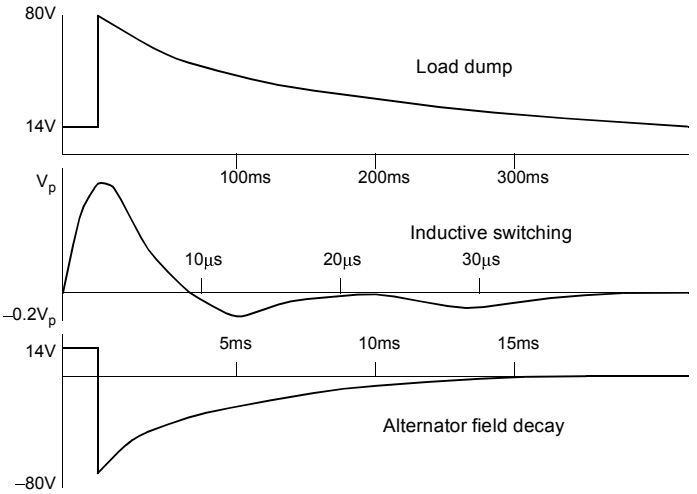


Figure 5.22 Automotive transients according to ISO 7637-1

Work on common mode transients on telephone subscriber lines [68] has shown that the amplitude versus rate of occurrence distribution also follows a roughly inverse cubic law as in Figure 5.20. Actual amplitudes were lower than those on the mains (peak amplitudes rarely exceeded 300V). A transient ringing frequency of 1MHz and rise times of 10–20ns were found to be typical. Telephone and data lines that enter a building from outside are particularly likely to be subject to lightning surges, and any ports that are connected to such lines should be designed to withstand such surges.

5.3.3 Electrostatic discharge

When two non-conductive materials are rubbed together or separated, electrons from one material are transferred to the other. This results in the accumulation of triboelectric charge on the surface of the material. The amount of the charge caused by movement of the materials is a function of the separation of the materials in the triboelectric series (Figure 5.23(a)) – positive materials give up electrons more readily, negative materials acquire them more readily. Additional factors are the closeness and area of contact, and rate of separation.

The voltage to which an object can be charged depends on its capacitance, following the law Q = CV. The human body can be charged by triboelectric induction to several kV. Because a perfect insulator does not allow movement of electrons, surface charges on an insulator remain in the area within which they were generated, but the human body is conductive and so a triboelectrically induced charge distributes itself over the body. The rate at which charge will bleed off a body to its surroundings, and so become neutralized, depends on the surface resistivity of the body and its surroundings. This in turn is a function of relative humidity: The more moisture there is in the air, the lower the surface resistivity of insulators and hence the quicker that charges bleed away. In practice, since movement is constantly generating charge, there is a balance between generation and dissipation which results in a typical level of charge voltage that can be found in a particular environment (Figure 5.23(b)).

When the body (in the worst case, holding a metal object such as a key) approaches a conductive object, the charge is transferred to that object normally via a spark, when the potential gradient across the narrowing air gap is high enough to cause breakdown. The energy involved in the charge transfer may be low enough to be imperceptible to the subject; at the other extreme it can be extremely painful. It is not essential that the target object is grounded. Charge transfer can occur between any two capacitive objects as long as there is a static potential difference between them, and a disruptive discharge current pulse will flow.

5.3.3.1 The ESD waveform

When an electrostatically charged object is brought close to a grounded target the resultant discharge current consists of a very fast (sub-nanosecond) edge followed by a comparatively slow bulk discharge curve. The characteristic of the hand/metal ESD current waveform is a function of the approach speed, the voltage, the geometry of the electrode and the relative humidity. The equivalent circuit for such a situation is shown in Figure 5.23(c). The capacitance C_D (typically 150pF for the human body) is charged via a high resistance up to the electrostatic voltage V. The actual value of V will vary as the charging and leakage paths change with the environmental circumstances and movements of the subject. When a discharge is initiated, the free space capacitance C_S, which is directly across the discharge point, produces an initial current peak the value

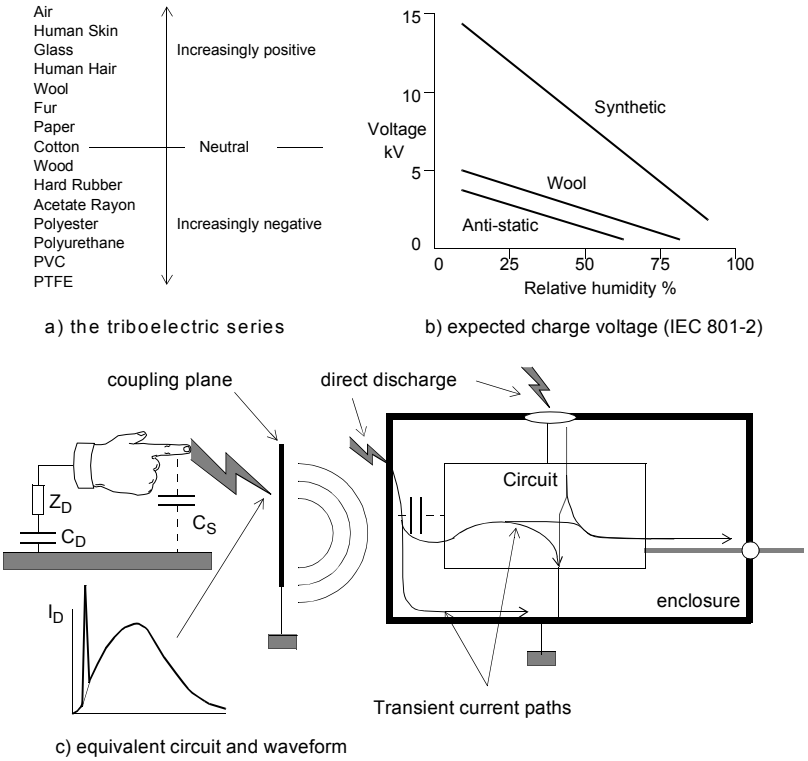


Figure 5.23 The electrostatic discharge

of which is only limited by the local circuit stray impedance, while the main discharge current is limited by the body's bulk inductance and resistance Z_D.

The principal effects of an ESD in terms of equipment malfunction are produced by the discharge current pulse di/dt and its indirect effects. The rate of change of electric field dE/dt when the local static charge voltage collapses can also couple capacitively into high impedance circuits, and in some circumstances the high static electric field itself, before a discharge happens, may cause undesirable effects.

5.3.3.2 Coupling paths

The resultant sub-nanosecond transient equalizing current of several tens of amps follows a complex route to ground through the equipment and is very likely to upset digital circuit operation if it passes through the circuit tracks. The paths are defined more by stray capacitance, case bonding and track or wiring inductance than by the designer's intended circuit. The high magnetic field associated with the current can induce transient voltages in nearby conductors that are not actually in the path of the current. Even if not discharged directly to the equipment, a nearby discharge such as to a metal desk or chair will generate an intense radiated field which will couple into unprotected equipment.

Critical areas which can act as sink points for the ESD are exposed metalwork, apertures, front panel components and connectors. Components and apertures can allow a discharge to take place via creepage across a surface to the circuits inside an enclosure, even if the enclosure itself is insulating. The breakdown voltage gradient in dry air is approximately 30kV per cm but this is reduced considerably across a surface, especially if the surface is contaminated with dirt or other substances.

5.3.3.3 Secondary discharge

A common problem arises when a product enclosure is connected externally to ground at a different point and via a different route than the internal circuit. Because of the inductance of the various connections, a transient voltage will appear inside the enclosure, between the enclosure and the circuit (Figure 5.24). This voltage can then cause a secondary discharge to occur at unpredictable points inside the enclosure, which can be much more damaging and disruptive than the source discharge, since there is a lower impedance to limit the current, and also because a higher induced voltage occurs on a PCB track when an ESD occurs within a resonant structure. To prevent this, it is essential to bond the enclosure and the circuit board together at a suitable point, typically at an interface ground (see section 6.2.3).

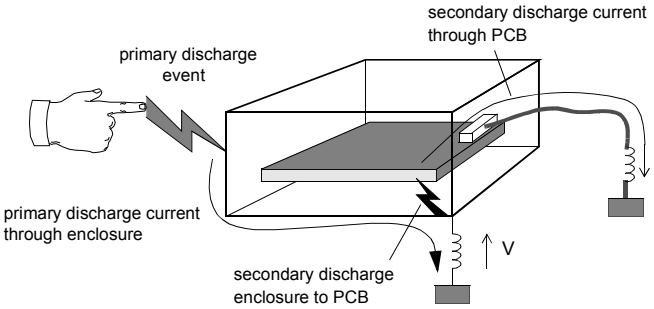


Figure 5.24 The cause of secondary discharge

5.3.4 LF magnetic fields

Magnetic fields at low frequencies can induce interference voltages in closed wiring loops, their magnitude depending on the area that is intersected by the magnetic field. Non-toroidal mains transformers and switch-mode supply transformers are prolific sources of such fields and they will readily interfere with sensitive circuitry or components within the same equipment. Any other equipment needs to be immune to the proximity of such sources. Particular environments may result in high low-frequency or dc magnetic field strengths, such as electrolysis plant where very high currents are used, or certain medical apparatus.

50Hz currents in supply conductors are typical sources of magnetic fields. If the currents in a cable are balanced, i.e. the cable carries live and neutral together or all three phases together, then at a distance the magnetic fields from each conductor cancel and the net field is near zero. Close in to the cable though, the fields do not cancel perfectly since their source conductors are located at slightly different positions. The fields also will not cancel if the currents are not balanced, i.e. if there is some return

path outside the cable – this is the same situation as was discussed earlier in section 5.1.5.2 for common mode current flow.

The flux density at a distance r metre at right angles to a single long conductor carrying a current I amps is given by

$$B = (0.2 \cdot I)/r \text{ microtesla} \quad (5.13)$$

To find the field at a distance from a group of conductors, as in a cable, each carrying current of a particular phase and amplitude, it is only necessary to calculate the appropriate geometry and perform a vector sum of the field contributions from each conductor. A threshold value of 1μT is often recommended as a level below which an installation is acceptable [85].

The voltage developed by an external magnetic field in a single turn loop is:

$$V = A \cdot dB/dt \quad (5.14)$$

where A is the loop area in m^2 and
B is the flux density normal to the plane of the loop in Tesla

It is rare for such fields to affect digital or large signal analogue circuits, but they can be troublesome with low level circuits where the interference is within the operating bandwidth, such as audio or precision instrumentation. Specialized devices which are affected by magnetic fields, such as photomultiplier or cathode ray tubes, may also be susceptible.

5.3.4.1 Magnetic field screening

Conventional screening is ineffective against LF magnetic fields, because it relies on reflection rather than absorption of the field. Due to the low source impedance of magnetic fields reflection loss is low. Since it is only the component of flux normal to the loop which induces a voltage, changing the relative orientation of source and loop may be effective. LF magnetic shielding is only possible with materials which exhibit a high absorption loss such as steel, mu-metal or permalloy. As the frequency rises these materials lose their permeability and hence shielding efficiency, while non-magnetic materials such as copper or aluminium become more effective. Around 100kHz shielding efficiencies are about equal. Permeable metals are also saturated by high field strengths, and are prone to lose their permeability through handling. See section 8.3.2 on page 295 for more discussion.

5.3.5 Supply voltage phenomena

Low frequency disturbances on the mains supply are covered in some detail in IEC61000 part 2 sections 1 and 2. Section 1 [147] describes the environment, i.e. the nature of the disturbances that can be expected on public mains supplies, while section 2 [148] gives compatibility levels, i.e. the levels of disturbances that can be expected. The phenomena considered are:

- harmonics and inter-harmonics
- voltage fluctuations, dips and short supply interruptions
- voltage unbalance in three-phase supplies
- mains signalling
- power frequency variation

Harmonics are considered further in section 5.4.

Brown-outs (voltage dips) and interruptions are a feature of all mains distribution networks, and are usually due to fault clearing or load switching elsewhere in the system (Figure 5.25). Such events will not be perceived by ordinary electronic equipment if its input reservoir hold-up time is sufficient, but if this is not the case then restarts and output transients can be experienced. Thyristor inverters may experience commutation failure and synchronous devices may lose synchronism. Typically, interruptions (as opposed to power cuts) can last for 10–500ms.

Load and line voltage fluctuations are maintained between +10% and −15% of the nominal line voltage in most industrialized countries. As a result of HD472/BS7697 [161], the EU countries are moving towards 230V ±10% at the point of connection to the consumer. Between 1995 and 1st January 2003, countries with a previously declared nominal voltage of 240V will have a range of 230V +10%–6%, and those with a previous voltage of 220V will have a range of 230V +6% −10%. Slow changes in the voltage within these limits occur on a diurnal pattern as the load on the power system varies. The declared voltage does not include voltage drops within the customer's premises, and so you should design stabilized power supplies to meet at least the −15% limit.

Dips exceeding 10% of nominal voltage occur up to 4 times per month for urban consumers and more frequently in rural areas where the supply is via overhead lines [75][148]. Note that much wider voltage (and frequency) fluctuations and more frequent interruptions are common in those countries which do not have a well-developed supply network. They are also common on supplies which are derived from small generators.

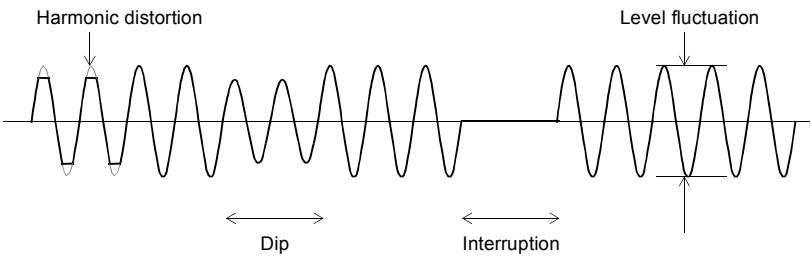


Figure 5.25 Mains supply fluctuations

Heavy industrial loads such as resistance and arc welding machines, large motors and arc furnaces can cause short-term step or random fluctuations and can affect many consumers fed from the same source. The main effect of these disturbances is flicker of lamp loads, which can cause physiological discomfort. Electronic power supply circuits can normally be designed to ignore them, although other circuits which use the 50Hz signal (e.g. for timing or phase reference) should have their operating bandwidth severely restricted by a 50Hz bandpass filter to ensure immunity from low-amplitude step changes.

5.4 Mains harmonics

One EMC phenomenon, which comes under the umbrella of the EMC Directive and is usually classified as an "emission", is the harmonic content of the mains input current. This is mildly confusing since the equipment is not actually "emitting" anything: it simply draws its power at harmonics of the line frequency as well as at the fundamental.

5.4.1 The supplier's problem

The problem of mains harmonics is principally one for the supply authorities, who are mandated to provide a high quality electricity supply. If the aggregate load at a particular mains distribution point has a high harmonic content, the non-zero distribution source impedance will cause distortion of the voltage waveform at this point, and possibly, due to supply network resonances, at other remote points. This in turn may cause problems for other users, and the currents themselves may also create problems (such as overheating of transformers and compensating components) for the supplier. The supplier does of course have the option of uprating the distribution components or installing special protection measures, but this is expensive and the supplier has room to argue that the users should bear some of the costs of the pollution they create.

Throughout the last few decades, harmonic pollution has been increasing and it has been principally due to low power electronic loads installed in large numbers. Between them, domestic TV sets and office information technology equipment account for about 80% of the problem. Other types of load which also take significant harmonic currents are not widely enough distributed to cause a serious problem yet, or are dealt with individually at the point of installation as in the case of industrial plant. The supply authorities are nevertheless sufficiently worried to want to extend harmonic emission limits to all classes of electronic products.

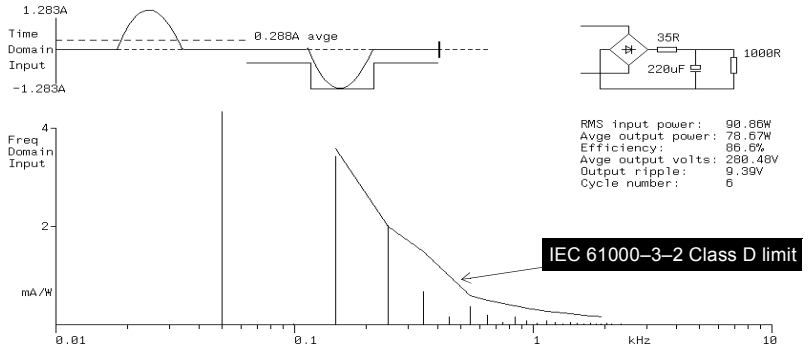
IEC 61000-2-2 defines the compatibility level in terms of total harmonic distortion factor as 8% THD.

5.4.2 Non-linear loads

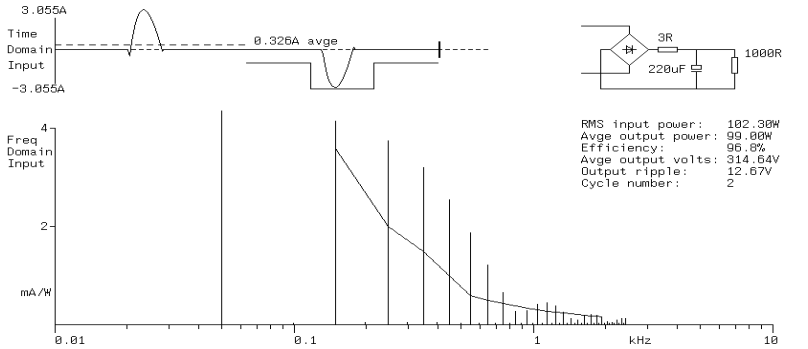
A plain resistive load across the mains draws current only at the fundamental frequency (50Hz in Europe). Most electronic circuits are anything but resistive. The universal rectifier-capacitor input draws a high current at the peak of the voltage waveform and zero current at other times; the well known triac phase control method for power control (lights, motors, heaters etc.) begins to draw current only partway through each half cycle. These current waveforms can be represented as a Fourier series, and it is the harmonic amplitudes of the series that are subject to regulation.

The standard which covers mains harmonics is IEC 61000-3-2, published in 1995. Its requirements are detailed in section 3.2 where you will see that it applies either fixed limits to the harmonic content up to 2kHz (40th harmonic) or variable limits depending on the power drawn by the equipment; choice of limits depends on the class of product.

The limits are effectively an additional design constraint on the values of the input components, most notably the input series impedance (which is not usually considered as a desirable input component at all). Figure 5.26(a), which is a Fourier analysis of the current waveform calculated in the time domain, shows the harmonic content of input current for a rectifier-reservoir combination with a fairly high series resistance. This value of series resistance would not normally be found except with very inefficient transformer-input supplies. The fifth harmonic content just manages to meet Class D.



(a)



(b)

Figure 5.26 Mains input current harmonics for rectifier-reservoir circuit

5.4.2.1 The effect of series resistance

Figure 5.26(b) illustrates the difference in input harmonics resulting from a tenfold reduction in input resistance. This level of input resistance would be typical for a direct-off-line switching supply and many highly efficient supplies could boast a lower R_S. The peak input current has increased markedly while its duty cycle has shrunk, leading to a much higher crest factor (ratio of peak to root mean square current) and thus higher levels of harmonics.

Increasing input series resistance to meet the harmonic limits is expensive in terms of power dissipation except at very low powers. In practice, deliberately dissipating between 10 and 20% of the input power rapidly becomes unreasonable above levels of 50–100W. In fact, the requirements of IEC 61000-3-2 do not apply to equipment having an active input power below 75W. Alternatives are to include a series input choke, which since it must operate down to 150Hz at the full input current is expensive in size and weight; or to include electronic power factor correction (PFC), which

converts the current waveform to a near-sinusoid but is expensive in cost and complexity.

5.4.2.2 Power factor correction

PFC is essentially a switchmode converter on the front-end of the supply and therefore is likely to contribute extra RF switching noise at the same time as it reduces input current harmonics. It is possible to combine PFC with the other features of a direct-off-line switching supply, so that if you are intending to use a SMPS anyway there will be little extra penalty. It also fits well with other contemporary design requirements such as the need for a "universal" (90–260V) input voltage range. Such power supplies can already be bought off-the-shelf, but unless you are a power supply specialist, to design a PFC-SMPS yourself could take considerable extra design and development effort. The availability of special-purpose control ICs makes the task easier.

Figure 5.27 shows the basis of operation of a power factor correction circuit. Instead of an input rectifier/reservoir combination, the rectified input feeds a switchmode boost converter circuit directly whose operational input voltage range extends from near-zero to the peak supply voltage. The pulse width of the switching circuit is regulated to give an average input current which approximates to the required sinusoidal waveshape. The effective distortion is very low, and therefore so is the harmonic content.

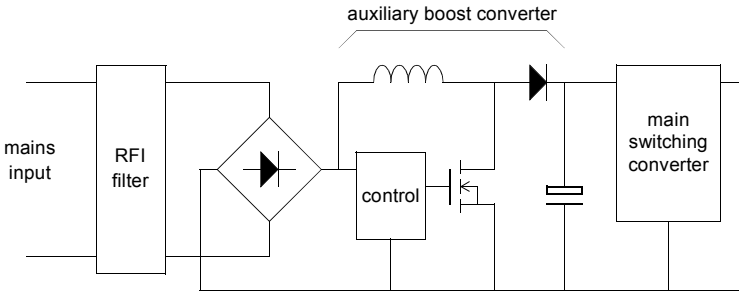


Figure 5.27 Schematic of a switchmode PFC circuit

5.4.2.3 Phase control

Power control circuits which vary the switch-on point with the phase of the mains waveform are another major source of harmonic distortion on the input current. Lighting controllers are the leading example of these. Figure 5.28 shows the harmonic content of such a waveform switched at 90° (the peak of the cycle, corresponding to half power). The maximum harmonic content occurs at this point, decreasing as the phase is varied either side of 90°. Lighting dimmers without input filtering or PFC of greater than about 5A rating are outlawed, since the limits are set at an absolute value.

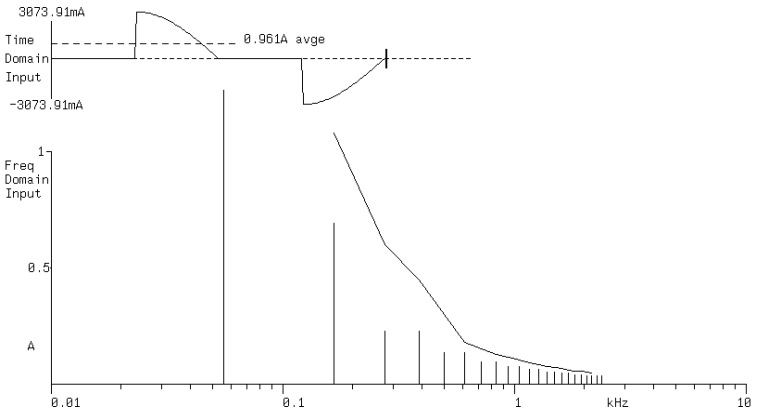


Figure 5.28 Mains input current harmonics for 500W phase control circuit at half power

Chapter 6

Layout and grounding

Designing for good EMC starts from the principle of controlling the flow of interference into and out of the equipment. You must assume that interference will occur to and will be generated by any product which includes active electronic devices. To improve the electromagnetic compatibility of the product you place barriers and route currents such that incoming interference is diverted or absorbed before it enters the circuit, and outgoing interference is diverted or absorbed before it leaves the circuit. A good analogy is to think of the circuit as a town, and the EMC control measures as bypasses or ring roads. The interference (traffic) is routed around the town rather than being forced to flow through it; the disruption to the town's operation is that much less.

In either case, you can conceive the control measures as applying at three levels, primary, secondary and tertiary, as shown in Figure 6.1.

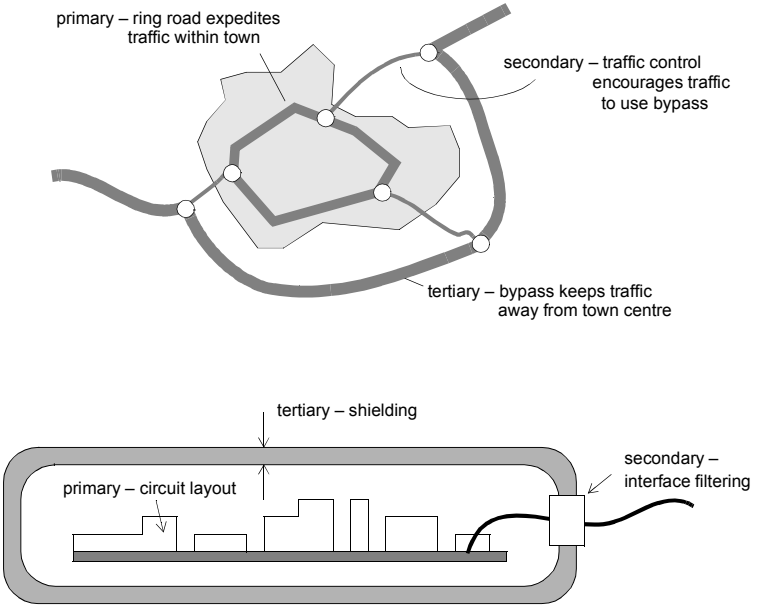


Figure 6.1 EMC control measures

Control at the primary level involves circuit design measures such as decoupling, balanced configurations, bandwidth and speed limitation, and especially board layout and grounding. For some low-performance circuits, and especially those which have no connecting cables, such measures may be sufficient in themselves. At the secondary level you must always consider the interface between the internal circuitry and external cables. This is invariably a major route for interference in both directions, and for some products (particularly where the circuit design has been frozen) all the control may have to be applied by filtering at these interfaces. Choice and mounting of connectors forms an important part of this exercise.

Full shielding (the tertiary level) is an expensive choice to make and you should only choose this option when all other measures have been applied. But since it is difficult or impossible to predict the effectiveness of primary measures in advance, it is wise to allow for the possibility of being forced to shield the enclosure. This means adapting the mechanical design so that a metal case could be used, or if a moulded enclosure is essential, you should ensure that apertures and joints in the mouldings can be adequately bonded at RF, that ground connections can be made at the appropriate places and that the moulding design allows for easy application of a conductive coating.

Chapter 7 looks at circuit design, and Chapter 8 considers the "classical" EMC aspects of interfaces, filters and shielding. This chapter covers layout and grounding.

6.1 Equipment layout and grounding

The most cost-effective approach is to consider the equipment's layout and ground regime at the beginning. No unit cost is added by a designed-in ground system. Ninety per cent of post-design EMC problems are due to inadequate layout or grounding: a well-designed layout and ground system can offer both improved immunity and protection against emissions, while a poorly designed one may well be a conduit for emissions and incoming interference. The most important principles are:

- partition the system to allow control of interference currents
- consider ground as a path for current flow, both of interference into the equipment and conducted out from it
- consider it also as a means of preventing interference currents from affecting signal circuits; this means careful placement of grounding points, and minimizing both the ground impedance itself and its transfer impedance to the circuit
- design the conducting parts of the mechanical structure in the knowledge that they are unavoidably carrying interference currents, which you want to keep separate from your circuit.

6.1.1 System partitioning

The first design step is to partition the system. A poorly partitioned, or non-partitioned system (Figure 6.2) may have its component sub-systems separated into different areas of the board or enclosure, but the interfaces between them will be ill-defined and the external ports will be dispersed around the periphery. This makes it difficult to control the common mode currents that will exist at the various interfaces. Dispersal of the ports means that the distances between ports on opposite sides of the system is large, leading to high induced ground voltages as a result of incoming interference, and efficient coupling to the cables of internally generated emissions.

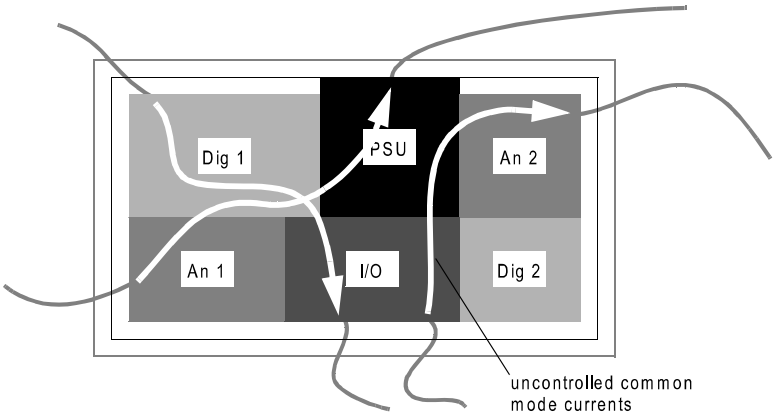


Figure 6.2 The haphazard system

Usually the only way to control emissions and immunity of such a system is by placing an overall shield around it and filtering each interface. In many cases it will be difficult or impossible to maintain integrity of the shield and still permit proper operation – the necessary apertures and access points will preclude effective attenuation through the shield.

6.1.1.1 The partitioned system

Partitioning separates the system into critical and non-critical sections from the point of view of EMC. Critical sections are those which contain radiating sources such as microprocessor logic or video circuitry, or which are particularly susceptible to imported interference: microprocessor circuitry and low-level analogue circuits. Non-critical sections are those whose signal levels, bandwidths and circuit functions are such that they are not susceptible to interference nor capable of causing it: non-clocked logic, linear power supplies and power amplifier stages are typical examples. Figure 6.3 shows this method of separation.

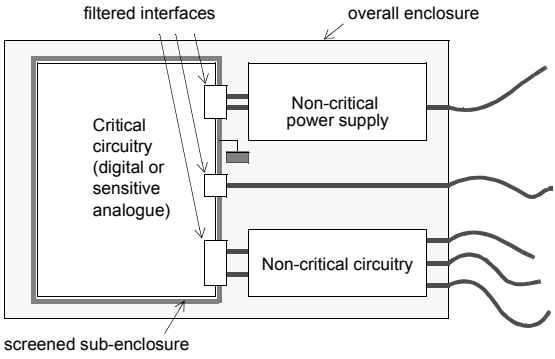


Figure 6.3 System partitioning

Control of critical sections

Critical sections can then be enclosed in a shielded enclosure into and out of which all external connections are carefully controlled. This enclosure may encase the whole product or only a portion of it, depending on the nature of the circuits: your major design goal should be to minimize the number of controlled interfaces, and to concentrate them physically close together. Each interface that needs to be filtered or requires screened cabling adds unit cost to the product. A system with no electrical interface ports – such as a pocket calculator or infra-red remote controller – represents an ideal case from the EMC point of view.

Note that the shield acts both as a barrier to radiated interference and as a reference point for ground return currents. In many cases, particularly where a full ground plane pcb construction is used, the latter is the more important function and it may be possible to do without an enclosing shield.

6.1.2 Grounding

Once the system has been properly partitioned, you can then ensure that it is properly grounded. Before continuing, it is as well to note that there is some confusion in terminology. In conventional electrical usage, "grounding" is American for the same function as is "earthing" in English; that is, a safety protective function. Since this is an English book and the EMC function is different, the words "ground" and "grounding" will be used here to distinguish the EMC function while "earth" and "earthing" will be used for the safety function.

The accepted purpose for grounding is to give a reference for external connections to the system. The classical definition of a ground is "an equipotential point or plane which serves as a reference for a circuit or system". Unfortunately this definition is meaningless in the presence of ground current flow. Even where signal currents are negligible, induced ground currents due to environmental magnetic or electric fields will cause shifts in ground potential. A good grounding system will minimize these potential differences by comparison with the circuit operating levels, but it cannot eliminate them. It has been suggested [5] that the term "ground" as conventionally used should be dropped in favour of "reference point" to make the purpose of the node clear.

An alternative definition for a ground is "a low impedance path by which current can return to its source"[98]. This emphasizes current flow and the consequent need for low impedance, and is more appropriate when high frequencies are involved. Ground currents always circulate as part of a loop. The task is to design the loop in such a way that induced voltages remain low enough at critical places. You can only do this by designing the ground circuit to be as compact and as local as possible.

The most important EMC function of a ground system is to *minimize interference voltages at critical points compared to the desired signal*. To do this, it must present a low *transfer* impedance path at these critical locations. The concept of transfer impedance is introduced in section 6.1.2.2.

6.1.2.1 Current through the ground impedance

When designing a ground layout you must know the actual path of the ground return current. The amplifier example in Figure 6.4 illustrates this. The high-current output ΔI returns to the power supply from the load; if it is returned through the path Z1–Z2–Z3 (Figure 6.4(a)) then an unwanted voltage component is developed across Z2 which is in series with the input V_S, and depending on its magnitude and phase the circuit will oscillate. This is an instance of common impedance coupling, as per section 5.1.1.

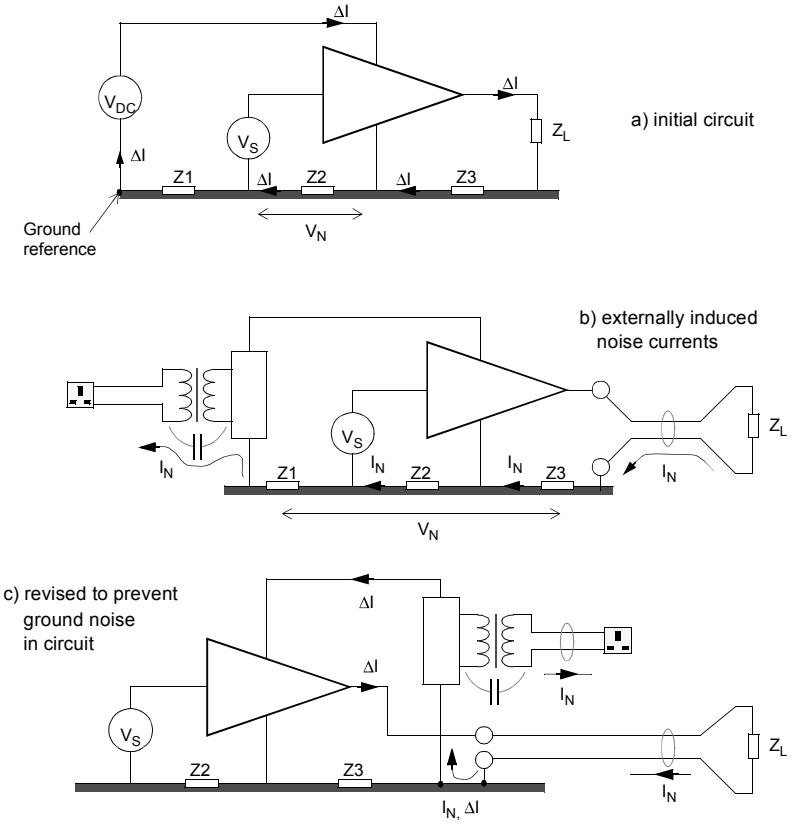


Figure 6.4 Ground current paths in an example circuit

For EMC purposes, instability is not usually the problem; rather it is the interference voltages V_N which are developed across the impedances that create emission or susceptibility problems. At high frequencies (above a few kHz) or high rates of change of current the impedance of any linear connection is primarily inductive and increases with frequency ($V = -L \cdot di/dt$), hence ground noise increases in seriousness as the frequency rises. The effect of adding external connections is illustrated in Figure 6.4(b). Interference current I_N induced in, say, the output lead, flows through the ground system, passing through Z2 again and therefore inducing a voltage in series with the input, before exiting via stray capacitance to the mains supply connection. The same route could be taken in reverse by incoming mains-borne noise.

To deal with the problem, it is simply necessary to ensure that the interfering currents are not allowed to flow through the sensitive part of the ground network, as is shown by the rearrangement of Figure 6.4(c). On a circuit diagram these circuits would appear identical; in practical realization, when laid out on a PCB, they are different.

6.1.2.2 Transfer impedance

For EMC purposes, grounding provides a set of interconnected current paths, designed to have a low transfer impedance Z_T, in order to minimize interfering voltages at sensitive interfaces which may or may not be ground-referred. Z_T determines the strength of the unwanted source in the signal circuit due to interference current flowing in the common mode circuit. Depending on the interface under consideration, we tackle the transfer impedance of an appropriate part of the interconnected grounding paths. The result is a grounding structure, whose three-dimensional shape is designed for low Z_T. The structure can be realized as a "shielding" enclosure, a chassis plate, a plane layer on a PCB, or a cable conduit, whatever is required by the application.

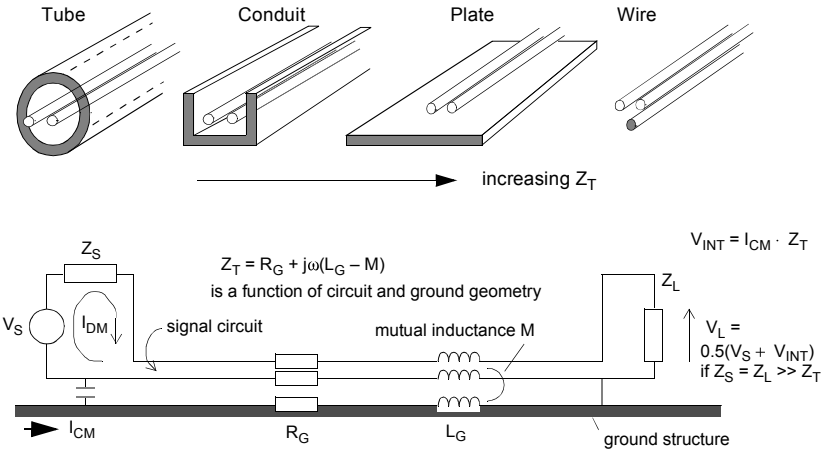


Figure 6.5 Transfer impedance of the ground structure

The important quality of such a structure is that when a disturbance current flows in it, only a small interference voltage V_{INT} is generated differentially in the signal circuit. The dominant contribution to Z_T for external interference currents flowing in the ground is mutual inductance between common- and differential-mode circuits. Z_T is reduced in proportion to the mutual inductance linking the structure and the circuit. The grounding structure should have minimum resistance R_G and self-inductance L_G. Z_T is minimized by a solid enclosing tube – you may recognize this as a coaxial shielded cable – and is worst if the structure is non-existent, since all interference current then flows in the circuit. A haphazard ground structure with appreciable series impedance – caused by apertures and discontinuities, see section 8.3.3 – is little better, and the first level of usefulness is offered by a parallel wire conductor. Practical compromise structures are the conduit or the flat plate. The closer the differential mode circuit is physically to such a grounding structure, the less the Z_T, provided that the structure is unbroken in the direction of current flow.

This discussion has concentrated on ground currents, since in general the low inherent impedance of ground structures allows relatively high interference currents to flow; EMC consists in recognizing this and taking the appropriate precautions. It is important, though, that noise voltages are not allowed to build up on the grounding

structure relative to the circuit, since the close coupling recommended above for low-Z_T purposes also implies a high capacitance, which in turn would allow such voltages to couple more readily into the circuit. This suggests that the circuit 0V reference should itself be connected to the ground structure at least at one point, normally close to the most sensitive part of the circuit; but this will *encourage* the distribution of current between the ground structure and the circuit! This paradox can only be resolved by physically designing the ground structure for the least possible Z_T.

6.1.3 Ground systems

Ignoring for now the need for a safety earth, a grounding system as intended for a circuit reference can be configured as single point, multi-point or as a hybrid of these two.

6.1.3.1 Single point

The single point grounding system (Figure 6.6(a)) is conceptually the simplest, and it eliminates common impedance ground coupling and low frequency ground loops. Each circuit module has its own connection to a single ground, and each rack or sub-unit has one bond to the chassis. Any currents flowing in the rest of the ground network do not couple into the circuit. This system works well up to frequencies in the MHz region, but the distances involved in each ground connection mean that common mode potentials between circuits begin to develop as the frequency is increased. At distances of odd multiples of a quarter wavelength, the circuits are effectively isolated from each other. At the same time, stray capacitance starts to contribute to "sneak" current paths that bypass the single point wiring.

A modification of the single point system (Figure 6.6(b)) ties together those circuit modules with similar characteristics and takes each common point to the single ground. This allows a degree of common impedance coupling between those circuits where it won't be a problem, and at the same time allows grounding of high frequency circuits to remain local. The noisiest circuits are closest to the common point in order to minimize the effect of the common impedance. When a single module has more than one ground, these should be tied together with back-to-back diodes to prevent damage when the circuit is disconnected.

6.1.3.2 Multi-point

Hybrid and multi-point grounding (Figure 6.6(c)) can overcome the RF problems associated with pure single point systems. Multi-point grounding is necessary for digital and large signal high frequency systems. Modules and circuits are bonded together with many short ($< 0.1\lambda$) links to minimize ground-impedance-induced common mode voltages. Alternatively, many short links to a chassis, ground plane or other low impedance conductive body are made. This may not be suitable for sensitive audio circuits, if the loops that are introduced then cause magnetic field pick-up. It is difficult to keep 50/60Hz interference out of such circuits, but this is only a problem if the circuits themselves can be affected by it, and if its amplitude is large because the loop areas are large. Circuits which operate at higher frequencies or levels are not susceptible to this interference. The multi-point subsystem can be brought down to a single point ground in the overall system.

6.1.3.3 Hybrid

Hybrid grounding uses reactive components (capacitors or inductors) to make the grounding system act differently at low frequencies and at RF. This may be necessary

in sensitive wideband circuits. In the example of Figure 6.6(c), the sheath of a relatively long cable is grounded directly to chassis via capacitors to prevent RF standing waves from forming. The capacitors block dc and low-frequencies and therefore prevent the formation of an undesired extra ground loop between the two modules.

When using such reactive components as part of the ground system, you need to take care that spurious resonances (which could enhance interference currents) are not introduced into it. For example if 0.1μF capacitors are used to decouple a cable whose self-inductance is 0.1μH, the resonant frequency of the combination is 1.6MHz. Around this frequency the cable screen will appear to be anything but grounded!

When you are using separate DC grounds and an RF ground plane (such as is offered by the chassis or frame structure), reference each sub-system's DC ground to the frame by a 10–100nF capacitor. The two should be tied together by a low impedance link at a single point where the highest di/dt signals occur, such as the processor motherboard or the card cage backplane.

6.1.3.4 The impedance of ground wires

When a grounding wire runs for some distance alongside a ground plane or chassis

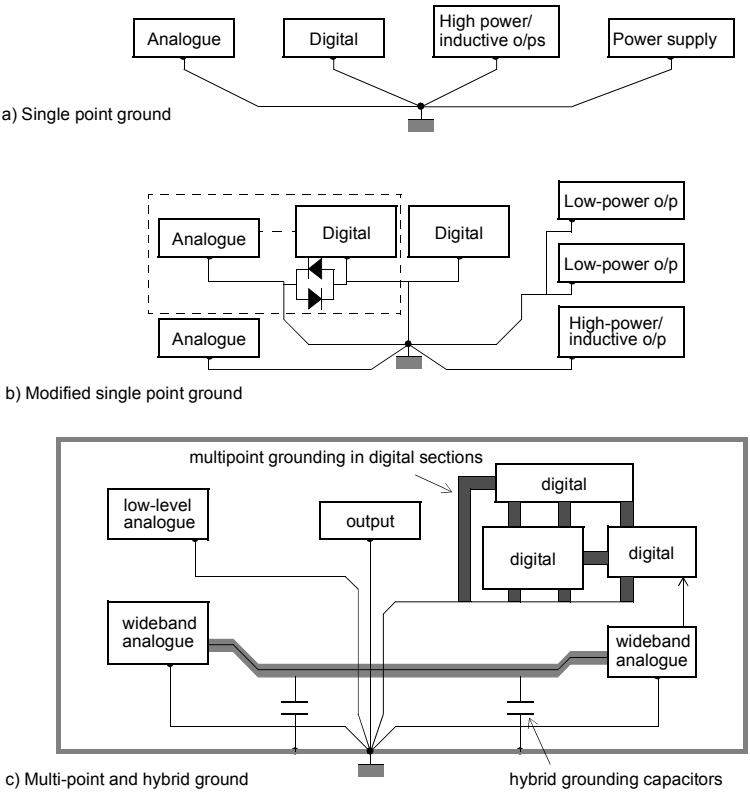


Figure 6.6 Grounding systems

before being connected to it, it appears as a transmission line. This can be modelled as an LCR network with the L and C components determining the characteristic impedance Z_0 of the line (Figure 6.7). As the operating frequency rises, the inductive

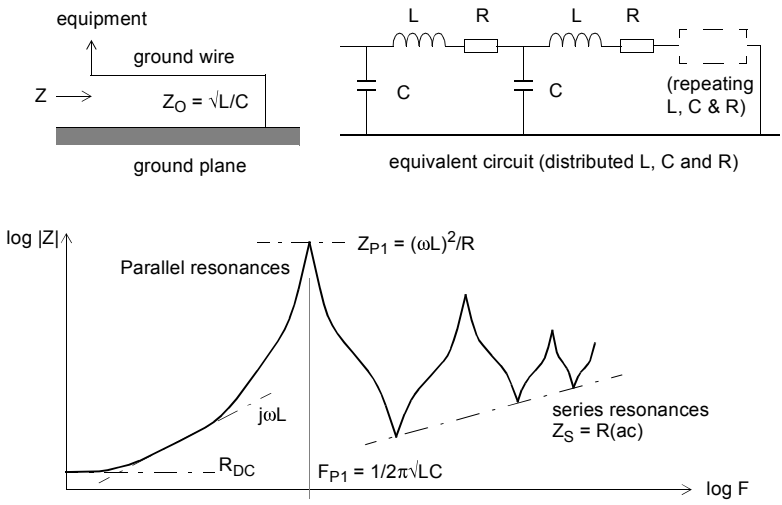


Figure 6.7 The impedance of long ground wires

reactance exceeds the resistance of the wire and the impedance increases up to the first parallel resonant point. At this point the impedance seen at the end of the wire is high, typically hundreds of ohms (determined by the resistive loss in the circuit). After first resonance, the impedance for a lossless circuit follows the law:

$$Z = Z_O \cdot \tan(\omega \cdot x \cdot \sqrt{L/C}) \quad (6.1)$$

where x is the distance along the wire to the short

and successive series (low-impedance) and parallel (high-impedance) resonant frequencies are found. As the losses rise due to skin effect, so the resonant peaks and nulls become less pronounced. To stay well below the first resonance and hence remain an effective conductor, the ground wire should be less than 1/20th of the shortest operating wavelength.

6.1.3.5 The safety earth

From the foregoing discussion, you can see that the safety earth (the green and yellow wire) is not an RF ground at all. Many designers may argue that everything is connected to earth via the green and yellow wire, without appreciating that this wire has a high and variable impedance at RF. In general the safety earth connection is not necessary for EMC purposes: after all, battery powered apparatus can function quite successfully without it. A good low impedance connection to an RF reference provided locally by a chassis, frame or plate *is* necessary and in many cases must be provided *in parallel with* the safety earth. On the other hand, if we are considering mains emissions or incoming mains-borne disturbances, which are propagating in common mode with respect to the

safety earth, then a safety earth connection is required for EMC purposes, so that filter capacitors can be tied to it. This is not because it is an earth, but because it is the return path for the disturbance currents.

It may even be necessary for you to take the safety earth *out* of the RF circuit deliberately, by inserting a choke of the appropriate current rating in series with it (see section 8.2.3.6). This is because it can offer an alternative path for interference currents to invade or circulate within the system, and interrupting this path is a simple way of improving EMC.

6.1.3.6 Ground map

A fundamental tool for use throughout the equipment design is a ground map. This is a diagram which shows all the ground reference points and grounding paths (via structures, cable screens etc. as well as tracks and wiring) for the whole equipment. It concentrates on grounding only; all other circuit functions are omitted or shown in block form. Its creation, maintenance and enforcement throughout the project design should be the responsibility of the EMC design authority.

6.1.3.7 Summary

In the context of product-level grounding, and so for dimensions up to say 1m, at frequencies below 1MHz single-point grounding is possible and in some circumstances preferable. Above 10MHz a single-point ground system is not feasible because wire and track inductance raises the ground impedance unacceptably, and stray capacitance allows unintended ground return paths to exist. For high frequencies multi-point grounding to a low inductance ground plane or shield is essential. This creates ground loops which may be susceptible to magnetic field induction, so should be avoided or specially treated in a hybrid manner when used with very sensitive circuits.

For EMC purposes, *even a circuit which is only intended to operate at low frequencies must exhibit good immunity from RF interference*. This means that those aspects of its ground layout which are exposed to the interference – essentially all external interfaces – must be designed for multi-point grounding. At the bare minimum, some low-inductance ground plate or plane must be provided at the interfaces.

Grounding principles

- All conductors have a finite impedance which increases with frequency
- Two physically separate ground points are not at the same potential unless no current flows between them
- At high frequencies there is no such thing as a single point ground

6.2 PCB layout

The way in which you design a printed circuit board makes a big difference to the overall EMC performance of the product which incorporates it. The principles outlined above must be carried through onto the PCB, particularly with regard to partitioning, interface layout and ground layout. This means that the circuit designer must exert tight control over the layout draughtsman, especially when CAD artwork is being produced. Conventional CAD layout software works on a node-by-node basis, which if allowed to will treat the entire ground system as one node, with disastrous results for the high frequency performance if left uncorrected.

Design of a PCB with multilayer technology is discussed shortly. But if you are using older technology, i.e. double- or single-sided, the safest way to lay out a PCB is to start with the ground traces, manually if necessary, then to incorporate critical signals such as HF clocks or sensitive nodes which must be routed near to their ground returns, and then to track the rest of the circuitry at will. As much information should be provided with the circuit diagram as possible, to give the layout draughtsman the necessary guidance at the beginning. These notes should include:

- physical partitioning of the functional sub-modules on the board
- positioning requirements of sensitive components and I/O ports
- marked up on the circuit diagram, the various *different* ground nodes that are being used, together with which connections to them must be regarded as critical
- where the various ground nodes may be commoned together, and where they must *not* be
- which signal tracks must be routed close to the ground tracks, plus any other constraints on the signal track routing

6.2.1 Ground layout without a ground plane

6.2.1.1 Track impedance

Careful placement of ground connections goes a long way towards reducing the noise voltages that are developed across ground impedances. But on any non-trivial printed circuit board it is impractical to eliminate circulating ground currents entirely. The other aspect of ground design is to minimize the value of the ground impedance itself.

Track impedance is dominated by inductance at frequencies higher than a few kHz (Figure 6.8). You can reduce the inductance of a connection in two ways:

- minimizing the length of the conductor, and if possible increasing its width;
- running its return path parallel and close to it.

The inductance of a PCB track is primarily a function of its length, and only secondarily a function of its width. For a single conductor of diameter d and length l inches, equation (6.2) gives the self-inductance (further equations are given in Appendix C):

$$L = 0.0051 \,.\, l \,.\, (\ln(4l/d) - 0.75) \text{ microhenries} \qquad (6.2)$$

Because of the logarithmic relationship of inductance and diameter, doubling this dimension does not produce a 50% decrease in inductance. Paralleling tracks will reduce the inductance *pro rata* provided that they are separated by enough distance to

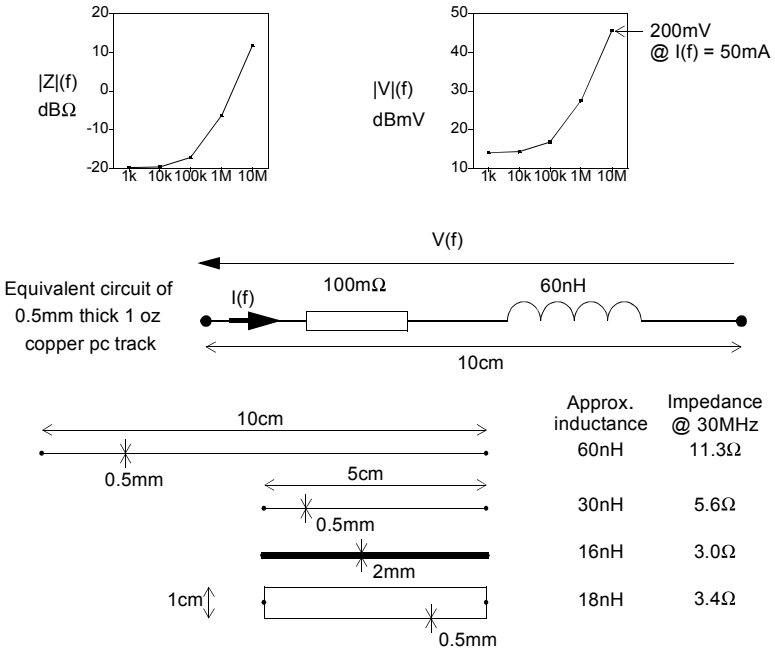


Figure 6.8 Impedance of printed circuit tracks

neutralize the effect of mutual inductance (see Figure 5.4). For narrow conductors spaced more than a centimetre apart, mutual inductance effects are negligible.

6.2.1.2 Gridded ground

The logical extension to paralleling ground tracks is to form the ground layout in a grid structure (Figure 6.9). This maximizes the number of different paths that ground return current can take and therefore minimizes the ground inductance for any given signal route. Such a structure is well suited to digital layout with multiple packages, when individual signal/return paths are too complex to define easily [64].

A wide ground track is preferred to narrow for minimum inductance, but even a narrow track linking two otherwise widely-separated points is better than none. The grid layout is best achieved by putting the grid structure down first, before the signal or power tracks are laid out. You can follow the X-Y routing system for double-sided boards, where the X-direction tracks are all laid on one side and the Y-direction tracks all on the other, provided the via hole impedance at junctions is minimized. Offensive (high di/dt) signal tracks can then be laid close to the ground tracks to keep the overall loop area small; this may call for extra ground tracking, which should be regarded as an acceptable overhead.

Ground style versus circuit type

Low frequency precision analogue circuits should not share the same ground as digital circuits, because the digital ground noise may corrupt their operation, and it is

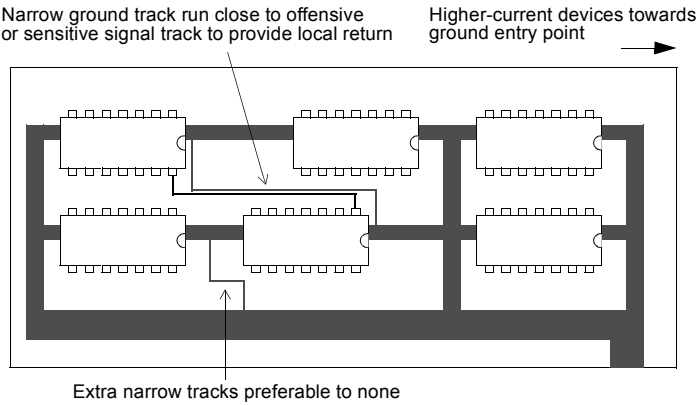


Figure 6.9 The gridded ground structure

preferable to define the ground paths accurately to prevent common impedance coupling. Provided that the bandwidth of such circuits is low then high frequency noise due to ground inductance is less of a problem. It is perfectly in order to devote separate ground areas to different classes of circuit such that each area represents a multi-point network, while the link between areas represents a single-point connection.

The one type of ground configuration that you should not use for any class of circuit is the "comb" style in which several ground spurs are run from one side of the board (Figure 6.10). Such a layout forces return currents to flow in a wide loop even if the signal track is short and direct, and contributes both to increased radiation coupling and to increased ground noise generation. The significant common ground impedance introduced between packages on the board may also cause circuit malfunction. The comb can easily be converted to a proper grid by adding bridging tracks at intervals across the spurs.

6.2.2 Using a ground plane

The limiting case of a gridded ground is when an infinite number of parallel paths are provided and the ground conductor is continuous, and it is then known as a ground plane. This is easy to realize with a multilayer board and offers the lowest possible ground path inductance. It is essential for RF circuits and digital circuits with high clock speeds, and offers the extra advantages of greater packing density and a defined characteristic impedance for all signal tracks [96]. A common four-layer configuration includes the power supply rail as a separate plane, which gives a low power-ground impedance at high frequencies.

The main EMC purpose of a ground plane is to provide a low-impedance ground and power return path to minimize induced ground noise. Shielding effects on signal tracks are secondary and are in any case nullified by the components and their lead wires, when these stand proud of the board. There is little to be gained in general from having power and ground planes outside the signal planes on four-layer boards, especially considering the extra aggravation involved in testing, diagnostics and rework. The exception will be where there is significant E-field (dv/dt) coupling to or

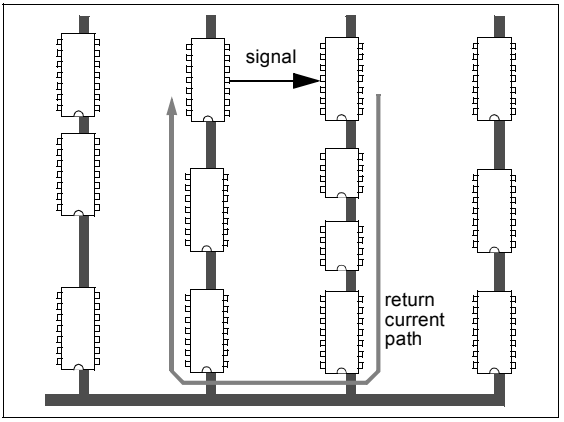


Figure 6.10 Undesirable: the comb ground structure

from the tracks which exceeds the coupling due to the components. In this case putting the power and ground planes to the outside of the board will provide an E-field shield to these tracks, but it is rare that such coupling is the dominant factor.

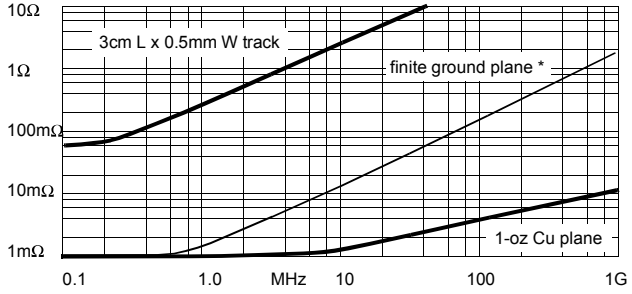


Figure 6.11 Impedance of ground plane versus track

Figure 6.11 compares the impedance between any two points (independent of spacing) on a ground plane *of infinite extent* with the equivalent impedance of a short length of track. The impedance starts to rise at higher frequencies because the skin effect increases the effective resistance of the plane, but this effect follows the square root of frequency (10dB/decade) rather than the inductive wire impedance which is directly proportional to frequency (20dB/decade). For a *finite* ground plane, the geometrical centre should see the ideal impedance while points near the outside will see much higher values as the impedance becomes markedly inductive. The corollary of this is that you should never place critical tracks or devices near the outside edge of the ground plane. An approximation for the inductance of the return path per unit length for

a given signal track in the bulk of the PCB has been given by [53] as

$$L \approx 5\,(d/w)\ \text{nH/cm} \qquad (6.3)$$

where w is the width of the plane, d is the distance between the signal track of interest and the return plane, and the length of the return path is much greater than d.

6.2.2.1 Ground plane on double-sided pcbs

A partial ground plane is also possible on double-sided pcbs. This is not achieved merely by filling all unused space with copper and connecting it to ground – since the purpose of the ground plane is to provide a low inductance ground path, it must be positioned under (or over) the tracks which need this low inductance return. At high frequencies, return current does not take the geometrically shortest return path but will flow preferentially in the neighbourhood of its signal trace. This is because such a route encloses the least area and hence has the lowest overall inductance. Thus the use of an overall ground plane ensures that the optimum return path is always available, allowing the circuit to achieve minimum inductive loop area by its own devices [125].

A partial ground plane

Figure 6.12 illustrates the development of the ground plane concept from the limiting case of two parallel identical tracks. To appreciate the factors which control inductance, remember that the total loop inductance of two parallel tracks which are carrying current in *opposite* directions (signal and return) is given by equation (6.4):

$$L = L1 + L2 - 2M \qquad (6.4)$$

where L1, L2 are the inductances of each track and
M is the mutual inductance between them

M is inversely proportional to the spacing of the tracks; if they were co-located it would be equal to L and the loop inductance would be zero. In contrast, the inductance of two identical tracks carrying current in the *same* direction is given by:

$$L = (L + M)/2 \qquad (6.5)$$

so that a closer spacing of tracks *increases* the total inductance, towards that of one track on its own. Since the ground plane is carrying the return current for signal tracks above it, it should be kept as close as possible to the tracks to keep the loop inductance to a minimum. For a continuous ground plane this is set only by the thickness of the intervening board laminate.

6.2.2.2 Ground planes for low cost boards

The ground plane approach is well established for high-value, high-speed digital circuits for which multilayer PCBs are the norm. What is sometimes less appreciated is that it is directly relevant to low-cost analogue circuits as well. Adding a ground plane to a cheap single-sided analogue board is often the single most cost effective change for improving EMC.

Despite the encroachment of digital technology, analogue circuits are still widely used for simple, cost-sensitive applications, particularly in the consumer market. Examples are security sensors, timers and residual current detectors. For these products, cost is the driving factor and both component count and assembly time must be kept to a minimum. Volumes may be high and assembly is often done in low labour cost areas, so that through hole insertion is still economic by comparison with surface

mounting. PCB technology may be single sided on PRBF, if double-sided PTH on fibreglass represents too high a cost. These products typically are unconcerned with RF emissions, and historically EMC has never been considered in their design. Under the EMC Directive though, RF and transient immunity is important, even as it is for reliability of operation. This immunity can frequently best be achieved by implementing a ground plane on the board.

Adding a grounded copper layer

A plane can be implemented retrospectively by simply adding a top copper layer to a single-sided board design, without changing the original layout (Figure 6.13). The top copper etch pattern is limited to clearance holes around each component lead – the original pad pattern in reverse. The top layer is connected by a through wire or eyelet to the 0V track on the underside. Note that it *must* be connected at least at one point – a floating copper layer is worse than useless, since it merely increases capacitive coupling between the enclosure or outside, and the circuit.

This construction does not make the plane behave in the optimum fashion, where

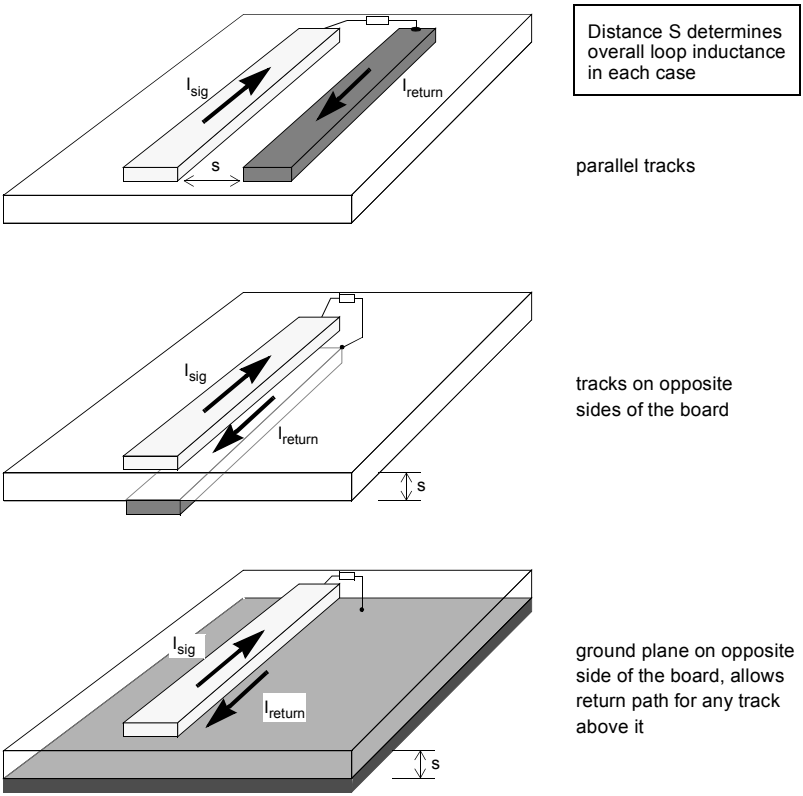


Figure 6.12 Return current paths

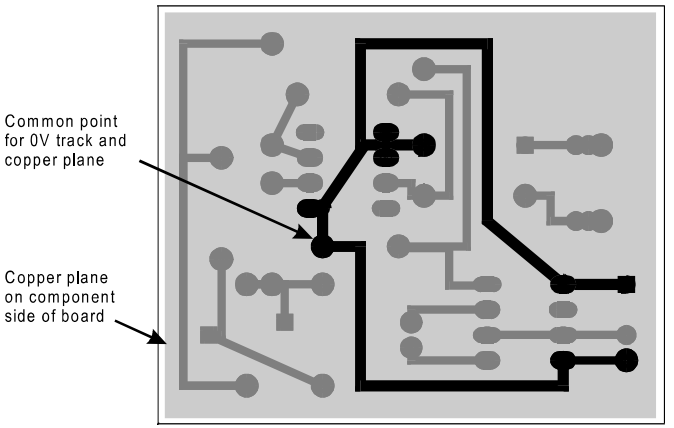


Figure 6.13 Simple copper layer added to a single sided PCB

current flowing within it minimizes magnetic coupling to the circuits – the plane ensuring minimum possible loop area for each circuit path. It cannot do this as long as the 0V returns for each and every circuit are not connected to it. It does, though, act as a partial electric field screen, reducing the effect of capacitive coupling to the tracks. This is most effective for higher-impedance circuits where capacitive coupling is the prime threat. It will also reduce differential voltages across the length and width of the PCB, induced either magnetically or electrically. You can think of it as creating a "quasi-equipotential" area for RF interference over the region of the circuit.

Its effect is maximized if the 0V connection is made in the vicinity of the most sensitive part of the circuit, and if this part of the circuit is located away from the edges of the plane. The purpose of this is to ensure that the remaining interference-induced voltage differences between the plane and the circuit tracks are lowest in the most critical area.

Making the copper layer into a ground plane

If some cost increase is permissible and a double sided PTH board can be used, then it is preferable to transfer all 0V current onto the plane layer, which then becomes a true ground plane. All circuit 0V connections are returned to the ground plane via PTH pads and the original 0V track is redundant. In a revised or new layout, the 0V track is omitted entirely, possibly allowing a tighter component and tracking density. Figure 6.14 shows this transition.

This will have the effect not only of reducing capacitive coupling to the circuit, as discussed above, but also magnetic coupling, since all circuit paths now inherently have the least loop area. As long as sensitive circuits are located well inboard of the edges of the plane they will enjoy the greatest protection. Fringing fields at the edge of a ground plane increase its effective inductance, and magnetic coupling to the circuit tracks worsens.

It is not essential that the ground plane area covers the whole of the board, or even all of the tracks, as long as it does cover the tracks and circuit areas which are critical for immunity.

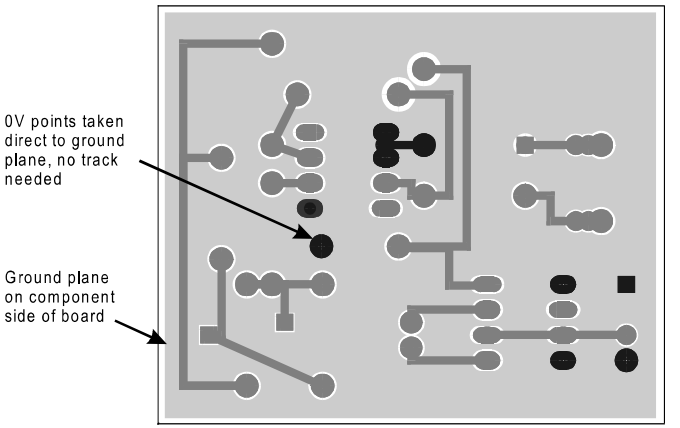


Figure 6.14 Taking all 0V connections to the ground plane

6.2.2.3 *Breaks in the ground plane*

What *is* essential is that the plane remains unbroken in the direction of current flow. Any deviations from an unbroken plane effectively increase the loop area and hence the inductance. If breaks are necessary it is preferable to include a small bridging track next to a critical signal track to link two adjacent areas of plane (Figure 6.15). A slot in the

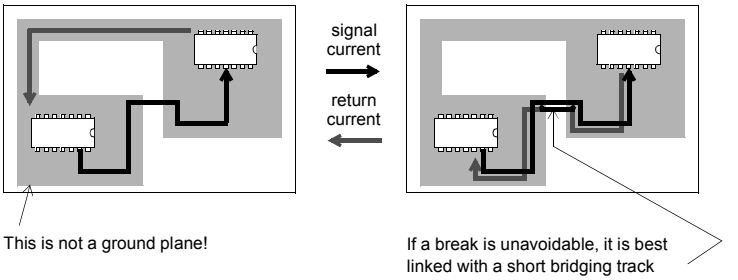


Figure 6.15 A broken ground plane

ground plane will nullify the beneficial effect of the plane if it interrupts the current, however narrow it is. This is why a multilayer construction with an unbroken internal ground plane is the easiest to design, especially for fast logic which requires a closely controlled track characteristic impedance. Where double-sided board with a partial ground plane is used, bridging tracks as shown in Figure 6.15 should accompany all critical tracks, especially those which carry sensitive signals a significant way across the board.

The most typical source of ground plane breaks is a slot due to a row of through hole connections, such as required by a SIL or DIL IC package (Figure 6.16). The effect of

such a slot is worst for the tracks in its centre, since the return current is diverted all the way to the edge of the slot. This translates to greater ground inductance and an unnecessary increase in induced interference voltage in this area of the board's ground network. If the slot straddles a particularly sensitive circuit then worsened immunity will result, even though you have gone to the trouble of putting a ground plane onto the board. It is a simple matter to ensure that each pair of holes is bridged by a thin copper trace – most etching technology is capable of this degree of resolution – it adds nothing to the production cost and can give several dB improvement in immunity in the best case.

The inductance of a slot in the plane can be modelled as a length of short circuited transmission line. [53] gives an approximation for this inductance as shown in Figure 6.16. It is instructive to compare the order of magnitude of values this gives versus that obtained from equation (6.3): a 3cm track over an unbroken ground plane of width 5cm, 0.8mm above it, gives 0.24nH return path inductance. A 3cm long slot under this track of width 1mm, with 4cm of board either side (i.e. board is 8cm x 5cm), will increase this inductance to 2.6nH.

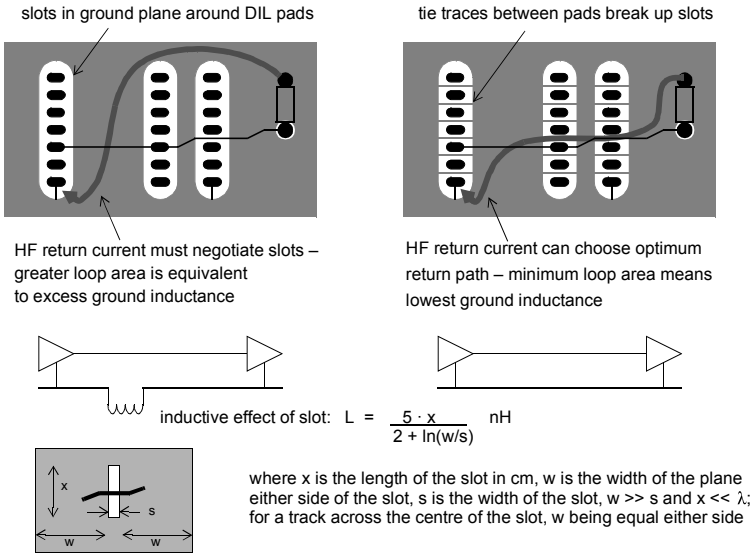


Figure 6.16 Dealing with slots at DIL pinouts

6.2.2.4 Multilayer boards

All of the foregoing, with respect to ground plane construction in the plane of the board, applies to multilayer technology. Additionally, the order of the layers becomes significant when high-speed circuits are implemented on multilayer boards.

In these configurations, the most important aspect is that every critical signal layer should be adjacent to a ground or power plane layer. Also, power and ground planes should be on adjacent layers to take advantage of the interlayer capacitance for high frequency decoupling. Critical tracks should be routed adjacent to ground rather than power planes, for preference. Such tracks (typically carrying high di/dt signals such as

clocks) should also not jump through vias from one ground reference layer to another, unless the ground layers are tied together with vias at that point.

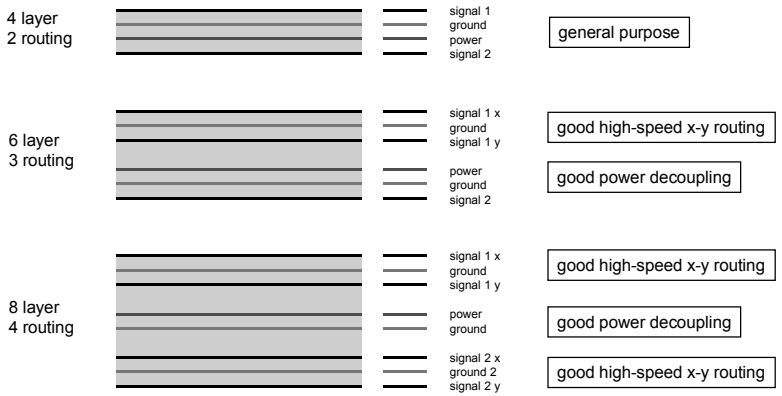


Figure 6.17 Layer stacking on a multilayer board

Figure 6.17 illustrates possible (not by any means mandatory) layer configurations for various layer multiples. If x- and y-orientation layers share a common ground plane this allows both constant impedance and minimum separation from the plane layer for high speed routing. High density designs can use more than one set of x-plane-y layers as shown in the 8-layer example above. If high-speed tracks can be distinguished from non-critical ones, the non-critical tracks can be run on a separate layer adjacent to a second plane (marked signal 2 in the 6-layer example). In all cases, putting power and ground planes on adjacent inner layers gives maximum distributed decoupling capacitance between them.

An extra ground plane on the outside layer of a board can be helpful when capacitive coupling, such as from large-area components carrying HF voltages, is significant. [108] describes a situation in which a microprocessor heatsink was electrically bonded to a ground plane on the board, and the inductance of the bond connection was noticeably more significant when the ground plane was on an inside layer than when it was outside. This resulted in several dB increase in emissions in the frequency range around 1GHz. If your circuit has very wideband EMC aspects then such an approach is worthwhile, but for less demanding applications the physical disadvantages associated with outside plane layers tend to reduce their attraction.

6.2.2.5 Crosstalk

A ground plane is a useful tool to combat crosstalk, which is strictly speaking an internal EMC phenomenon. Crosstalk coupling between two tracks is mediated via inductive, capacitive and common ground impedance routes, usually a combination of all three (Figure 6.18). The effect of the ground plane is to significantly reduce the common ground impedance Z_G, by between 40–70dB, in the case of an infinite ground plane compared to a narrow track.

The ground plane may also reduce mutual inductance coupling (M_{12}) by ensuring

that the coupled current loops are not co-planar. Capacitive coupling between the tracks will not be directly affected by the ground plane, but the lowered impedance of the line (equivalent to saying that C_{1G} and C_{2G} have been increased) will reduce capacitive crosstalk amplitude.

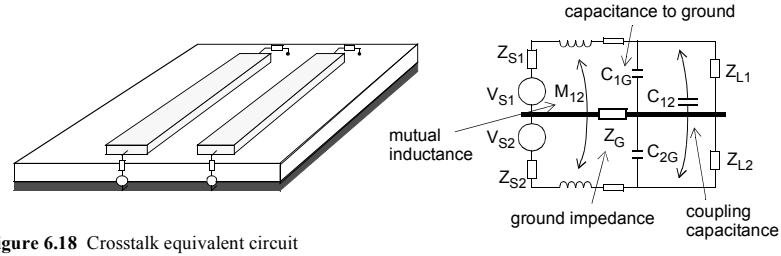


Figure 6.18 Crosstalk equivalent circuit

Crosstalk problems, or internal interference coupling, are by no means limited to digital circuits, although these tend to make the problem most visible. A common threat to the immunity of analogue circuits is crosstalk from other circuits carrying high interference currents or voltages. Mains-borne interference is the most widespread, but RF or transient interference induced onto signal cables can also be significant. You should always be on the lookout to minimize crosstalk from these sources by ensuring the maximum separation (hence minimum M_{12} and C_{12}) between the circuits; or by interposing electric field screening between them, if C_{12} is dominant; or by implementing a ground plane, to minimize Z_G and maximize C_{1G} and C_{2G}.

6.2.2.6 The advantage of surface mount

Surface mount technology (SMT) offers smaller component sizes and therefore should give a reduction in interference coupling, since the overall circuit loop area can be smaller. This is in fact the case, but to take full advantage of SMT a multilayer board construction with ground plane is necessary. There is a slight improvement when a double-sided board is re-laid out to take SMT components, which is mainly due to shrinking the overall board size and reducing the length of individual tracks. The predominant coupling is from tracks rather than components.

But when a multilayer board is used, the circuit loop area is reduced to the track length times the track-to-ground plane height. Now, the dominant coupling is from the extra area introduced by the component leadouts. The reduction in this area afforded by SMT components is therefore worthwhile. For EMC purposes, SMT and multilayer groundplane construction complement each other.

A further advantage of surface mount is that, rather than taking advantage of the component size reduction to pack more functions into a given board area, you can reduce the board area needed for a given function. This allows you more room to define quiet I/O areas and to fit suppression and filtering components when these prove to be needed.

6.2.3 Configuring I/O and circuit grounds

6.2.3.1 The interface ground structure

Decoupling and shielding techniques to reduce common mode currents appearing on cables both require a “clean” ground area, not contaminated by internally generated

noise. This forms the low transfer impedance grounding structure, as per section 6.1.2.2, for the cable interface. *Filtering at high frequencies is next to useless without such a ground.* Unless you consider this as part of the layout specification early in the design phase, such a ground will not be available. Provide an interface ground by grouping all I/O leads in one area and connecting their shields and decoupling capacitors to a separate ground plane in this area. The interface ground can be a separate area of the pcb [100] as shown in Figure 6.19, or it can be a metal plate on which the connectors are mounted. The external ground (which may be only the mains safety earth) and the metal or metallized case, if one is used, are connected here as well, via a low-inductance link. Figure 6.20 shows a typical arrangement for a product with digital, analogue and interface sections.

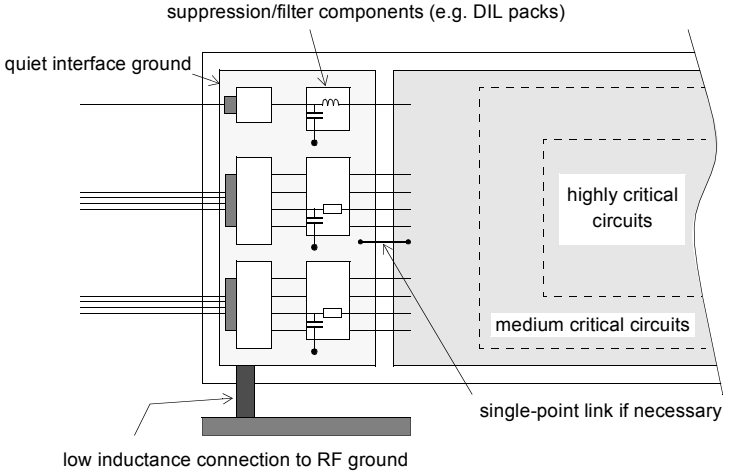


Figure 6.19 The interface ground on a PCB

This clean ground must only connect to the internal logic ground at one point. This prevents noise currents flowing through the interface ground plane and "contaminating" it. No other connections to the interface ground are allowed. As well as preventing common mode emissions, this layout also shunts incoming interference currents (transient or RF) to the interface ground and prevents them flowing through susceptible circuitry. If for other reasons it is essential to have leads interfacing with the unit or pcb at different places, you should still arrange to couple them all to a separate ground structure through which no circuit currents are flowing. In this case a chassis plate is mandatory.

These requirements can be ensured by devoting an area along one edge of the pcb to the interface ground plane, including the I/O resistive, capacitive and inductive filtering and suppression elements on it (but no other circuits), and separating the circuit 0V from it either absolutely, or by a single connecting link. RF-critical circuitry should be widely separated from the I/O area.

For ESD protection the circuit ground *must* be referenced to the chassis ground. This can easily be done by using a plated-through hole on the ground track and a metallic standoff spacer. If there has to be DC isolation between the two grounds at this point, use a 10–100nF RF (ceramic or polyester) capacitor. You can provide a clean I/O

ground on plug-in rack mounting cards by using wiping finger style contacts to connect this ground track directly to the chassis.

6.2.3.2 Separate circuit grounds

There are two schools of thought as to maintaining separate 0V references for different operational parts of a circuit. The first (see Figure 6.20) says that you should never extend a digital ground plane over an analogue section of the pcb as this will couple digital noise into the analogue circuitry. A single-point connection between digital and analogue grounds can be made at the system's analogue-to-digital converter. It is very important in this arrangement *not* to connect the digital circuitry separately to an external ground [43]. If you do this, extra current paths are set up which allow digital circuit noise to circulate in the clean ground.

Interfaces directly to the digital circuitry (for instance, to a port input or output) should be buffered so that they do not need to be referenced to the digital 0V. The best interface is an opto-isolator or relay, but this is of course expensive. When you can't afford isolation, a separate buffer IC which can be referenced to the I/O ground is preferable; otherwise, buffer the port with a series resistor or choke and decouple the line *at the board interface* (not somewhere in the middle of the board) with a capacitor and/or a transient suppressor to the clean ground. More is said about I/O filtering in section 8.2.4.

Notice how the system partitioning, discussed in section 6.1.1, is essential to allow you to group the I/O leads together and away from the noisy or susceptible sections. Also the mains cable, as far as EMC is concerned, is another I/O cable. Assuming that you are using a block mains filter, fit this to the "clean" ground reference plate directly.

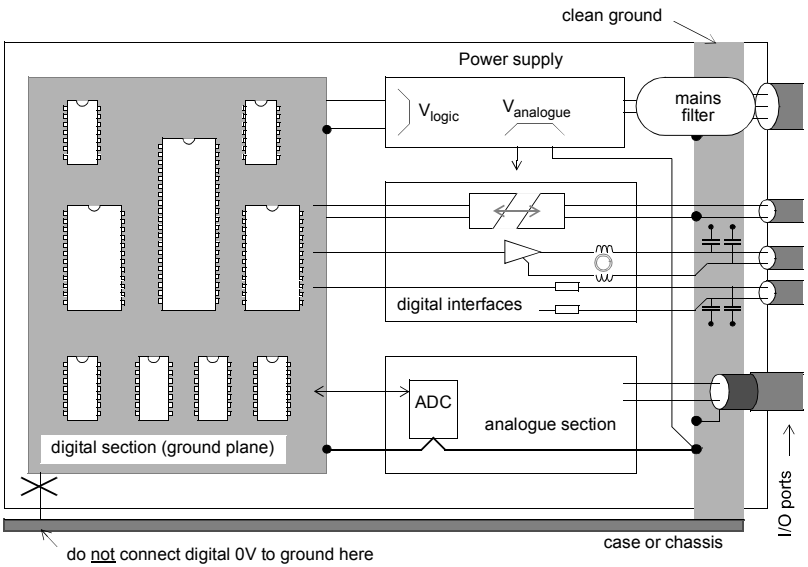


Figure 6.20 Multiple ground areas

6.2.3.3 Solid universal circuit ground

The second school of thought, diametrically opposed to the first, says that all parts of the circuit should be referenced to a single, unbroken 0V reference plane. If this approach is chosen, it is crucial that a high-quality, low impedance plane is used; any 0V tracks would be unacceptable. The effect of this construction is that all signal and power return currents flow in the plane, so that common impedance coupling between different parts of the circuit is unavoidable, and it is only careful layout and the low impedance of the plane which mitigates this coupling to an acceptable extent. Mixing sensitive analogue with high-speed digital circuits on the same board is risky, although with careful partitioning it can still be successful.

The advantage is that there is no opportunity for voltage differences to arise, as a result of interference or for any other reason, between different 0V nodes, since there are no different nodes. The tricky question of where exactly to place the separation boundary is avoided. So is the hazard of 0V differentials, potentially a problem with the first approach. If the board is mounted on a metal chassis, the ground plane can be tied to this chassis at multiple points, and this improves the RF "solidity" of the whole assembly, so that induced interference currents will inherently cause a lower level of internal disturbance.

In the end, you are free to use either approach, as long as the implications of the decision are appreciated. Segregation of grounds removes the threat of cross-interference between different parts of the circuit but requires you to think carefully about placing the boundaries and defining the circuit's relationship to the chassis; with complex multi-sectioned circuits it can be difficult to administer. Unifying the ground makes it easy to control the ground design but increases the risk of one part of the circuit interfering with another.

6.2.3.4 Cable screen connection

Input/output decoupling is of critical importance with either circuit grounding regime because it is vital to keep cable common mode interference currents to a minimum. As an example, consider Figure 6.21. If the cable screen or return is taken to the wrong point with respect to the output driver decoupling capacitor, the high-speed current transitions on the driver supply (which flow through the decoupling capacitor traces) generate common mode voltage noise V_N which is delivered to the cable and which appears as a radiated emission. Cable screens must always be taken to a point at which there is the minimum noise with respect to the system's ground reference. This means that the dedicated interface ground area must always be implemented and all cable connections either taken directly to it (screens) or via it (signal and power lines).

6.2.4 Rules for PCB layout

Because it is impractical to optimize the ground layout for all individual signal circuits, you have to concentrate on those which are the greatest threat. These are the ones which carry the highest di/dt most frequently, especially clock lines and data bus lines, and square-wave oscillators at high powers, especially in switching power supplies. From the point of view of susceptibility, sensitive circuits – particularly edge-triggered inputs, clocked systems, and precision analogue amplifiers – must be similarly treated. Once these circuits have been identified and partitioned you can concentrate on dealing with their loop inductance and ground coupling. The aim should be to ensure that circulating ground noise currents do not get the opportunity to enter or leave the system.

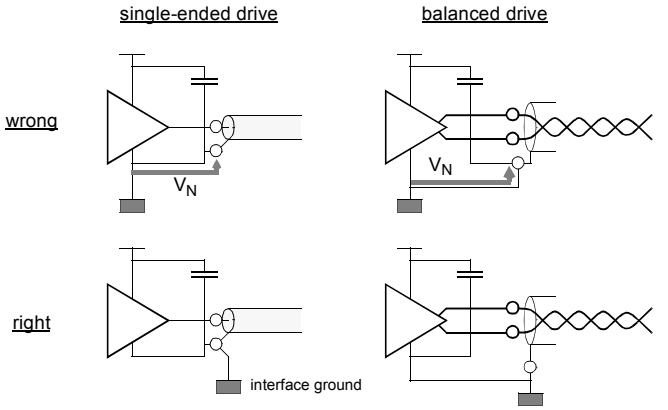


Figure 6.21 The point of connection of I/O cable screens

Grounding rules

- identify the circuits of high di/dt (for emissions) –
  clocks, bus buffers/drivers, high-power oscillators
- identify sensitive circuits (for susceptibility) –
  low-level analogue, fast digital data
- minimize their ground inductance by –
  minimizing the length and enclosed area
  implementing a ground plane
  keeping critical circuits away from the edge of the plane
- ensure that internal and external ground noise cannot couple out of or into the system: incorporate a clean interface ground
- partition the system to control common mode current flow between sections
- create, maintain and enforce a ground map