Deliverable 11: Place and Route

Submit electronically to Canvas no later than 6:00pm on December 6, 2019

Name: _____ NetID: _____

Important: This is group work—only one Canvas submission per group is required! Upload all results for this deliverable via a *single* zip-file that is named "D10-group-⟨NUMBER⟩-⟨BLOCK⟩.zip",where ⟨NUMBER⟩ is your group's number and ⟨BLOCK⟩ is the three-letter abbreviation of your block (e.g., EXA). Include the entire synthesizer simulator along with a description of how to use it so that we can reproduce your results. It is important that all students try to understand all of the work of the entire deliverable and not just parts of it.

Do not forget: You must specify the names of everyone who contributed to this submission as well as all the resources used (websites, books, documents, papers, etc.). Failing to specify who contributed to the submission or the used resources will result in a 20% penalty. Late deliverables will receive a 20% penalty for every day late (including submissions made after 6:00pm); deliverables more than 3 days late will not be accepted.

If you follow the submission rules, then you get 5 bonus points.

Task	**Maximum Points**	**Points**
Deliverable	100	
Follow submission rules	5	
Total	**100 (+5pts bonus)**	

Deliverable (100pts): Place and Route

This deliverable has four goals: (i) Ensure that your MATLAB model 100% matches your Verilog code (in case you have not done so yet), (ii) synthesize your Verilog code with Synopsys DC to generate an AT-plot, (iii) perform place-and-route using Cadence Innovus, and (iv) perform a post-layout simulation with your design from Candence Innovus in ModelSim. The following tasks should be completed:

Make MATLAB Match Verilog (20pts) If you have not done so already, make your MATLAB golden model match 100% your Verilog code. Perform extensive tests and include proof in your report of how many tests you have carried out. We want to see how many and what kind of test vectors you have tested with your design.

AT-Diagram with Synopsys DC (20pts) If you have not done so already, push your fully functional Verilog code through Synopsys DC. Perform a sweep in terms of the area and clock period by sweeping the clock constraint; try values between 10ns and 120ns (e.g., in steps of 10ns). Note that no manual labor is required as you can script it. Include a figure in your report showing the area (A) in um^2 and delay (D) in nanoseconds for all synthesized designs (no logarithmic axes required). Make sure that you report the actual achieved critical path and not the specified constraint! This plot will help us understand what the delay limit of your block is and how much area the entire synthesizer will consume.

Perform Place and Route (50pts) Use Cadence Innovus to place-and-route your synthesized Verilog code. Try to target the clock constraint from the previous task that minimizes the AT product. Include the following items in your report:

- Final area and delay obtained at the end of place and route
- Illustration of where the critical path is in your design after place and route
- Proof that your design has no hold violations
- High-resolution screenshot of the final layout

Perform a Post-Layout Simulation (10pts) Perform a post-layout simulation in ModelSim with the design obtained from Cadence Innovus. Make sure that the simulation passes for the same delay that Candece Innovus reports is achievable. Note that we will provide you with a script for this simulation as soon as you think your group is ready for this step.