CSE 404: Digital System Design Sessional

4-Bit PC Instructions Implementation
Block Diagram

Section: A1

Group: 4

Group Members:
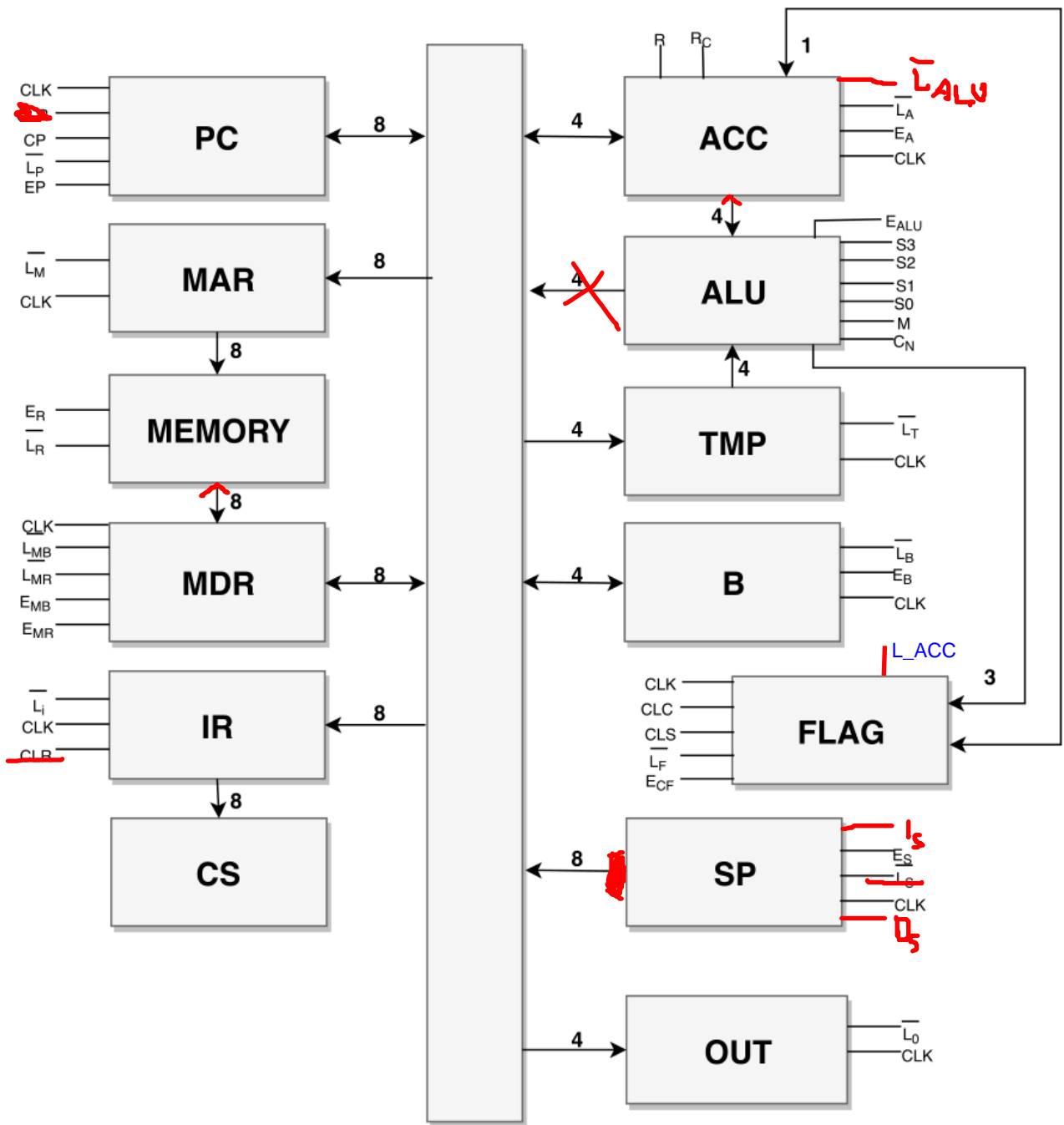
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PC — CLK, [handwritten red], CP, $\overline{L_P}$, EP

8

MAR — $\overline{L_M}$, CLK

8

MEMORY — E_R, $\overline{L_R}$

8

MDR — CLK, L_{MB}, L_{MR}, E_{MB}, E_{MR}

8

IR — $\overline{L_i}$, CLK, CLR

8

CS

ACC — R, R_C, 1, $\overline{L_A}$, E_A, CLK — $\overline{L_{ALU}}$

4

4

ALU — E_{ALU}, S3, S2, S1, S0, M, C_N

4 ✕

4

TMP — $\overline{L_T}$, CLK

4

B — $\overline{L_B}$, E_B, CLK

FLAG — CLK, CLC, CLS, $\overline{L_F}$, E_{CF} — L_ACC, 3

SP — I_S, E_S, L_S, CLK, D_S

8

OUT — $\overline{L_0}$, CLK

4

Instructions:

CLR	Clear Register
CLK	Clock Pulse
Cp	Increment PC
$\overline{L_P}$	Load PC from bus
Ep	Output PC from bus
$\overline{L_M}$	Load MAR from bus
E_R	Output RAM[MAR] to MDR line
$\overline{L_R}$	Load RAM[MAR] from MDR
$\overline{L_{MB}}$	Load MDR from bus
$\overline{L_{MR}}$	Load MDR from RAM
E_{MB}	Output MDR to bus
E_{MR}	Output MDR to RAM
$\overline{L_I}$	Load IR from bus
$\overline{L_A}$	Load ACC from bus
E_A	Output ACC to bus
R	Rotate Left
R_C	Rotate with Carry
E_{ALU}	Output ALU value to bus
S0, S1, S2, S3, C_{IN}, M	ALU mode selection
$\overline{L_T}$	Load Temp from bus
$\overline{L_B}$	Load Reg. B from bus
E_A	Output Reg. B to bus
CLC	Clear Carry flag
CLS	Clear Sign flag
$\overline{L_F}$	Load flag from ALU
E_{CF}	Output Carry flag
E_S	Output SP to bus
$\overline{L_S}$	Load SP from bus
$\overline{L_0}$	Load Output Reg from bus