IC Name	IC No
Quad D-FF with Tristate Output	74LS173
4-bit Buffer with Tristate Output	74LS244
1-bit Quad BUS Buffer with Tristate Output	74LS126
4-bit Bidirectional Universal Shift Register	74LS194
4-bit Synchronous Up/Down Counter	74LS193
Universal Counter Digital Primitive	COUNTER_8
3:8 Decoder	74LS138
1:4 MUX	74LS153
1:2 MUX	74LS157
HEX Buffer with Tristate Output	74LS366
2-input XOR	74LS386
EPROM	2732
RAM	6116
2-input OR	74LS32
2-input AND	74LS08
HEX Inverter (NOT)	74LS04
2-input NAND	74LS00
Arithmetic Logic Unit_IC	74LS181

Table 0.1: IC Information

Carry	Operation	M	C_N	$S3$	$S2$	$S1$	$S0$
0	ADD	0	1	1	0	0	1
0	ADC	0	1	1	0	0	1
0	SUB	0	0	0	1	1	0
0	SBB	0	0	0	1	1	0
0	INC	0	0	0	0	0	0
0	AND	1	X	1	0	1	1
0	NOT	1	X	0	0	0	0
0	XOR	1	X	0	1	1	0
1	ADD	0	1	1	0	0	1
1	ADC	0	0	1	0	0	1
1	SUB	0	0	0	1	1	0
1	SBB	0	1	1	0	0	1
1	INC	0	0	0	0	0	0
1	AND	1	X	1	0	1	1
1	NOT	1	X	0	0	0	0
1	XOR	1	X	0	1	1	0

Table 0.2: Control Signals of Arithmetic Logic Unit_IC Operations

S1	S0	SR	SL	Operation
0	1	0	X	Shift Left [LSB padded with 0]
0	1	1	X	Shift Left [LSB padded with 1]
1	0	X	0	Shift Right [MSB padded with 0]
1	0	X	1	Shift Right [MSB padded with 0]

Table 0.3: Table for IC 74LS194