CSE 404: Digital System Design Sessional

4-Bit PC Instructions Implementation

Block Diagram

Section: A1

Group: 4

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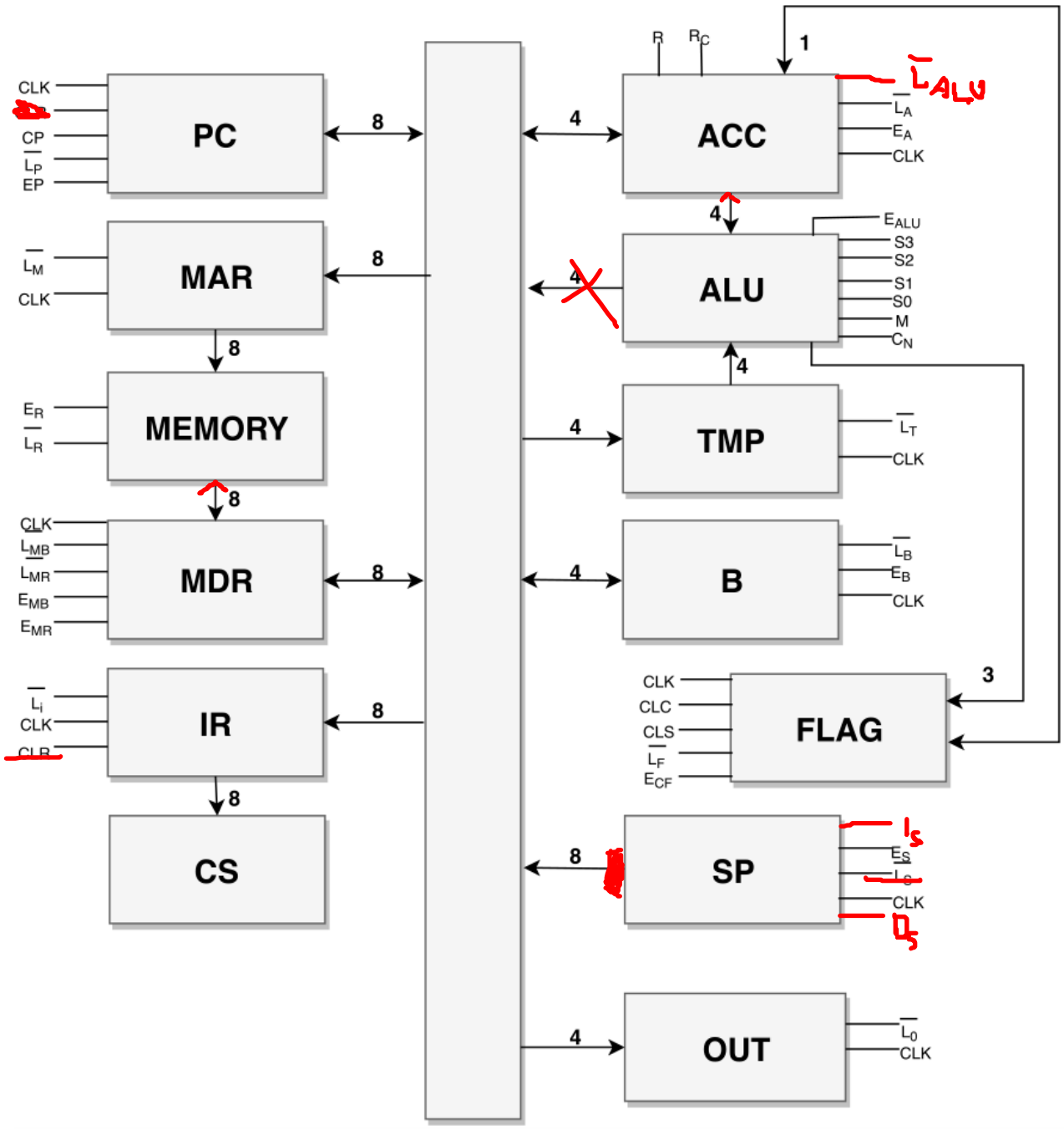
PC
CLK
CP
LP
EP
8
MAR
LM
CLK
8
MEMORY
ER
LR
8
MDR
CLK
LMB
LMR
EMB
EMR
8
IR
Li
CLK
CLR
8
CS
4
ACC
R
RC
1
LA
EA
CLK
4
ALU
EALU
S3
S2
S1
S0
M
CN
4
4
TMP
LT
CLK
4
B
LB
EB
CLK
CLK
CLC
CLS
LF
ECF
FLAG
3
8
SP
ES
LS
CLK
4
OUT
L0
CLK

Instructions:

CLR	Clear Register
CLK	Clock Pulse
Cp	Increment PC
$\overline{L_P}$	Load PC from bus
Ep	Output PC from bus
$\overline{L_M}$	Load MAR from bus
E_R	Output RAM[MAR] to MDR line
$\overline{L_R}$	Load RAM[MAR] from MDR
$\overline{L_{MB}}$	Load MDR from bus
$\overline{L_{MR}}$	Load MDR from RAM
E_{MB}	Output MDR to bus
E_{MR}	Output MDR to RAM
$\overline{L_I}$	Load IR from bus
$\overline{L_A}$	Load ACC from bus
E_A	Output ACC to bus
R	Rotate Left
R_C	Rotate with Carry
E_{ALU}	Output ALU value to bus
S0, S1, S2, S3, C_{IN}, M	ALU mode selection
$\overline{L_T}$	Load Temp from bus
$\overline{L_B}$	Load Reg. B from bus
E_A	Output Reg. B to bus
CLC	Clear Carry flag
CLS	Clear Sign flag
$\overline{L_F}$	Load flag from ALU
E_{CF}	Output Carry flag
E_S	Output SP to bus
$\overline{L_S}$	Load SP from bus
$\overline{L_0}$	Load Output Reg from bus