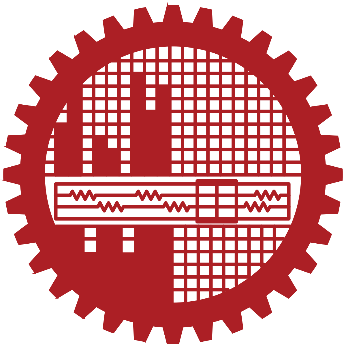
**CSE 404: Digital System Design Sessional**

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**4-Bit PC Instructions Implementation**

**Block Diagram**

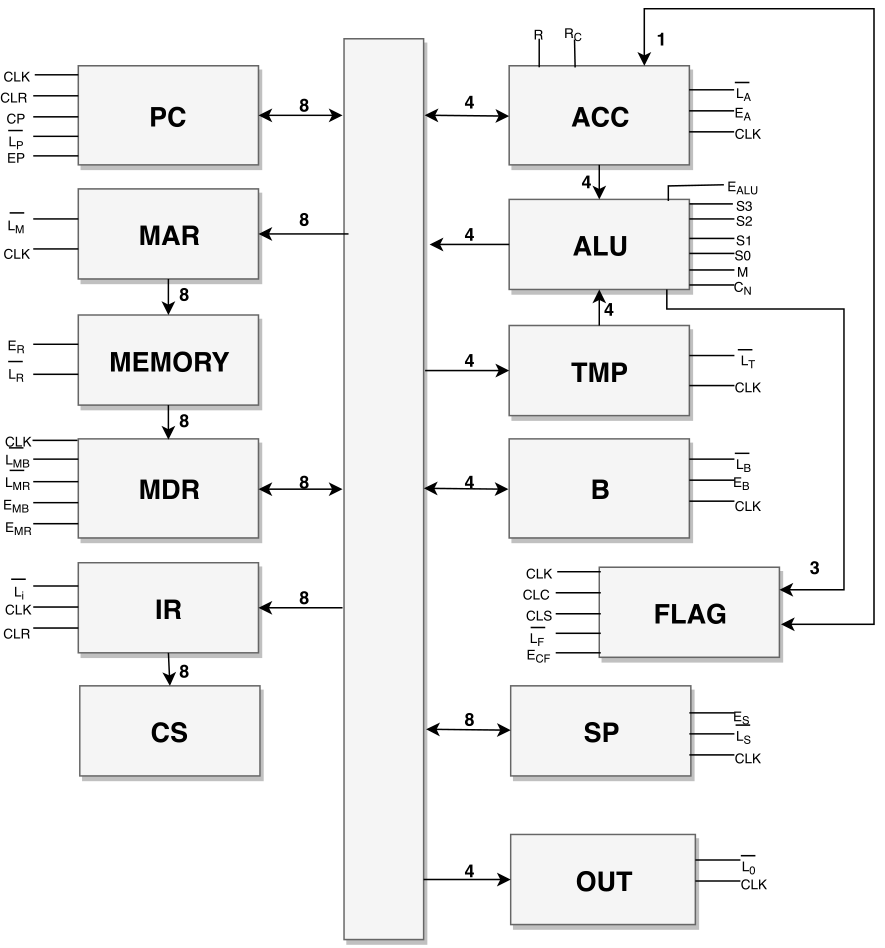
**Section:** A1 **Group Members:**

**Group:** 41405009

1405013

1405014 1405015

1405016

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|  |  |
| --- | --- |
| CLR | Clear Register |
| CLK | Clock Pulse |
| Cp | Increment PC |
|  | Load PC from bus |
| Ep | Output PC from bus |
|  | Load MAR from bus |
| ER | Output RAM[MAR] to MDR line |
|  | Load RAM[MAR] from MDR |
|  | Load MDR from bus |
|  | Load MDR from RAM |
| EMB | Output MDR to bus |
| EMR | Output MDR to RAM |
|  | Load IR from bus |
|  | Load ACC from bus |
| EA | Output ACC to bus |
| R | Rotate Left |
| RC | Rotate with Carry |
| EALU | Output ALU value to bus |
| S0, S1, S2, S3, CIN, M | ALU mode selection |
|  | Load Temp from bus |
|  | Load Reg. B from bus |
| EA | Output Reg. B to bus |
| CLC | Clear Carry flag |
| CLS | Clear Sign flag |
|  | Load flag from ALU |
| ECF | Output Carry flag |
| ES | Output SP to bus |
|  | Load SP from bus |
|  | Load Output Reg from bus |

**Instructions:**