

DSP Project

The reg & MUX module:

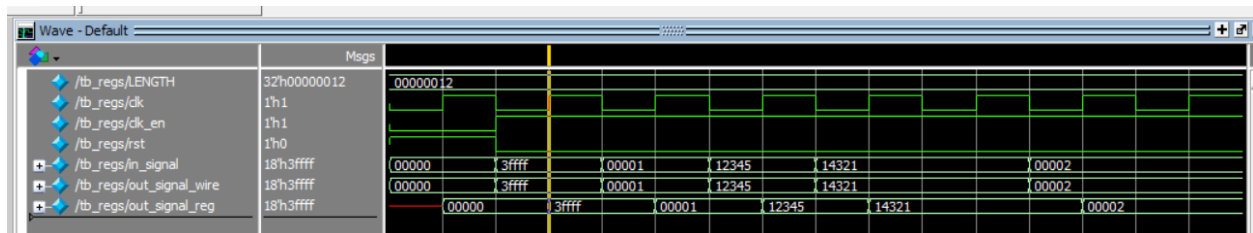
```
D:\Digital design diploma\Projects\Project1\regs.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v x regs_tb.v x regs.v x VM_FSM.v x D_flipflop.v x VM_FSM_t
1 module regs(clk,clk_en,rst,in_signal,out_signal);
2   parameter USE_REG = 0;
3   parameter LENGTH = 18;
4   parameter RST_MODE = "SYNC";
5   input wire clk,clk_en;
6   input wire rst;
7   input wire [LENGTH-1:0] in_signal;
8   output reg [LENGTH-1:0] out_signal;
9
10  generate
11    if (USE_REG == 1 && RST_MODE == "ASYNC") begin
12      always @(posedge clk or posedge rst) begin
13        if (rst)
14          out_signal <= 0;
15        else if (clk_en)
16          out_signal <= in_signal;
17      end
18    end else if (USE_REG == 1 && RST_MODE == "SYNC") begin
19      always @(posedge clk) begin
20        if (rst)
21          out_signal <= 0;
22        else if (clk_en)
23          out_signal <= in_signal;
24      end
25    end else begin
26      always @(*) begin
27        out_signal = in_signal;
28      end
29    end
30  endgenerate
31
32 endmodule
33
```

The testbench:

```
D:\Digital design diploma\Projects\Project1\regs_tb.v - Sublime Text (UNREGISTERED)
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1 module tb_regs;
2
3     localparam LENGTH = 18;
4     reg clk;
5     reg clk_en;
6     reg rst;
7     reg [LENGTH-1:0] in_signal;
8     wire [LENGTH-1:0] out_signal_wire;
9     wire [LENGTH-1:0] out_signal_reg;
10    initial begin
11        clk = 0;
12        forever #5 clk = ~clk;
13    end
14
15    regs #(.USE_REG(0),.LENGTH(LENGTH),
16        .RST_MODE("SYNC")) uut_wire (.clk(clk),.clk_en(clk_en),.rst(rst),.in_signal(in_signal),
17        .out_signal(out_signal_wire)
18    );
19    regs #(.USE_REG(1),.LENGTH(LENGTH),
20        .RST_MODE("SYNC")) uut_reg (.clk(clk),.clk_en(clk_en),.rst(rst),.in_signal(in_signal),
21        .out_signal(out_signal_reg)
22    );
23
24    initial begin
25        clk_en = 0;
26        rst = 0;
27        in_signal = 0;
28        rst = 1;
29        #10;
30        rst = 0;
31        in_signal = 18'h3FFFF;
32        clk_en = 1;
33        #10;
34        in_signal = 18'h00001;
35        #10;
36        in_signal = 18'h12345;
37        #10;
38        in_signal = 18'h54321;
39        clk_en = 1;
40        #20;
41        in_signal = 18'h00002;
42        #10;
43        $stop;
44    end
45 endmodule
46
```

Waveform:



Main project code:

```
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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM.v x D_flipflop.v x VM_FSM_tb.v x RAM_S.v x LFSR_tb.v x

1 module DSP(A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,clk,OPMODE,
2   CEA,CEB,CEC,CED,CECARRYIN,CEM,CEOPMODE,CEP,
3   RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP,
4   BCOUT,PCIN,BCIN,PCOUT);
5   parameter A0REG = 0;
6   parameter A1REG = 1;
7   parameter B0REG = 0;
8   parameter B1REG = 1;
9   parameter CREG = 1;
10  parameter DREG=1;
11  parameter MREG = 1;
12  parameter PREG = 1;
13  parameter CARRYINREG = 1;
14  parameter CARRYOUTREG = 1;
15  parameter OPMODEREG = 1;
16  parameter CARRYINSEL = "OPMODE5"; //string CARRYIN or OPMODE5 else out -> 0
17  parameter B_INPUT = "DIRECT"; //B input (attribute = DIRECT) or the cascaded input(BCIN) from the previous DSP48A1 slice (attribute = CASCADE).
18  parameter RSTTYPE = "SYNC"; //send in instantiation
19
20  input [17:0]A,B,D;
21  input [47:0]C,PCIN;
22  input CARRYIN,clk,CEA,CEB,CEC,CED,CEM,CEP,CECARRYIN,CEOPMODE;
23  input [17:0]BCIN;
24  input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
25  input [7:0]OPMODE;
26
27  output [47:0]P;
28  output [35:0]M;
29  output [17:0]BCOUT;
30  output [47:0]PCOUT;
31  output CARRYOUT,CARRYOUTF;
32
33  wire [7:0]OPMODE_out;
34  wire [17:0]B_IN;
35  wire [17:0]D_out;
36  wire [17:0]B0_out; //D and B0 get added
37  wire [17:0]Pre_AS_out;
38  wire [17:0]M1_out;
39  wire [17:0]A0_out;
40  wire [47:0]C_out;
41  wire [17:0]A1_out;
42  wire [17:0]B1_out;
43  wire [35:0]Mult_out;
44  wire [35:0]M_out; //out of instan
45  reg [47:0]Mx_out;
46  reg [47:0]Mz_out;
47  wire [48:0]Post_AS_out; //[48] is for carryout
48  wire [47:0]P_out;
49  wire CYI_IN;
50  wire CYI_OUT;
51  wire CYO_OUT; //the in is Post_AS_out[48]
```

```

45  reg [47:0]Mx_out;
46  reg [47:0]Mz_out;
47  wire [48:0]Post_AS_out;//[48] is for carryout
48  wire [47:0]P_out;
49  wire CYI_IN;
50  wire CYI_OUT;
51  wire CYO_OUT;//the in is Post_AS_out[48]
52  wire [47:0]D_CONC;
53
54  generate
55      if(B_INPUT == "DIRECT") begin
56          assign B_IN = B;
57      end
58  else if(B_INPUT == "CASCADE") begin
59      assign B_IN = BCIN;
60  end
61  endgenerate
62
63  generate
64      if(CARRYINSEL == "OPMODE5") begin
65          assign CYI_IN = OPMODE_out[5];
66      end
67      else if(CARRYINSEL == "CARRYIN") begin
68          assign CYI_IN = CARRYIN;
69      end
70  endgenerate
71
72  //-----Instantiations-----\\
73
74
75  regs #(.USE_REG(OPMODEREG),.LENGTH(8),.RST_MODE(RSTTYPE)) OPMODE_REG (
76      .clk(clk),
77      .clk_en(CEOPMODE),
78      .rst(RSTOPMODE),
79      .in_signal(OPMODE),
80      .out_signal(OPMODE_out)
81  );
82
83  regs #(.USE_REG(DREG),.LENGTH(18),.RST_MODE(RSTTYPE)) D_REG (
84      .clk(clk),
85      .clk_en(CED),
86      .rst(RSTD),
87      .in_signal(D),
88      .out_signal(D_out)
89  );
90

```

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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM

```
89 );
90
91 regs #(.USE_REG(B0REG),.LENGTH(18),.RST_MODE(RSTTYPE)) B0_REG (
92     .clk(clk),
93     .clk_en(CEB),
94     .rst(RSTB),
95     .in_signal(B_IN),
96     .out_signal(B0_out)
97 );
98
99 regs #(.USE_REG(A0REG),.LENGTH(18),.RST_MODE(RSTTYPE)) A0_REG (
100     .clk(clk),
101     .clk_en(CEA),
102     .rst(RSTA),
103     .in_signal(A),
104     .out_signal(A0_out)
105 );
106
107 regs #(.USE_REG(CREG),.LENGTH(48),.RST_MODE(RSTTYPE)) C_REG (
108     .clk(clk),
109     .clk_en(CEC),
110     .rst(RSTC),
111     .in_signal(C),
112     .out_signal(C_out)
113 );
114
115 regs #(.USE_REG(B1REG),.LENGTH(18),.RST_MODE(RSTTYPE)) B1_REG (
116     .clk(clk),
117     .clk_en(CEB),
118     .rst(RSTB),
119     .in_signal(M1_out),
120     .out_signal(B1_out)
121 );
122
123 regs #(.USE_REG(A1REG),.LENGTH(18),.RST_MODE(RSTTYPE)) A1_REG (
124     .clk(clk),
125     .clk_en(CEA),
126     .rst(RSTA),
127     .in_signal(A0_out),
128     .out_signal(A1_out)
129 );
130
131 regs #(.USE_REG(MREG),.LENGTH(36),.RST_MODE(RSTTYPE)) M_REG (
132     .clk(clk),
133     .clk_en(CEM),
134     .rst(RSTM),
135     .in_signal(Mult_out),
136     .out_signal(M_out)
137 );
138
```

```

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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM.v x D_flipflop.v

137 );
138
139 regs #(.USE_REG(CARRYINREG),.LENGTH(1),.RST_MODE(RSTTYPE)) CYI_REG (
140     .clk(clk),
141     .clk_en(CECARRYIN),
142     .rst(RSTCARRYIN),
143     .in_signal(CYI_IN),
144     .out_signal(CYI_OUT)
145 );
146
147 regs #(.USE_REG(CARRYOUTREG),.LENGTH(1),.RST_MODE(RSTTYPE)) CYO_REG (
148     .clk(clk),
149     .clk_en(CECARRYIN),
150     .rst(RSTCARRYIN),
151     .in_signal(Post_AS_out[48]),
152     .out_signal(CYO_OUT)
153 );
154
155 regs #(.USE_REG(PREG),.LENGTH(48),.RST_MODE(RSTTYPE)) P_REG (
156     .clk(clk),
157     .clk_en(CEP),
158     .rst(RSTP),
159     .in_signal(Post_AS_out[47:0]),
160     .out_signal(P)
161 );
162
163 //-----\\
164
165
166 assign Pre_AS_out = (OPMODE_out[6])? D_out - B0_out : D_out + B0_out;
167 assign Post_AS_out = (OPMODE_out[7])? Mz_out - (Mx_out + CYI_OUT) : Mz_out + Mx_out + CYI_OUT;
168 assign M1_out = (OPMODE_out[4])? Pre_AS_out : B0_out;
169 assign Mult_out = B1_out * A1_out;
170 assign D_CONC = {D_out[11:0],A1_out[17:0],B1_out[17:0]};
171 assign BCOUT = B1_out;
172 assign M = M_out;
173 assign CARRYOUTF = CYO_OUT;
174 assign CARRYOUT = CYO_OUT;
175 assign PCOUT = P;
176
177 always @(*) begin
178     case(OPMODE_out[3:2])
179         2'b00 : Mz_out = 48'b0;
180         2'b01 : Mz_out = PCIN;
181         2'b10 : Mz_out = P;
182         2'b11 : Mz_out = C_out;
183     endcase
184 end
185

```

```

182         2'b11 : Mz_out = C_out;
183     endcase
184 end
185
186 always @(*) begin
187     case(OPMODE_out[1:0])
188         2'b00 : Mx_out = 48'b0;
189         2'b01 : Mx_out = {12'b000000000000,Mult_out};
190         2'b10 : Mx_out = P;
191         2'b11 : Mx_out = D_CONC;
192     endcase
193 end
194
195 endmodule

```

Testbench:

```
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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM

1  module tb_DSP;
2
3  parameter A0REG = 0;
4  parameter A1REG = 1;
5  parameter B0REG = 0;
6  parameter B1REG = 1;
7  parameter CREG = 1;
8  parameter DREG=1;
9  parameter MREG = 1;
10 parameter PREG = 1;
11 parameter CARRYINREG = 1;
12 parameter CARRYOUTREG = 1;
13 parameter OPMODEREG = 1;
14 parameter CARRYINSEL = "OPMODE5";
15 parameter B_INPUT = "DIRECT";
16 parameter RSTTYPE = "SYNC";
17
18 reg [17:0] A;
19 reg [17:0] B;
20 reg [17:0] D;
21 reg [47:0] C;
22 reg [47:0] PCIN;
23 reg CARRYIN;
24 reg clk;
25 reg CEA;
26 reg CEB;
27 reg CEC;
28 reg CED;
29 reg CEM;
30 reg CEP;
31 reg CECARRYIN;
32 reg CEOPMODE;
33 reg [17:0] BCIN;
34 reg RSTA;
35 reg RSTB;
36 reg RSTC;
37 reg RSTCARRYIN;
38 reg RSTD;
39 reg RSTM;
40 reg RSTOPMODE;
41 reg RSTP;
42 reg [7:0] OPMODE;
43
44
45 wire [47:0] P;
46 wire [35:0] M;
47 wire [17:0] BCOUT;
48 wire [47:0] PCOUT;
49 wire CARRYOUT;
50 wire CARRYOUTF;
```

```
D:\Digital design diploma\Projects\Project1\DSP_tb.v - Sublime Text (UNREGISTERED)
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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM.v x D_flipflop.v x VM_FSM_tb.v x RAM_S.v x

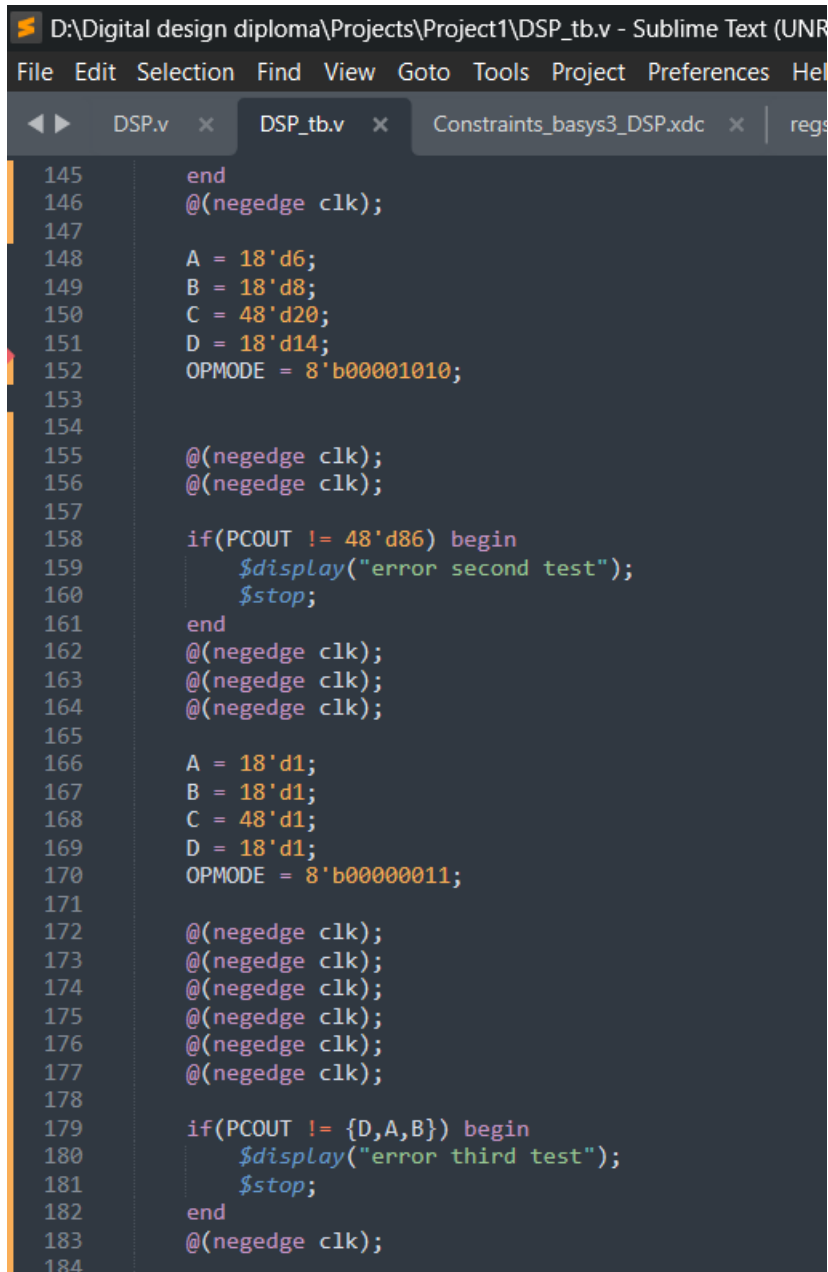
49 wire CARRYOUT;
50 wire CARRYOUTF;
51
52 wire [47:0] P2;
53 wire [35:0] M2;
54 wire [17:0] BCOUT2;
55 wire [47:0] PCOUT2;
56 wire CARRYOUT2;
57 wire CARRYOUTF2;
58
59 // Instantiate the DSP module
60 DSP #(.A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG), .CREG(CREG), .DREG(DREG), .MREG(MREG),
61 .PREG(PREG), .CARRYINREG(CARRYINREG), .CARRYOUTREG(CARRYOUTREG), .OPMODEREG(OPMODEREG),
62 .CARRYINSEL(CARRYINSEL), .B_INPUT(B_INPUT), .RSTTYPE(RSTTYPE)
63 ) dut ( .A(A), .B(B), .C(C), .D(D), .CARRYIN(CARRYIN), .clk(clk), .CEA(CEA), .CEB(CEB), .CEC(CEC), .CED(CED), .CEM(CEM),
64 .CEP(CEP), .CECARRYIN(CECARRYIN), .CEOPMODE(CEOPMODE), .BCIN(BCIN), .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC),
65 .RSTCARRYIN(RSTCARRYIN), .RSTD(RSTD), .RSTM(RSTM), .RSTOPMODE(RSTOPMODE), .RSTP(RSTP), .OPMODE(OPMODE), .P(P), .M(M),
66 .BCOUT(BCOUT), .PCIN(PCIN), .PCOUT(PCOUT), .CARRYOUT(CARRYOUT), .CARRYOUTF(CARRYOUTF)
67 );
68
69 DSP #(.A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG), .CREG(CREG), .DREG(DREG), .MREG(MREG),
70 .PREG(PREG), .CARRYINREG(CARRYINREG), .CARRYOUTREG(CARRYOUTREG), .OPMODEREG(OPMODEREG),
71 .CARRYINSEL("CARRYIN"), .B_INPUT("CASCADE"), .RSTTYPE(RSTTYPE)
72 ) dut_2 ( .A(A), .B(B), .C(C), .D(D), .CARRYIN(CARRYIN), .clk(clk), .CEA(CEA), .CEB(CEB), .CEC(CEC), .CED(CED), .CEM(CEM),
73 .CEP(CEP), .CECARRYIN(CECARRYIN), .CEOPMODE(CEOPMODE), .BCIN(BCIN), .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC),
74 .RSTCARRYIN(RSTCARRYIN), .RSTD(RSTD), .RSTM(RSTM), .RSTOPMODE(RSTOPMODE), .RSTP(RSTP), .OPMODE(OPMODE), .P(P2), .M(M2),
75 .BCOUT(BCOUT2), .PCIN(PCIN), .PCOUT(PCOUT2), .CARRYOUT(CARRYOUT2), .CARRYOUTF(CARRYOUTF2)
76 );
77
78
79 initial begin
80     clk = 0;
81     forever #2 clk = ~clk;
82 end
83
84 initial begin
85
86     A = 0;
87     B = 0;
88     C = 0;
89     D = 0;
90     PCIN = 0;
91     CARRYIN = 0;
92     CEA = 0;
93     CEB = 0;
94     CEC = 0;
95     CED = 0;
96     CEM = 0;
97     CEP = 0;
98     CECARRYIN = 0;
99     CEOPMODE = 0;
```


First test:

```
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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM.v x D_flipflop.v x VM_

97 CEP = 0;
98 CECARRYIN = 0;
99 CEOPMODE = 0;
100 BCIN = 0;
101 RSTA = 0;
102 RSTB = 0;
103 RSTC = 0;
104 RSTCARRYIN = 0;
105 RSTD = 0;
106 RSTM = 0;
107 RSTOPMODE = 0;
108 RSTP = 0;
109 OPMODE = 0;
110
111 @(negedge clk);
112 RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
113 @(negedge clk);
114 RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0; RSTCARRYIN = 0; RSTOPMODE = 0;
115 @(negedge clk);
116 CEA = 1;
117 CEB = 1;
118 CEC = 1;
119 CED = 1;
120 CEM = 1;
121 CEP = 1;
122 CECARRYIN = 1;
123 CEOPMODE = 1;
124 PCIN = 48'd5;
125 CARRYIN = 1'b0;
126 @(negedge clk);
127
128 A = 18'd3;
129 B = 18'd4;
130 C = 48'd10;
131 D = 18'd7;
132
133 OPMODE = 8'b00011101;
134
135 @(negedge clk);
136 @(negedge clk);
137 @(negedge clk);
138 @(negedge clk);
139 @(negedge clk);
140 @(negedge clk);
141
142 if(PCOUT != 48'd43) begin
143     $display("error first test");
144     $stop;
145 end
146 @(negedge clk);
147
```

Second & Third tests:



```
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DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x reg
145     end
146     @(negedge clk);
147
148     A = 18'd6;
149     B = 18'd8;
150     C = 48'd20;
151     D = 18'd14;
152     OPMODE = 8'b00001010;
153
154
155     @(negedge clk);
156     @(negedge clk);
157
158     if(PCOUT != 48'd86) begin
159         $display("error second test");
160         $stop;
161     end
162     @(negedge clk);
163     @(negedge clk);
164     @(negedge clk);
165
166     A = 18'd1;
167     B = 18'd1;
168     C = 48'd1;
169     D = 18'd1;
170     OPMODE = 8'b00000011;
171
172     @(negedge clk);
173     @(negedge clk);
174     @(negedge clk);
175     @(negedge clk);
176     @(negedge clk);
177     @(negedge clk);
178
179     if(PCOUT != {D,A,B}) begin
180         $display("error third test");
181         $stop;
182     end
183     @(negedge clk);
184
```

Cascade:

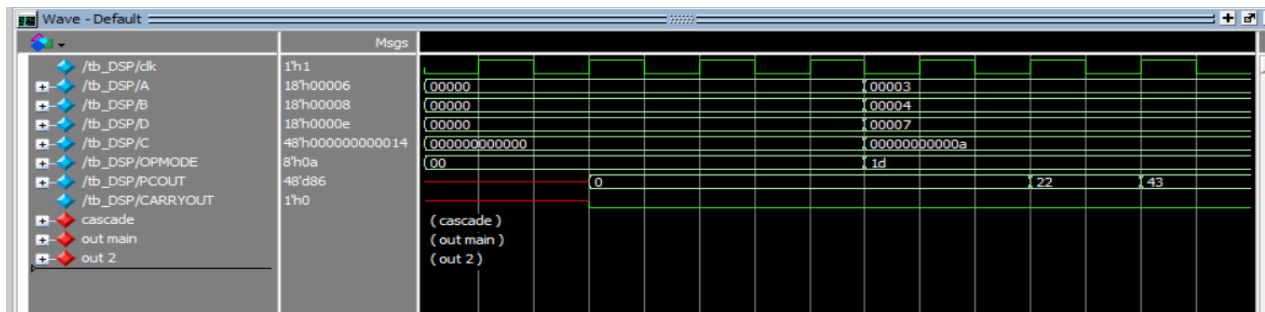
```
181     $stop;
182 end
183 @(negedge clk);
184
185 A = 18'd2;
186 B = 18'd9;
187 C = 48'd10;
188 D = 18'd11;
189 BCIN = 18'd8;
190 CARRYIN = 1'b1;
191 PCIN = 48'd20;
192 OPMODE = 8'b10000101;
193
194 @(negedge clk);
195 @(negedge clk);
196 @(negedge clk);
197 @(negedge clk);
198 @(negedge clk);
199 @(negedge clk);
200
201 if(PCOUT2 != 48'd3) begin
202     $display("error cascade test");
203     $stop;
204 end
205 @(negedge clk);
206 $stop;
207 end
208
209 endmodule
210
```

Do file:

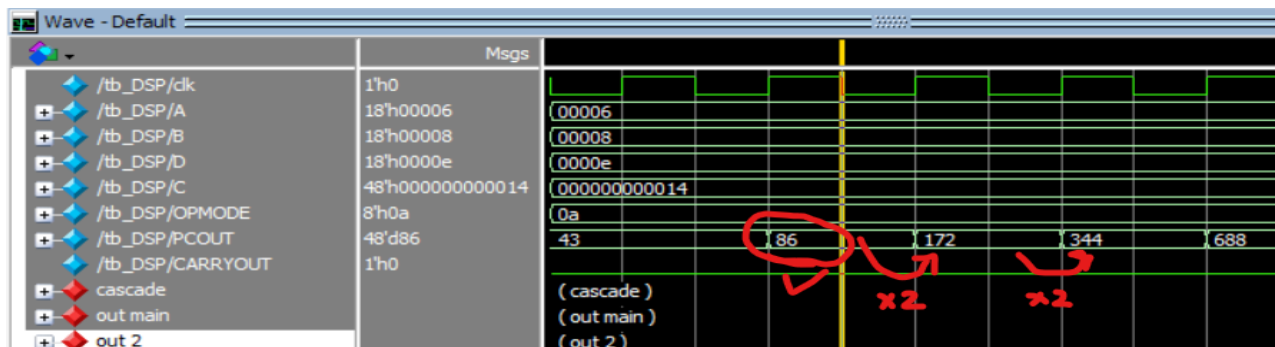
```
File Edit View
vlib work
vlog DSP.v DSP_tb.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
#quit -sim
```

Waveforms:

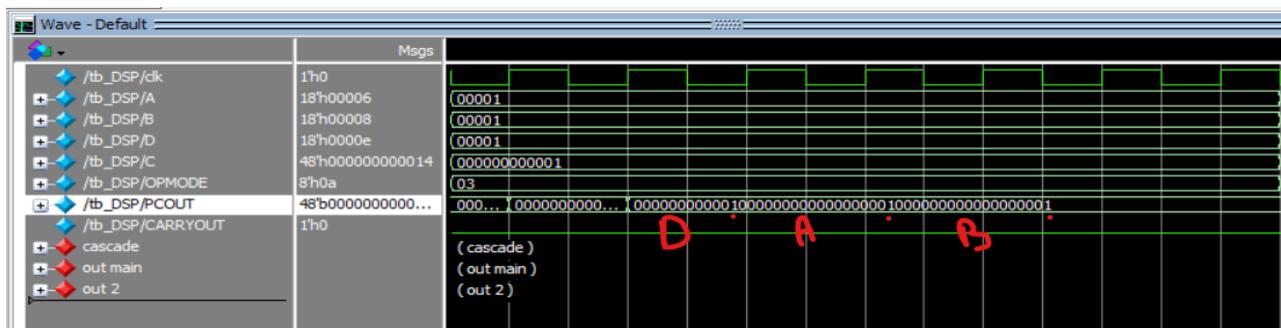
First test:



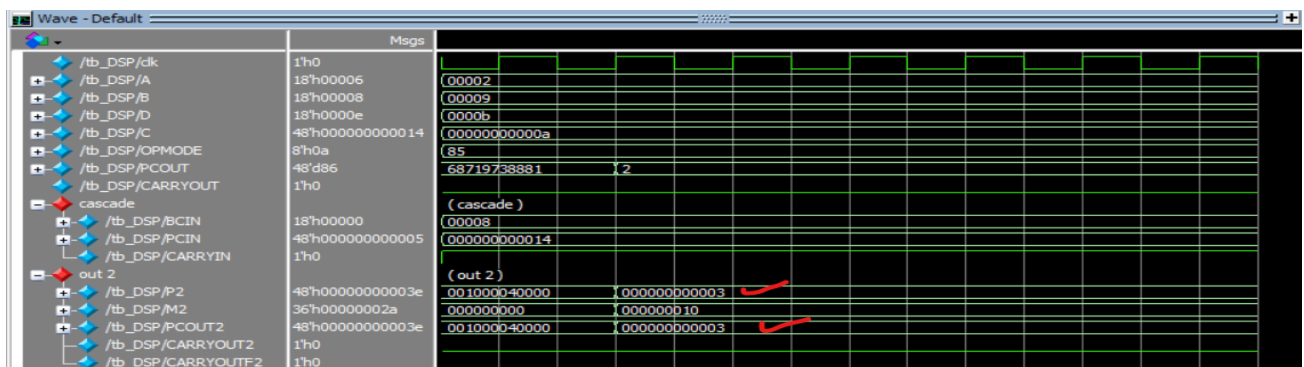
Second test:



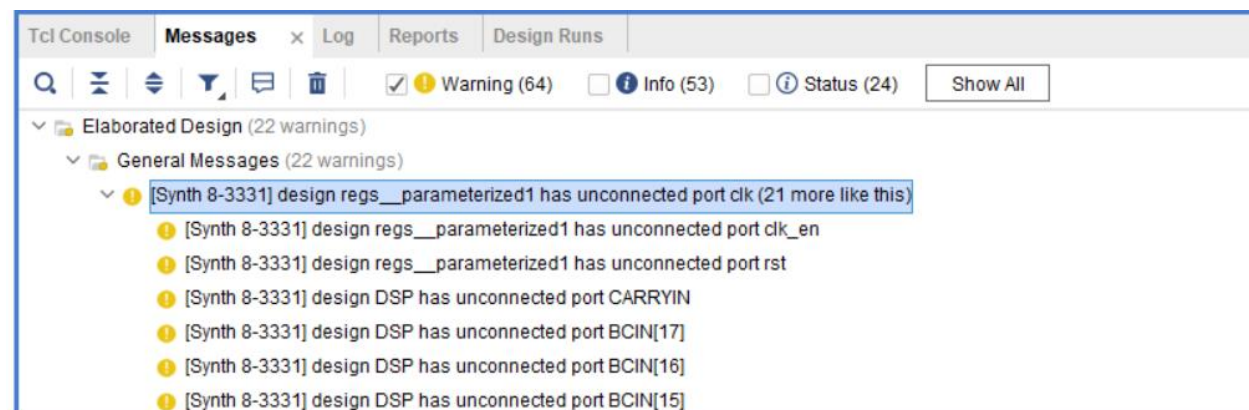
third test:



Cascade:

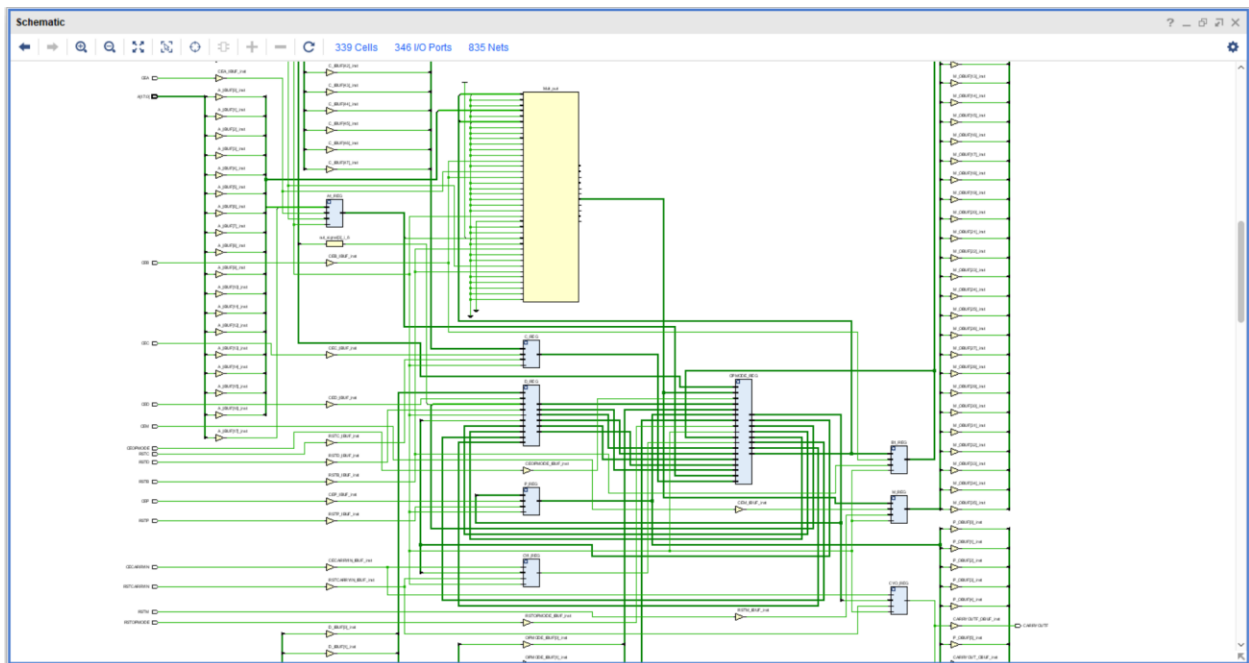
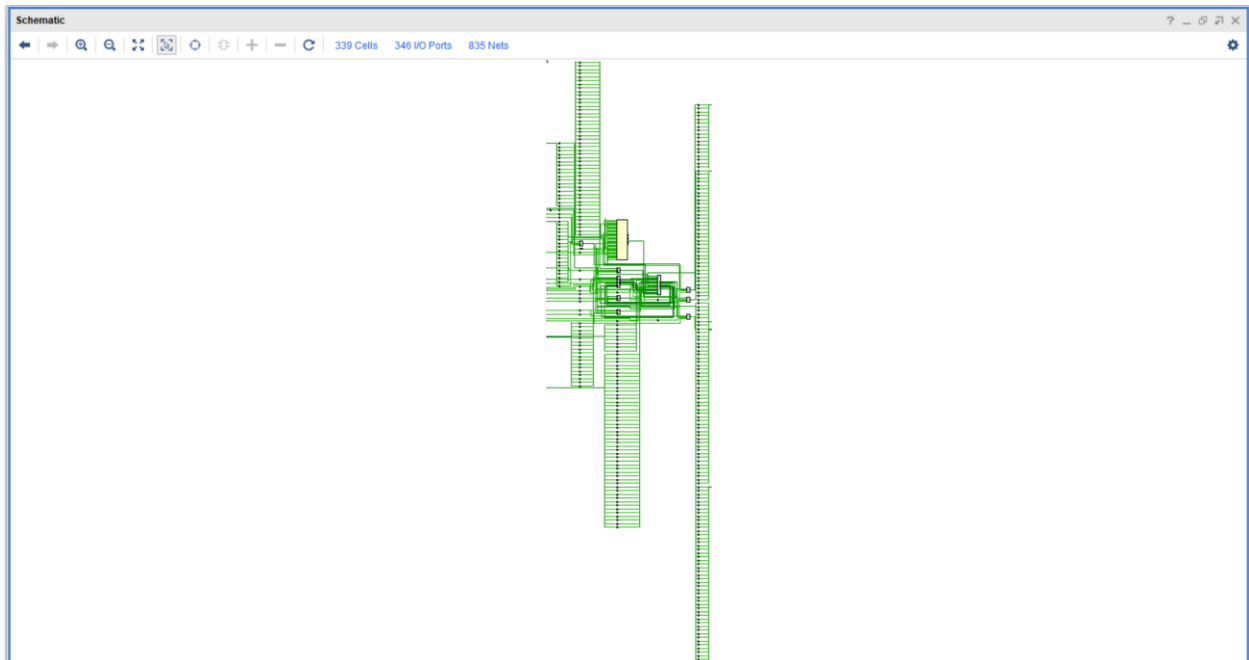


Schematic:



As the parameter default is direct not cascade so the input used in cascade are not used.

Synthesis:



Utilizations:

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Debug																														
Hierarchy																																				
<table><tr><th>Name</th><th>Slice LUTs (134600)</th><th>Slice Registers (269200)</th><th>DSPs (740)</th><th>Bonded IOB (500)</th><th>BUFGCTRL (32)</th></tr><tr><td>DSP</td><td>230</td><td>196</td><td>1</td><td>327</td><td>1</td></tr><tr><td>A1_REG (regs__para...</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td></tr><tr><td>B1_REG (regs__para...</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td></tr><tr><td>C_REG (regs__param...</td><td>0</td><td>48</td><td>0</td><td>0</td><td>0</td></tr></table>							Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	DSP	230	196	1	327	1	A1_REG (regs__para...	0	18	0	0	0	B1_REG (regs__para...	0	18	0	0	0	C_REG (regs__param...	0	48	0	0	0
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)																															
DSP	230	196	1	327	1																															
A1_REG (regs__para...	0	18	0	0	0																															
B1_REG (regs__para...	0	18	0	0	0																															
C_REG (regs__param...	0	48	0	0	0																															

utilization_1

Timing report:

Tcl ConsoleMessagesLogReportsDesign RunsTimingUtilizationDebug? _ □ □

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Design Timing Summary

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
➤ Check Timing (326)
➤ Intra-Clock Paths
Inter-Clock Paths
Other Path Groups

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.793 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 140	Total Number of Endpoints: 140	Total Number of Endpoints: 197

All user specified timing constraints are met.

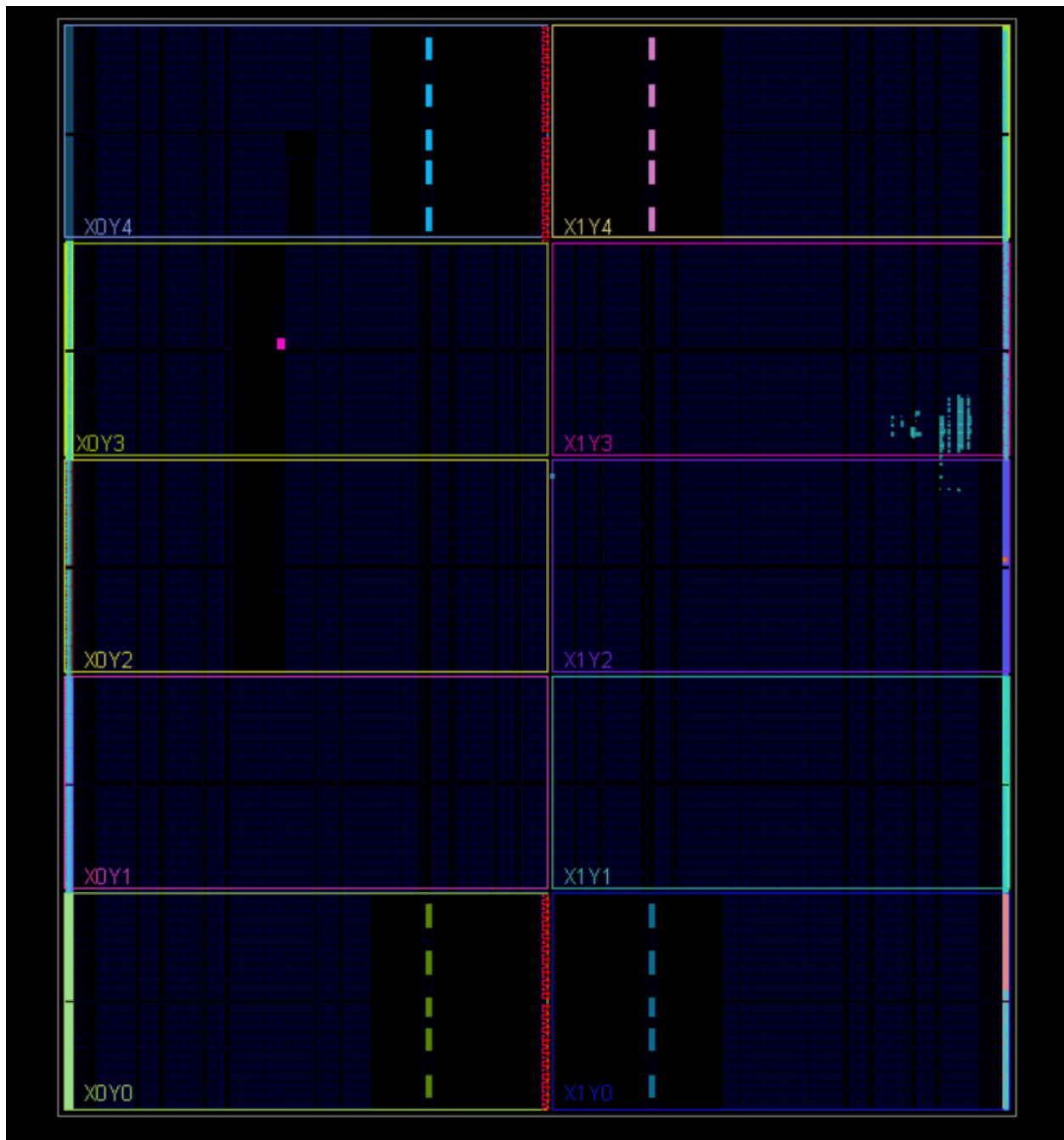
Timing Summary - timing_1

Messages:

Tcl Console	Messages	Log	Reports	Design Runs	Timing	Utilization	Debug
<div><div>Warning (42)</div><div>Info (44)</div><div>Status (22)</div><div>Show All</div></div>							
<div>Synthesis (42 warnings)<div>[Synth 8-3331] design regs__parameterized1 has unconnected port clk (40 more like this)</div><div>[Constraints 18-5210] No constraint will be written out.</div></div>							

Implementation:

Schematic:



Utilization:

Tcl Console	Messages	Log	Reports	Design Runs	Power	DRC	Methodology	Timing	Utilization	x	?	_	□	↗
Hierarchy														
Hierarchy														
Summary														
▼ Slice Logic														
▼ Slice LUTs (<1%)														
LUT as Logic (<1%)														
▼ Slice Registers (<1%)														
Register as Flip Flop														
utilization_1														
Name														
1														
Slice LUTs (133800)														
Slice Registers (267600)														
Slice (33450)														
LUT as Logic (133800)														
LUT Flip Flop Pairs (133800)														
DSPs (740)														
Bonded IOB (500)														
BUFCTRL (32)														
▼ DSP														
A1_REG (regs__para...														
B1_REG (regs__para...														
C_REG (regs__param...														

Timing:

Tcl Console	Messages	Log	Reports	Design Runs	Power	DRC	Methodology	Timing	Utilization	x	?	_	□	↗
Design Timing Summary														
General Information														
Timer Settings														
Design Timing Summary														
Clock Summary (1)														
Check Timing (326)														
Intra-Clock Paths														
Inter-Clock Paths														
Other Path Groups														
Timing Summary - impl_1 (saved)														
Timing Summary - timing_1														
Timing Summary - timing_2														
Setup														
Hold														
Pulse Width														
Worst Negative Slack (WNS): 1.491 ns														
Worst Hold Slack (WHS): 0.261 ns														
Worst Pulse Width Slack (WPWS): 4.500 ns														
Total Negative Slack (TNS): 0.000 ns														
Total Hold Slack (THS): 0.000 ns														
Total Pulse Width Negative Slack (TPWS): 0.000 ns														
Number of Failing Endpoints: 0														
Number of Failing Endpoints: 0														
Number of Failing Endpoints: 0														
Total Number of Endpoints: 159														
Total Number of Endpoints: 159														
Total Number of Endpoints: 216														
All user specified timing constraints are met.														

Message:

Tcl Console	Messages	x	Log	Reports	Design Runs	Power	DRC	Methodology	Timing	Utilization	x	?	_	□	↗
Warning (44)															
Info (230)															
Status (462)															
Show All															
[Synth 8-3331] design regs__parameterize01 has unconnected port clk (40 more like this)															
[Constraints 18-5210] No constraint will be written out.															
Implementation (1 warning)															
Route Design (1 warning)															
DRC (1 warning)															
Pin Planning (1 warning)															
[DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCC0: The CONFIG_MODE property of current_design specifies a configuration mode (SPIv4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), and Y27 (IO_L6P_T0_FCS_B_14)															

Constrain file:

```
D:\Digital design diploma\Projects\Project1\Constraints_basys3_DSP.xdc - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v x DSP_tb.v x Constraints_basys3_DSP.xdc x regs.v x regs_tb.v x VM_FSM.v x D_flipflop.v x VM_FSM_tb.v

1  ## This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6  ## Clock signal
7  ## to choose the clk pin
8  set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
9  ## set the clock
10 create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]
11
12
13 ## Switches
14 # set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [get_ports {opcode[0]}]
15 # set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 } [get_ports {opcode[1]}]
16 # set_property -dict { PACKAGE_PIN W16 IOSTANDARD LVCMOS33 } [get_ports {A[0]}]
17 # set_property -dict { PACKAGE_PIN W17 IOSTANDARD LVCMOS33 } [get_ports {A[1]}]
18 # set_property -dict { PACKAGE_PIN W15 IOSTANDARD LVCMOS33 } [get_ports {A[2]}]
19 # set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [get_ports {A[3]}]
20 # set_property -dict { PACKAGE_PIN W14 IOSTANDARD LVCMOS33 } [get_ports {B[0]}]
21 # set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVCMOS33 } [get_ports {B[1]}]
22 # set_property -dict { PACKAGE_PIN V2 IOSTANDARD LVCMOS33 } [get_ports {B[2]}]
23 # set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 } [get_ports {B[3]}]
24 # set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
25 # set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
26 # set_property -dict { PACKAGE_PIN W2 IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
27 # set_property -dict { PACKAGE_PIN U1 IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
28 # set_property -dict { PACKAGE_PIN T1 IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
29 # set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]
30
31
32
33
34
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37
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39
40
41
42
43
44
45
46 ##STARTUPE2 primitive.
47 #set_property -dict { PACKAGE_PIN D18 IOSTANDARD LVCMOS33 } [get_ports {QspiDB[0]}]
48 #set_property -dict { PACKAGE_PIN D19 IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
49 #set_property -dict { PACKAGE_PIN G18 IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
50 #set_property -dict { PACKAGE_PIN F18 IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
51 #set_property -dict { PACKAGE_PIN K19 IOSTANDARD LVCMOS33 } [get_ports {QspiCSn}]
52
53
54 ## Configuration options, can be used for all designs
55 set_property CONFIG_VOLTAGE 3.3 [current_design]
56 set_property CFGBVS VCC0 [current_design]
57
58 ## SPI configuration mode options for QSPI boot, can be used for all designs
59 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
60 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
61 set_property CONFIG_MODE SPIx4 [current_design]
```