DSP Project

The reg & MUX module:

D:\Digital design diploma\Projects\Project1\regs.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

DSP.v | regs_tb.v | regs.v | VM_FSM.v | D_flipflop.v | VM_FSM_t

```
1  module regs(clk,clk_en,rst,in_signal,out_signal);
2  parameter USE_REG = 0;
3  parameter LENGTH = 18;
4  parameter RST_MODE = "SYNC";
5  input wire clk,clk_en;
6  input wire rst;
7  input wire [LENGTH-1:0] in_signal;
8  output reg [LENGTH-1:0] out_signal;
9
10 generate
11     if (USE_REG == 1 && RST_MODE == "ASYNC") begin
12         always @(posedge clk or posedge rst) begin
13             if (rst)
14                 out_signal <= 0;
15             else if (clk_en)
16                 out_signal <= in_signal;
17         end
18     end else if(USE_REG == 1 && RST_MODE == "SYNC") begin
19         always @(posedge clk) begin
20             if (rst)
21                 out_signal <= 0;
22             else if (clk_en)
23                 out_signal <= in_signal;
24         end
25     end else begin
26         always @(*) begin
27             out_signal = in_signal;
28         end
29     end
30 endgenerate
31
32 endmodule
33
```

The testbench:

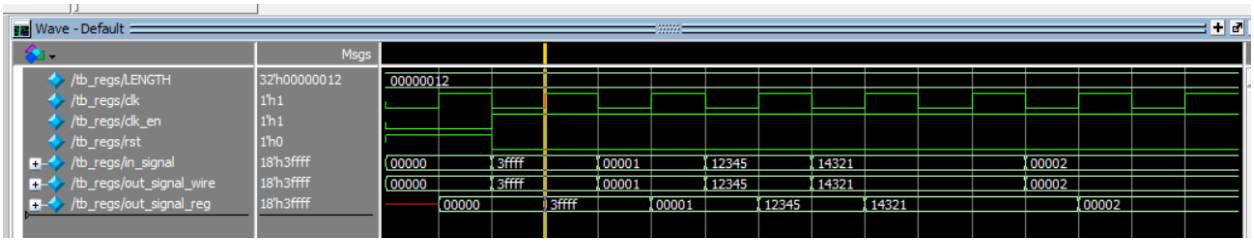
D:\Digital design diploma\Projects\Project1\regs_tb.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

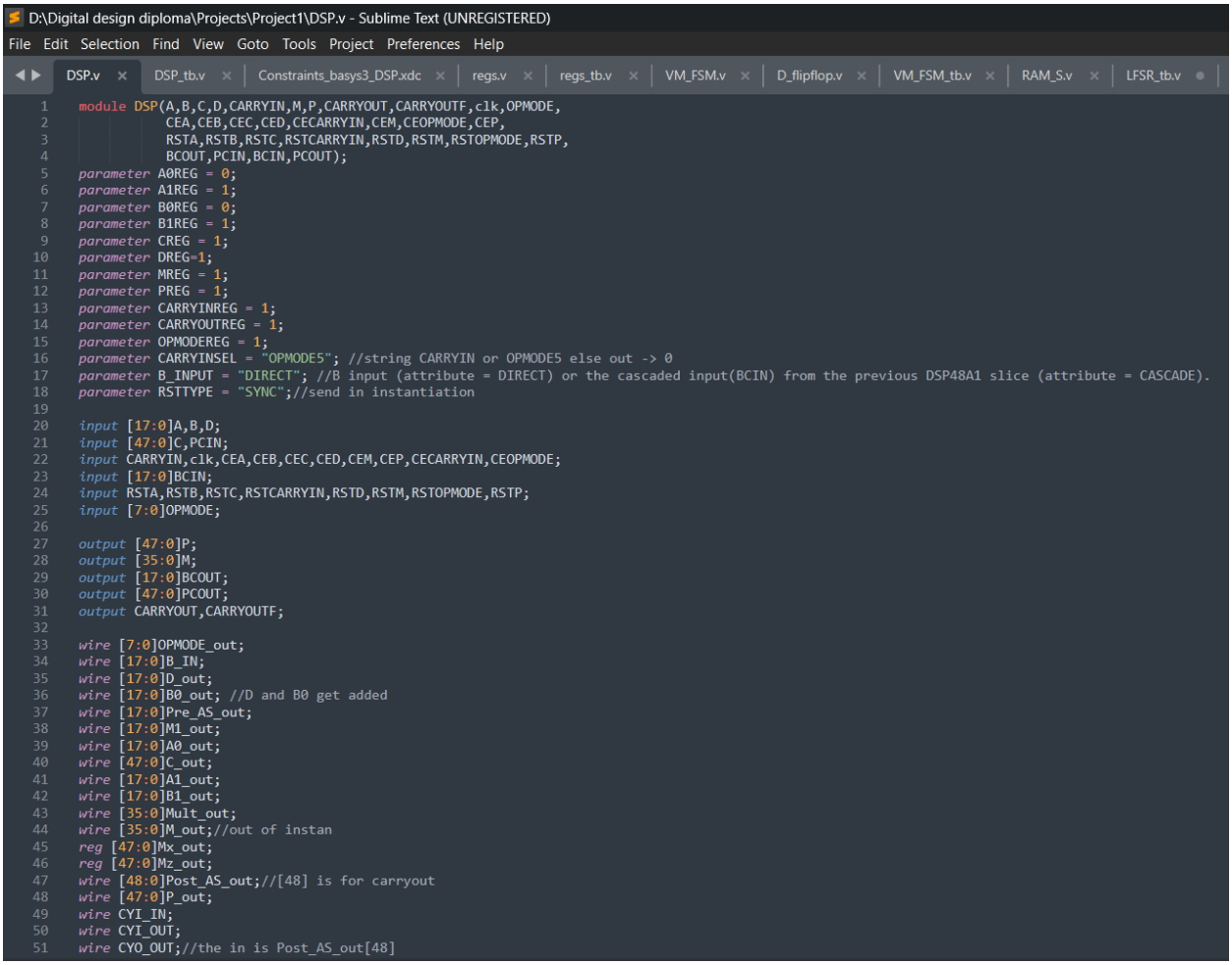
DSP.v | regs_tb.v | regs.v | VM_FSM.v | D_flipflop.v | VM_FSM_tb.v | RAM_S.v

```
1  module tb_regs;
2
3      localparam LENGTH = 18;
4      reg clk;
5      reg clk_en;
6      reg rst;
7      reg [LENGTH-1:0] in_signal;
8      wire [LENGTH-1:0] out_signal_wire;
9      wire [LENGTH-1:0] out_signal_reg;
10     initial begin
11         clk = 0;
12         forever #5 clk = ~clk;
13     end
14
15 regs #(.USE_REG(0),.LENGTH(LENGTH),
16     .RST_MODE("SYNC")) uut_wire (.clk(clk),.clk_en(clk_en),.rst(rst),.in_signal(in_signal),
17                                  .out_signal(out_signal_wire)
18                                 );
19 regs #(.USE_REG(1),.LENGTH(LENGTH),
20     .RST_MODE("SYNC")) uut_reg (.clk(clk),.clk_en(clk_en),.rst(rst),.in_signal(in_signal),
21                                  .out_signal(out_signal_reg)
22                                  );
23
24     initial begin
25         clk_en = 0;
26         rst = 0;
27         in_signal = 0;
28         rst = 1;
29         #10;
30         rst = 0;
31         in_signal = 18'h3FFFF;
32         clk_en = 1;
33         #10;
34         in_signal = 18'h00001;
35         #10;
36         in_signal = 18'h12345;
37         #10;
38         in_signal = 18'h54321;
39         clk_en = 1;
40         #20;
41         in_signal = 18'h00002;
42         #10;
43         $stop;
44     end
45 endmodule
46
```

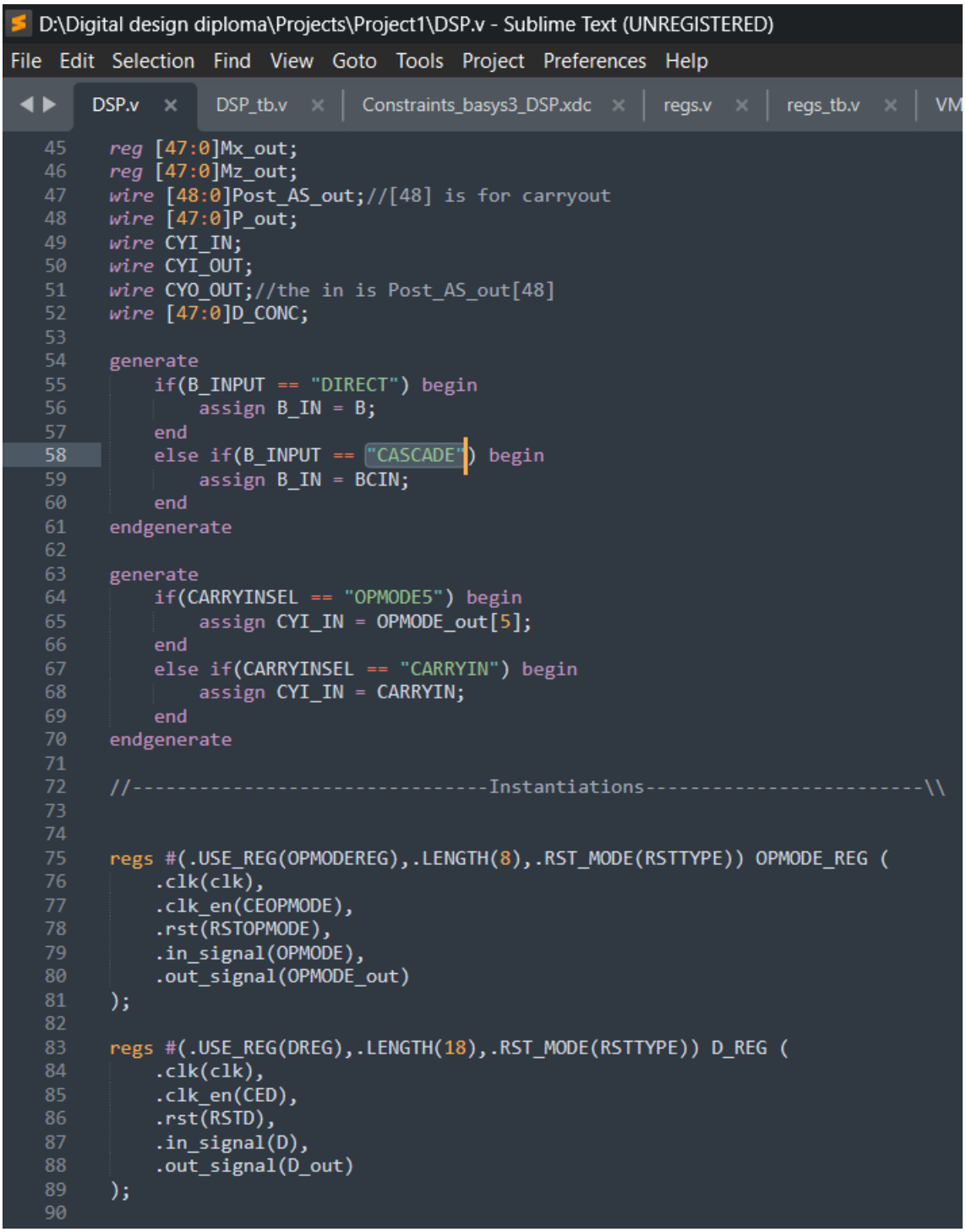
Waveform:

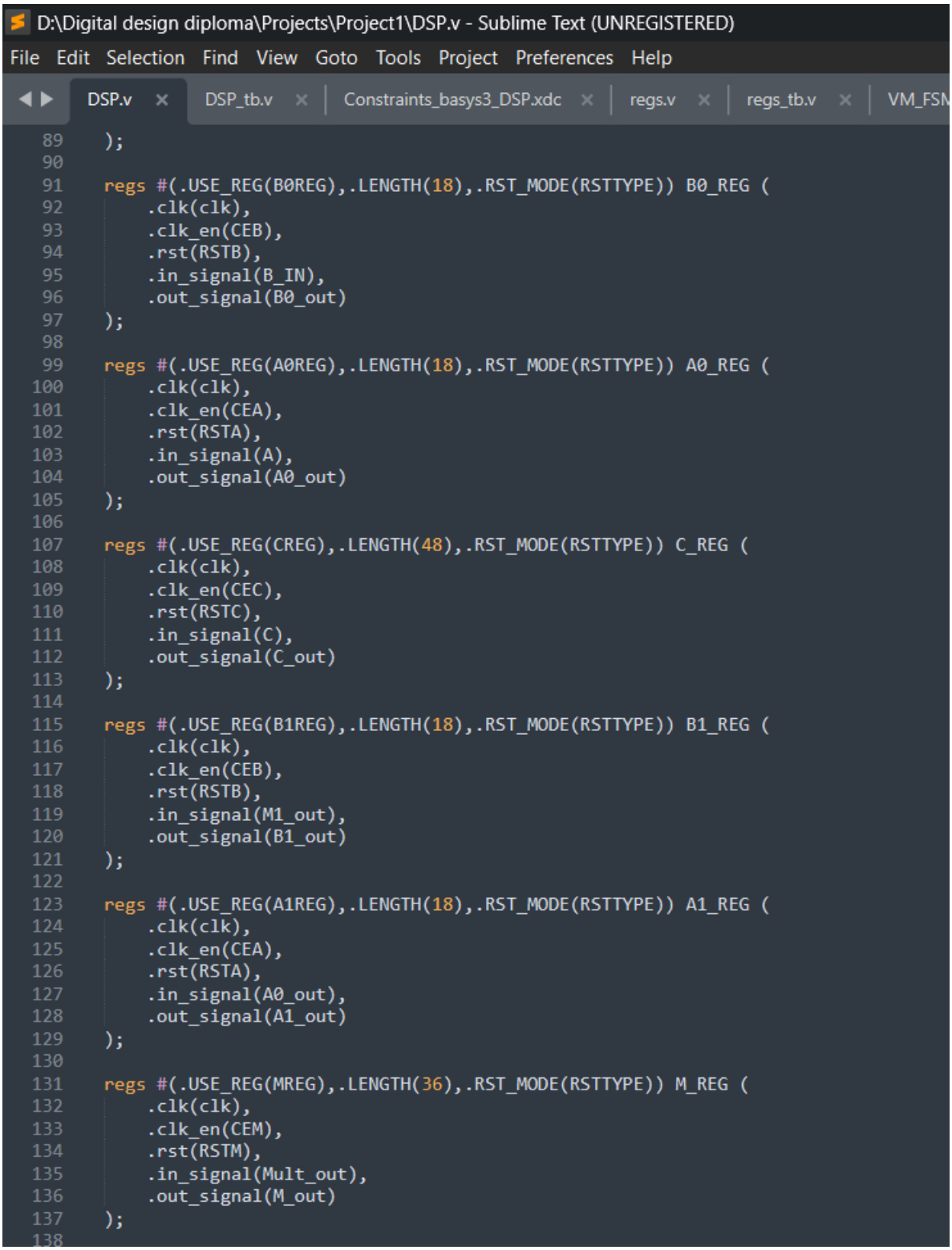


Main project code:




```
module DSP(A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,clk,OPMODE,
           CEA,CEB,CEC,CED,CECARRYIN,CEM,CEOPMODE,CEP,
           RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP,
           BCOUT,PCIN,BCIN,PCOUT);
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG=1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5"; //string CARRYIN or OPMODE5 else out -> 0
parameter B_INPUT = "DIRECT"; //B input (attribute = DIRECT) or the cascaded input(BCIN) from the previous DSP48A1 slice (attribute = CASCADE).
parameter RSTTYPE = "SYNC";//send in instantiation

input [17:0]A,B,D;
input [47:0]C,PCIN;
input CARRYIN,clk,CEA,CEB,CEC,CED,CEM,CEP,CECARRYIN,CEOPMODE;
input [17:0]BCIN;
input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
input [7:0]OPMODE;

output [47:0]P;
output [35:0]M;
output [17:0]BCOUT;
output [47:0]PCOUT;
output CARRYOUT,CARRYOUTF;

wire [7:0]OPMODE_out;
wire [17:0]B_IN;
wire [17:0]D_out;
wire [17:0]B0_out; //D and B0 get added
wire [17:0]Pre_AS_out;
wire [17:0]M1_out;
wire [17:0]A0_out;
wire [47:0]C_out;
wire [17:0]A1_out;
wire [17:0]B1_out;
wire [35:0]Mult_out;
wire [35:0]M_out;//out of instan
reg [47:0]Mx_out;
reg [47:0]Mz_out;
wire [48:0]Post_AS_out;//[48] is for carryout
wire [47:0]P_out;
wire CYI_IN;
wire CYI_OUT;
wire CYO_OUT;//the in is Post_AS_out[48]
```


D:\Digital design diploma\Projects\Project1\DSP.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v
DSP_tb.v
Constraints_basys3_DSP.xdc
regs.v
regs_tb.v
VM
45 reg [47:0]Mx_out;
46 reg [47:0]Mz_out;
47 wire [48:0]Post_AS_out;//[48] is for carryout
48 wire [47:0]P_out;
49 wire CYI_IN;
50 wire CYI_OUT;
51 wire CYO_OUT;//the in is Post_AS_out[48]
52 wire [47:0]D_CONC;
53
54 generate
55 if(B_INPUT == "DIRECT") begin
56 assign B_IN = B;
57 end
58 else if(B_INPUT == "CASCADE") begin
59 assign B_IN = BCIN;
60 end
61 endgenerate
62
63 generate
64 if(CARRYINSEL == "OPMODE5") begin
65 assign CYI_IN = OPMODE_out[5];
66 end
67 else if(CARRYINSEL == "CARRYIN") begin
68 assign CYI_IN = CARRYIN;
69 end
70 endgenerate
71
72 //--------------------------------Instantiations-------------------------\\
73
74
75 regs #(.USE_REG(OPMODEREG),.LENGTH(8),.RST_MODE(RSTTYPE)) OPMODE_REG (
76 .clk(clk),
77 .clk_en(CEOPMODE),
78 .rst(RSTOPMODE),
79 .in_signal(OPMODE),
80 .out_signal(OPMODE_out)
81);
82
83 regs #(.USE_REG(DREG),.LENGTH(18),.RST_MODE(RSTTYPE)) D_REG (
84 .clk(clk),
85 .clk_en(CED),
86 .rst(RSTD),
87 .in_signal(D),
88 .out_signal(D_out)
89);
90


D:\Digital design diploma\Projects\Project1\DSP.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v
DSP_tb.v
Constraints_basys3_DSP.xdc
regs.v
regs_tb.v
VM_FSM
);
regs #(.USE_REG(B0REG),.LENGTH(18),.RST_MODE(RSTTYPE)) B0_REG (
.clk(clk),
.clk_en(CEB),
.rst(RSTB),
.in_signal(B_IN),
.out_signal(B0_out)
);
regs #(.USE_REG(A0REG),.LENGTH(18),.RST_MODE(RSTTYPE)) A0_REG (
.clk(clk),
.clk_en(CEA),
.rst(RSTA),
.in_signal(A),
.out_signal(A0_out)
);
regs #(.USE_REG(CREG),.LENGTH(48),.RST_MODE(RSTTYPE)) C_REG (
.clk(clk),
.clk_en(CEC),
.rst(RSTC),
.in_signal(C),
.out_signal(C_out)
);
regs #(.USE_REG(B1REG),.LENGTH(18),.RST_MODE(RSTTYPE)) B1_REG (
.clk(clk),
.clk_en(CEB),
.rst(RSTB),
.in_signal(M1_out),
.out_signal(B1_out)
);
regs #(.USE_REG(A1REG),.LENGTH(18),.RST_MODE(RSTTYPE)) A1_REG (
.clk(clk),
.clk_en(CEA),
.rst(RSTA),
.in_signal(A0_out),
.out_signal(A1_out)
);
regs #(.USE_REG(MREG),.LENGTH(36),.RST_MODE(RSTTYPE)) M_REG (
.clk(clk),
.clk_en(CEM),
.rst(RSTM),
.in_signal(Mult_out),
.out_signal(M_out)
);

D:\Digital design diploma\Projects\Project1\DSP.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

DSP.v | DSP_tb.v | Constraints_basys3_DSP.xdc | regs.v | regs_tb.v | VM_FSM.v | D_flipflop.v

```
137   );
138
139   regs #(.USE_REG(CARRYINREG),.LENGTH(1),.RST_MODE(RSTTYPE)) CYI_REG (
140       .clk(clk),
141       .clk_en(CECARRYIN),
142       .rst(RSTCARRYIN),
143       .in_signal(CYI_IN),
144       .out_signal(CYI_OUT)
145   );
146
147   regs #(.USE_REG(CARRYOUTREG),.LENGTH(1),.RST_MODE(RSTTYPE)) CYO_REG (
148       .clk(clk),
149       .clk_en(CECARRYIN),
150       .rst(RSTCARRYIN),
151       .in_signal(Post_AS_out[48]),
152       .out_signal(CYO_OUT)
153   );
154
155   regs #(.USE_REG(PREG),.LENGTH(48),.RST_MODE(RSTTYPE)) P_REG (
156       .clk(clk),
157       .clk_en(CEP),
158       .rst(RSTP),
159       .in_signal(Post_AS_out[47:0]),
160       .out_signal(P)
161   );
162
163   //-------------------------------------------------------------------------\\
164
165
166   assign Pre_AS_out = (OPMODE_out[6])? D_out - B0_out : D_out + B0_out;
167   assign Post_AS_out = (OPMODE_out[7])? Mz_out - (Mx_out + CYI_OUT) : Mz_out + Mx_out + CYI_OUT;
168   assign M1_out = (OPMODE_out[4])? Pre_AS_out : B0_out;
169   assign Mult_out = B1_out * A1_out;
170   assign D_CONC = {D_out[11:0],A1_out[17:0],B1_out[17:0]};
171   assign BCOUT = B1_out;
172   assign M = M_out;
173   assign CARRYOUTF = CYO_OUT;
174   assign CARRYOUT = CYO_OUT;
175   assign PCOUT = P;
176
177   always @(*) begin
178       case(OPMODE_out[3:2])
179           2'b00 : Mz_out = 48'b0;
180           2'b01 : Mz_out = PCIN;
181           2'b10 : Mz_out = P;
182           2'b11 : Mz_out = C_out;
183       endcase
184   end
```

```
182           2'b11 : Mz_out = C_out;
183       endcase
184   end
185
186   always @(*) begin
187       case(OPMODE_out[1:0])
188           2'b00 : Mx_out = 48'b0;
189           2'b01 : Mx_out = {12'b000000000000,Mult_out};
190           2'b10 : Mx_out = P;
191           2'b11 : Mx_out = D_CONC;
192       endcase
193   end
194
195   endmodule
```

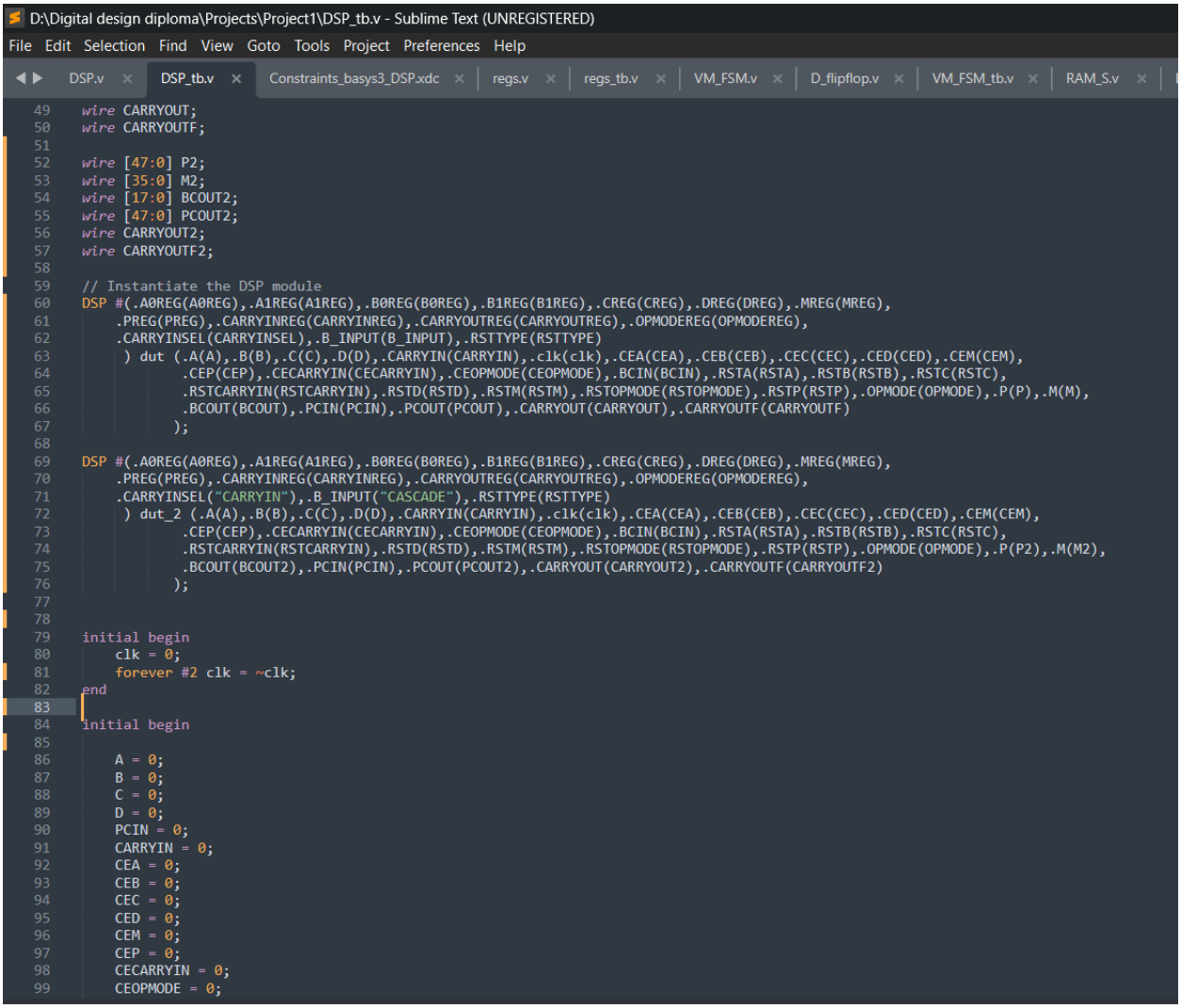
Testbench:

D:\Digital design diploma\Projects\Project1\DSP_tb.v - Sublime Text (UNREGISTERED)

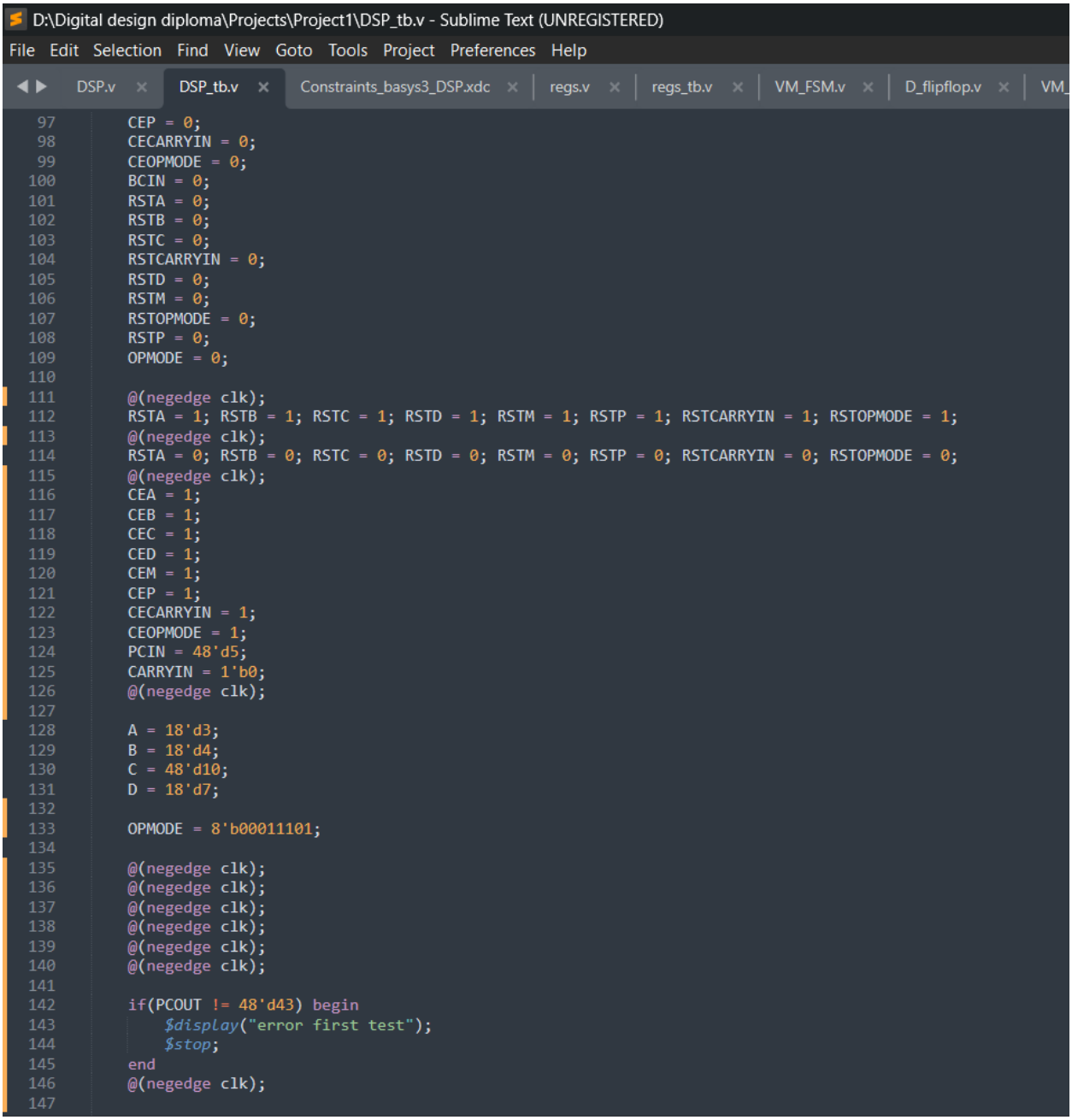
File Edit Selection Find View Goto Tools Project Preferences Help

DSP.v | DSP_tb.v | Constraints_basys3_DSP.xdc | regs.v | regs_tb.v | VM_FSM

```
module tb_DSP;

parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG=1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";

reg [17:0] A;
reg [17:0] B;
reg [17:0] D;
reg [47:0] C;
reg [47:0] PCIN;
reg CARRYIN;
reg clk;
reg CEA;
reg CEB;
reg CEC;
reg CED;
reg CEM;
reg CEP;
reg CECARRYIN;
reg CEOPMODE;
reg [17:0] BCIN;
reg RSTA;
reg RSTB;
reg RSTC;
reg RSTCARRYIN;
reg RSTD;
reg RSTM;
reg RSTOPMODE;
reg RSTP;
reg [7:0] OPMODE;


wire [47:0] P;
wire [35:0] M;
wire [17:0] BCOUT;
wire [47:0] PCOUT;
wire CARRYOUT;
wire CARRYOUTF;
```


D:\Digital design diploma\Projects\Project1\DSP_tb.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v
DSP_tb.v
Constraints_basys3_DSP.xdc
regs.v
regs_tb.v
VM_FSM.v
D_flipflop.v
VM_FSM_tb.v
RAM_S.v
wire CARRYOUT;
wire CARRYOUTF;
wire [47:0] P2;
wire [35:0] M2;
wire [17:0] BCOUT2;
wire [47:0] PCOUT2;
wire CARRYOUT2;
wire CARRYOUTF2;
// Instantiate the DSP module
DSP #(.A0REG(A0REG),.A1REG(A1REG),.B0REG(B0REG),.B1REG(B1REG),.CREG(CREG),.DREG(DREG),.MREG(MREG),
.PREG(PREG),.CARRYINREG(CARRYINREG),.CARRYOUTREG(CARRYOUTREG),.OPMODEREG(OPMODEREG),
.CARRYINSEL(CARRYINSEL),.B_INPUT(B_INPUT),.RSTTYPE(RSTTYPE)
) dut (.A(A),.B(B),.C(C),.D(D),.CARRYIN(CARRYIN),.clk(clk),.CEA(CEA),.CEB(CEB),.CEC(CEC),.CED(CED),.CEM(CEM),
.CEP(CEP),.CECARRYIN(CECARRYIN),.CEOPMODE(CEOPMODE),.BCIN(BCIN),.RSTA(RSTA),.RSTB(RSTB),.RSTC(RSTC),
.RSTCARRYIN(RSTCARRYIN),.RSTD(RSTD),.RSTM(RSTM),.RSTOPMODE(RSTOPMODE),.RSTP(RSTP),.OPMODE(OPMODE),.P(P),.M(M),
.BCOUT(BCOUT),.PCIN(PCIN),.PCOUT(PCOUT),.CARRYOUT(CARRYOUT),.CARRYOUTF(CARRYOUTF)
);
DSP #(.A0REG(A0REG),.A1REG(A1REG),.B0REG(B0REG),.B1REG(B1REG),.CREG(CREG),.DREG(DREG),.MREG(MREG),
.PREG(PREG),.CARRYINREG(CARRYINREG),.CARRYOUTREG(CARRYOUTREG),.OPMODEREG(OPMODEREG),
.CARRYINSEL("CARRYIN"),.B_INPUT("CASCADE"),.RSTTYPE(RSTTYPE)
) dut_2 (.A(A),.B(B),.C(C),.D(D),.CARRYIN(CARRYIN),.clk(clk),.CEA(CEA),.CEB(CEB),.CEC(CEC),.CED(CED),.CEM(CEM),
.CEP(CEP),.CECARRYIN(CECARRYIN),.CEOPMODE(CEOPMODE),.BCIN(BCIN),.RSTA(RSTA),.RSTB(RSTB),.RSTC(RSTC),
.RSTCARRYIN(RSTCARRYIN),.RSTD(RSTD),.RSTM(RSTM),.RSTOPMODE(RSTOPMODE),.RSTP(RSTP),.OPMODE(OPMODE),.P(P2),.M(M2),
.BCOUT(BCOUT2),.PCIN(PCIN),.PCOUT(PCOUT2),.CARRYOUT(CARRYOUT2),.CARRYOUTF(CARRYOUTF2)
);
initial begin
clk = 0;
forever #2 clk = ~clk;
end
initial begin
A = 0;
B = 0;
C = 0;
D = 0;
PCIN = 0;
CARRYIN = 0;
CEA = 0;
CEB = 0;
CEC = 0;
CED = 0;
CEM = 0;
CEP = 0;
CECARRYIN = 0;
CEOPMODE = 0;

First test:


D:\Digital design diploma\Projects\Project1\DSP_tb.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
DSP.v
DSP_tb.v
Constraints_basys3_DSP.xdc
regs.v
regs_tb.v
VM_FSM.v
D_flipflop.v
97 CEP = 0;
98 CECARRYIN = 0;
99 CEOPMODE = 0;
100 BCIN = 0;
101 RSTA = 0;
102 RSTB = 0;
103 RSTC = 0;
104 RSTCARRYIN = 0;
105 RSTD = 0;
106 RSTM = 0;
107 RSTOPMODE = 0;
108 RSTP = 0;
109 OPMODE = 0;
110
111 @(negedge clk);
112 RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
113 @(negedge clk);
114 RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0; RSTCARRYIN = 0; RSTOPMODE = 0;
115 @(negedge clk);
116 CEA = 1;
117 CEB = 1;
118 CEC = 1;
119 CED = 1;
120 CEM = 1;
121 CEP = 1;
122 CECARRYIN = 1;
123 CEOPMODE = 1;
124 PCIN = 48'd5;
125 CARRYIN = 1'b0;
126 @(negedge clk);
127
128 A = 18'd3;
129 B = 18'd4;
130 C = 48'd10;
131 D = 18'd7;
132
133 OPMODE = 8'b00011101;
134
135 @(negedge clk);
136 @(negedge clk);
137 @(negedge clk);
138 @(negedge clk);
139 @(negedge clk);
140 @(negedge clk);
141
142 if(PCOUT != 48'd43) begin
143 $display("error first test");
144 $stop;
145 end
146 @(negedge clk);
147

Second & Third tests:

Cascade:

```
181             $stop;
182         end
183         @(negedge clk);
184 
185         A = 18'd2;
186         B = 18'd9;
187         C = 48'd10;
188         D = 18'd11;
189         BCIN = 18'd8;
190         CARRYIN = 1'b1;
191         PCIN = 48'd20;
192         OPMODE = 8'b10000101;
193 
194         @(negedge clk);
195         @(negedge clk);
196         @(negedge clk);
197         @(negedge clk);
198         @(negedge clk);
199         @(negedge clk);
200 
201         if(PCOUT2 != 48'd3) begin
202             $display("error cascade test");
203             $stop;
204         end
205         @(negedge clk);
206         $stop;
207     end
208 
209     endmodule
210 
```

Do file:

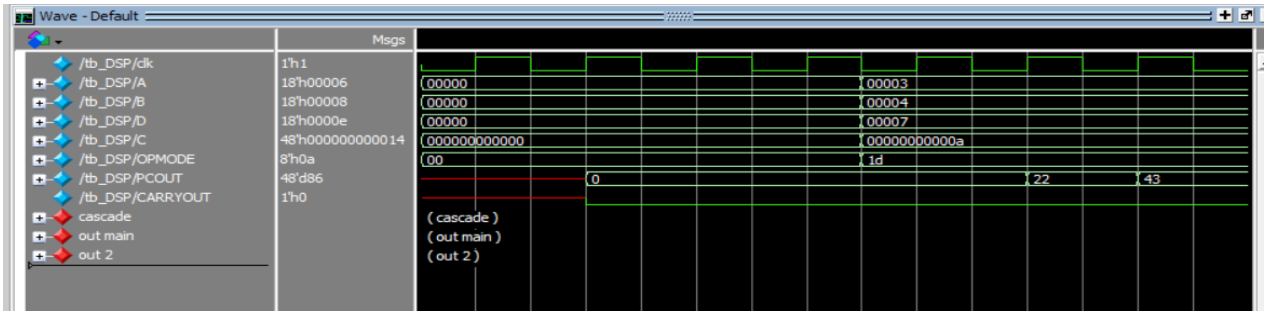
/_S.do | data.txt | DSP.do

File Edit View

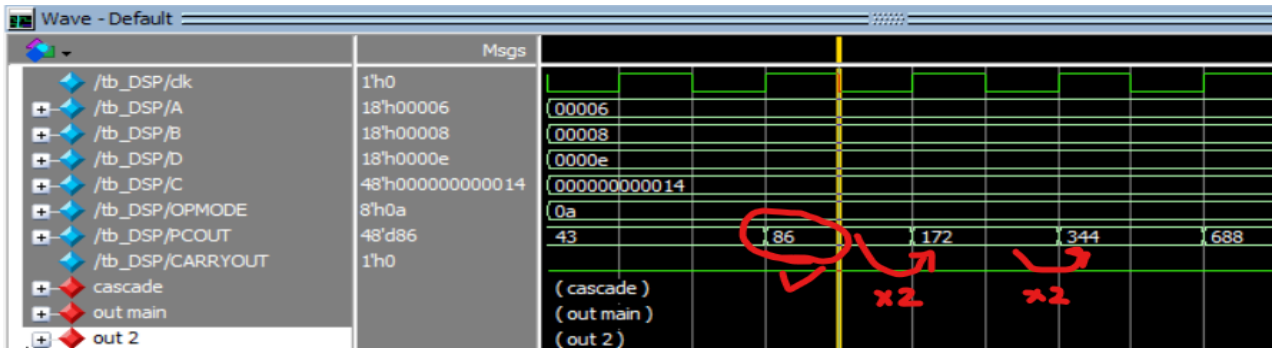
```
vlib work
vlog DSP.v DSP_tb.v
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
#quit -sim
```

Waveforms:

First test:

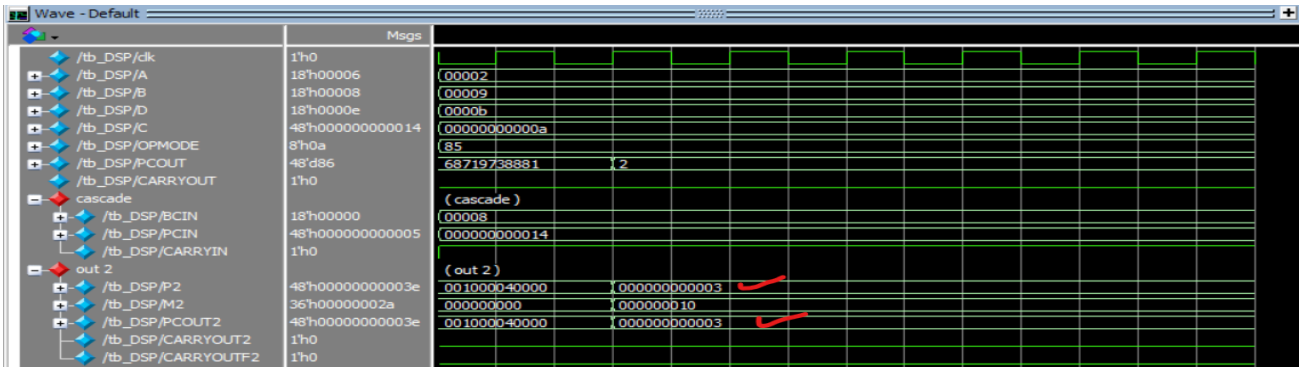


Second test:



third test:

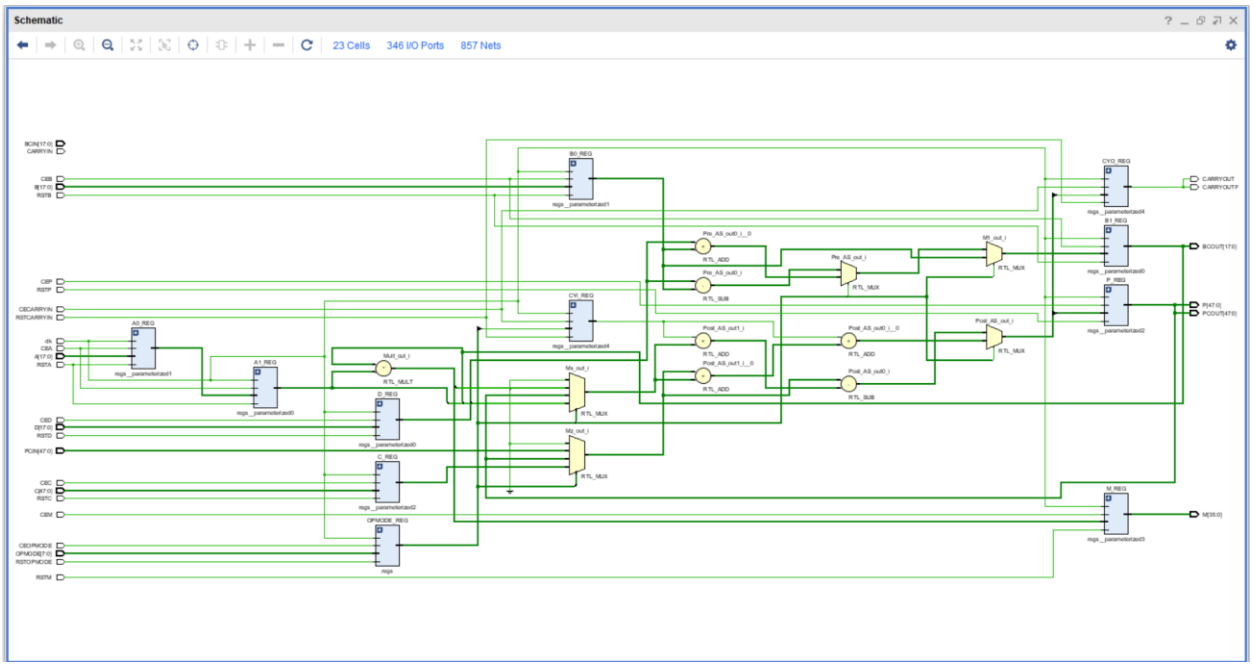
Cascade:

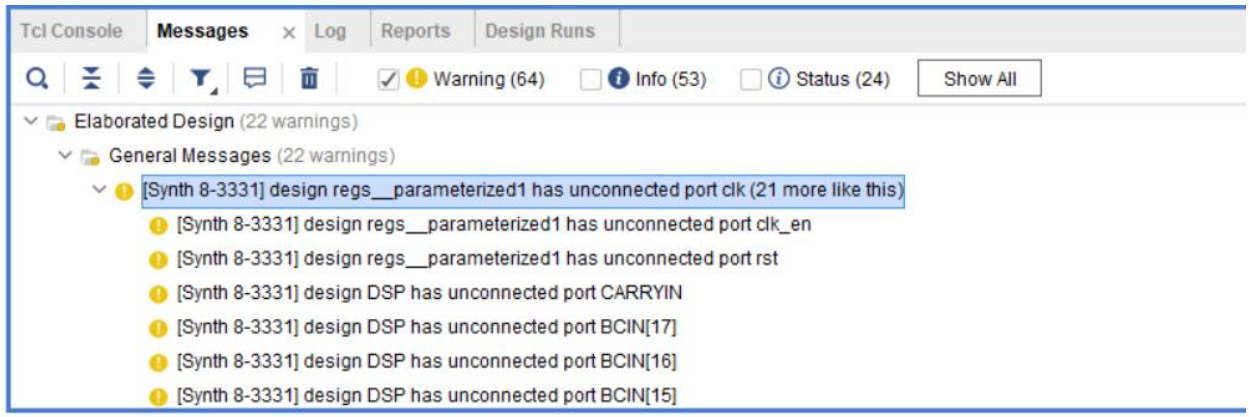


Vivado:

Elaboration:

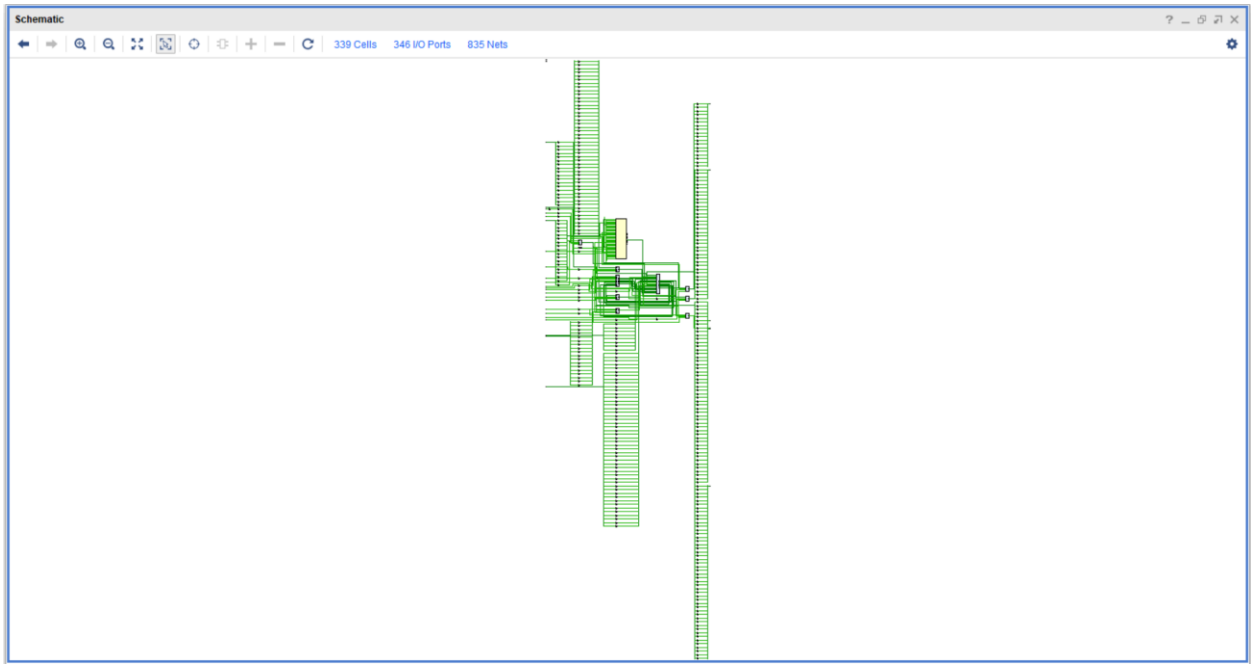
Schematic:

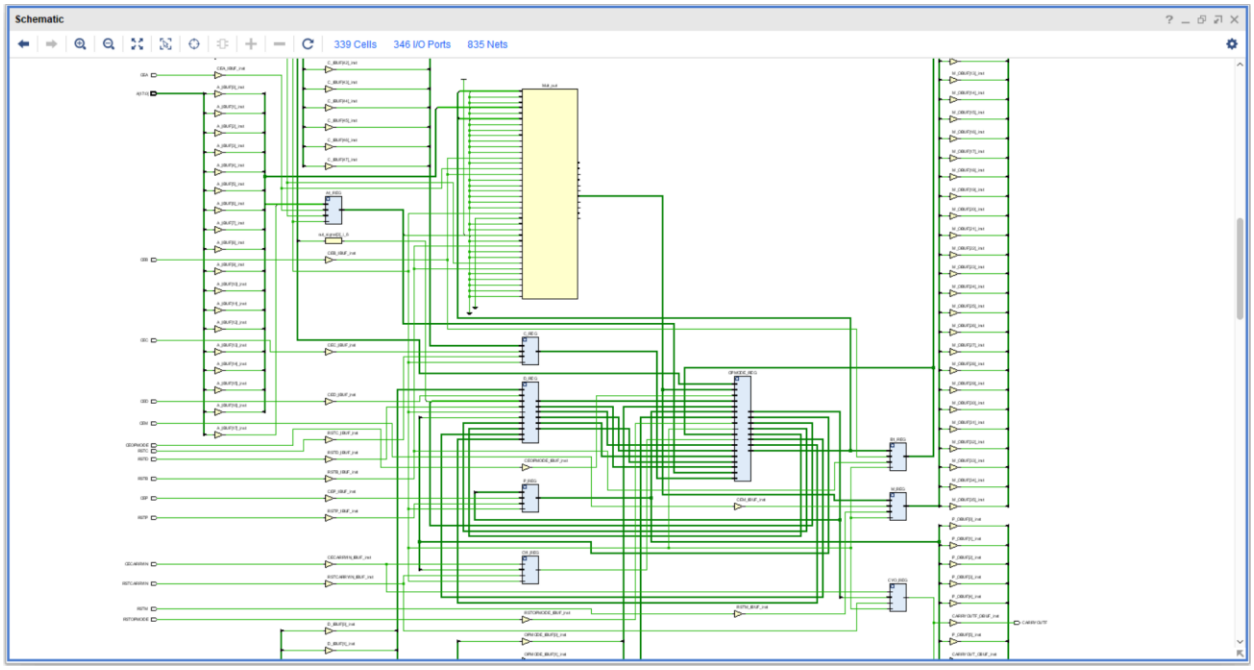




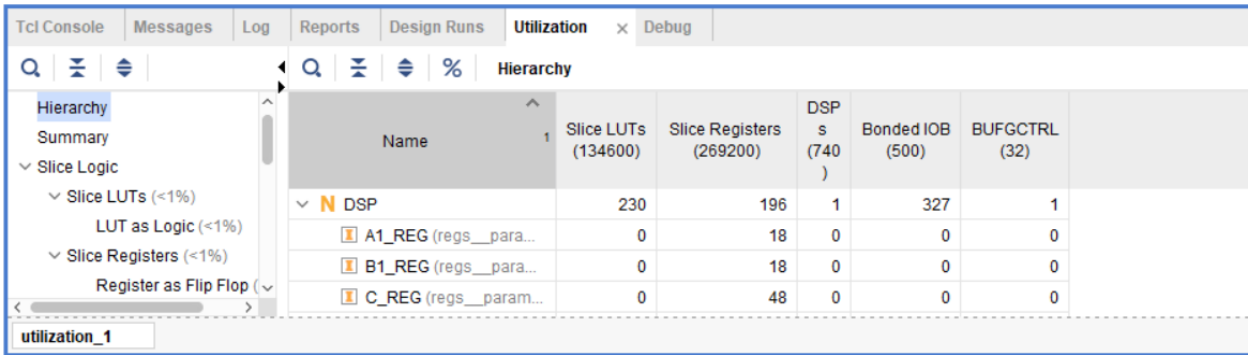
As the parameter default is direct not cascade so the input used in cascade are not used.

Synthesis:

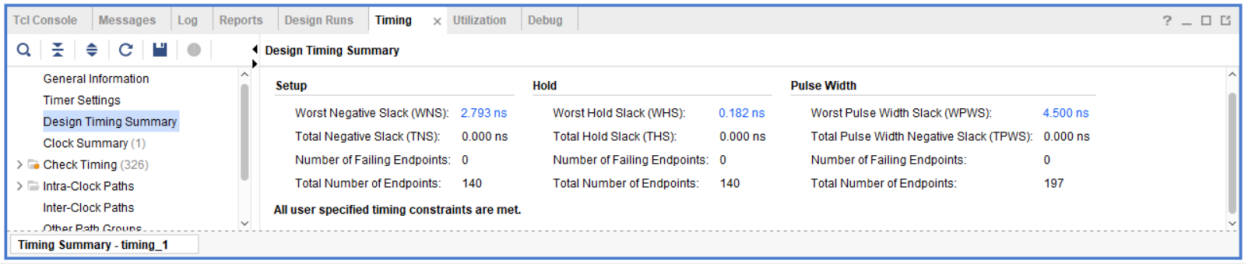

Schematic
339 Cells
346 I/O Ports
835 Nets


Schematic
339 Cells
346 I/O Ports
835 Nets

Utilizations:



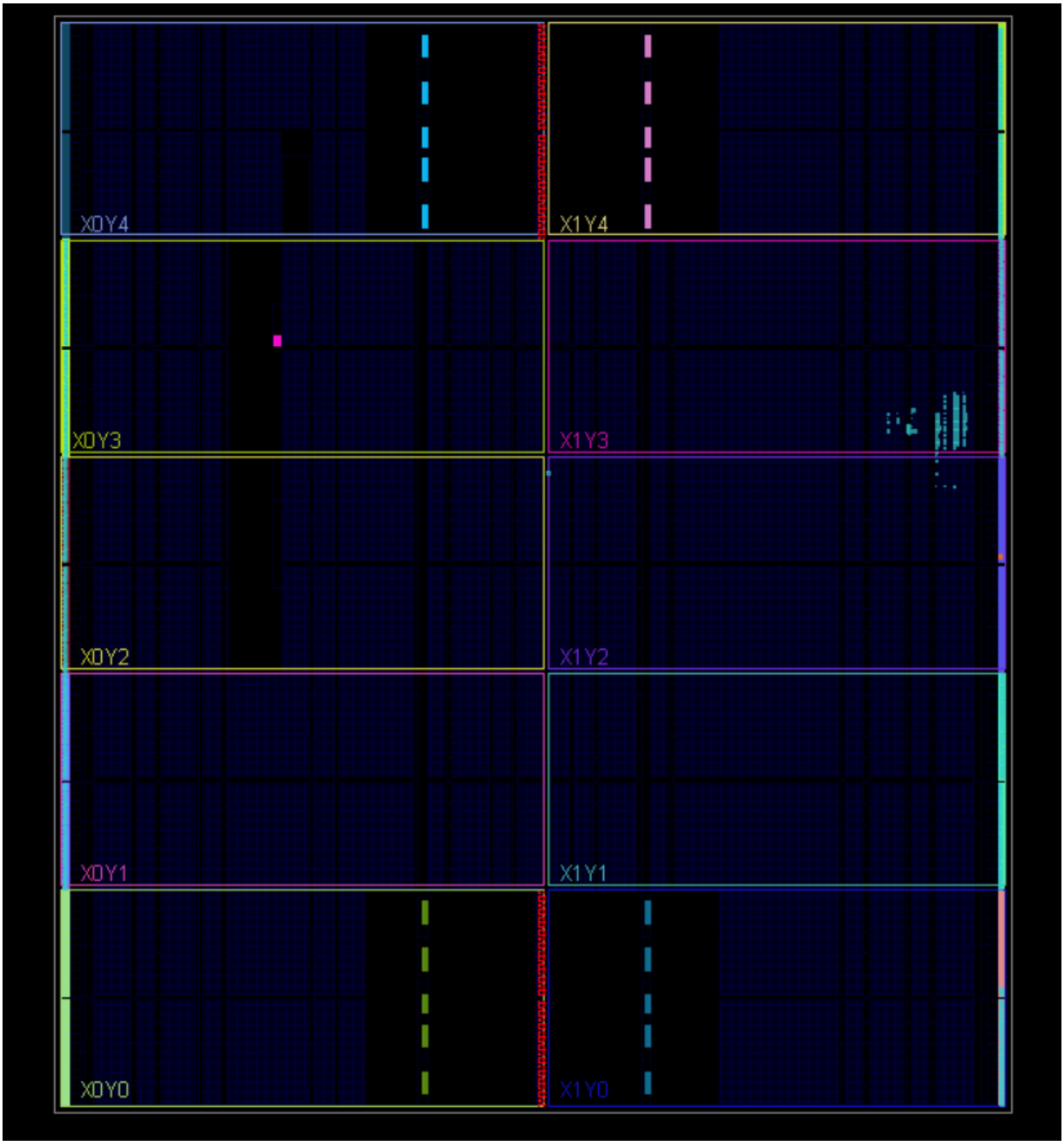
Timing report:



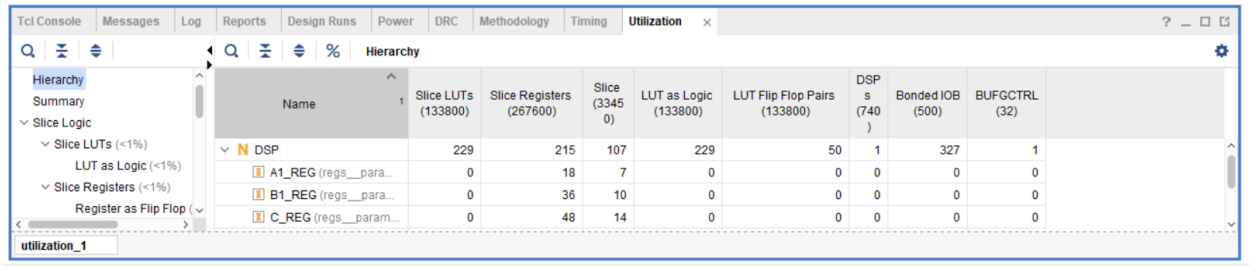
Messages:

Implementation:

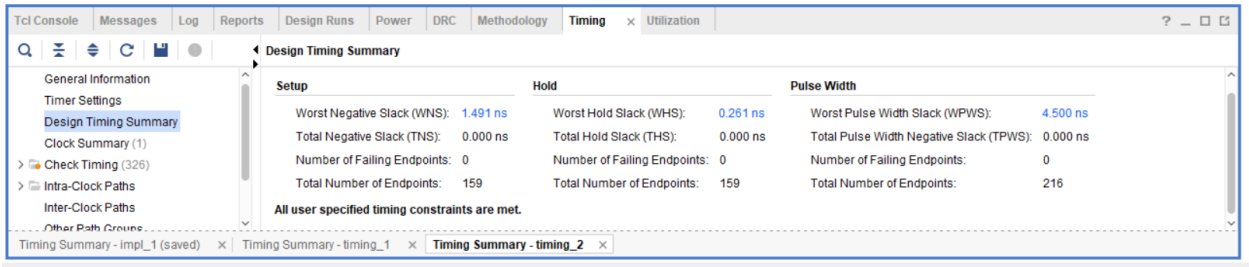
Schematic:



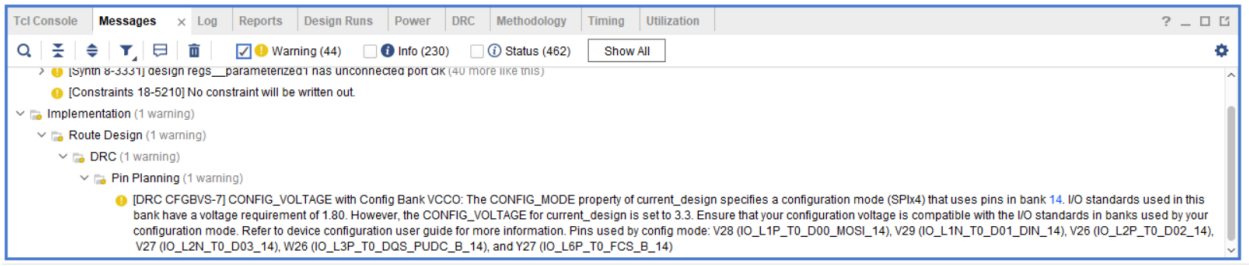
Utilization:



Timing:



Message:



Constrain file: