

Project 2 - SPI Slave with Single Port RAM

Team members:

Omar Ahmed Ragab

Modules:

RAM module:

```
D:\Digital design diploma\Projects\Project2\RAM.v • - Sublime Text (UNREGISTERED)
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SPI_Wrapper_tb.v x | SPI_Wrapper.v x | SPI.v x | SPI_Netlist.v x | untitled ●

1  module RAM(clk,rst_n,rx_valid,din,dout,tx_valid);
2  parameter MEM_DEPTH = 256;
3  parameter ADDR_SIZE = 8;
4  input clk,rst_n,rx_valid;
5  input [ADDR_SIZE+1:0]din;
6  output reg [ADDR_SIZE-1:0]dout;
7  output reg tx_valid;
8
9
10 reg [ADDR_SIZE-1:0]mem[MEM_DEPTH-1:0];
11 reg [ADDR_SIZE-1:0]temp_address;
12
13
14 always @(posedge clk) begin
15     if (~rst_n) begin
16         dout <= 0;
17         tx_valid <= 0;
18         temp_address <= 0;
19     end
20     else begin
21         case(din[9:8])
22             2'b00 : if (rx_valid) begin
23                 temp_address <= din[ADDR_SIZE-1:0];
24                 tx_valid <= 0;
25             end
26             2'b01 : if (rx_valid) begin
27                 mem[temp_address] <= din[ADDR_SIZE-1:0];
28                 tx_valid <= 0;
29             end
30             2'b10 : begin
31                 if (rx_valid) begin
32                     temp_address <= din[ADDR_SIZE-1:0];
33                 end
34             end
35             2'b11 : begin
36                 dout <= mem[temp_address];
37                 tx_valid <= 1;
38             end
39             default : tx_valid <= 0;
40         endcase
41     end
42 end
43 end
44 endmodule
```

SPI module:

```
D:\Digital design diploma\Projects\Project2\SPI.v - Sublime Text (UNREGISTERED)
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SPI_Wrapper_tb.v x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled RAM

1  module SPI(MOSI,SS_n,clk,rst_n,tx_data,tx_valid,MISO,rx_data,rx_valid);
2  parameter IDLE = 3'b000;
3  parameter CHK_CMD = 3'b001;
4  parameter WRITE = 3'b010;
5  parameter READ_ADD = 3'b011;
6  parameter READ_DATA = 3'b100;
7
8  input MOSI,SS_n,clk,rst_n;
9  input [7:0]tx_data;
10 input tx_valid;
11
12 output reg MISO;
13 output reg [9:0]rx_data;
14 output reg rx_valid;
15
16 //(* fsm_encoding = "one_hot" *)
17 reg [2:0]cs,ns;
18
19 reg read;
20 reg [3:0] bit_count;
21 reg [3:0] bit_count2;
22 reg count_switch;
23 reg rx_temp;
24
25
26
27 always @(posedge clk or negedge rst_n) begin
28     if (~rst_n) begin
29         cs <= IDLE;
30     end
31     else begin
32         cs <= ns;
33     end
34 end
35
36
37 always @(*) begin
38     case(cs)
39         IDLE : begin
40             if (SS_n == 1) begin
41                 ns = IDLE;
42             end
43             else begin
44                 ns = CHK_CMD;
45             end
46         end
47         CHK_CMD : begin
48             if (SS_n == 1) begin
```

Line 16, Column 3

```
45         end
46     end
47     CHK_CMD : begin
48         if (SS_n == 1) begin
49             ns = IDLE;
50         end
51         else if (SS_n == 0 && MOSI == 0) begin
52             ns = WRITE;
53         end
54         else if (SS_n == 0 && MOSI == 1 && read == 1) begin
55             ns = READ_DATA;
56         end
57         else if (SS_n == 0 && MOSI == 1 && read == 0) begin
58             ns = READ_ADD;
59         end
60         else begin
61             ns = cs;
62         end
63     end
64     WRITE : begin
65         if (SS_n == 0 && bit_count < 4'd10) begin
66             ns = WRITE;
67         end
68         else begin
69             ns = IDLE;
70         end
71     end
72     READ_ADD : begin
73         if (SS_n == 0 && bit_count < 4'd10) begin
74             ns = READ_ADD;
75         end
76         else begin
77             ns = IDLE;
78         end
79     end
80     READ_DATA : begin
81         if (SS_n == 0 && bit_count2 < 4'd8) begin
82             ns = READ_DATA;
83         end
84         else begin
85             ns = IDLE;
86         end
87     end
88 endcase
89 end
90
```

```
89     end
90
91     always @(posedge clk or negedge rst_n) begin
92         if(~rst_n) begin
93             rx_valid <= 1'b0;
94             rx_data <= 10'b0;
95             bit_count <= 4'b0;
96             bit_count2 <= 4'b0;
97             count_switch <= 1'b0;
98             read <= 1'b0;
99             MISO <= 1'b0;
100         end
101         else begin
102             if(cs == IDLE) begin
103                 rx_valid <= 1'b0;
104                 rx_data <= 0;
105                 bit_count <= 0;
106                 bit_count2 <= 0;
107                 count_switch <= 0;
108             end
109             else if (cs == WRITE) begin
110                 rx_data[9-bit_count] <= rx_temp;
111                 bit_count <= bit_count + 1'b1;
112                 if (bit_count == 4'd9) begin
113                     rx_valid <= 1'b1;
114                 end else begin
115                     rx_valid <= 1'b0;
116                 end
117             end
118             else if(cs == READ_ADD) begin
119                 read <= 1'b1;
120                 rx_data[9-bit_count] <= rx_temp;
121                 bit_count <= bit_count + 1'b1;
122                 if (bit_count == 4'd9) begin
123                     rx_valid <= 1'b1;
124                 end else begin
125                     rx_valid <= 1'b0;
126                 end
127             end
128             else if (cs == READ_DATA) begin
129                 read <= 1'b0;
130                 if (count_switch == 0 && bit_count < 4'd9) begin
131                     rx_data[9-bit_count] <= rx_temp;
132                     bit_count <= bit_count + 1'b1;
133                 end
134                 else if(bit_count == 4'd9) begin
135                     rx_valid <= 1'b1;
136                     count_switch <= 1'b1;
```

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SPI_Wrapper_tb.v x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled RAM.v Constraints

```
125         rx_valid <= 1'b0;
126     end
127 end
128 else if (cs == READ_DATA) begin
129     read <= 1'b0;
130     if (count_switch == 0 && bit_count < 4'd9) begin
131         rx_data[9-bit_count] <= rx_temp;
132         bit_count <= bit_count + 1'b1;
133     end
134     else if (bit_count == 4'd9) begin
135         rx_valid <= 1'b1;
136         count_switch <= 1'b1;
137     end
138     if (bit_count2 < 4'd8 && count_switch == 1 && tx_valid == 1) begin
139         bit_count <= 4'b0;
140         rx_valid <= 1'b0;
141         MISO <= tx_data[7-bit_count2];
142         bit_count2 <= bit_count2 + 1'b1;
143     end
144     else begin
145         MISO <= 1'b0;
146     end
147 end
148 end
149 end
150
151 always @(posedge clk) begin
152     rx_temp <= MOSI;
153 end
154
155 endmodule
```

Wrapper module:

```
D:\Digital design diploma\Projects\Project2\SPI_Wrapper.v - Sublime Text (UNREGISTERED)
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SPI_Wrapper_tb.v x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled RAM

1  module SPI_Wrapper(MOSI,SS_n,clk,rst_n,MISO);
2  input MOSI,SS_n,clk,rst_n;
3  output MISO;
4
5  wire [9:0]rx_data;
6  wire tx_valid,rx_valid;
7  wire [7:0]dout;
8
9
10
11  RAM ram_inst (.clk(clk),.rst_n(rst_n),
12              |.rx_valid(rx_valid),.din(rx_data),
13              |.dout(dout),.tx_valid(tx_valid)
14              );
15
16
17
18  SPI spi_inst (.MOSI(MOSI),.SS_n(SS_n),.clk(clk),.rst_n(rst_n),
19              |.tx_data(dout),.tx_valid(tx_valid),.MISO(MISO),
20              |.rx_data(rx_data),.rx_valid(rx_valid)
21              );
22
23
24
25
26  endmodule
```

Testbench:

```
D:\Digital design diploma\Projects\Project2\SPI_Wrapper_tb.v - Sublime Text (UNREGISTERED)
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SPI_Wrapper_tb.v x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled RAM.v

1  module SPI_Wr_tb();
2
3  reg MOSI;
4  reg SS_n;
5  reg clk;
6  reg rst_n;
7  wire MISO;
8
9
10 SPI_Wrapper DUT (.MOSI(MOSI),.SS_n(SS_n),
11                  .clk(clk),.rst_n(rst_n),.MISO(MISO)
12                  );
13 initial begin
14     clk = 0;
15     forever #5 clk = ~clk;
16 end
17
18 initial begin
19     MOSI = 0;
20     SS_n = 1;
21     rst_n = 0;
22     @(negedge clk);
23     rst_n = 1;
24     @(negedge clk);
25     SS_n = 0;
26     MOSI = 0;
27     @(negedge clk);
28     send_byte(10'h0FC);
29     @(negedge clk);
30     @(negedge clk);
31     @(negedge clk);
32     SS_n = 1;
33     @(negedge clk);
34     SS_n = 0;
35     MOSI = 0;
36     @(negedge clk);
37     send_byte(10'h1B1);
38     @(negedge clk);
39     @(negedge clk);
40     @(negedge clk);
41     SS_n = 1;
42     @(negedge clk);
43     @(negedge clk);
44     @(negedge clk);
45     SS_n = 0;
46     MOSI = 1;
47     @(negedge clk);
48     send_byte(10'h2FC);

```

Line 14, Column 12


```
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SPI_Wrapper_tb.v x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled

41     SS_n = 1;
42     @(negedge clk);
43     @(negedge clk);
44     @(negedge clk);
45     SS_n = 0;
46     MOSI = 1;
47     @(negedge clk);
48     send_byte(10'h2FC);
49     @(negedge clk);
50     @(negedge clk);
51     @(negedge clk);
52     SS_n = 1;
53     @(negedge clk);
54     SS_n = 0;
55     MOSI = 1;
56     @(negedge clk);
57     send_byte(10'h3BC);
58     repeat(14) begin
59         @(negedge clk);
60     end
61
62     SS_n = 1;
63     $stop;
64 end
65
66 task send_bit(input reg data);
67     begin
68         MOSI = data;
69         @(negedge clk);
70     end
71 endtask
72
73 task send_byte(input [9:0] data);
74     integer i;
75     begin
76         for (i = 9; i >= 0; i = i - 1) begin
77             send_bit(data[i]);
78         end
79     end
80 endtask
81
82 endmodule
```

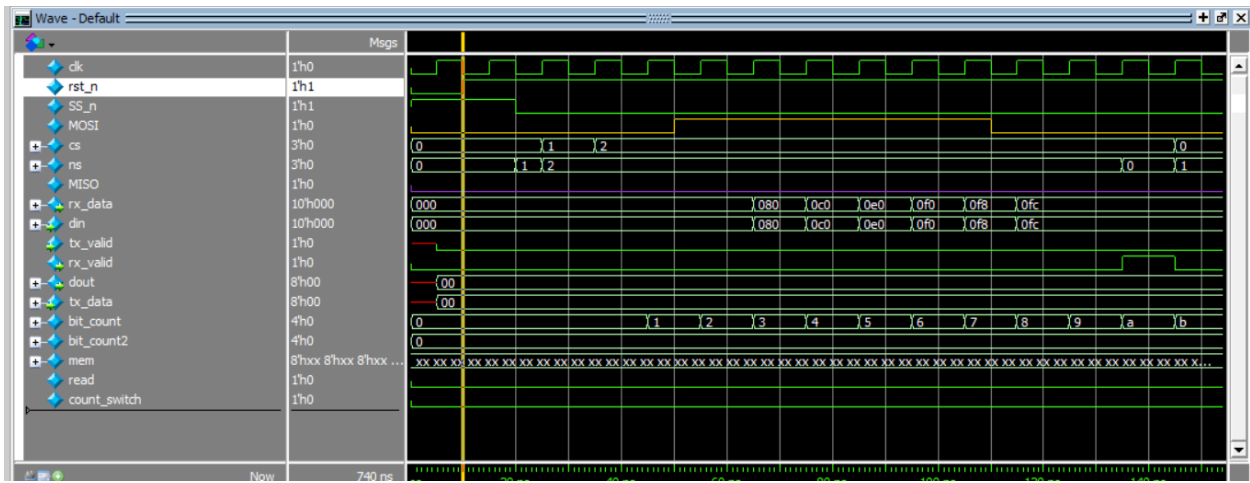
I won't lie I used chat GPT to make a TB for the SPI module alone and know how to make task.

But the overall module (SPI wrapper that connects SPI with RAM) I made myself but took the tasks.

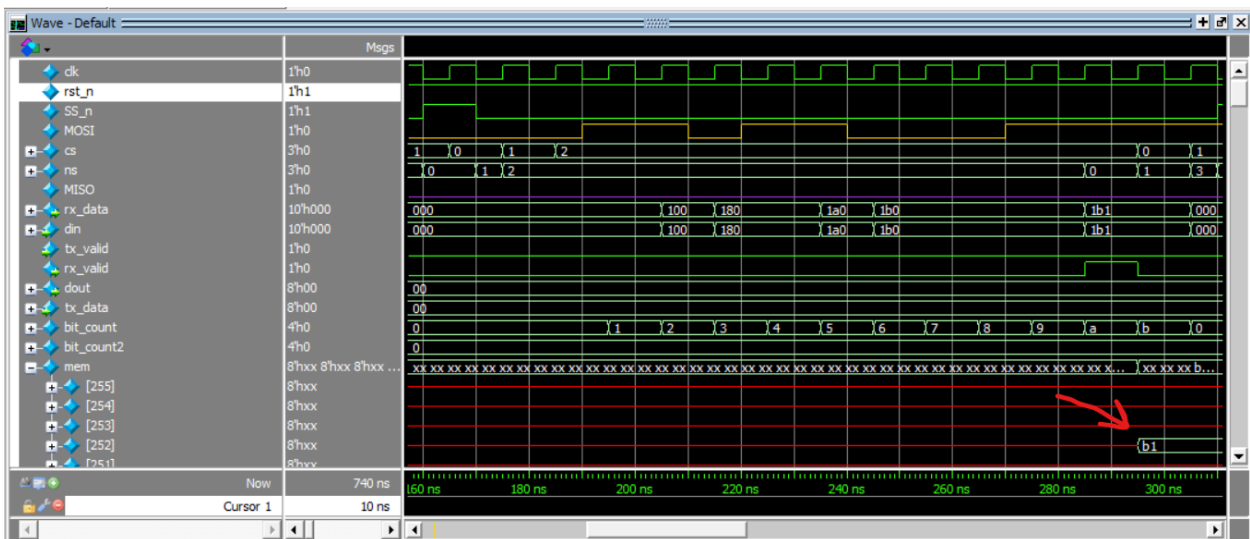
Absolutely all the design I made my self (it took more than 3 days) and it wasn't much helpful as its not trained a lot on the HDLs.

Waveform:

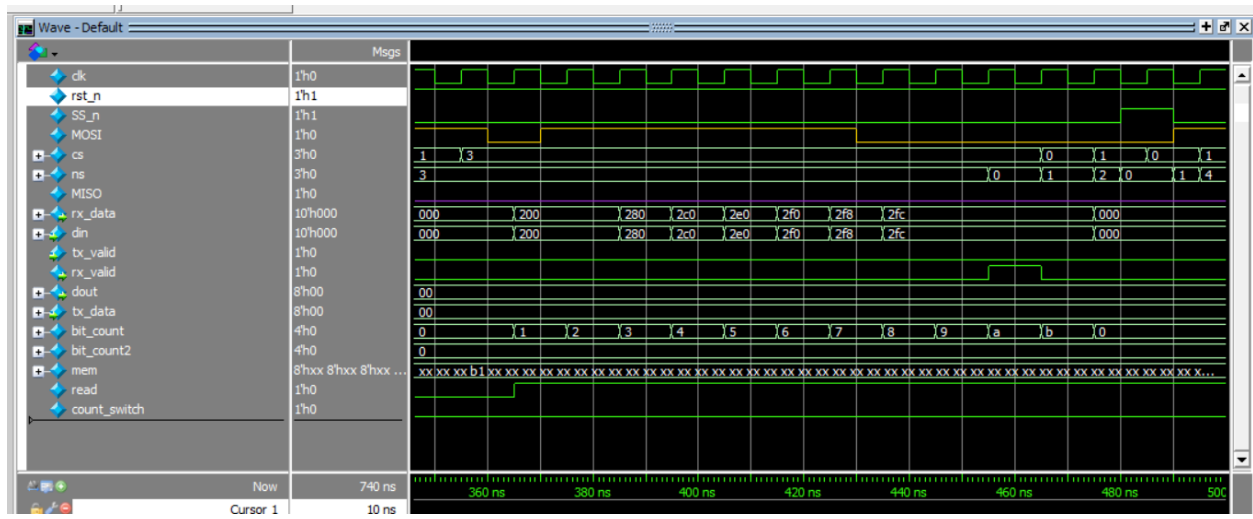
First state:



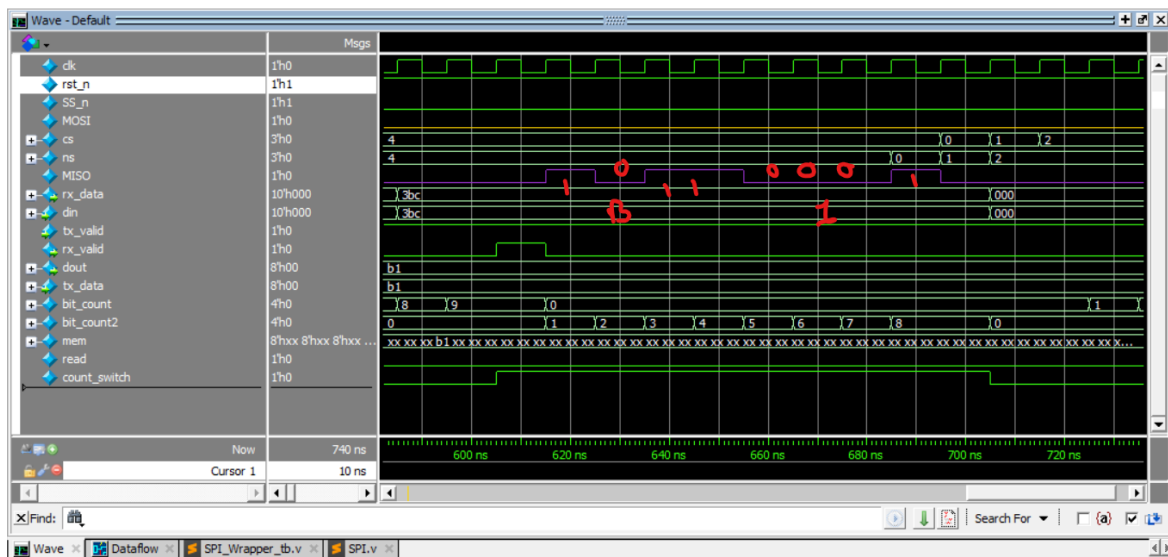
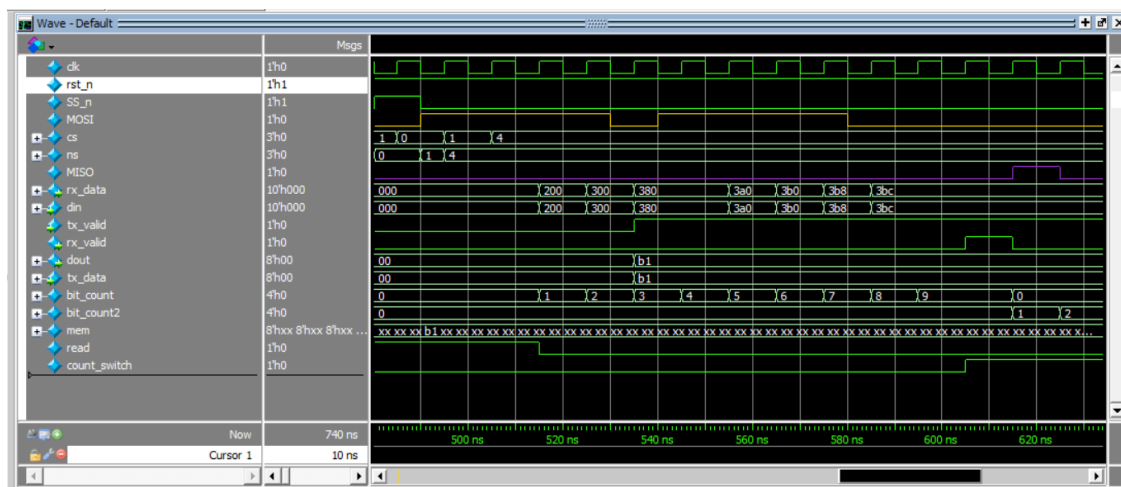
Second state:



third state:

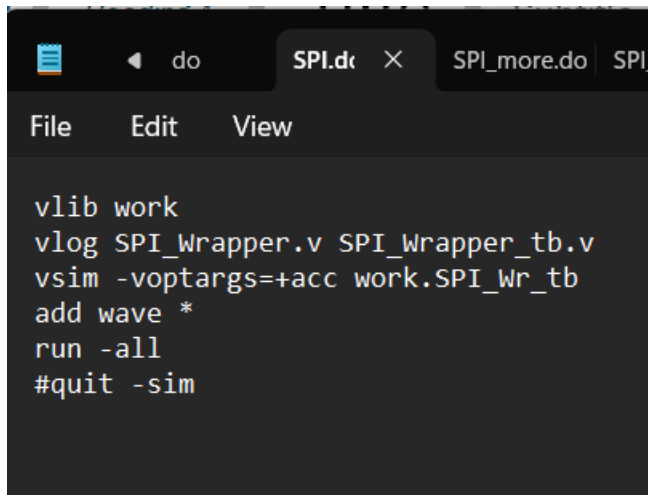


fourth state:



The do file:

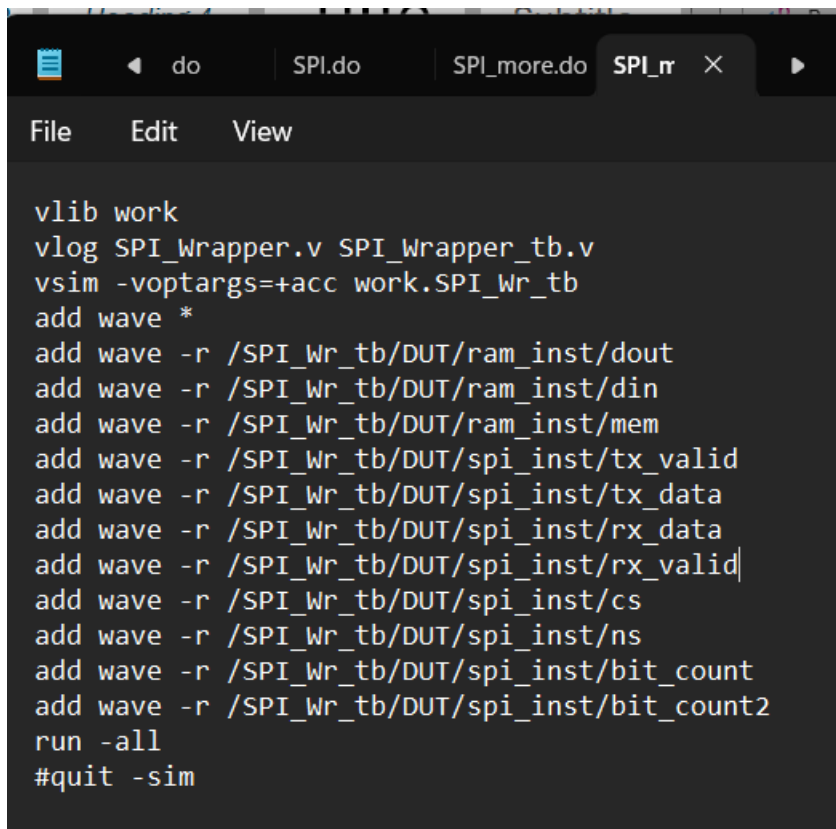
The normal one:



```
vlib work
vlog SPI_Wrapper.v SPI_Wrapper_tb.v
vsim -voptargs=+acc work.SPI_Wr_tb
add wave *
run -all
#quit -sim
```

With more waves for details:

Its name SPI_more.do:



```
vlib work
vlog SPI_Wrapper.v SPI_Wrapper_tb.v
vsim -voptargs=+acc work.SPI_Wr_tb
add wave *
add wave -r /SPI_Wr_tb/DUT/ram_inst/dout
add wave -r /SPI_Wr_tb/DUT/ram_inst/din
add wave -r /SPI_Wr_tb/DUT/ram_inst/mem
add wave -r /SPI_Wr_tb/DUT/spi_inst/tx_valid
add wave -r /SPI_Wr_tb/DUT/spi_inst/tx_data
add wave -r /SPI_Wr_tb/DUT/spi_inst/rx_data
add wave -r /SPI_Wr_tb/DUT/spi_inst/rx_valid
add wave -r /SPI_Wr_tb/DUT/spi_inst/cs
add wave -r /SPI_Wr_tb/DUT/spi_inst/ns
add wave -r /SPI_Wr_tb/DUT/spi_inst/bit_count
add wave -r /SPI_Wr_tb/DUT/spi_inst/bit_count2
run -all
#quit -sim
```

Constrain file:

```
D:\Digital design diploma\Projects\Project2\Constraints_basys3_SPL.xdc - Sublime Text (UNREGISTERED)
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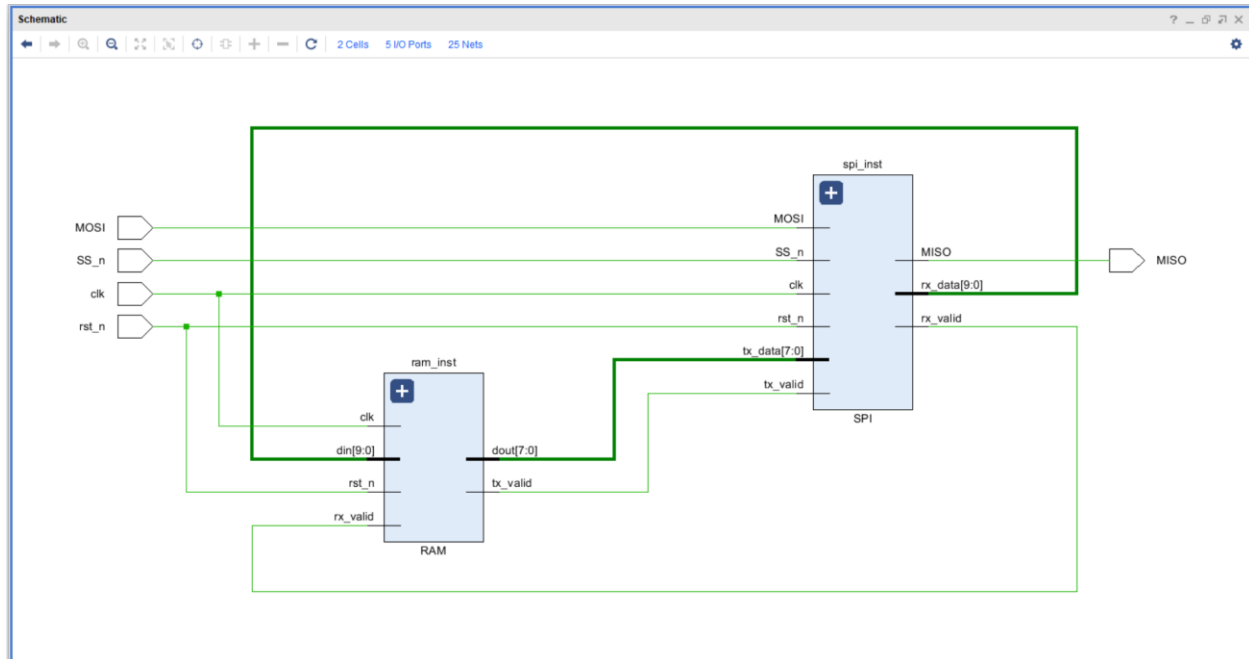
SPL_Wrapper_tb.v x SPL_Wrapper.v x SPL.v x SPI_Netlist.v x untitled RAM.v Constraints_basys3_SPL.xdc

1  ## This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal name
5
6  ## Clock signal
7  ## to choose the clk pin
8  set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
9  ## set the clock
10 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
11
12
13 ## Switches
14 set_property -dict { PACKAGE_PIN V17    IOSTANDARD LVCMOS33 } [get_ports {rst_n}]
15 set_property -dict { PACKAGE_PIN V16    IOSTANDARD LVCMOS33 } [get_ports {SS_n}]
16 set_property -dict { PACKAGE_PIN W16    IOSTANDARD LVCMOS33 } [get_ports {MOSI}]
17 # set_property -dict { PACKAGE_PIN W17    IOSTANDARD LVCMOS33 } [get_ports {A[1]}]
18 # set_property -dict { PACKAGE_PIN W15    IOSTANDARD LVCMOS33 } [get_ports {A[2]}]
19 # set_property -dict { PACKAGE_PIN V15    IOSTANDARD LVCMOS33 } [get_ports {A[3]}]
20 # set_property -dict { PACKAGE_PIN W14    IOSTANDARD LVCMOS33 } [get_ports {B[0]}]
21 # set_property -dict { PACKAGE_PIN W13    IOSTANDARD LVCMOS33 } [get_ports {B[1]}]
22 # set_property -dict { PACKAGE_PIN V2     IOSTANDARD LVCMOS33 } [get_ports {B[2]}]
23 # set_property -dict { PACKAGE_PIN T3     IOSTANDARD LVCMOS33 } [get_ports {B[3]}]
24 # set_property -dict { PACKAGE_PIN T2     IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
25 # set_property -dict { PACKAGE_PIN R3     IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
26 # set_property -dict { PACKAGE_PIN W2     IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
27 # set_property -dict { PACKAGE_PIN U1     IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
28 # set_property -dict { PACKAGE_PIN T1     IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
29 # set_property -dict { PACKAGE_PIN R2     IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]
30
31
32 ## LEDs
33 set_property -dict { PACKAGE_PIN U16    IOSTANDARD LVCMOS33 } [get_ports {MISO}]
34 # set_property -dict { PACKAGE_PIN E19    IOSTANDARD LVCMOS33 } [get_ports {out[1]}]
35 # set_property -dict { PACKAGE_PIN U19    IOSTANDARD LVCMOS33 } [get_ports {out[2]}]
36 # set_property -dict { PACKAGE_PIN V19    IOSTANDARD LVCMOS33 } [get_ports {out[3]}]
37 # set_property -dict { PACKAGE_PIN U18    IOSTANDARD LVCMOS33 } [get_ports {out[4]}]
38 # set_property -dict { PACKAGE_PIN U17    IOSTANDARD LVCMOS33 } [get_ports {out[5]}]
39 # set_property -dict { PACKAGE_PIN U15    IOSTANDARD LVCMOS33 } [get_ports {out[6]}]
40 # set_property -dict { PACKAGE_PIN U14    IOSTANDARD LVCMOS33 } [get_ports {out[7]}]
41 # set_property -dict { PACKAGE_PIN U13    IOSTANDARD LVCMOS33 } [get_ports {out[8]}]
42 # set_property -dict { PACKAGE_PIN U12    IOSTANDARD LVCMOS33 } [get_ports {out[9]}]
43 # set_property -dict { PACKAGE_PIN U11    IOSTANDARD LVCMOS33 } [get_ports {out[10]}]
44 # set_property -dict { PACKAGE_PIN U10    IOSTANDARD LVCMOS33 } [get_ports {out[11]}]
45 # set_property -dict { PACKAGE_PIN U9     IOSTANDARD LVCMOS33 } [get_ports {out[12]}]
46 # set_property -dict { PACKAGE_PIN U8     IOSTANDARD LVCMOS33 } [get_ports {out[13]}]
47 # set_property -dict { PACKAGE_PIN U7     IOSTANDARD LVCMOS33 } [get_ports {out[14]}]
48 #set_property -dict { PACKAGE_PIN D19    IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
49 #set_property -dict { PACKAGE_PIN G18    IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
50 #set_property -dict { PACKAGE_PIN F18    IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
51 #set_property -dict { PACKAGE_PIN K19    IOSTANDARD LVCMOS33 } [get_ports {QspiCSn}]
52
53
54 ## Configuration options, can be used for all designs
55 set_property CONFIG_VOLTAGE 3.3 [current_design]
56 set_property CFGBVS VCCO [current_design]
57
58 ## SPI configuration mode options for QSPI boot, can be used for all designs
59 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
60 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
61 set_property CONFIG_MODE SPIx4 [current_design]
```

Vivado:

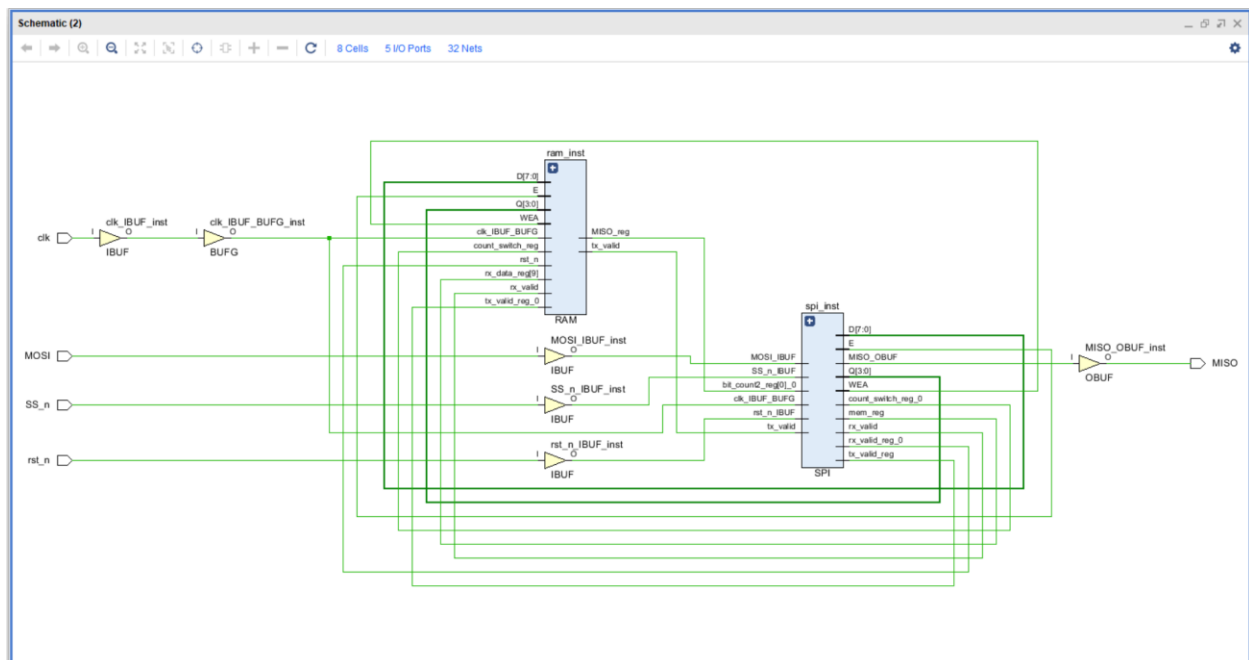
Sequential:

Elaboration design:



Synthesis:

Schematic:



Report:

```
28 INFO: [Synth 8-6157] synthesizing module 'SPI' [D:/Digital design diploma/Projects/Project2/SPI.v:1]
29 Parameter IDLE bound to: 3'b000
30 Parameter CHK_CMD bound to: 3'b001
31 Parameter WRITE bound to: 3'b010
32 Parameter READ_ADD bound to: 3'b011
33 Parameter READ_DATA bound to: 3'b100
34 INFO: [Synth 8-155] case statement is not full and has no default [D:/Digital design diploma/Projects/Project2/SPI.v:38]
35 INFO: [Synth 8-6155] done synthesizing module 'SPI' (2#1) [D:/Digital design diploma/Projects/Project2/SPI.v:1]
36 INFO: [Synth 8-6155] done synthesizing module 'SPI_Wrapper' (3#1) [D:/Digital design diploma/Projects/Project2/SPI_Wrap
37 -----
38 Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 431.047 ; gain = 152.555
```

Timing report:

Design Timing Summary			
General Information	Setup	Hold	Pulse Width
Timer Settings	Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (1)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Check Timing (16)	Total Number of Endpoints: 76	Total Number of Endpoints: 76	Total Number of Endpoints: 38
Intra-Clock Paths	All user specified timing constraints are met.		
Inter-Clock Paths			
Other Path Groups			

Messages:

Tcl Console Messages x Log Reports Design Runs Utilization Timing Debug

Warning (4) Info (47) Status (28) Show All

Synthesis (4 warnings)

- [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [SPLv:41] (2 more like this)
- [Constraints 18-5210] No constraint will be written out

Critical path:

Schematic (2) x

6 Cells 5 Nets

ram_inst

mem_reg

MISO_reg

SPI

RAM

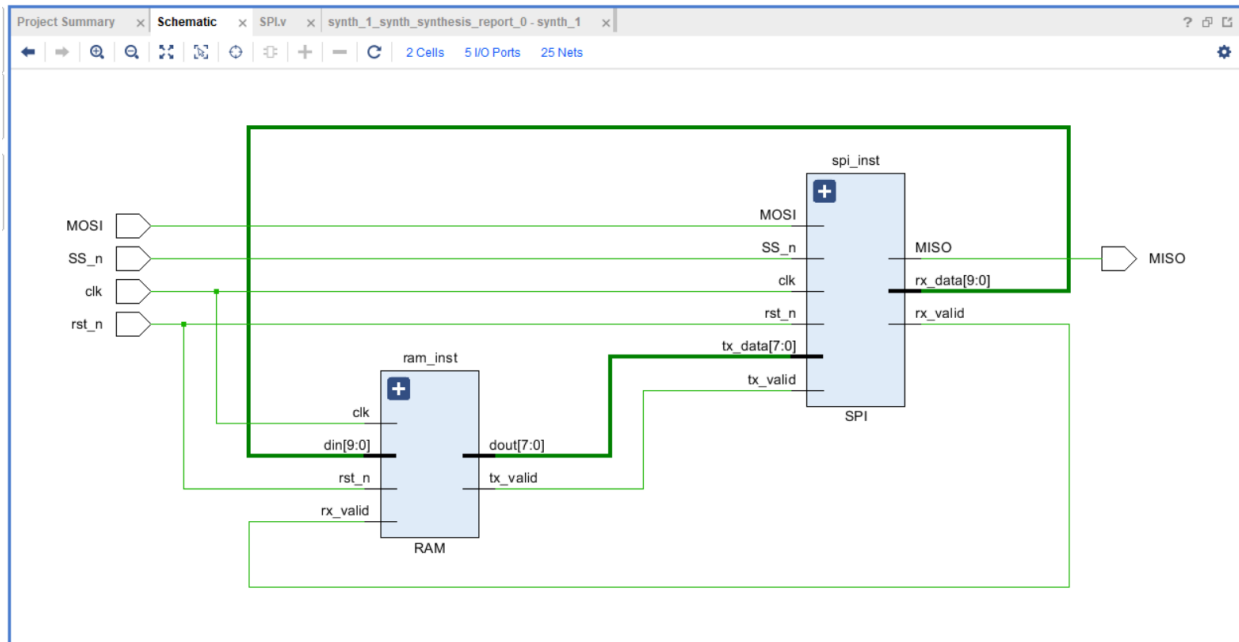
Reports Design Runs Timing x Debug

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.898	2	1	ram_inst/mem..eg/CLKBWRCLK	spl_inst/MISO_reg/D	3.951	2.702	1.249	10.000
Path 2	6.800	2	6	ram_inst/tb_valid_reg/C	spl_inst/bit_count_reg[0]/CE	2.818	0.875	1.943	10.000
Path 3	6.800	2	6	ram_inst/tb_valid_reg/C	spl_inst/bit_count_reg[1]/CE	2.818	0.875	1.943	10.000

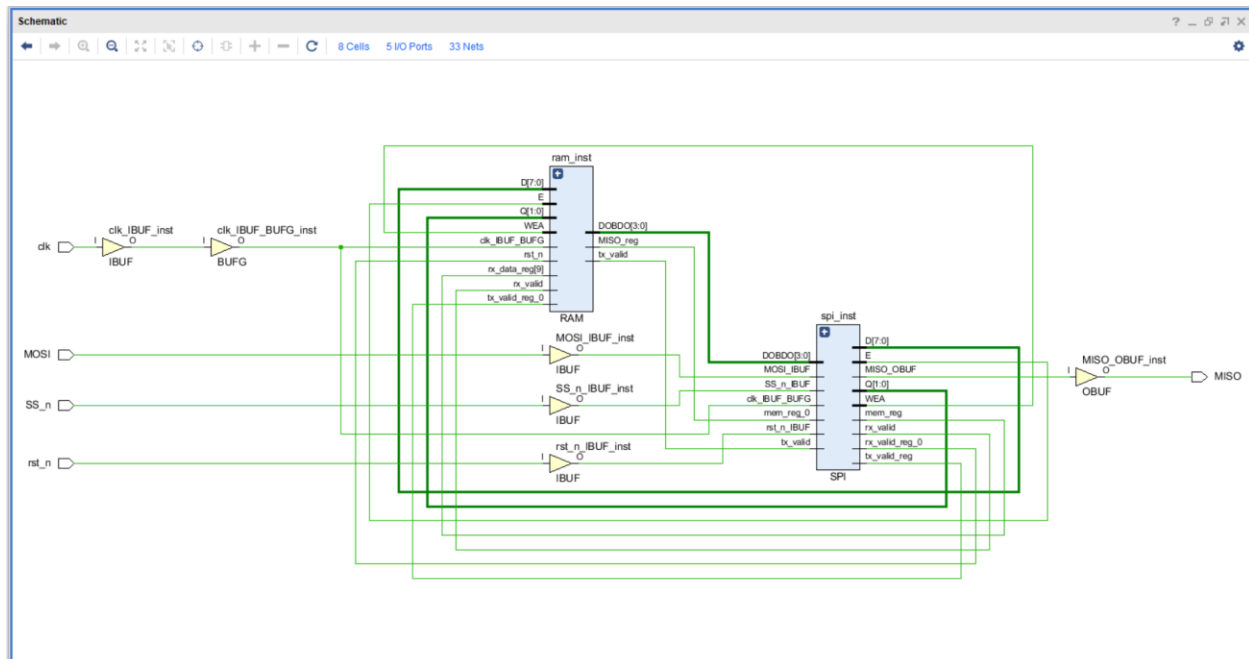
Gray encoding:

Elaboration design:



Synthesis:

Schematic:



Timing report:

Design Timing Summary			
All user specified timing constraints are met.			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 5.236 ns		Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 76		Total Number of Endpoints: 76	Total Number of Endpoints: 38

Report:

```
INFO: [Synth 8-6157] synthesizing module 'SPI' [D:/Digital design diploma/Projects/Project2/SPI.v:1]
Parameter IDLE bound to: 3'b000
Parameter CHK_CMD bound to: 3'b001
Parameter WRITE bound to: 3'b010
Parameter READ_ADD bound to: 3'b011
Parameter READ_DATA bound to: 3'b100
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [D:/Digital design diploma/Projects/Project2/SPI.v:
INFO: [Synth 8-1551] case statement is not full and has no default [D:/Digital design diploma/Projects/Project2/SPI.v:38]
```

Tcl Console Messages x Log Reports Design Runs Timing Debug

Warning (2) Info (48) Status (33) Show All

Synthesis (2 warnings)

- [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [SPI.v:41]
- [Constraints 18-5210] No constraint will be written out.

Critical path:

Schematic (2) x Path 2 - timing_1 x Path 12 - timing_1 x synth_1_synth_synthesis_report_0 - synth_1

6 Cells 5 Nets

ram_inst

mem_reg

spi_inst

MISO_i_3

MISO_i_2

MISO_reg

LUT5

LUT6

SPI

RAM

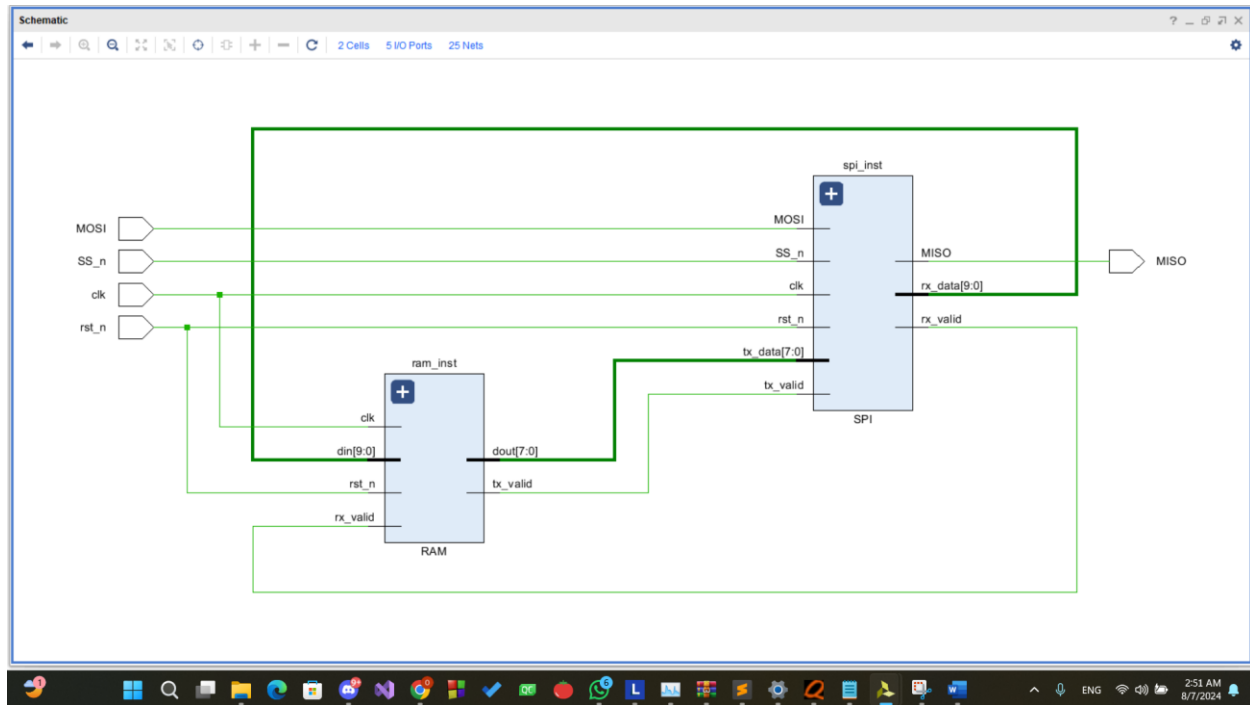
Reports Design Runs Timing x Debug

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.236	2	1	ram_inst/mem_reg/CLKBWRCLK	spi_inst/MISO_reg/D	4.613	2.702	1.911	10.00
Path 2	6.689	3	9	spi_inst/count_switch_reg/C	spi_inst/rx_valid_reg/D	3.160	0.999	2.161	10.00

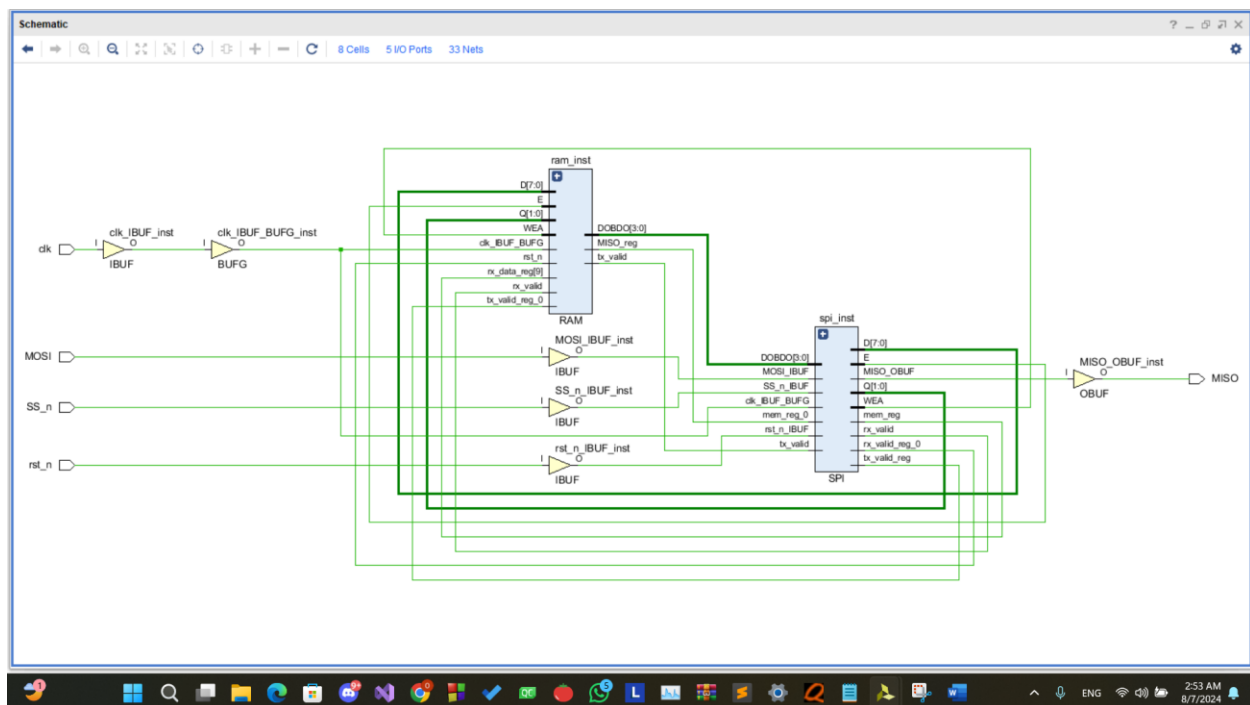
One Hot encoding:

Elaboration design:



Synthesis:

Schematic:



Timing report:

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.236 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 76	Total Number of Endpoints: 76	Total Number of Endpoints: 40
All user specified timing constraints are met.		

Report:

```
6 INFO: [Synth 8-226] default block is never used [D:/Digital design diploma/Projects/Project2/RAM.v:21]
7 INFO: [Synth 8-6155] done synthesizing module 'RAM' (1#1) [D:/Digital design diploma/Projects/Project2/RAM.v:1]
8 INFO: [Synth 8-6157] synthesizing module 'SPI' [D:/Digital design diploma/Projects/Project2/SPI.v:1]
9   Parameter IDLE bound to: 3'b000
10  Parameter CHK_CMD bound to: 3'b001
11  Parameter WRITE bound to: 3'b010
12  Parameter READ_ADD bound to: 3'b011
13  Parameter READ_DATA bound to: 3'b100
14 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [D:/Digital design diploma/Projects/Project2/SPI
15 INFO: [Synth 8-155] case statement is not full and has no default [D:/Digital design diploma/Projects/Project2/SPI.v:38]
```

Messages

Warning (2) Info (48) Status (41) Show All

Synthesis (2 warnings)

- [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [SPI.v:41]
- [Constraints 18-5210] No constraint will be written out.

Critical path:

Schematic (2)

ram_inst

mem_reg

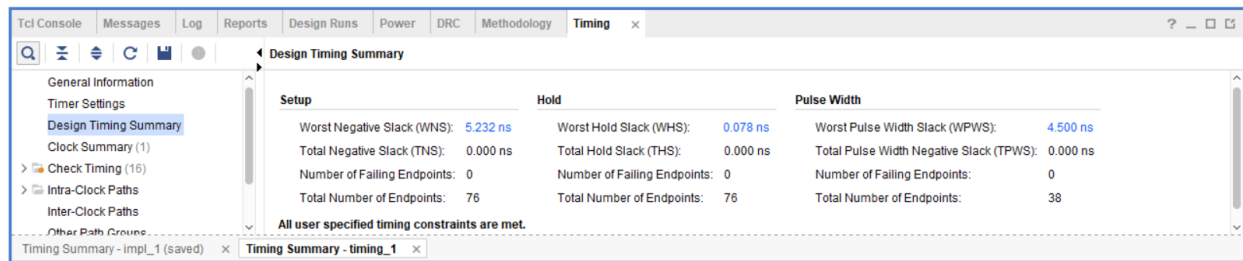
spi_inst

Timing

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.236	2	1	ram_inst/mem_reg/CLKBWRCLK	spi_inst/MISO_reg/D	4.613	2.702	1.911	10.00
Path 2	6.424	3	7	spi_inst/count_switch_reg/C	spi_inst/bit_count_reg[0]/CE	3.194	0.999	2.195	10.00

After implementation I compared between the 3 encoding types:

For gray encoding:

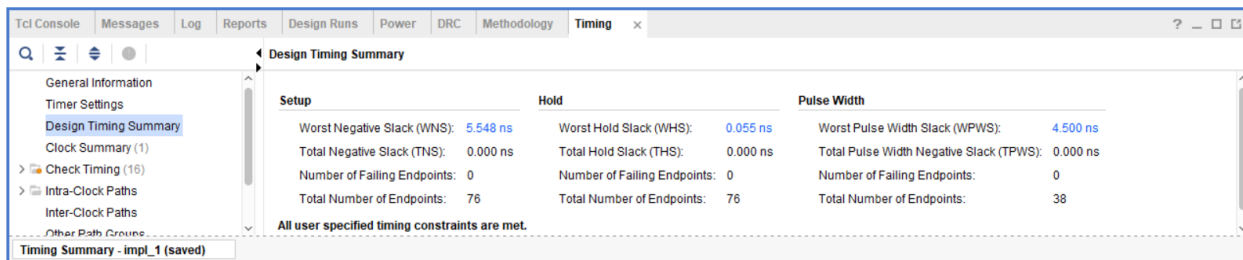


The screenshot shows the 'Design Timing Summary' window for a gray encoding implementation. The window has a sidebar on the left with a tree view containing 'General Information', 'Timer Settings', 'Design Timing Summary' (selected), 'Clock Summary (1)', 'Check Timing (16)', 'Intra-Clock Paths', and 'Inter-Clock Paths'. The main area displays a table with three columns: 'Setup', 'Hold', and 'Pulse Width'. Each column contains four rows of timing data. At the bottom, a status bar indicates 'All user specified timing constraints are met.'.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.232 ns	Worst Hold Slack (WHS): 0.078 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 76	Total Number of Endpoints: 76	Total Number of Endpoints: 38

All user specified timing constraints are met.

For seq encoding:

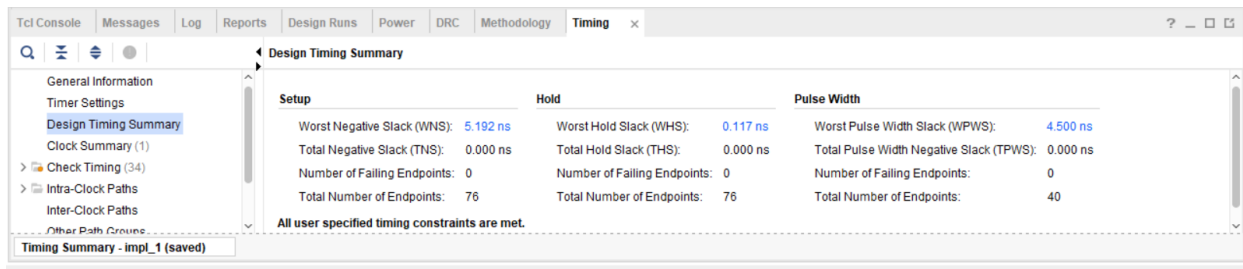


The screenshot shows the 'Design Timing Summary' window for a sequential encoding implementation. The window has a sidebar on the left with a tree view containing 'General Information', 'Timer Settings', 'Design Timing Summary' (selected), 'Clock Summary (1)', 'Check Timing (16)', 'Intra-Clock Paths', and 'Inter-Clock Paths'. The main area displays a table with three columns: 'Setup', 'Hold', and 'Pulse Width'. Each column contains four rows of timing data. At the bottom, a status bar indicates 'All user specified timing constraints are met.'.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.548 ns	Worst Hold Slack (WHS): 0.055 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 76	Total Number of Endpoints: 76	Total Number of Endpoints: 38

All user specified timing constraints are met.

For one_hot encoding:



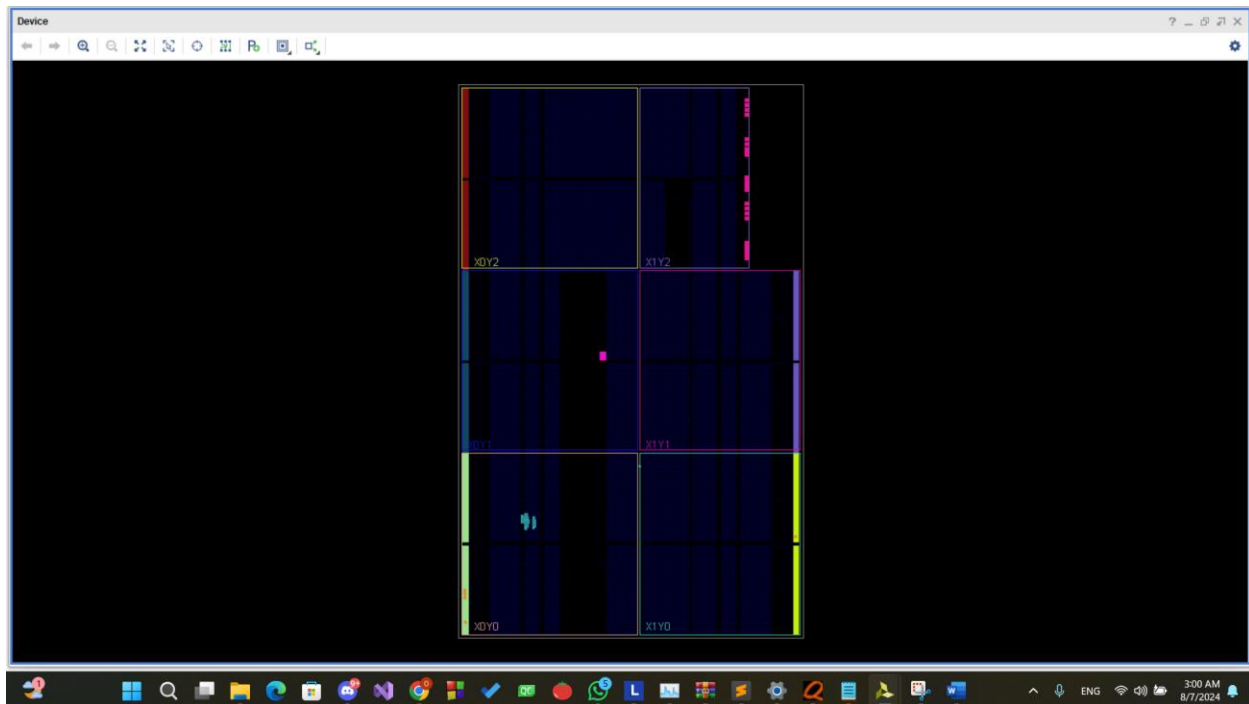
The screenshot shows the 'Design Timing Summary' window for a one-hot encoding implementation. The window has a sidebar on the left with a tree view containing 'General Information', 'Timer Settings', 'Design Timing Summary' (selected), 'Clock Summary (1)', 'Check Timing (34)', 'Intra-Clock Paths', and 'Inter-Clock Paths'. The main area displays a table with three columns: 'Setup', 'Hold', and 'Pulse Width'. Each column contains four rows of timing data. At the bottom, a status bar indicates 'All user specified timing constraints are met.'.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.192 ns	Worst Hold Slack (WHS): 0.117 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 76	Total Number of Endpoints: 76	Total Number of Endpoints: 40

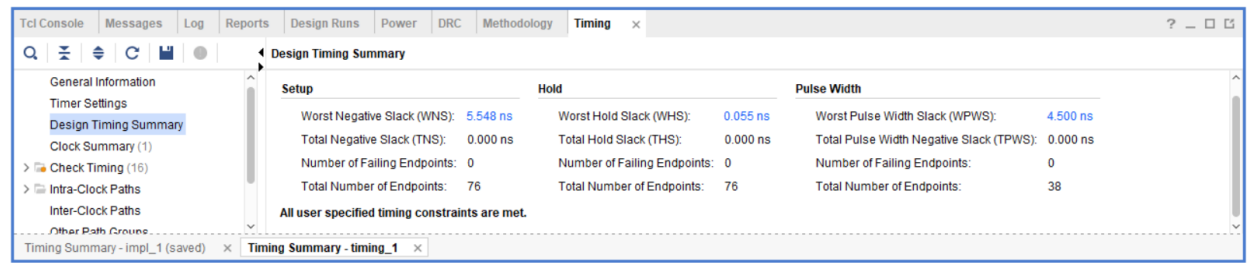
All user specified timing constraints are met.

The sequential showed best setup time slack so, I completed the implementation using sequential.

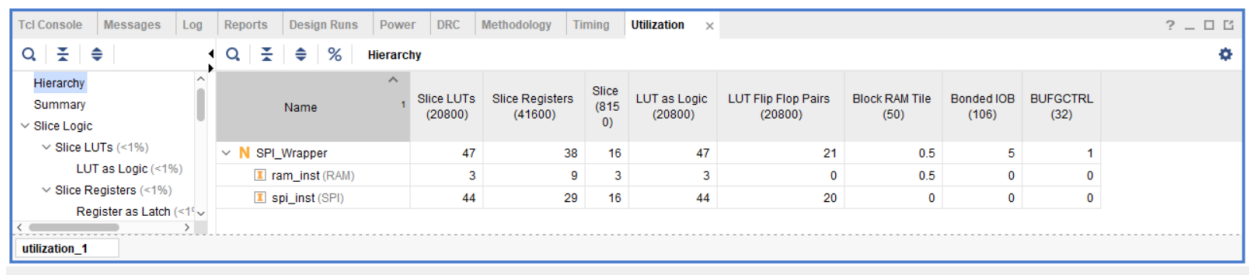
Device:



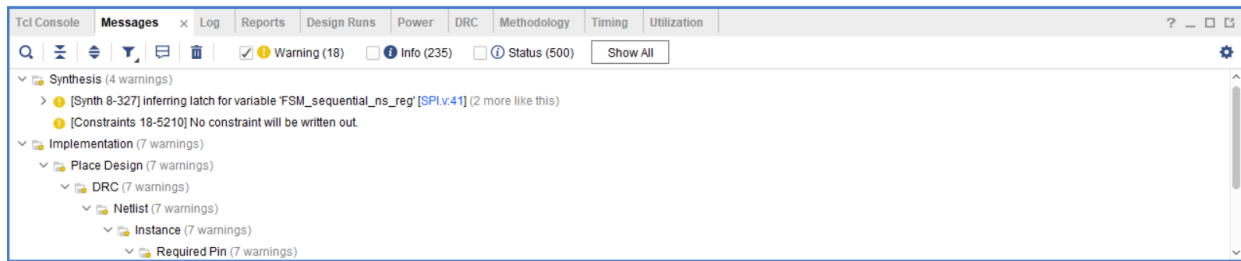
Timing report:



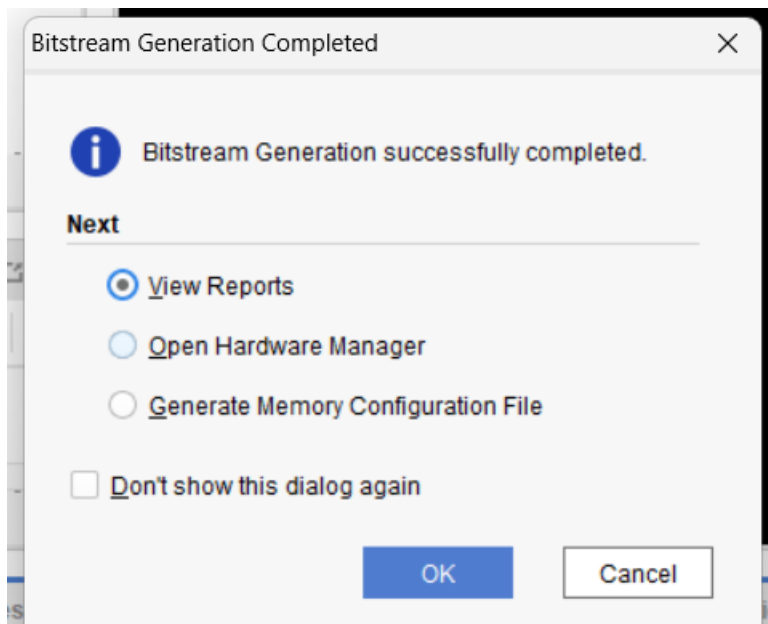
Utilization report:



Messages:



Bitstream:



Netlist:

```
DA:\Digital design diploma\Projects\Project2\SPI_Netlist.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
SPI_Wrapper.tbv x SPI_Wrapper.v x SPI.v x SPI_Netlist.v x untitled x RAM.v x Constraints_bays3_SPl.xdc x Constraints_bays3_DSP.xdc x VM_FSM.v x SPI_1st.v x RAM.tbv x DSP.tbv x D_Splflop.v x I.tbv x

1 // Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
2 //
3 // Tool Version: Vivado v.2018.2 (win64) Build 2258646 Thu Jun 14 20:03:12 PDT 2018
4 // Date : Wed Aug 7 03:06:36 2024
5 // Host : omar_rogab running 64-bit major release (build 9280)
6 // Command : write_verilog (D:/Digital design diploma/Projects/Project2/SPI_Netlist.v)
7 // Design : SPI_Wrapper
8 // Purpose : This is a Verilog netlist of the current design or from a specific cell of the design. The output is an
9 // IIEE 1364-2001 compliant Verilog HDL file that contains netlist information obtained from the input
10 // design files.
11 // Device : xc7a35t1cp236-1L
12 //
13 timescale 1 ps / 1 ps
14
15 module RAM
16 (tx_valid,
17 MISO_reg,
18 clk_IBUF_BUF,
19 rx_valid,
20 \rx_data_reg[9] ,
21 rst_n,
22 D,
23 MEA,
24 tx_valid_reg_0,
25 Q,
26 count_switch_reg,
27 t);
28 output tx_valid;
29 output MISO_reg;
30 input clk_IBUF_BUF;
31 input rx_valid;
32 input \rx_data_reg[9] ;
33 input rst_n;
34 input [7:0]D;
35 input [0:0]MEA;
36 input tx_valid_reg_0;
37 input [3:0]Q;
38 input count_switch_reg;
39 input [0:0]t;
40
41 wire \const0;
42 wire \const1;
43 wire [7:0]D;
44 wire [0:0]t;
45 wire MISO_i_3_n_0;
46 wire MISO_i_4_n_0;
47 wire MISO_reg;
```