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-- Company:

-- Engineer:

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-- Create Date: 22:13:06 11/29/2018

-- Design Name:

-- Module Name: DownCounter - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity DownCounter is

Port (

clk: in STD\_LOGIC;

reset: in STD\_LOGIC;

T\_value:in std\_logic\_vector(7 downto 0);

Load:in STD\_LOGIC;

Dec:in STD\_LOGIC;

Zeroflag:out STD\_LOGIC);

end DownCounter;

architecture Behavioral of DownCounter is

begin

process(clk, reset)

variable counter: std\_logic\_vector(7 downto 0);

variable zero: std\_logic;

begin

if(reset = '1') then

counter := (others=>'0');

elsif(clk' event and clk='1') then

if (Load ='1') then

counter := T\_value;

elsif(Dec='1') then

counter := counter - 1;

if(counter = “0000000”) then

zero:='1';

end if;

end if;

end if;

if(zero = '1') then

counter := (others=>'0');

end if;

end process;

Zeroflag<=zero;

end Behavioral;

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reset <= '1';

wait for clk\_period\*5;

-- count up

reset <= '0';

Load <= '1';

T\_value <= “00001111”;

wait for clk\_period\*20;

-- count down

Dec <= '1';

wait for clk\_period\*20;

-- reset

reset <= '1';

wait for clk\_period\*2;

-- count down after reset

reset <= '0';

wait for clk\_period\*20;

wait for clk\_period\*10;