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CSE 230

CSE/EEE230 Assignment 7
Due April 711:59PM

1. What is the CPI for a single cycle process model?

Single cycle process = 1 instruction per cycle
CPI = cycles per instructions

$$\text{CPI} = \frac{CPU_{time}}{INSTRUCTION\ EXECUTED * CLOCK\ CYCLE\ TIME}$$

CPI = 1

Use the following for problems 2 through 6:

- memory read/writes take 200 ps
- ALU/adder operations take 100 ps
- (each) register read/writes take 75 ps.

R-format: instruction fetch + register read + ALU execution + register write = 200ps + 75ps +100ps + 75ps = 450ps

Lw : instruction fetch + register read + ALU execution + Read memory + register write = 200ps + 75ps +100ps + 200ps + 75ps = 650ps

Sw : instruction fetch + register read + ALU execution + write memory = 200ps + 75ps +100ps + 200ps = 575ps

Beq: instruction fetch + register read + ALU execution = 200ps + 75ps +100ps = 375ps

2. Assume a processor only fetches instructions (in other words, there is no execution of the instructions). Assuming no additional delays, how long is the clock cycle for a single cycle implementation and a fixed length clock?

   Clock Cycle Time:
   For fixed length clock = **200ps**
   Single cycle implementation. = 200ps

3. Assume a processor is only able to support register addressing mode instructions. Assuming no additional delays, how long is the clock cycle for a single cycle implementation and a fixed length clock?

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instruction fetch + register read + ALU execution + register write = 200ps + 75ps +100ps + 75ps = 450ps

4. Assume a processor is only able to support pc-relative addressing mode instructions. Assuming no additional delays, how long is the clock cycle for a single cycle implementation and a fixed length clock?

instruction fetch + register read + ALU execution = 200ps + 75ps +100ps = 375ps

5. Assume a processor is only able to support pseudo-direct addressing mode instructions. Assuming no additional delays, how long is the clock cycle for a single cycle implementation and a fixed length clock?

instruction fetch + register read + ALU execution + write memory = 200ps + 75ps +100ps + 200ps = 575ps

6. Assume a processor supports all instructions and addressing modes. A program consists of 25% store words, 15% load words, 10% branches, 5% jumps and 45% alu operations. Assuming no additional delays, how long is the clock cycle for a single cycle implementation and a fixed length clock?

(0.25*200)+(0.15*75)+(0.1*200)+(0.05*100)+(0.45*100)= **155ps**

7. The control line values are given in Figure 5.18 in your text. For each of the instructions listed (r-type, lw, sw, beq), describe the effect that a single stuck-at-0 fault (the value is always 0) occurs for each of the 9 control lines. For example, RegDst is stuck at 1, but the other control lines have the correct value. Which instruction will work correctly and which will not work correctly and why?

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Q1

Stuck at 0	R format	lw	sw	Beq.
Reg Dst (0)	WILL NOT WORK. reg no. [11-15] needed to be selected.	WORK. register [20-16]	WORK. Always work	WORK
Branch (0)	WORKS. No branching is required	WORK	WORK	WONT WORK. due to AND GATE.
Mem to Reg (0)	WORKS. Not required in memory.	WONT WORK. need to write from memory to register	WORK. • dont need Mem to Reg.	WORK
Reg Write (0)	WONT WORK. Need to write data from memory to register.	WONT WORK	WORK. dont need to write data from memory to register.	WORK
ALU Src (0)	WORK. Always work	WONT WORK. need to select immidiate value as input	WONT WORK	WORK. Always work
Mem Read	WORK. Always work	WONT WORK. require data from memory	WORK. Always work	WORK. Always work
Mem write	WORK. Dont need to read	WORK. write to a register	WONT WORK. need to write in memory.	WORK. dont need memory.

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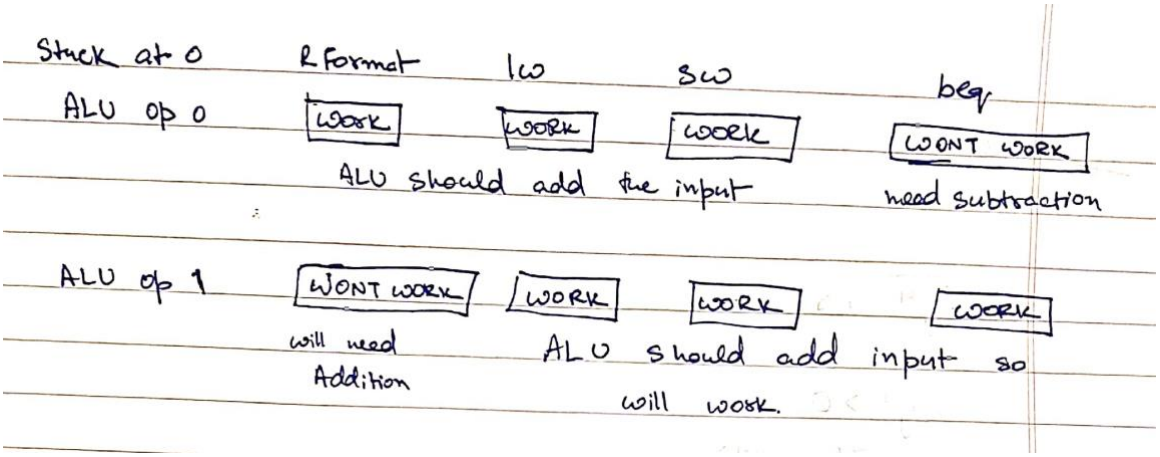

8. Describe what would have to change in the single-cycle processor to implement the jr instruction.

   By adding another control line in the single-cycle processor we can implement the jr instruction.

9. Describe what would have to change in the control for single-cycle processor to implement the addi instruction. Give the values of all 9 control lines for this change.

To implement addi there should be no modifications to path.