

Unit 4. Operational Amplifier

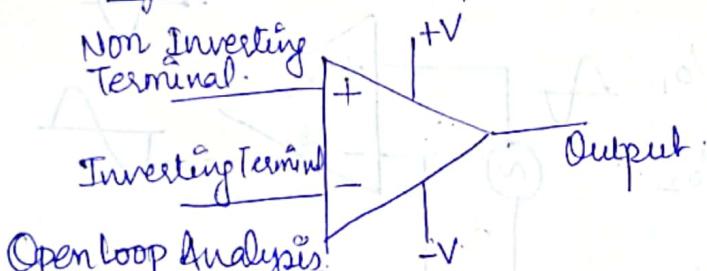
It was introduced in 1940s. The first op-amp was designed in 1948 using vacuum tubes. Op-amp is very high gain differential amplifier with high input impedance and low O/P impedance.

Op-amp consists of many differential amplifier stages to achieve a very high voltage gain.

Features of op-amp

- ① High differential voltage gain
- ② Low common mode gain
- ③ High CMRR
- ④ Two input terminals
- ⑤ High Input Impedance
- ⑥ Large bandwidth
- ⑦ Low Offset Voltage and current
- ⑧ Low output Impedance

Symbol → Basic op-amp

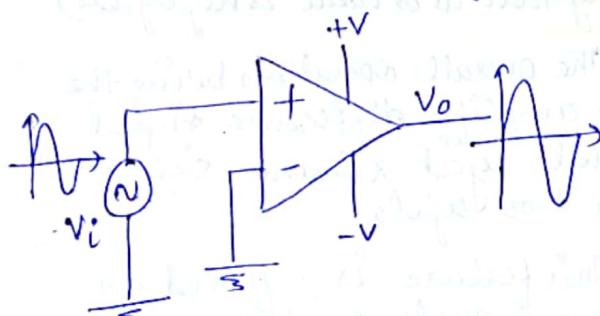


Open Loop Analysis

Single Ended Input → When input signal is connected to one I/P with the O/P Input connected to ground.

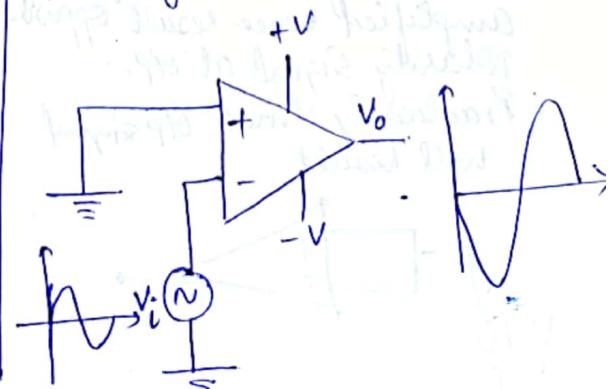
Case 1

When I/P applied to Non-Inverting I/P, O/P will have same polarity as applied at I/P signal.



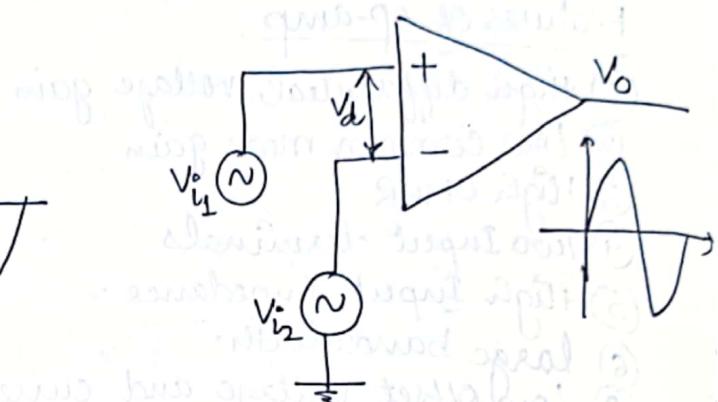
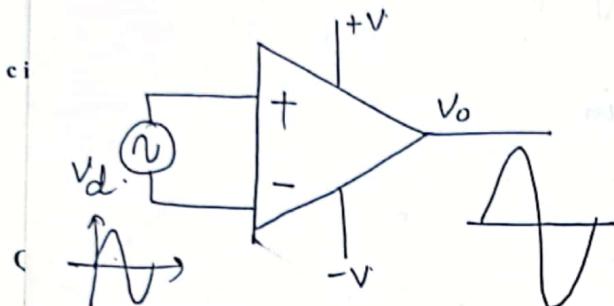
Case 2

When I/P applied to Inverting terminal, O/P will have opposite polarity than applied I/P.

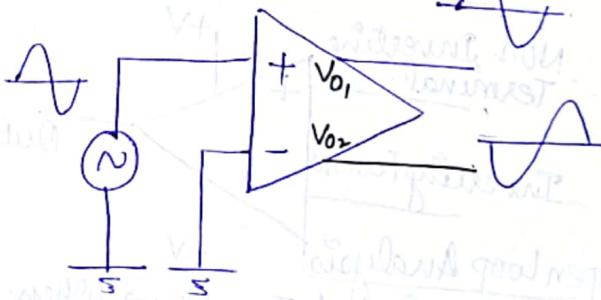
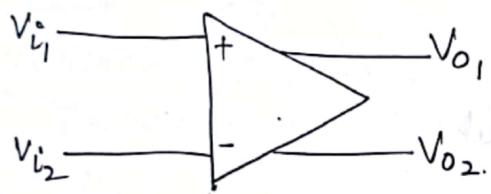


Double Ended (differential) Input :-

When signal is applied at each input, then operation is called as double ended Input operation.
If V_d is applied at input then amplified O/P will be received on other side (in same phase).



Double Ended O/P :-



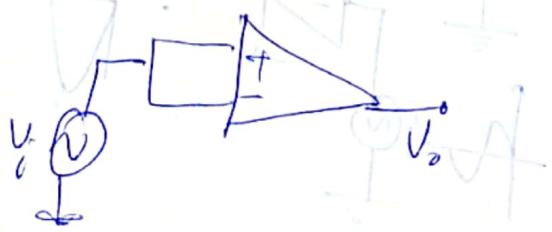
Double ended I/P with double ended O/p.

Common Mode operation:-

When same I/P signals are applied to both I/Ps Common Mode operation results.

Two I/P signals are equally amplified hence result opposite polarity signal at o/p.

Practically small O/P signal will result.



Common-Mode Rejection:-

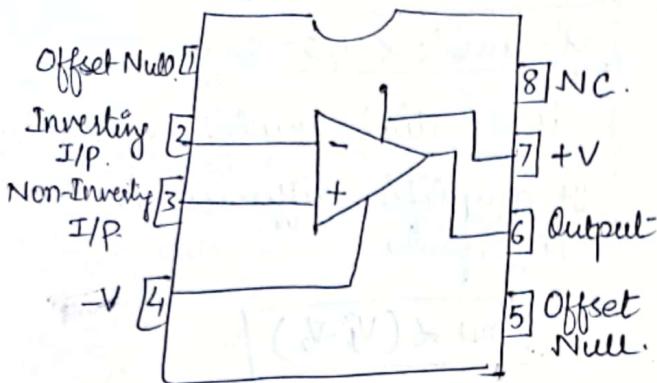
Signals that are ~~opp~~ opposite at I/P are highly amplified. If ~~same~~ same signal appear than O/P is very slightly amplified (or we can say that its ~~is~~ value is negligible)

The overall operation being the to amplify difference signal while reject common signal at the two signals.

This feature is referred as common mode rejection.

21/09

Block Diagram of op-amp (741 IC).



Inverting Terminal :-

If any signal is applied to this terminal O/P will have 180° phase shift or opposite polarity.

Non-Inverting Terminal :-

If any signal is applied to this terminal O/P will be in same polarity.

Offset Null :- To reduce the DC offset value or make it to null value.

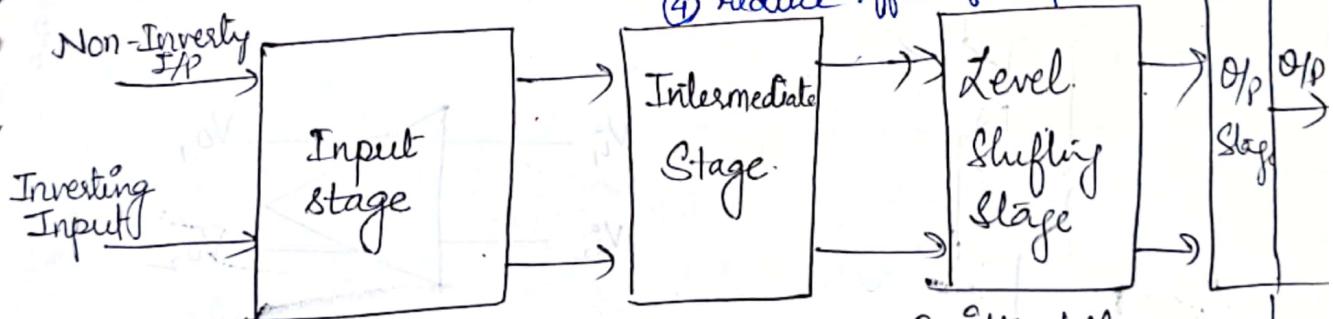
Closed loop :-

Negative Feedback Advantage :- Negative feedback reduces distortion, noise, sensitivity to external changes. It improves system bandwidth.

It provides gain stability (Change in gain reduced).

Block Diagram of an op-amp

- ① It reduces gain improves stability
- ② Reduces distortion
- ③ Increases input impedance
- ④ Reduces effect of temp & increase BW



Dual Input &
Balanced O/P.
differential amp

Dual I/P
unbalanced
O/P differential
amp -

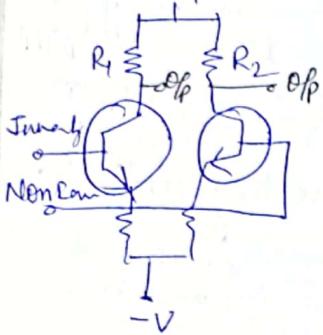
Emitter follower
with
Constant current
source

Complementary
symmetry
push-pull amp.

fig: Block Diagram
of op-amp

Input Stage :-

It provides most of the voltage gain of amplifier.



Intermediate stage :-

- Dual I/P & unbalanced O/P differential amp
- Drives the O/P of 1st stage
- It increases the overall gain

Level shifting stage



emitter follower with constant current source.. To shift DC level to zero w.r.t ground.

Output stage :-

- Complementary push-pull amplifier.
- It increases O/P voltage swing
- Raises current supply capability

→ Low resistance

Parameters of op-amp

Note:- differential amplifier circuit

It amplifies difference b/w two I/P signals.

$$V_{out} \propto (V_1 - V_2)$$

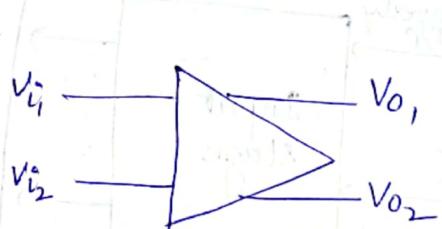
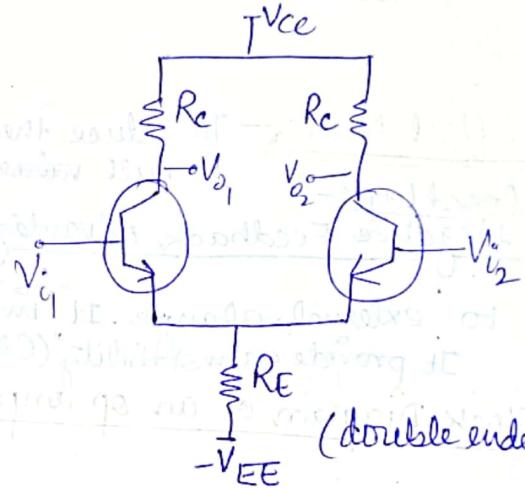
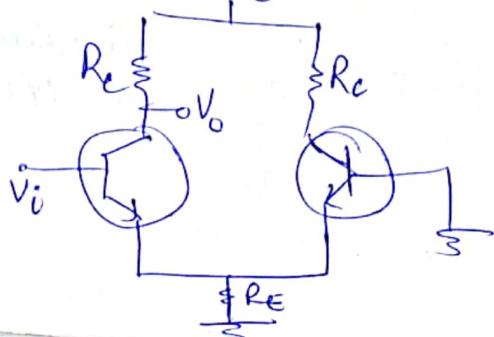


fig:- Basic differential amplifier circuit

If one I/P has app



Parameters

① Differential

When differ op-amp am between two voltage gain gain

$$V_{out} = A_d$$

$$A_d = \frac{V_{out}}{V_{diff}}$$

$$A_d = 20$$

2) Common Mode

If we I/P

If two I/I

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o is calle

signal

$$V_i$$

$$V_{out}$$

$$A$$

$$V_{out} =$$

Parameters of op-amp

① Differential gain (A_d):-

When differential amplifier or op-amp amplifies the difference between two input signal then voltage gain is called as differential gain.

$$V_{out} = A_d (V_1 - V_2)$$

$$A_d = \frac{V_{out}}{V_1 - V_2}$$

$$A_d = \frac{V_{out}}{V_{diff}}$$

$$A_d = 20 \log_{10} (A_d) \text{ dB.} \quad (\text{decibel})$$

2) Common Mode Gain

If two I/P

If two I/P signals are equal in all aspects to op-amp i.e. $V_1 = V_2$. Then ideally O/P must be zero. But practically V_o does not only depends of $V_1 - V_2$ but also depends on avg common level of two I/Ps. Such an avg of two I/Ps is called as common mode signal (V_{cm}).

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$V_{out} = V_{cm} A_{cm}$$

$$A_{cm} = \frac{V_{out}}{V_{cm}} \quad \text{Common Mode gain}$$

$$V_{out} = A_d V_{diff} + A_{cm} V_{cm}$$

3) Common Mode Rejection Ratio

The ability of op-amp to reject common mode signal is expressed by a ratio denoted by common mode rejection ratio (CMRR).

$$\boxed{CMRR = \frac{A_d}{A_{cm}}}$$

It is defined as a ratio of differential mode gain to common mode gain.

$$\boxed{CMRR \text{ in dB} = 20 \log_{10} \frac{A_d}{A_{cm}}}$$

offset current & voltages, Bias current

- i) Input Offset Voltage
- ii) O/P offset Voltage
- iii) Input offset Voltage
- iv) Input bias current

Input offset Voltage :- (V_{IO})

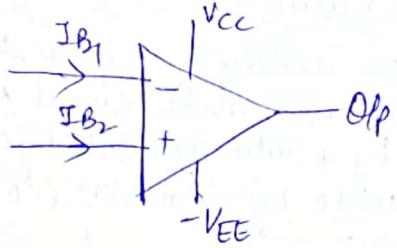
Due to certain unavoidable imbalance in the circuitry specially at I/P stage of op-amp. Even at zero input voltage, O/P is non-zero.

The small differential voltage at I/P of op-amp make O/P voltage zero is called as input offset voltage (V_{IO}). It is temp dependent quantity

$$\boxed{V_{IO} = V_{dc_1} - V_{dc_2}}$$

It is usually in mV

If offset current.



Ideally I_B1 & I_B2 should be equal. but practically due to circuit imbalances they are different.

The algebraic difference b/w currents into the inverting & non-inverting terminals is called as Input offset current (V_{IO}). (I_{FO})

$$|I_{j0}| = |I_{B_1} - I_{B_2}|.$$

I_B \rightarrow current flowing through non-magnetic levied

$I_{B_2} \rightarrow$ river

It is in nAs.

OIP offset Voltage:-

Ideally when both inputs are zero, O/P must be zero. But both input voltage & bias current contribute to produce o/p voltage at zero I/P. This voltage at O/P is called as O/P offset voltage.

Input Bias currents

Input bias current I_B is ~~an~~ the avg of the currents that flows into the inverting & non-inverting terminals.

$$I_B = I_{B_1} + I_{B_2}$$

J_B , & J_{B_2}

Ques The currents at the input of op-amp are 18 μ A & 22 μ A . Calculate :

- i) Bias current.
 - ii) I_P offset current.

PSRR

It is the ratio
I/p offset vol
in supply
power supp
it is also known
sensitivity

$$PSRR =$$

PSRR :

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time.

Slew Re

Bandwī

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of I/p sig
O/p can

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power b

PSRR

It is the ratio of change in I/P offset voltage due to change in supply voltage keeping other power supply voltage constant. It is also known as power supply sensitivity.

$$PSRR = \frac{\Delta V_{IO}}{\Delta V_{CC}} \quad | V_{EE} \rightarrow \text{const.}$$

$$PSRR = \frac{\Delta V_{IO}}{\Delta V_{EE}} \quad | V_{CC} \rightarrow \text{const.}$$

It is expressed in mV/V & μV/mV

Slew Rate (SR)

It is defined as the maximum rate of change of O/P voltage with time.

$$\boxed{\text{Slew Rate (s)} = \frac{dV_{out}}{dt} \text{ max}}$$

unit → V/μs.

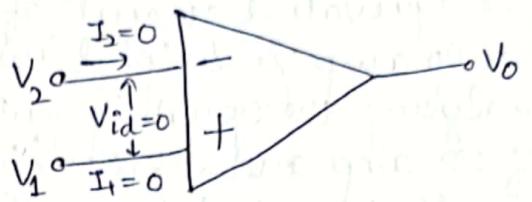
Bandwidth or Max signal freq

It is a max allowable freq. of I/P signal at which undistorted O/P can be obtained.

$$\boxed{f_m = \frac{S}{2\pi V_m}}$$

It is also known as full power bandwidth.

Ideal op-amp



→ It draws no current at both I/P terminals $I_1 = I_2 = 0$

→ Gain ∞

→ $V_{id} = 0$

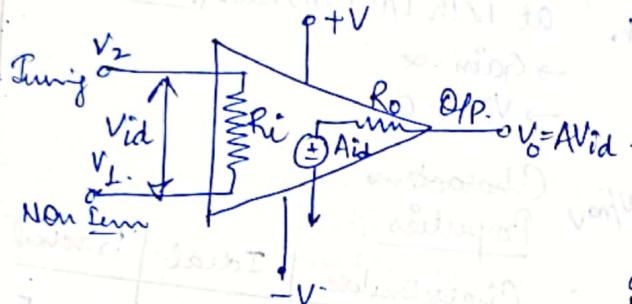
Characteristics Properties

Characteristics	Ideal	Practical
① Open loop voltage gain (A_v)	$A_v \infty$	2×10^5
② O/P Impedance (R_o)	0	75Ω
③ I/P Impedance (R_i)	∞	$2 M\Omega$
④ I/P offset current (I_{IO})	0	$200 nA$
⑤ I/P offset Voltage (V_{IO})	0	$2 mV$
⑥ Bandwidth	∞	$1 MHz$
⑦ CMRR.	∞	$90 dB$
⑧ Slew Rate	∞	$0.5V/\mu s$
⑨ Input bias current	0	$80 nA$
⑩ PSRR	0	$30 dB/V$

Ideal Equivalent Circ

Equivalent circuit of op-amp

The equivalent circuit of an op-amp is helpful in analysing the operating principle of op-amp and in observing the effect of feedback.



$R_o \rightarrow$ Thevenin Equivalent Resistance.

$$V_o = A V_{id}$$

$$V_{id} = V_1 - V_2$$

$$V_o = A(V_1 - V_2)$$

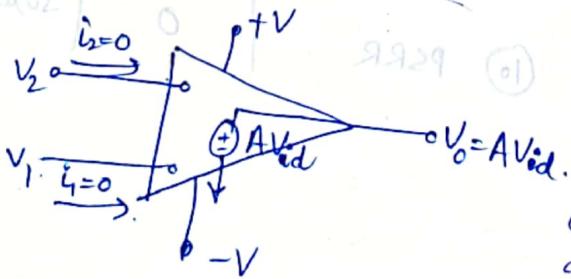
$A =$ Large-signal voltage gain

V_1 = Voltage at Non-Inverting terminal

$V_2 = \dots$, Inverting terminal

$V_{id} =$ differential I/p voltage

Ideal op-amps:-



- Ideal op-amp has no I/p current because I_{IP} resistance is infinite.
- O/P Resistance = 0

Clo:

① I



Virtual Ground Concept & Virtual Short

If one I/p terminal is geo.

According to the concept of virtual short, the potential difference b/w the two I/p. terminals of an op-amp is almost zero. In other words both the I/p terminal are at same I/p.

$$A_d = \frac{V_o}{V_d} = \infty$$

$$A_d = \infty$$

$$\therefore V_{id} = 0$$

$$V_1 - V_2 = 0$$

$$\boxed{V_1 = V_2}$$

Limitations of Open-loop op-amp:-

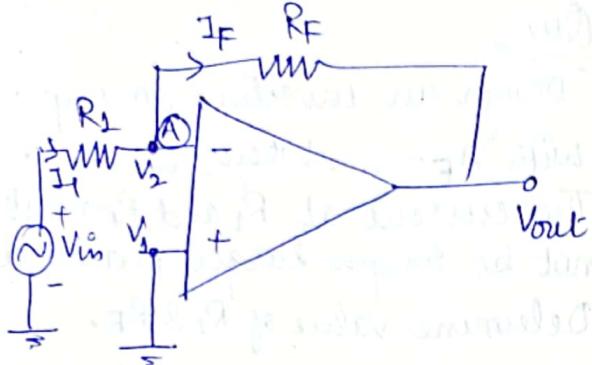
When op-amp is operated in open-loop configuration, the O/p is either positive saturation or negative saturation or switches b/w these two levels.

Therefore for this configuration op-amp may not be used for linear applications.

It is certainly used for non-linear application like, square wave generation, astable multivibrator etc.

Closed loop op-amp

① Inverting amplifier



$$A_v = \frac{V_{out}}{V_{in}}$$

$$V_{id} = V_1 - V_2$$

$$A_v = \infty \therefore V_{id} = 0$$

$$\boxed{V_1 = V_2}$$

by concept of virtual ground
also $\boxed{V_1 = V_2} = 0$

$$I_1 = \frac{V_{in} - 0}{R_1}$$

$$I_2 = \frac{V_2 - V_{out}}{R_2} = \frac{0 - V_{out}}{R_2}$$

by KCL at point A,

$$I_1 = I_2$$

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_2}$$

$$\boxed{V_{out} = -\frac{R_2}{R_1} V_{in}}$$

Closed loop gain A_F ,

$$\boxed{A_F = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}}$$

→ Closed loop gain of inverting amplifier can be changed by simply changing the values of two resistors.

→ Minus sign indicate that close loop amplifier provide signal inversion.



Ques Design an inverting op-amp amplifier circuit with a voltage gain of $A_F = \frac{V_o}{V_i} = -30$ and I/P resistance must be largest possible but under 1 MΩ.

Sol'n

$$A_F = -30$$

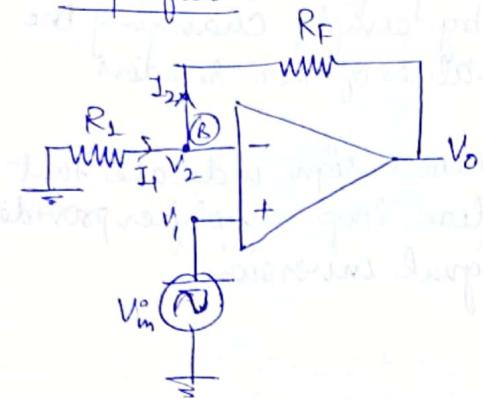
$$R_F = 1 \text{ M}\Omega$$

$$\Delta A_F = -\frac{R_F}{R_1 + R_2}$$

$$R_1 = -\frac{1 \times 10^6}{-30} = 33.33 \text{ k}\Omega$$

~~the A Equivalent~~

Closed loop Non-Inverting Amplifier



$$V_1 = V_m^o$$

$$V_1 = V_2 = V_m$$

apply KCL at Node (B).

$$\frac{0 - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$$

$$\frac{-V_m^o}{R_1} = \frac{V_m^o - V_o}{R_F}$$

$$V_m^o \left(\frac{1}{R_F} + \frac{1}{R_1} \right) = \frac{V_o}{R_F}$$

$$V_o = R_F \left(\frac{R_F + R_1}{R_F R_1} \right) V_m^o$$

$$V_o = \left(1 + \frac{R_F}{R_1} \right) V_m^o$$

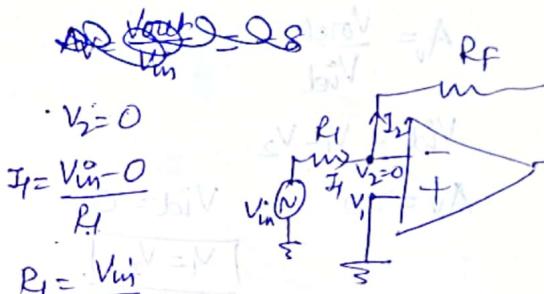
$$A_F = \frac{V_o}{V_m^o} = \left(1 + \frac{R_F}{R_1} \right)$$

- A_F always greater than 1.
- +ve of voltage gain represents o/p polarity is same as of i/p.

→ Voltage gain independent of open loop gain.

Ques

Design an inverting op-amp with $A_F = -8$. When $V_m = -1V$. The current at R_1 and R_F must not be larger than 15mA. Determine value of R_1 & R_F .



$$V_2 = 0$$

$$I_1 = \frac{V_m - 0}{R_1}$$

$$R_1 = \frac{V_m}{I_1}$$

$$= \frac{-1}{15 \times 10^{-3}} = 66.66 \text{ k}\Omega$$

(std value 68k\Omega)

$$R_F = -A_F R_1$$

$$= 8 \times 66.66 =$$

$$533.33 \text{ k}\Omega$$

$$533.33 \text{ k}\Omega = 533 \text{ k}\Omega$$

$$533 \text{ k}\Omega = 533 \text{ k}\Omega$$

Ques Design a non-inverting amplifier circuit that is capable of providing a voltage gain 10. (Resistor should not exceed 30 kΩ).

$$A_F = 1 + \frac{R_F}{R_1}$$

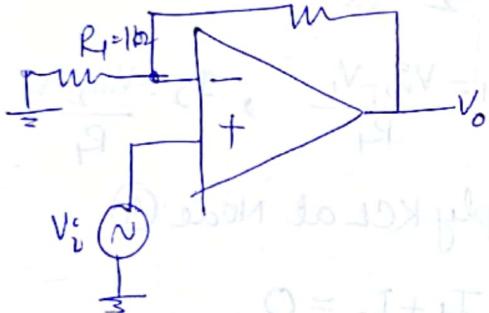
$$10 = 1 + \frac{R_F}{R_1}$$

$$\frac{R_F}{R_1} = 9$$

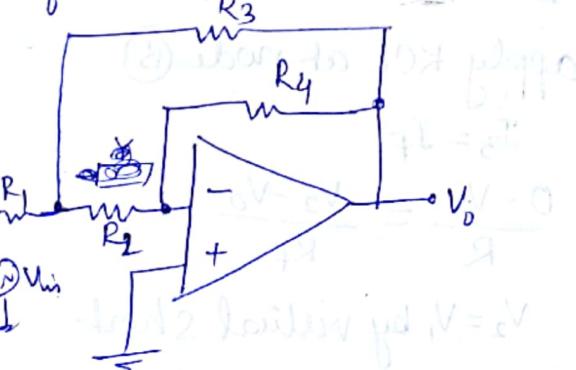
② Let $R_1 = 1\text{ k}\Omega$.

$$R_2 = 9\text{ k}\Omega$$

$$R_F = 9\text{ k}\Omega$$



Ques Obtain the function $\frac{V_o}{V_{in}}$ for given circuit. Assume op-amp is ideal. Y_i represent admittance of branch i .



$$Y_i = \frac{1}{R_i}$$

$$Y_1 = \frac{1}{R_1}, Y_2 = \frac{1}{R_2}$$

$$Y_1 + Y_2 = \left(\frac{1}{R_1} + \frac{1}{R_2}\right) Y$$

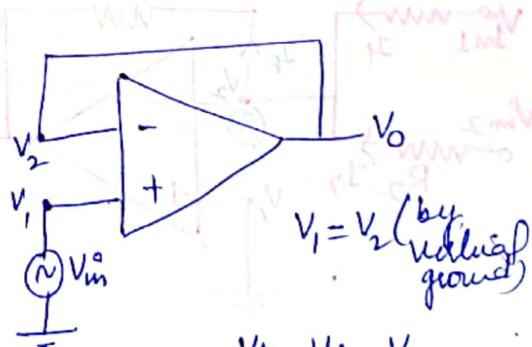
$$Y = \left(\frac{1}{R_1} + \frac{1}{R_2}\right) Y$$

Unity gain amplifier.

When gain of amplifier is unity then it is called as unity gain amplifier. In this It is a linear application of op-amp. Mean O/P & I/P are linearly related Voltage follower.

Unity gain Buffer Amplifier

$$A_F = 1, \quad V_{out} = V_{in}$$



$$V_1 = V_{in} = V_2$$

$$V_2 = V_0 \\ V_1 = V_{in}$$

$$V_0 = V_{in}$$

This is ideal buffer amplifier circuit. because it has high I_{in} , unity transmission gain, extremely

Intrinsic SC

$$n = p = n_i$$

$$n_i = BT^{3/2} e^{-E_g/kT}$$

$$B = 7.3 \times 10^{15} \text{ cm}^{-3} \text{ K}^{-3/2}$$

Extrinsic SC

Doping Concⁿ $n_n \approx N_D \rightarrow$ n-type

$$P_n = \frac{n_i^2}{N_D}$$

$P_p \approx N_A \rightarrow$ p-type

$$n_p \approx \frac{n_i^2}{N_A}$$

$$\begin{array}{c|c} S_o & G_e \\ \hline n_i = 1.5 \times 10^{10} & \end{array}$$

at Room Temp.

Current in SC

$$I_{D\text{drive}} = \mu p E$$

$$\mu p = 480 \text{ cm}^2/\text{Vs}$$

$$I_{D\text{drive}} = \mu n E$$

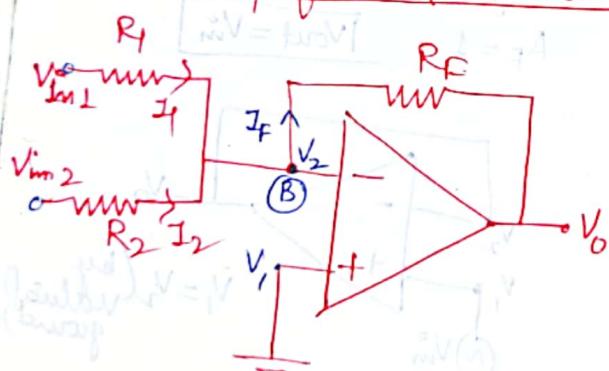
$$\mu n = 1350 \text{ cm}^2/\text{Vs}$$

low O/P resistance.

It is also known as isolation circuit because it provides a mean of isolating I/P signal from load.

Voltage Follower

Summer Amplifier or Adder circuit



$$V_1 = V_2 = 0$$

$$I_1 + I_2 = I_F$$

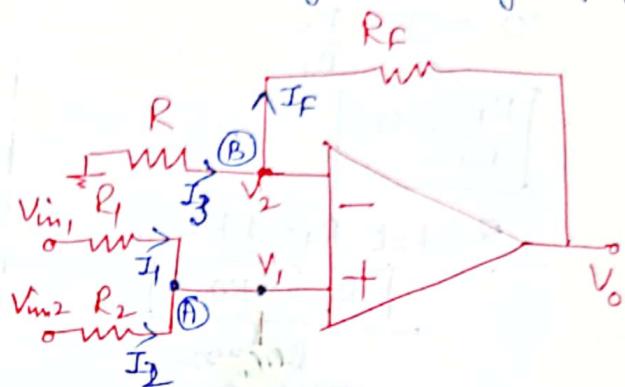
$$\frac{V_{in1} - V_2}{R_1} + \frac{V_{in2} - V_2}{R_2} = \frac{V_2 - V_o}{R_F}$$

$$V_{out} = -\frac{R_F}{R_1} \left[\frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2} \right]$$

If $R_1 = R_2 = R_F$

$$\text{then } V_{out} = -[V_{in1} + V_{in2}]$$

Non-Inverting Summing amplifier



$$I_1 = \frac{V_{in1} - V_1}{R_1}, \quad I_2 = \frac{V_{in2} - V_1}{R_2}$$

apply KCL at Node A

$$I_1 + I_2 = 0$$

$$\frac{V_{in1} - V_1}{R_1} + \frac{V_{in2} - V_1}{R_2} = 0$$

$$V_1 = \frac{R_2 V_{in1} + R_1 V_{in2}}{R_1 + R_2}$$

apply KCL at node B

$$I_3 = I_F$$

$$\frac{0 - V_2}{R} = \frac{V_2 - V_o}{R_F}$$

$V_2 = V_1$ by virtual short

$$V_1 \left(\frac{1}{R_F} + \frac{1}{R} \right) = \frac{V_o}{R_F}$$

$$V_o = \left(1 + \frac{R_F}{R} \right) V_L$$

Why we prefer Si over Ge

$$V_o = \frac{(R_2 V_{in1} + R_1 V_{in2})}{R_1 + R_2} \left(1 + \frac{R_F}{R} \right)$$

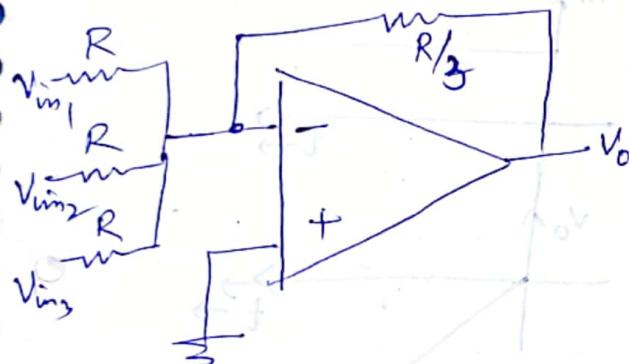
Now if $R_1 = R_2 = R = R_F$

$$V_o = V_{in1} + V_{in2}$$

Average circuit

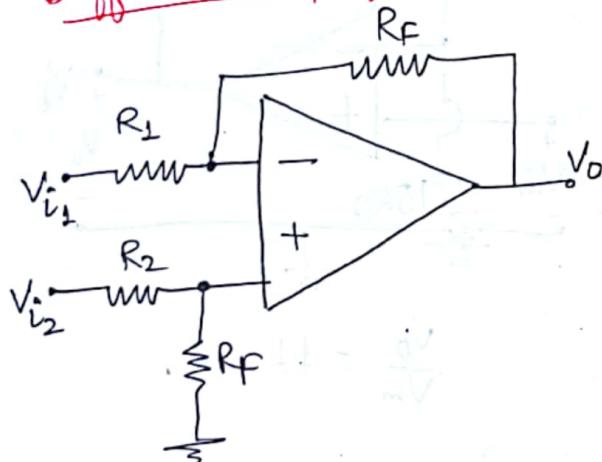
In inverting summing circuit, if resistance values are selected as follows:

$$R_1 = R_2 = R \quad R_F = \frac{R}{2}$$



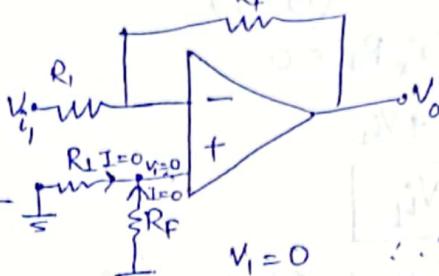
$$V_{out} = -\frac{(V_{in1} + V_{in2} + V_{in3})}{3}$$

Difference amplifier



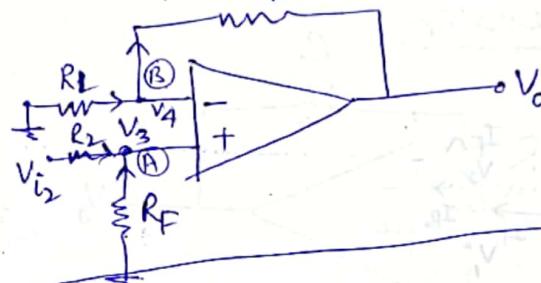
We will solve this by substitution theorem,

When $V_{i2}^a = 0$



$$V_o = -\frac{R_F}{R_1} V_{i1}^a$$

when $V_{i1}^a = 0$, R_F



apply KCL at node (A)

$$\frac{V_{i2} - V_3}{R_2} + \frac{V_3}{R_F} = 0$$

$$\frac{V_{i2}}{R_2} - V_3 \left[\frac{1}{R_2} - \frac{1}{R_F} \right] = 0$$

$$V_3 = \frac{R_2 R_F}{R_2 + R_F}$$

$$\text{by Voltage divider, } V_3 = \frac{R_F}{R_2 + R_F} V_{i2}^a$$

apply KCL at node (B)

$$\frac{-V_4}{R_1} = \frac{V_4 - V_o}{R_F}$$

$$\Rightarrow V_{o2} = \left(1 + \frac{R_F}{R_1} \right) V_4$$

$$V_{o2} = \left(\frac{R_1 + R_F}{R_F} \right) \times \frac{R_F}{(R_1 + R_F)} V_{i2}^a$$

V_{o2}

$$V_o = V_{o_1} + V_{o_2}$$

$$= -\frac{R_F}{R_1} V_{i_1} + \left(\frac{R_1 R_F}{R_2 + R_F} \right) V_{i_2}$$

Put $R_1 = R_2 = R_F = 0$

$$V_o = -V_{i_1} + V_{i_2}$$

$$V_o = V_{i_2} - V_{i_1}$$

This shows that O/P Voltage is proportional to the difference between two input voltages.

Integrator.

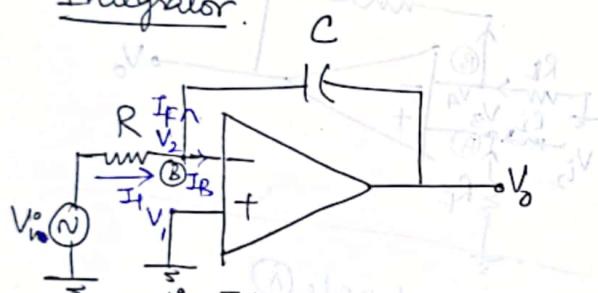


fig: Ideal Integrator Circuit

KCL at Node (B)

$$I_f = I_f + I_B$$

$$\therefore I_B = 0$$

$$I_f = I_f$$

$$\frac{V_i - V_2}{R} = \frac{V_o}{C}$$

$$V_2 = V_i = 0 \text{ by Virtual GND}$$

$$\frac{V_L}{R} = I_C$$

Current across cap,

$$I_C = \frac{CdV_C}{dt}$$

$$= \frac{C d(V_2 - V_o)}{dt}$$

$$= -C \frac{dV_o}{dt}$$

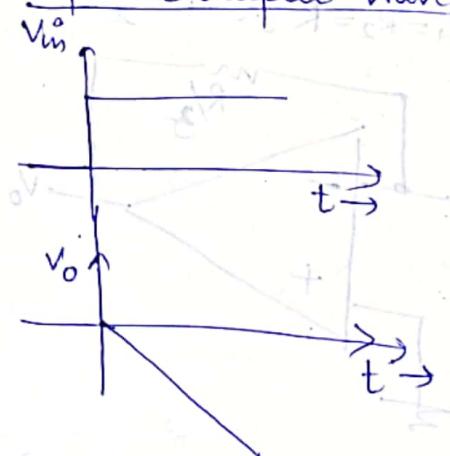
$$V_o \cdot \frac{V_i}{R} = -C \frac{dV_o}{dt}$$

$$V_o = -\frac{1}{RC} \int_0^t V_o dt + C$$

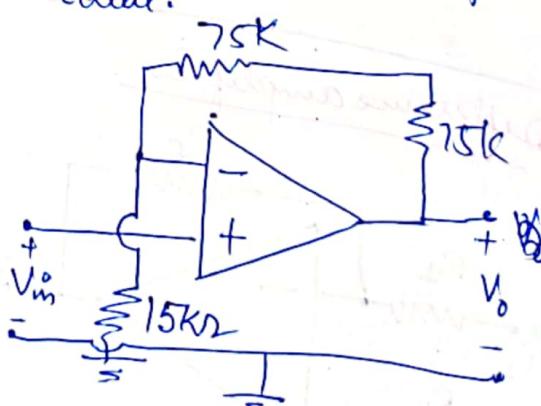
C → Integration Constant.

This shows that O/P Voltage is negative integration of I/P voltage. It is called as inverting integrator.

Input & Output Waveform.



Ques Find V_o/V_i if op-amp is ideal.



$$\frac{V_o}{V_{in}} = 11.$$

Problem with ideal integrator

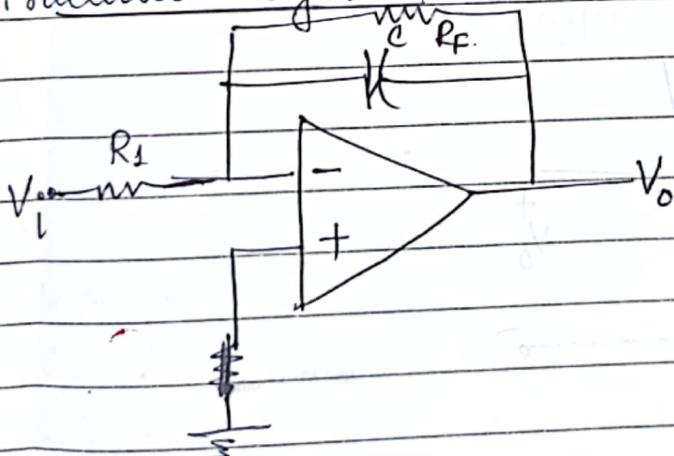
- ① In this C_f is connected in feedback path hence its reactance will decide the gain of inverting amplifier.

In absence of AC input the capacitive reactance will be ∞ . Hence gain is ∞ and a large O/P voltage is present in absence of I/P voltage which is error voltage.

- ② Input bias current will charge the cap. and vary O/P voltage to ramp up or ramp down.

- ③ Gain of amplifier is infinite ~~base~~ for dc ($f=0$), as freq increases gain decreases hence for high frequencies it can not integrate I/P signals.

Practical Integrator:-



we choose the value of R_f to be very high.

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Advantage of integrator

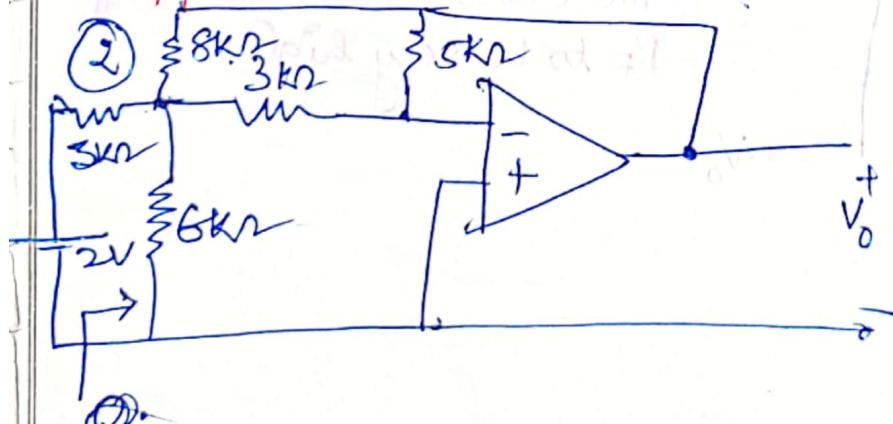
- It can integrate the input voltage over time.
- It can convert AC signals into DC signals.
- It can convert digital signals into analog signals.
- It can perform mathematical operations like differentiation and integration.

Disadvantage

Assume OP-amp is to be ideal.



Applications



~~R_f = 6 kΩ~~

$$V_C = 6V$$

t. No. Differentiator Circuit

KCL at node A

$$I_1 = I_F + I.$$

$$I = 0$$

$$\therefore I_1 = I_F$$

$$\frac{C dV_C}{dt} = \frac{0 - V_O}{R_F}$$

$$V_O = - C R_F \frac{dV_C}{dt}$$

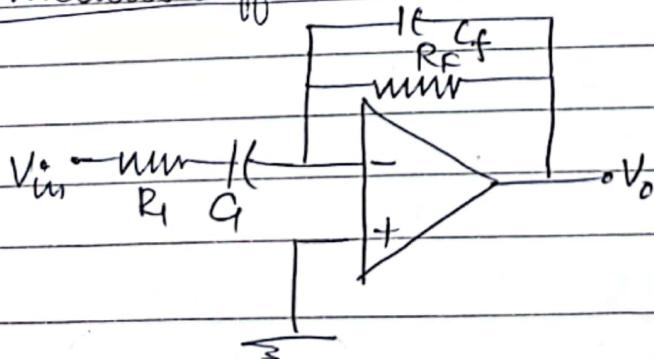
$$V_O = - C R_F \frac{d(V_m - 0)}{dt}$$

$$\boxed{V_O = - C R_F \frac{dV_m}{dt}}$$

Problem associated with differentiator :-

X_C decreases with increase in frequency hence the gain will increase with increase in freq. which make circuit unstable at high frequencies.

Practical differentiator circuit



→ due to X_C , the gain increased.

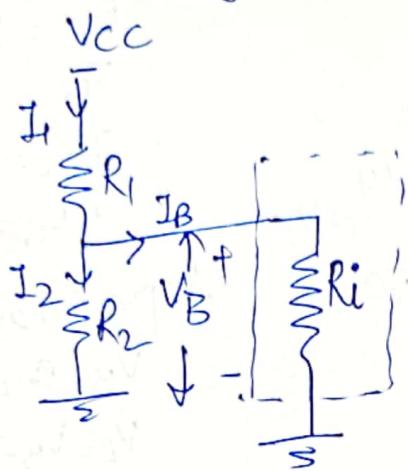
was drastically decreased.

→ For stabilization R_i & C_1 are used; it

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..... appear in above eqⁿ and I_B was not calculated. The Q-Point is therefore independent of I_{CQ} & V_{CEQ} .

Input section of voltage divider config. can be
represented by following circuit -



$$R_i = (1 + \beta) R_E$$

if $R_i \gg R_2$.

then $I_B \ll I_2$.

$$\therefore I_2 = I_1.$$

and R_1 & R_2 can be
considered as series element

$$\therefore \text{Voltage across } R_2 (V_B) = \frac{V_{CC} R_2}{R_1 + R_2}, \quad R_i = (1 + \beta) R_E$$

$$R_i \approx \beta R_E$$

- 1) The approximate approach can be applied with high
 2) level of accuracy if $\boxed{\beta R_E \geq 10 R_2}$

Now $V_B = \frac{V_{CC} R_2}{R_1 + R_2}, \quad V_{BE} = V_B - V_E$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

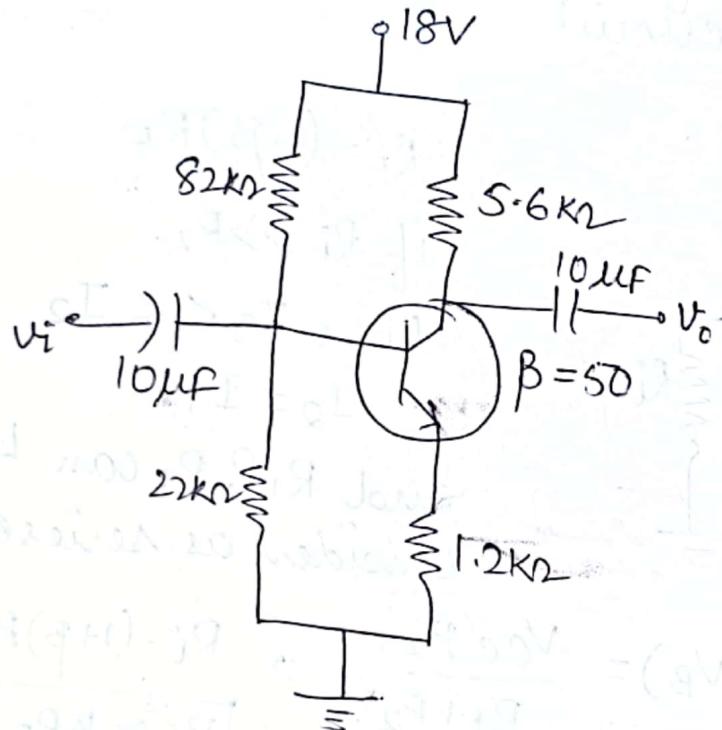
$$I_{CQ} \approx I_E$$

For Collector Emitter loop,

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

$$\boxed{V_{CEQ} = V_{CC} - I_C (R_C + R_E)}$$

From above equation it is observed that β does not appear in above eqⁿ and I_B was not calculated. The Q-Point is therefore independent of I_{CQ} & V_{CEQ} .



Exact Analysis,
 $R_{Th} = 17.35\text{ k}\Omega$
 $E_{Th} = 3.81\text{ V}$
 $I_B = 39.6\text{ mA}$
 $I_{CQ} = 1.98\text{ mA}$
 $V_{CEQ} = 4.54\text{ V}$.

Approximate Analysis,
 $V_B = E_{Th} = 3.81\text{ V}$
 $V_E = V_B - V_{BE} = 3.11\text{ V}$.
 $I_E = \frac{V_E}{R_E} = 2.59\text{ mA}$.
 $I_{CQ} = I_E = 2.59\text{ mA}$.
 $V_{CEQ} = V_{CC} - I_c(R_C + R_L)$
 $= 18 - 2.59 \times (5.6 + 1.2)$
 $\boxed{V_{CEQ} = 3.88\text{ V}}$.

	$I_{CQ}(\text{mA})$	$V_{CEQ}(\text{V})$
Exact	1.98	4.54
Approximate	2.59	3.88

→ I_{CQ} is 30% greater
 V_{CEQ} is 10% less.

→ $\beta R_E > 3R_2$. still results are very close.