

## Unit 2

BJT (

Bipolar Junction Transistor)

TRANSISTOR → TRANSFER + RESISTOR.

BJT is a three terminal device its operation depends on the interaction of both majority & minority carriers so it is a bipolar device.

Signals are transferred from low resistance to high resistance circuit. A transistor comprises two p-n junction formed by sandwiching either P type or N-type SC between a pair of opposite types.

Transistor type :-

Transistor can be classified in two types on its construction:

- 1) n-p-n Transistor
- 2) p-n-p Transistor

n-p-n Transistor → A transistor in which two layers of N-type SC are interfaced by a thin layer of P-type SC is known as n-p-n transistor.

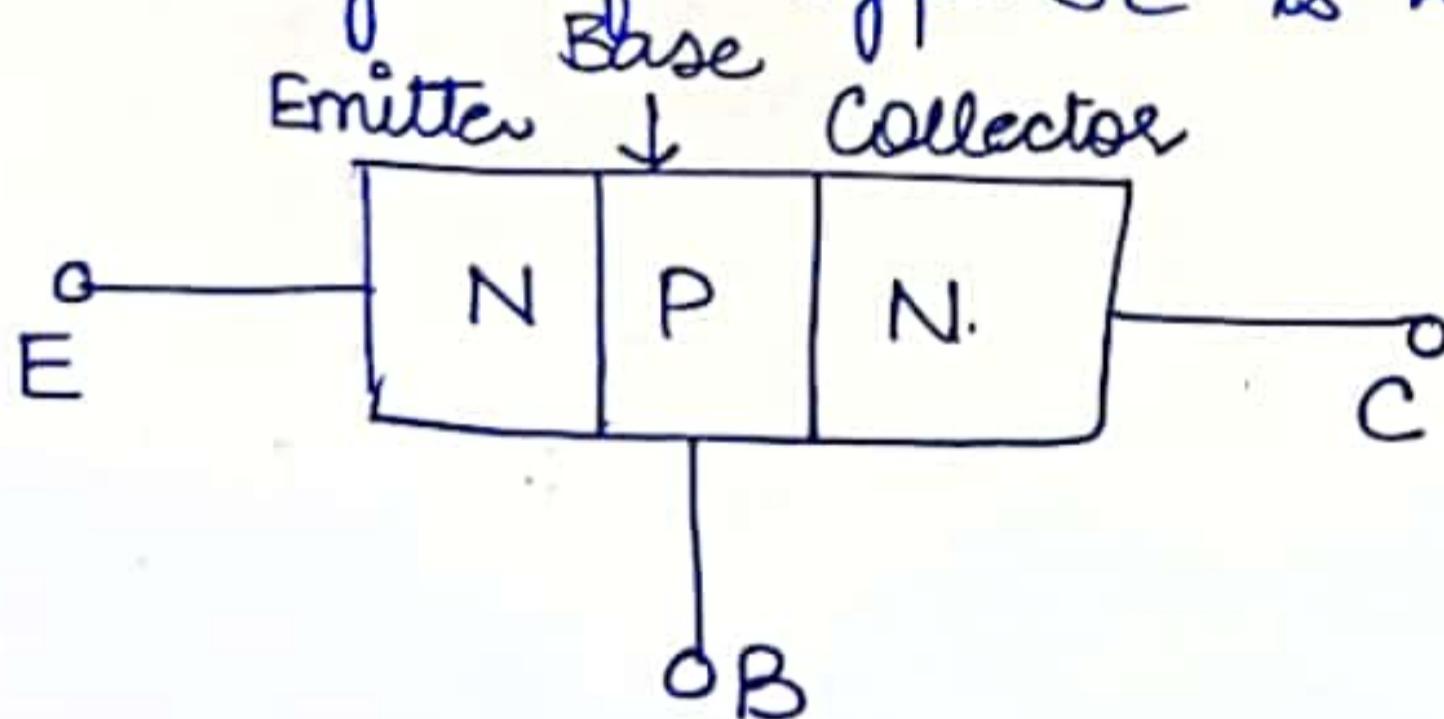


fig:-n-p-n transistor

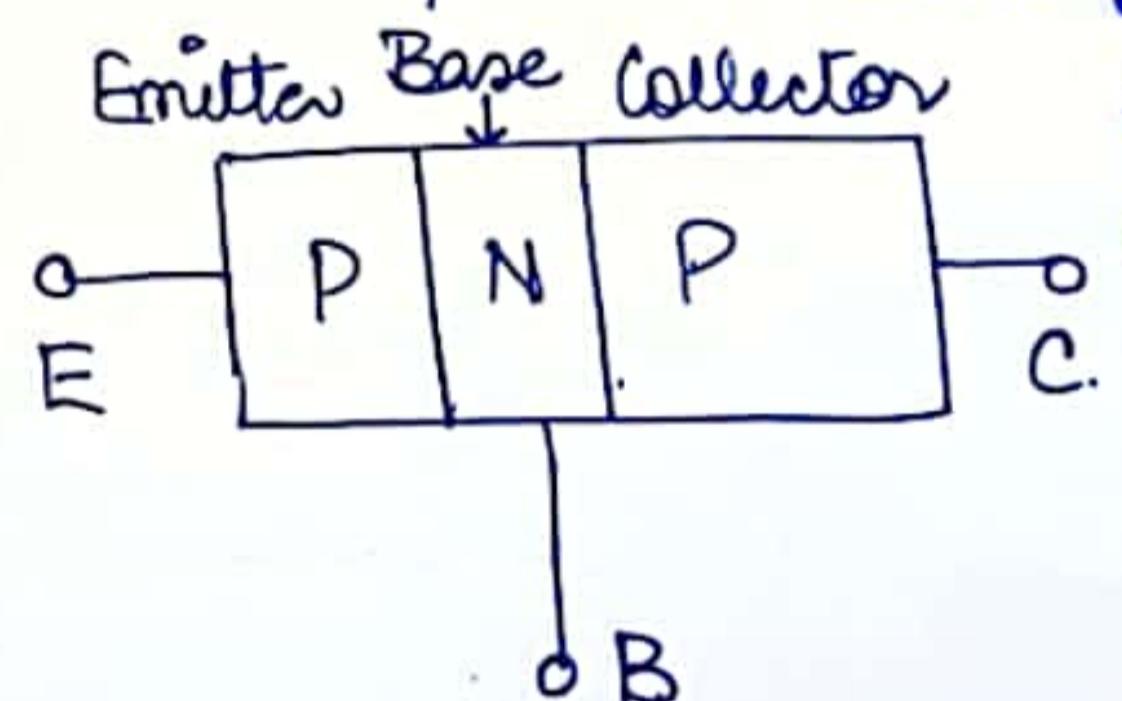


fig:p-n-p transistor

p-n-p transistor :- A transistor in which two layers of P-type SC are interfaced by this layer of N-type SC is known as p-n-p transistor.

### Class... Questions:-

A transistor has three regions of doped SCs.

- ① Emitter      ② Base      ③ Collector

① Emitter :- The heavily doped region of a transistor that supplies charge carriers is called as Emitter. Emitter is always F.B w.r.t. Base.

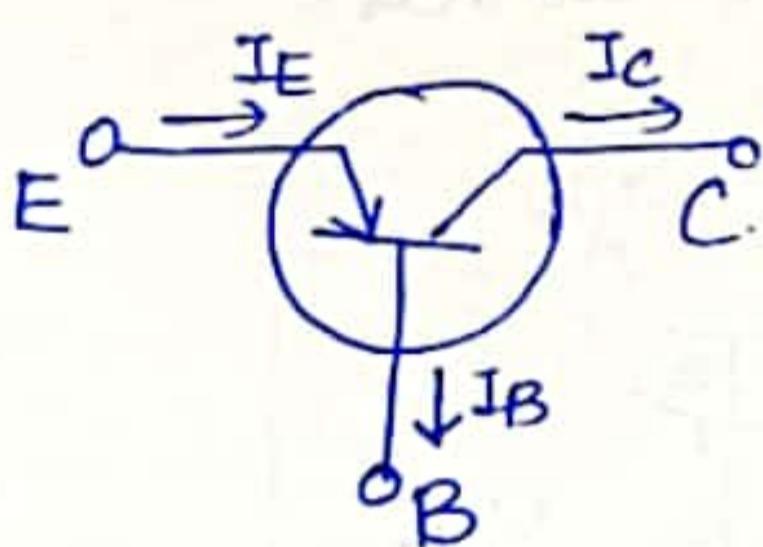
② Base :- The middle section of transistor is called as Base. It is thin and lightly doped region.

③ Collector :- The other side that collects the charge is called as collector. The doping level of collector is between heavy doping of emitter and light doping of base. The collector region is physically longer than the emitter region.

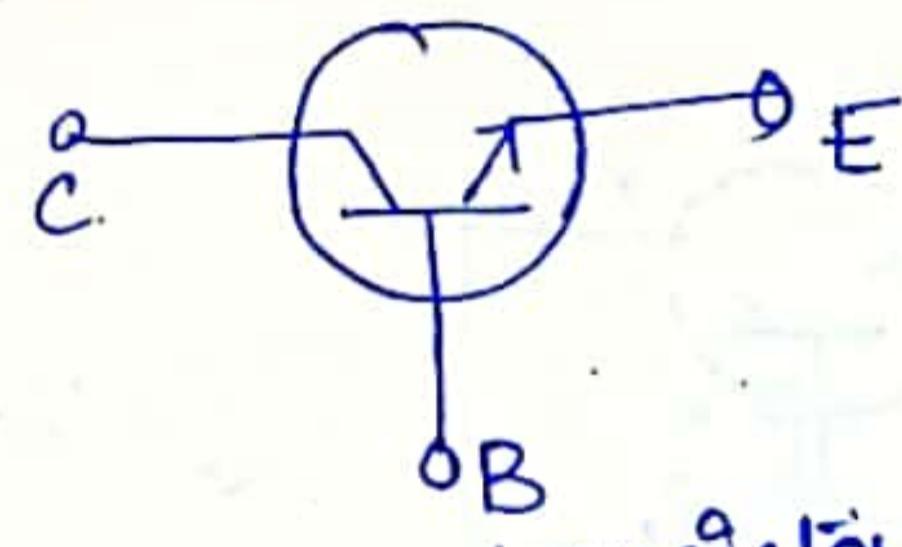
doping level :- Emitter > Collector > Base.

Area :- Collector > Emitter > Base

### Transistor Symbol :-



p-n-p transistor



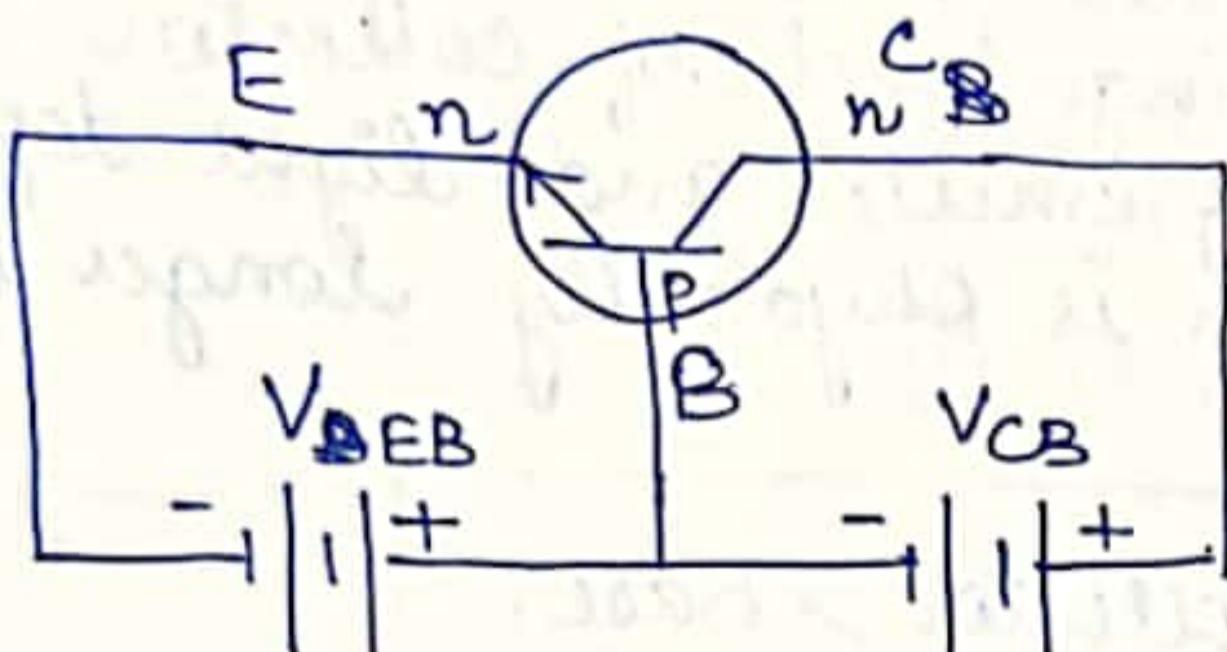
n-p-n transistor

### Transistor Action :-

The method of applying external voltage to a transistor is called as transistor biasing. Since there are two junctions in transistor namely emitter-base junction & collector-base junction. There are four possible ways of biasing two junctions.

Case	Emitter-Base Junction	Collector-base Junction	Region of operation
I.	F.B	R.B -	Active
II.	F.B	F.B	saturation
III	R.B	R.B	Cut-off
IV	R.B	F.B	Inverted

Active region :- In this Emitter base junction is F.B & Collector base junction is R.B.



This region of transistor is used as amplifier. In this region collector current depends on base region.

Saturation region :- Both junctions are F.B in this case. In this region transistor act like a closed switch.

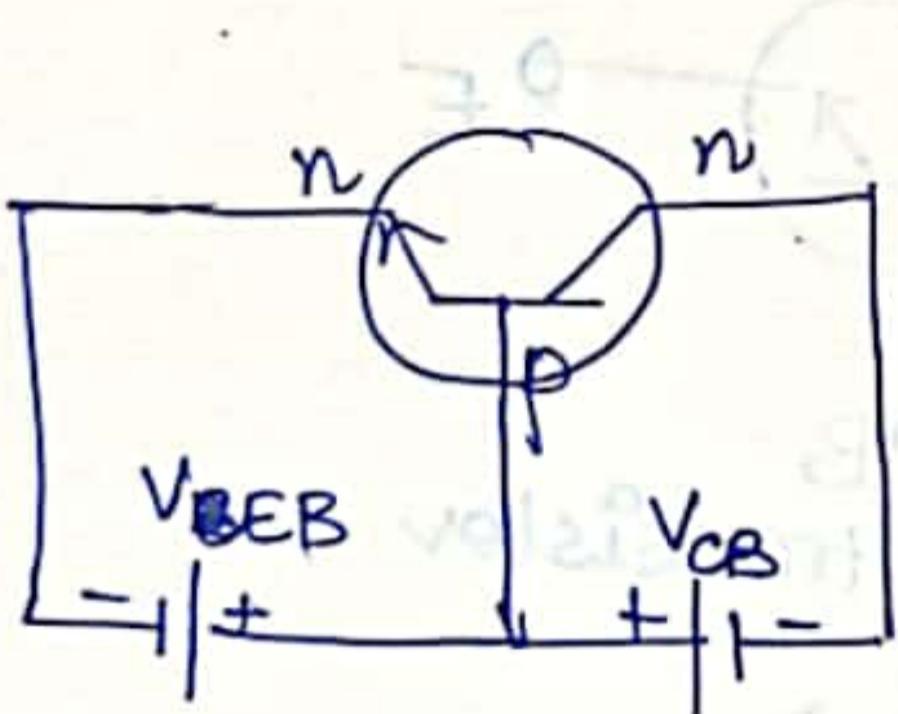


fig: In sat region.

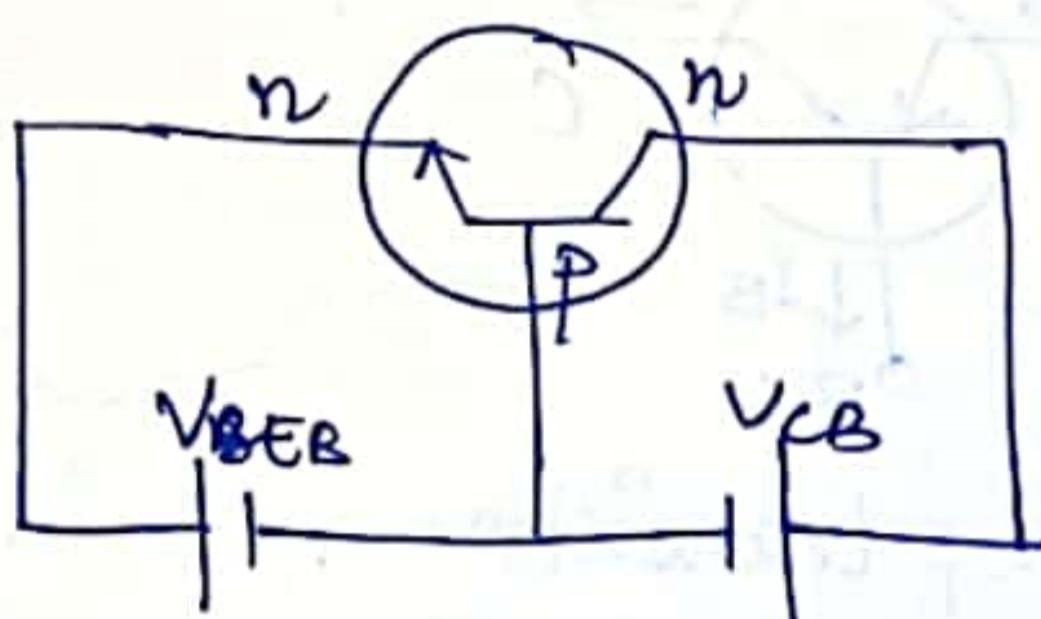


fig:- Cut-off region .

Cut-off region :- Both junctions are reverse biased. In this region transistor has practically zero current. In this region transistor work like open switch.

Inverted region :- E-B junction RB and CB junc F.B. doping level of emitter and collector is not the same. ∴ Collector can not inject the majority carriers into base.

\ Ques:- Questions:-  
In this region action of transistor is poor. This region  
is of little importance.

### Operation of Transistor:

### Unbiased Transistor

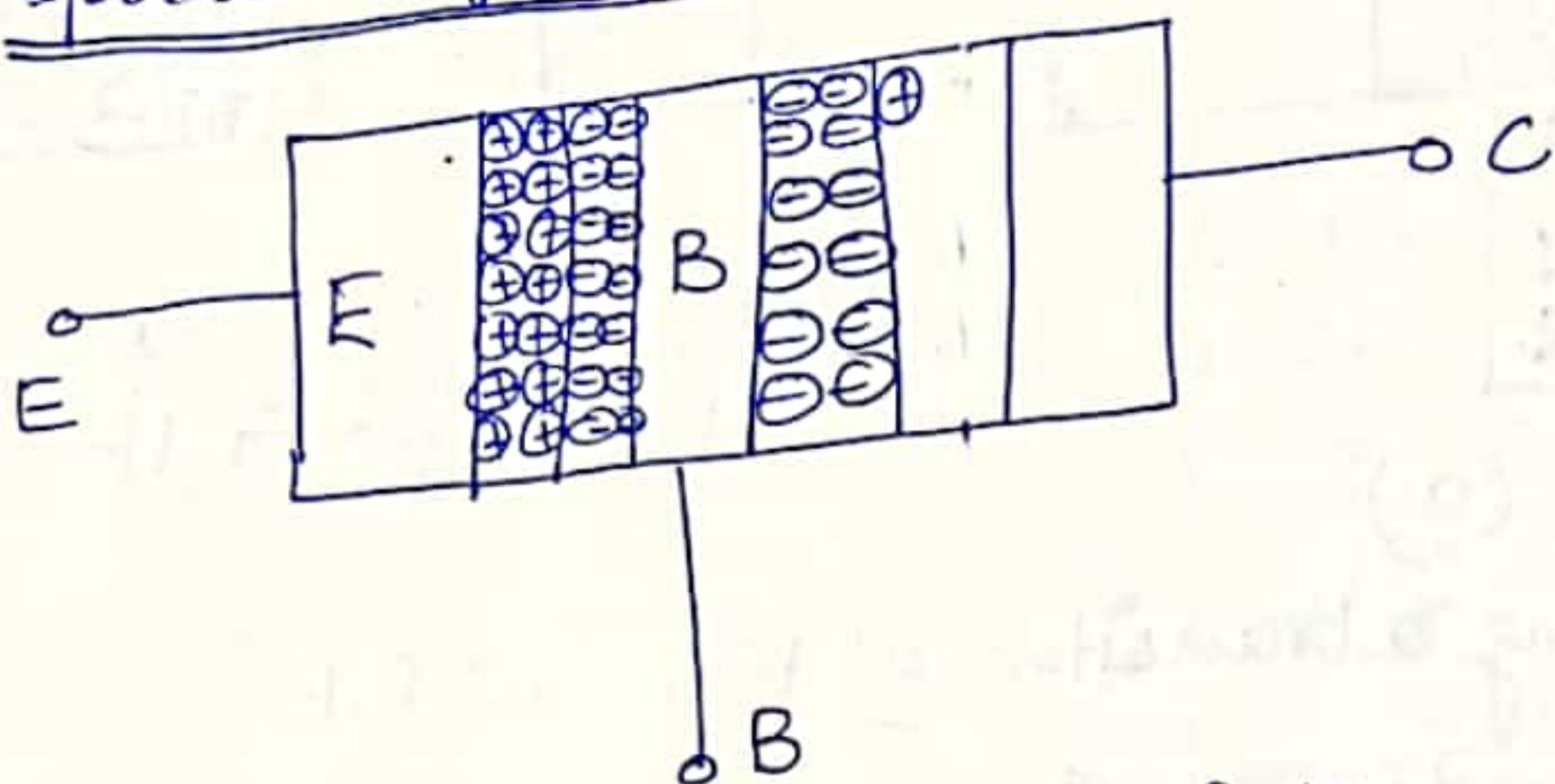


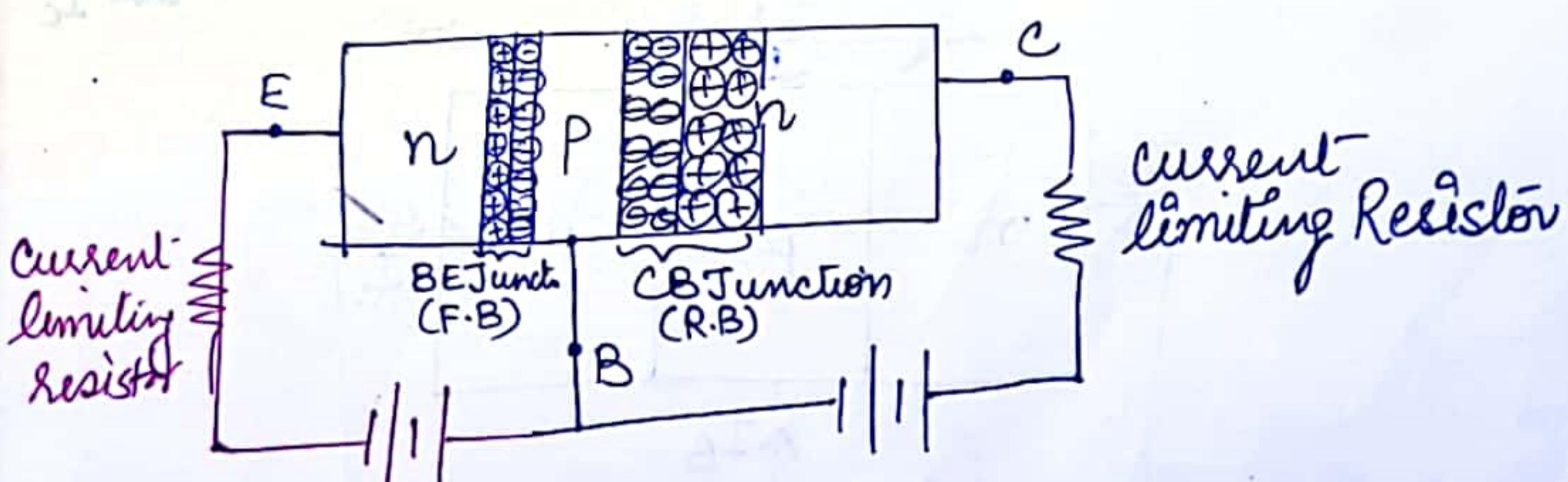
fig:- Unbiased Transistor

When no battery is connected b/w the different terminal of transistors then transistor is said to be an unbiased transistor.

- Diffusion of charge carriers across the junction produces two depletion regions.
- Junctions have different doping level hence width of depletion region are not same for two junctions.
- E-B depletion region → smaller than C-B depletion width.

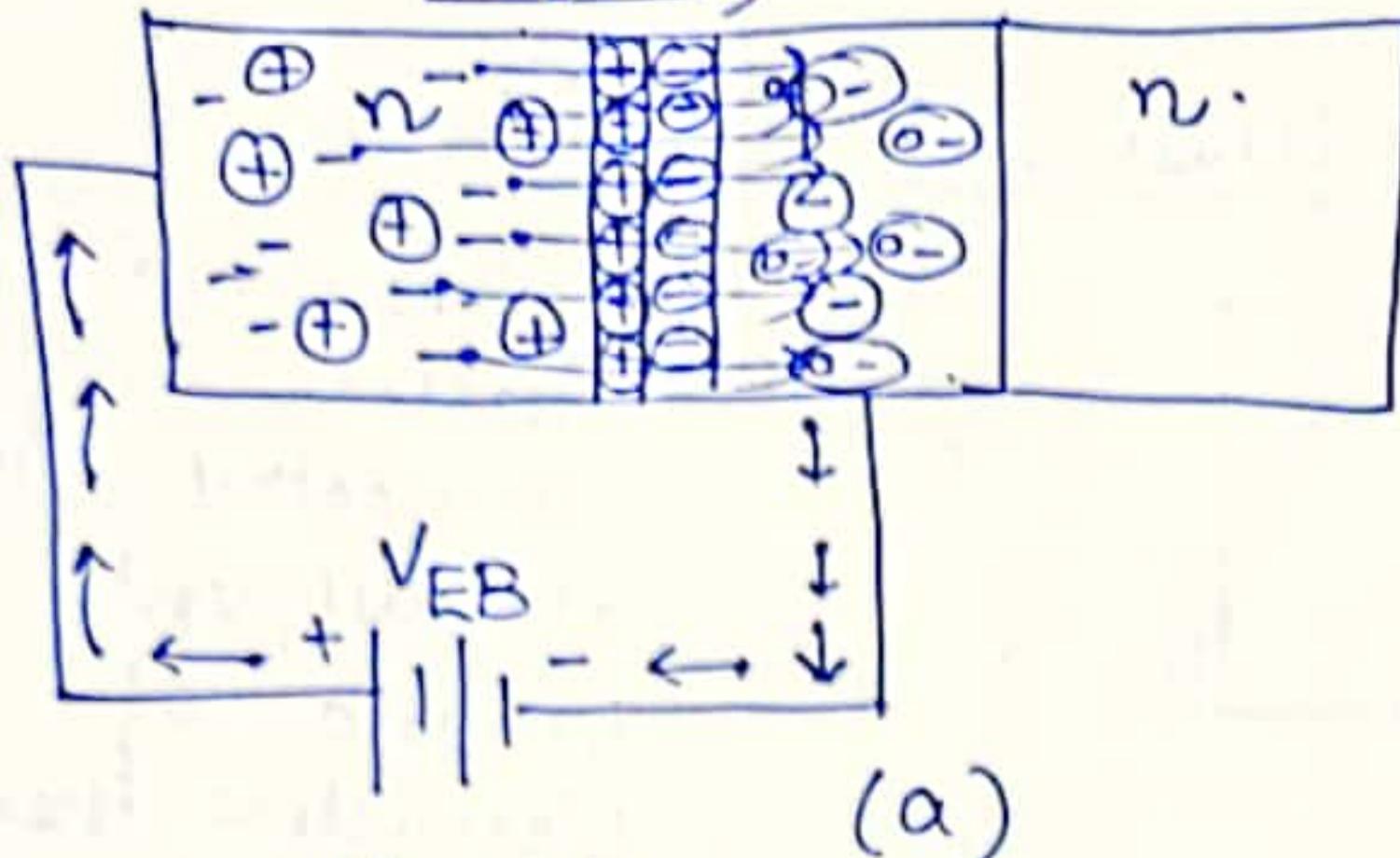
### Transistor operation in active region:-

Base-Emitter Junction (F.B) → depletion width Thin  
Base-Collector Junction (R.B) → depletion width Thick



Electrons are majority carriers of n side emitter start flowing towards p-type base. This constitute emitter current  $I_E$ .

Majority carrier flow.



B) Minority carriers

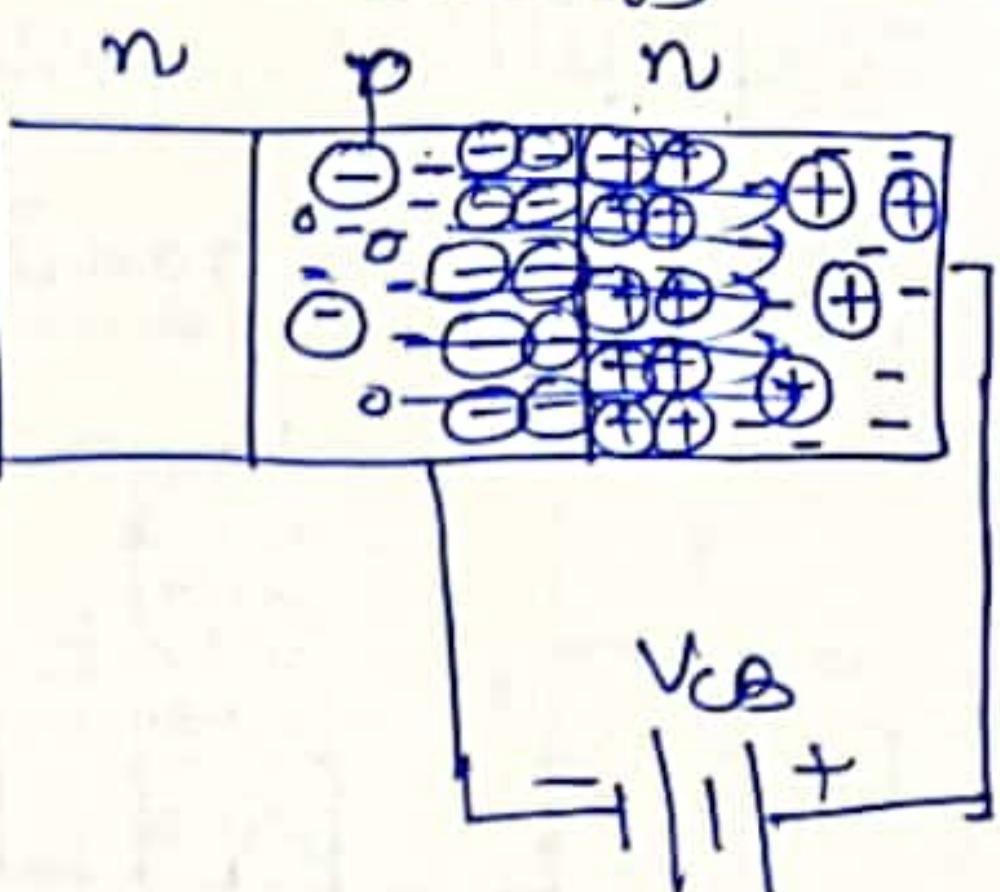
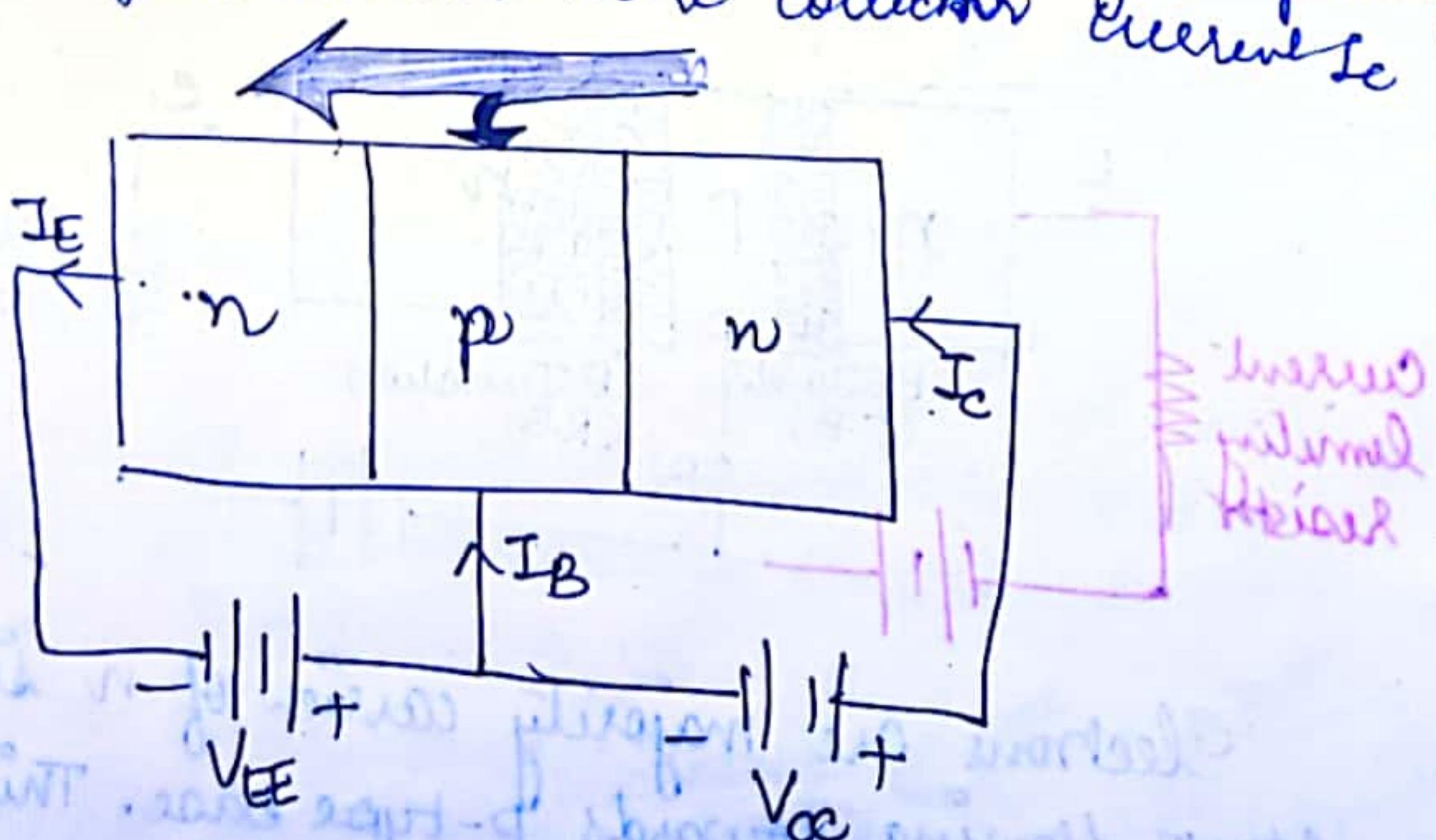


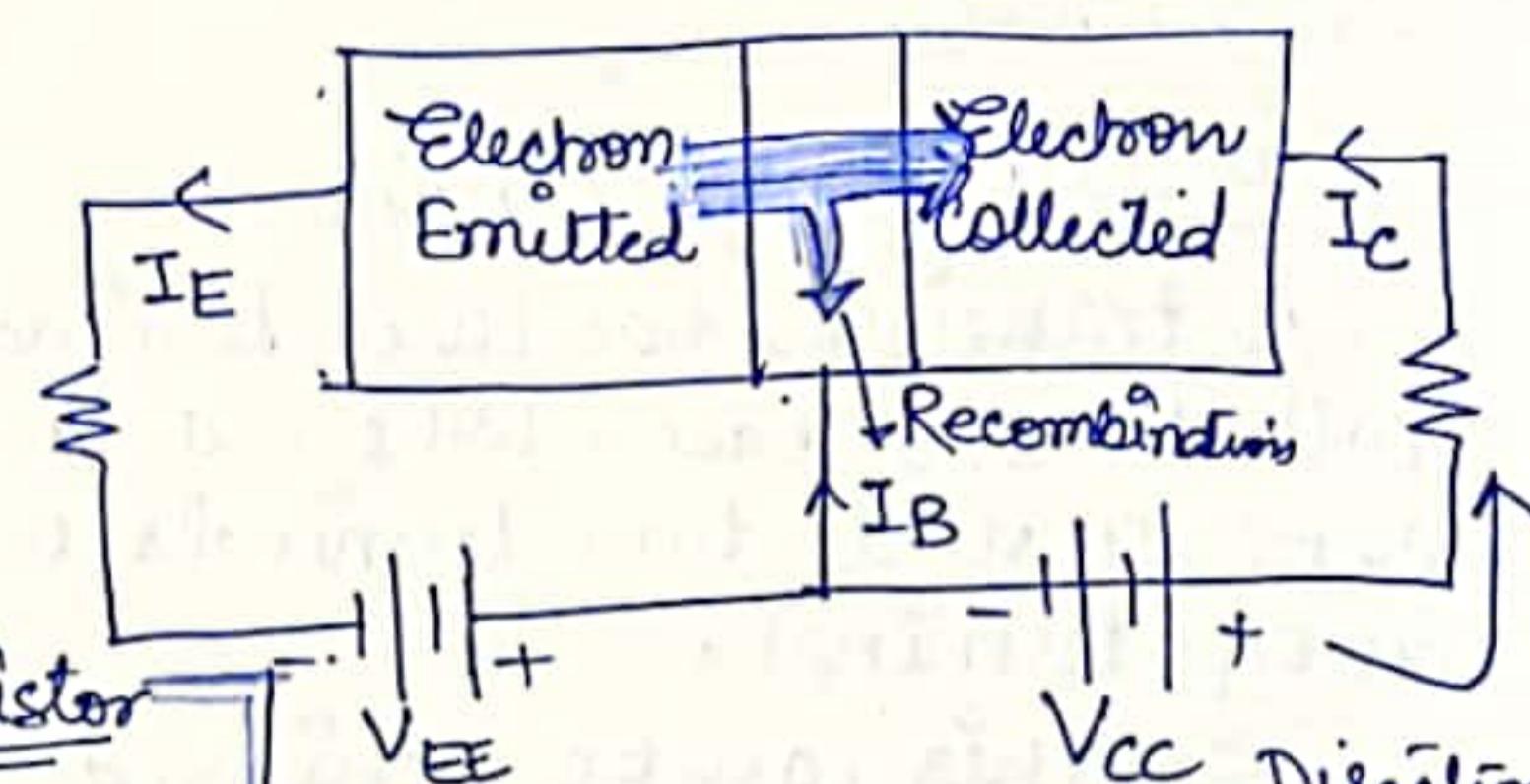
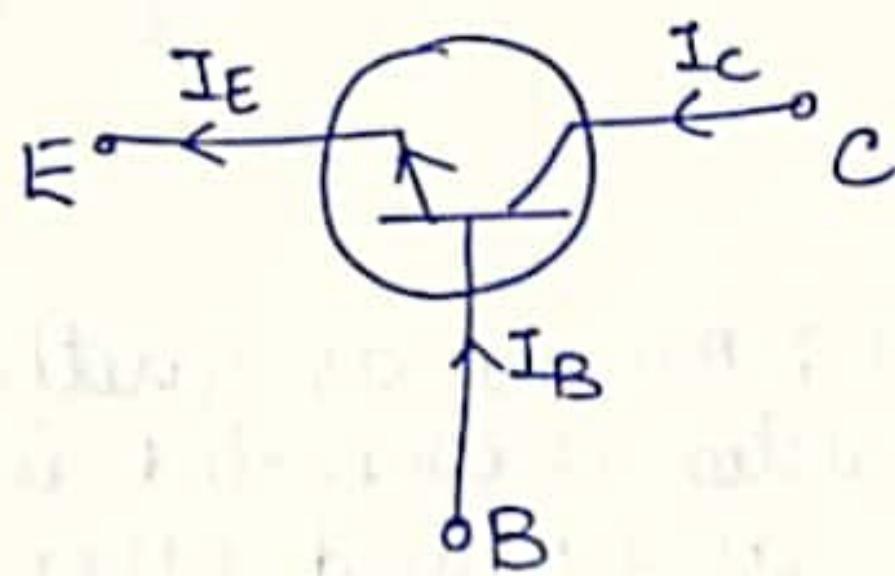
fig:- Biasing a transistor a) F.B b) R.B

Electron moving from emitter to base have three options as under:

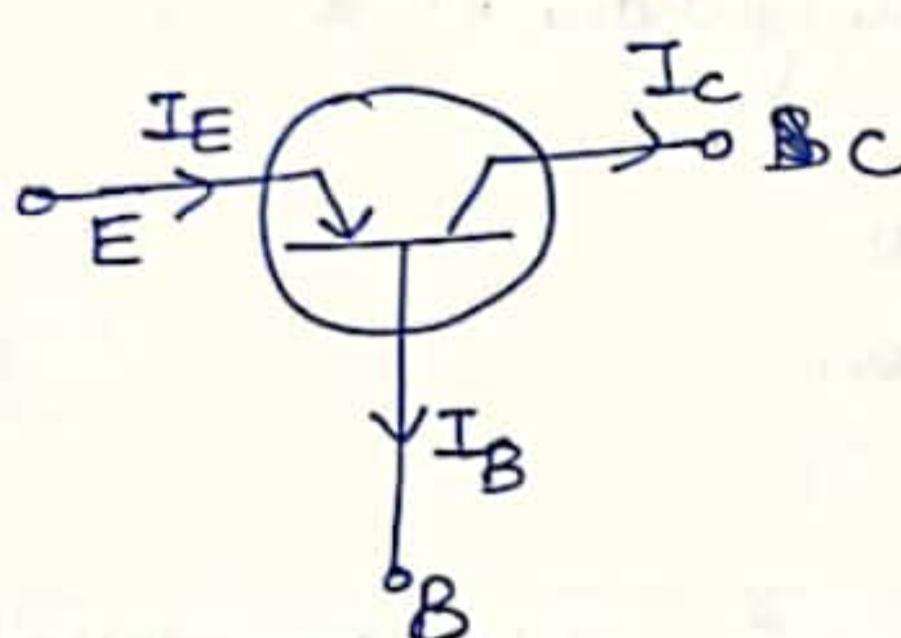
- They recombine with holes present in the base.  
As the base is thin and lightly doped and the no. of holes are very few. Hence very few electron will recombine with hole and constitute base current ( $I_B$ ) (approximately 2%).
- Some electron will diffuse in the base and out of base connection.
- Remaining large no. of electrons pass through depletion region of CB junctions and make collector current  $I_C$ .



Q1. Diode Questions:-

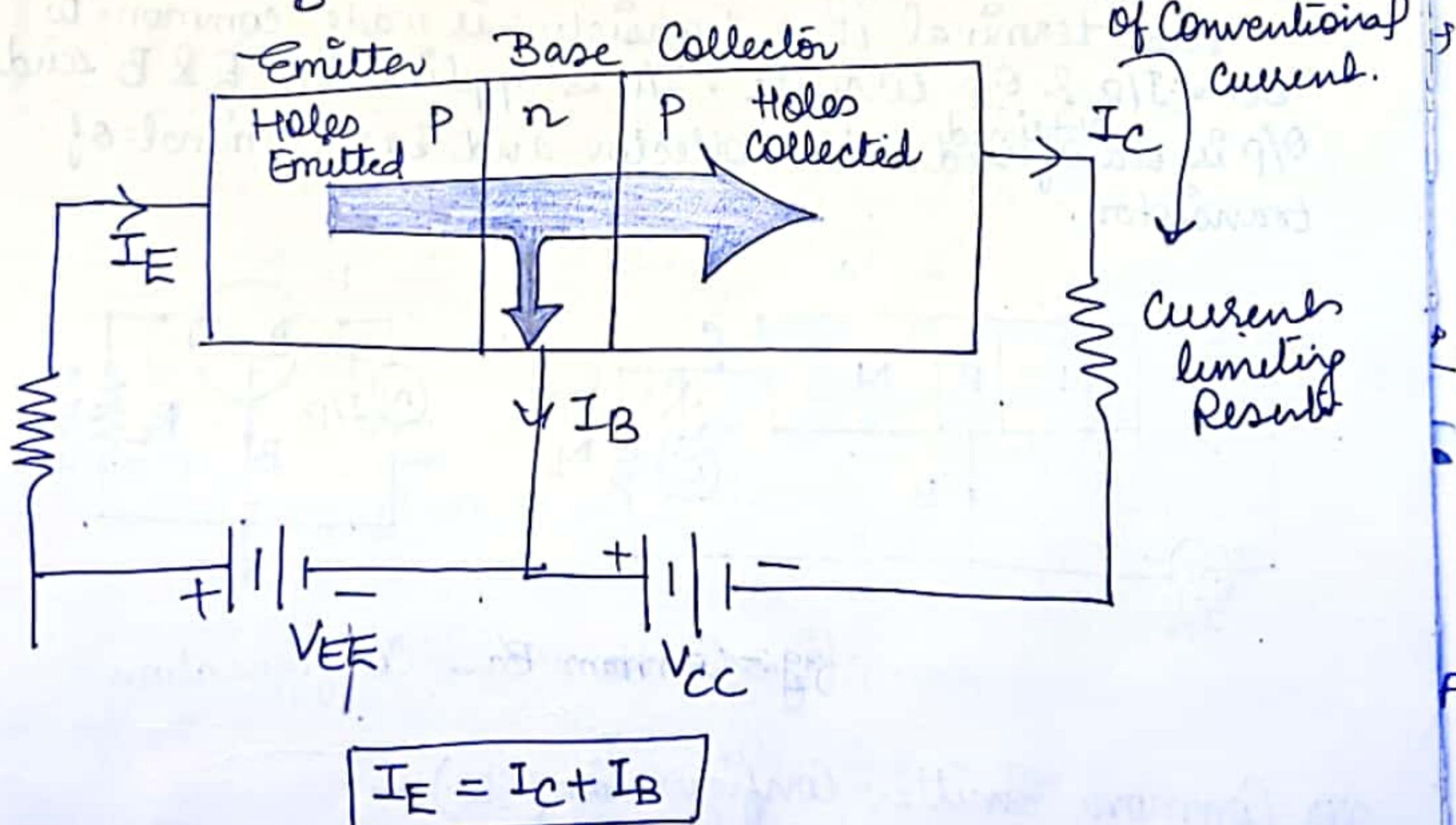


operation of a p-n-p transistor



$$I_E = I_C + I_B$$

Direction of conventional flow of current.



$$I_E = I_C + I_B$$

## Collector Currents

### Transistor Configuration

A transistor has three terminals : named as emitter, collector and base. When a transistor is connected in ckt. It need two terminals one as I/P and other as O/P terminal.

So this can be achieved by making one terminal as common. Following three configurations are :

- 1) Common base configuration
- 2) Common Collector Configuration
- 3) Common Emitter Configuration

#### i) Common base configuration :-

Base terminal of a transistor is made common to both I/P & O/P circuits. I/P is applied b/w E & B and O/P is obtained b/w collector and base terminal of transistor.

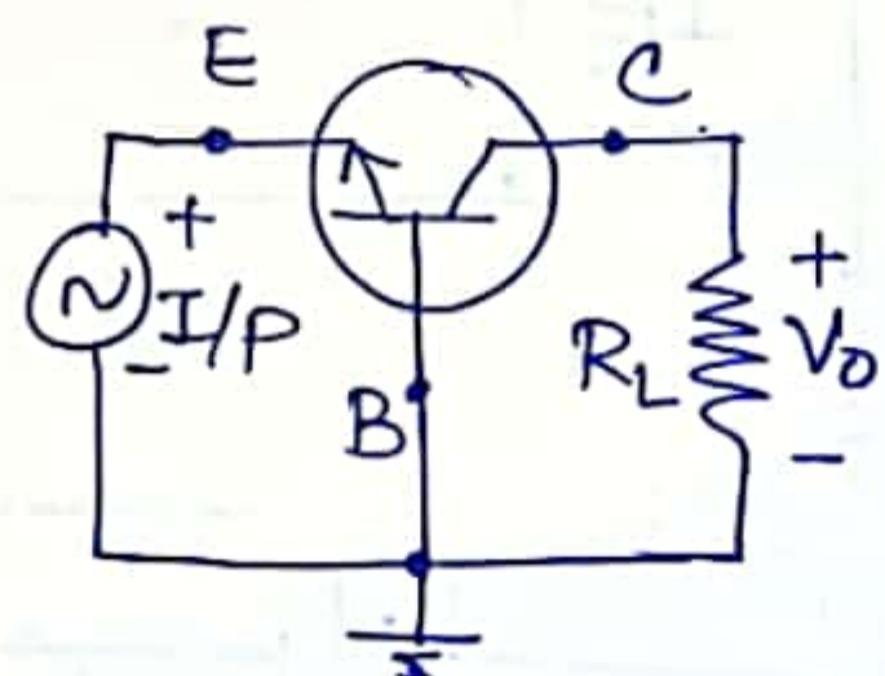
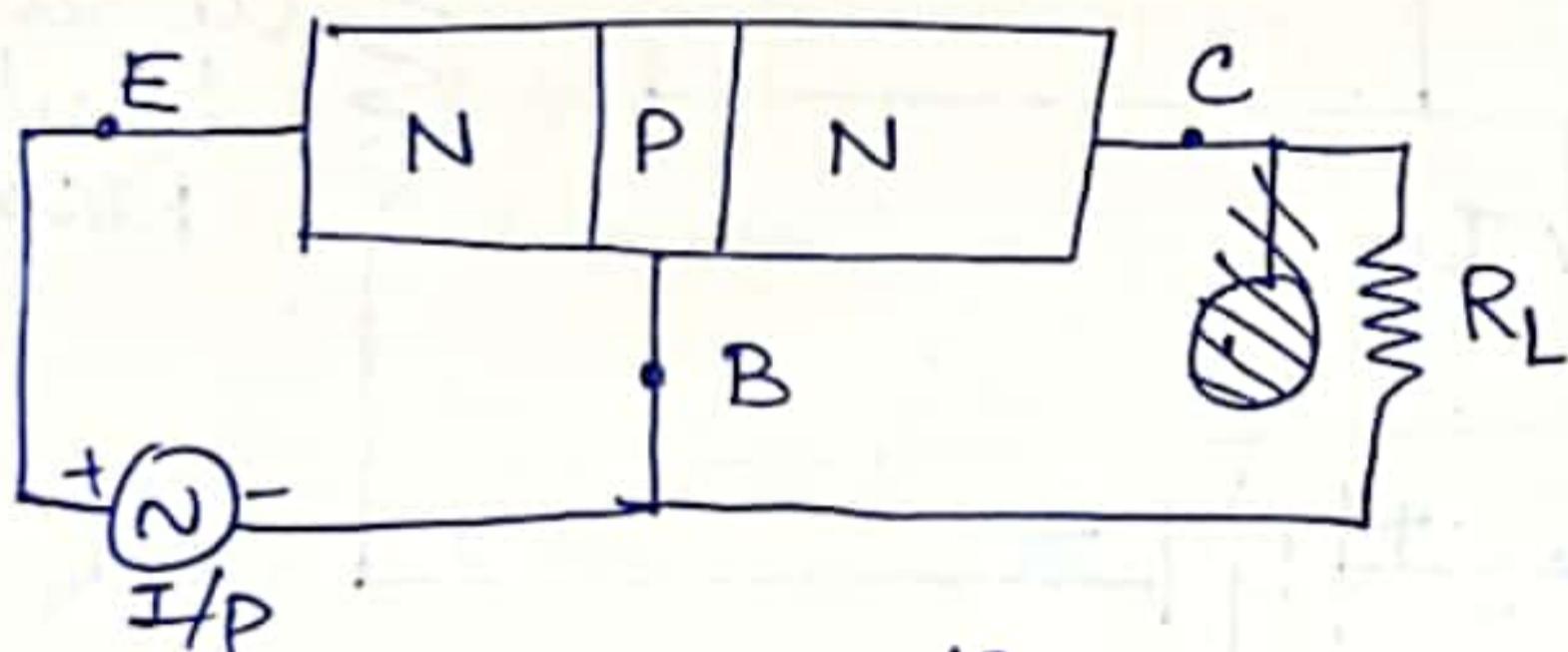
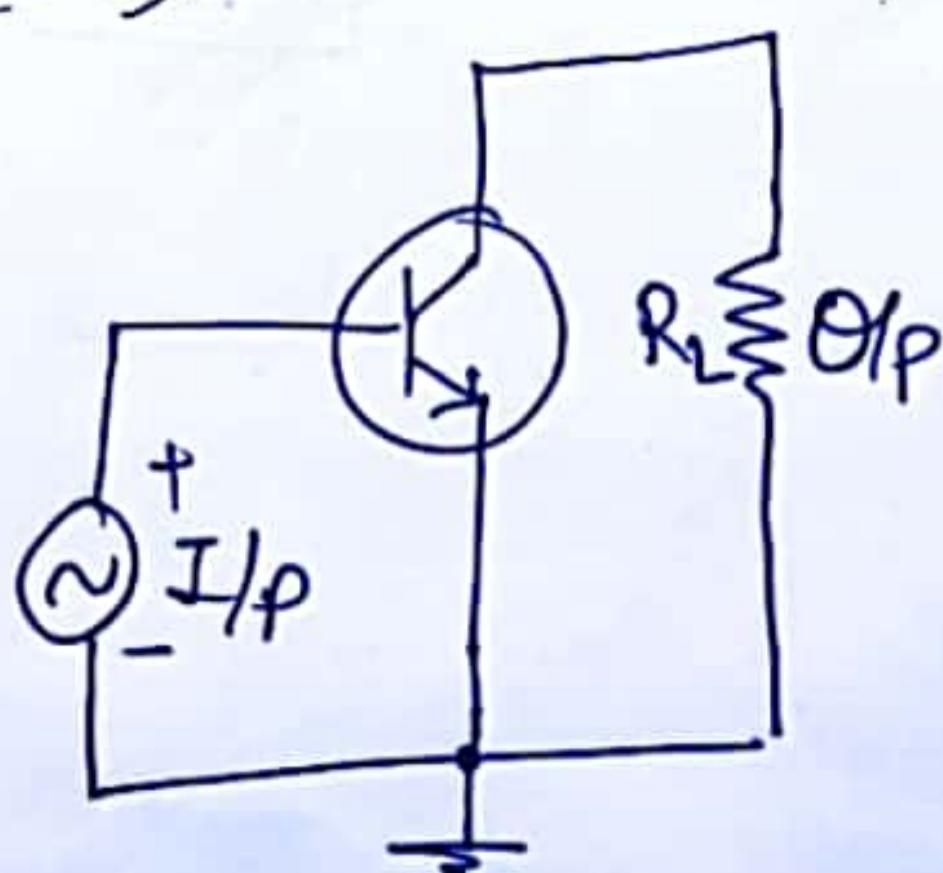
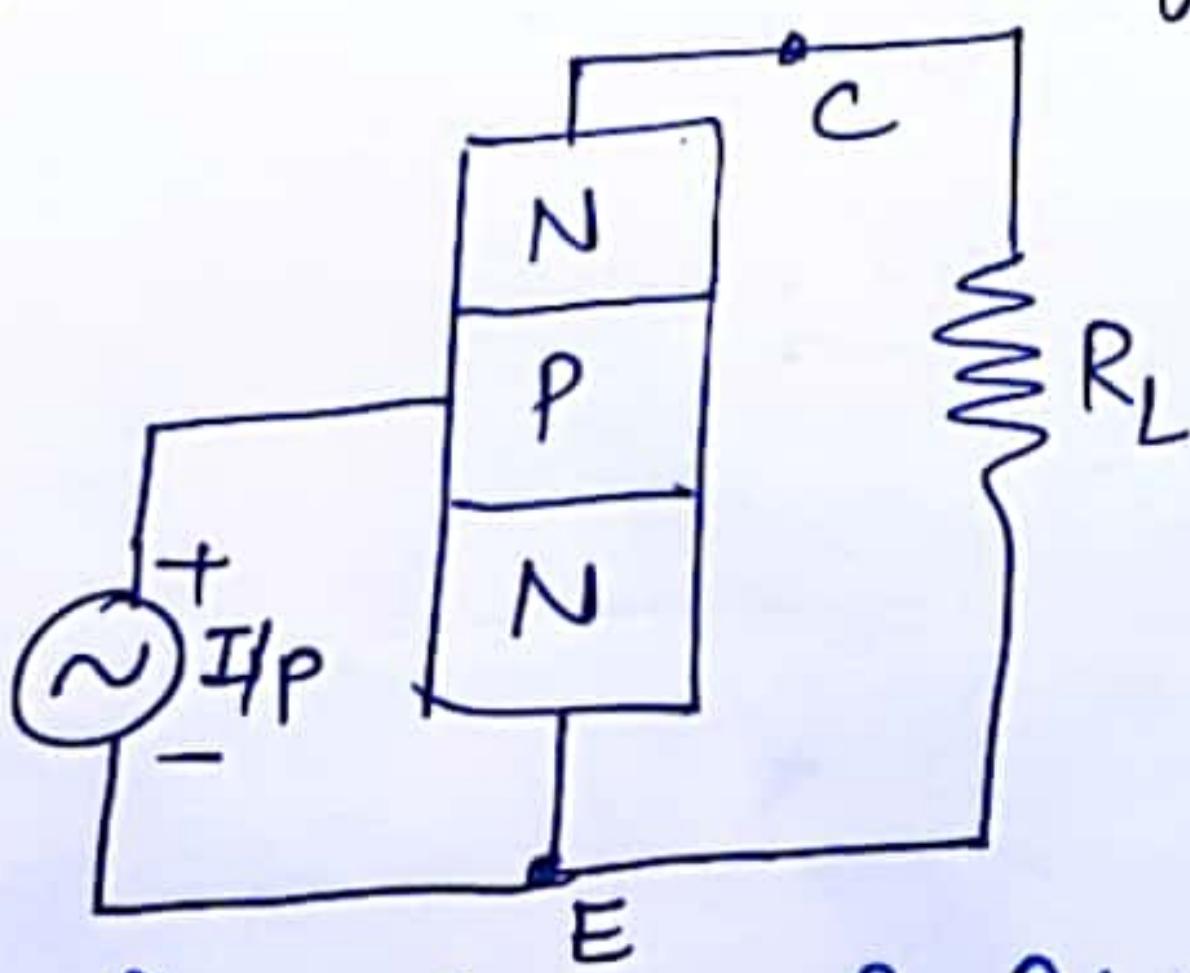


fig:- Common Base Configuration

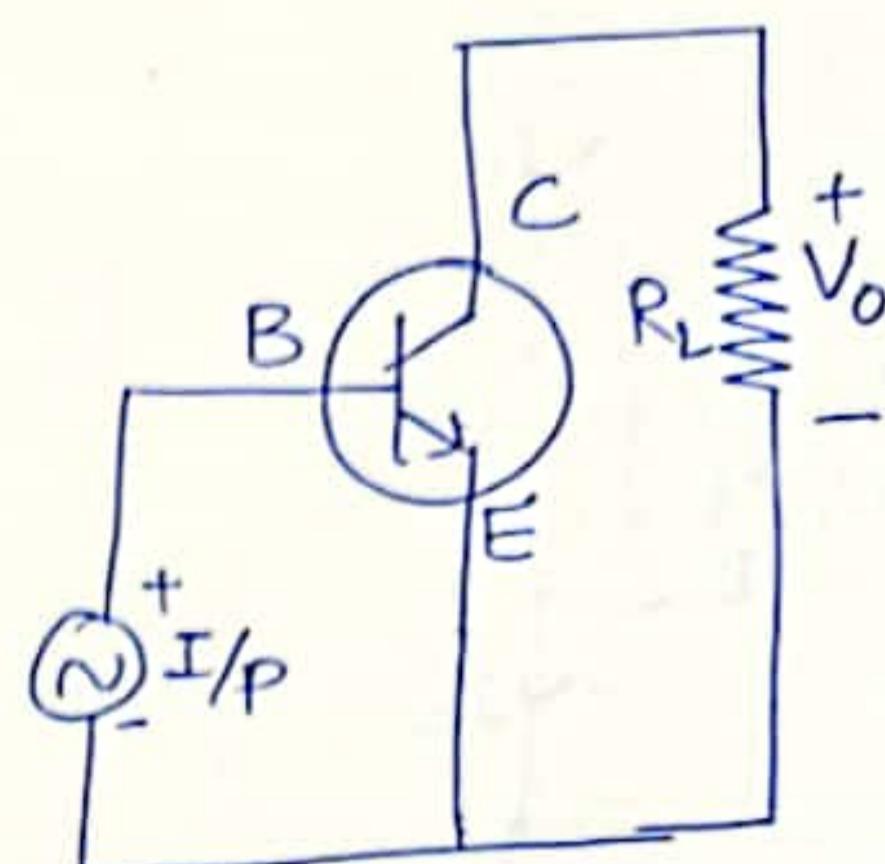
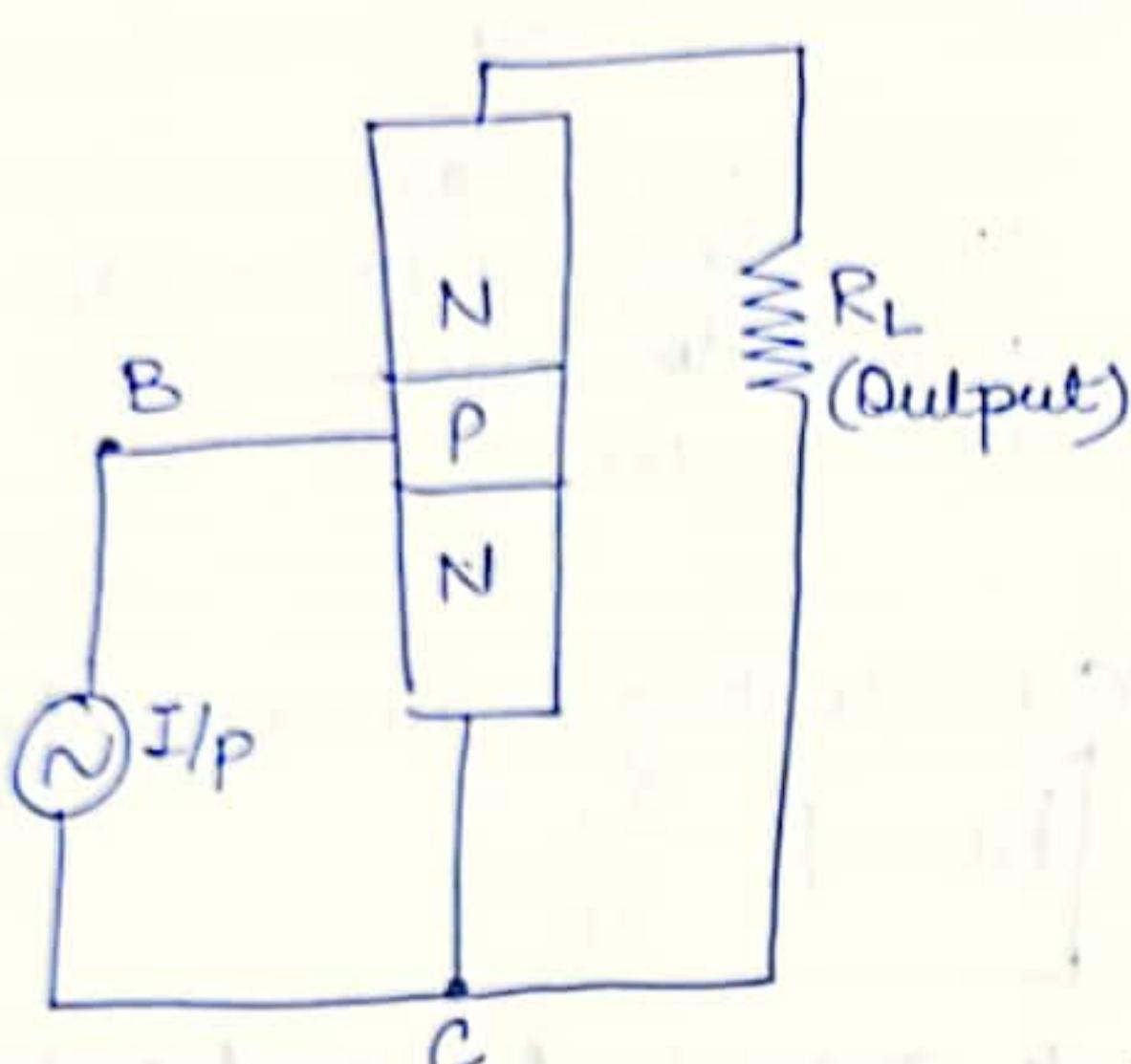
#### (ii) Common Emitter Configuration (CE):-



This configuration is widely used for many applications like amplifiers.

Ques:-  
switching circuit etc.

### (iii) Common Collector Configuration (CC)



Current Gain ( $\alpha$ ) in common base configuration:-

In this configuration, emitter current is I/P current and collector current is the O/P current.

The current gain of a transistor is defined as ratio of transistor O/P current to I/P current.

$$\boxed{\text{dc current gain } \alpha = \frac{I_C}{I_E} = h_{FB}}$$

① In  $\approx$  CB configuration  $I_C = 4.10 \text{ mA}$  &  $I_E = 5.18 \text{ mA}$ . Calculate CB d.c current gain ..

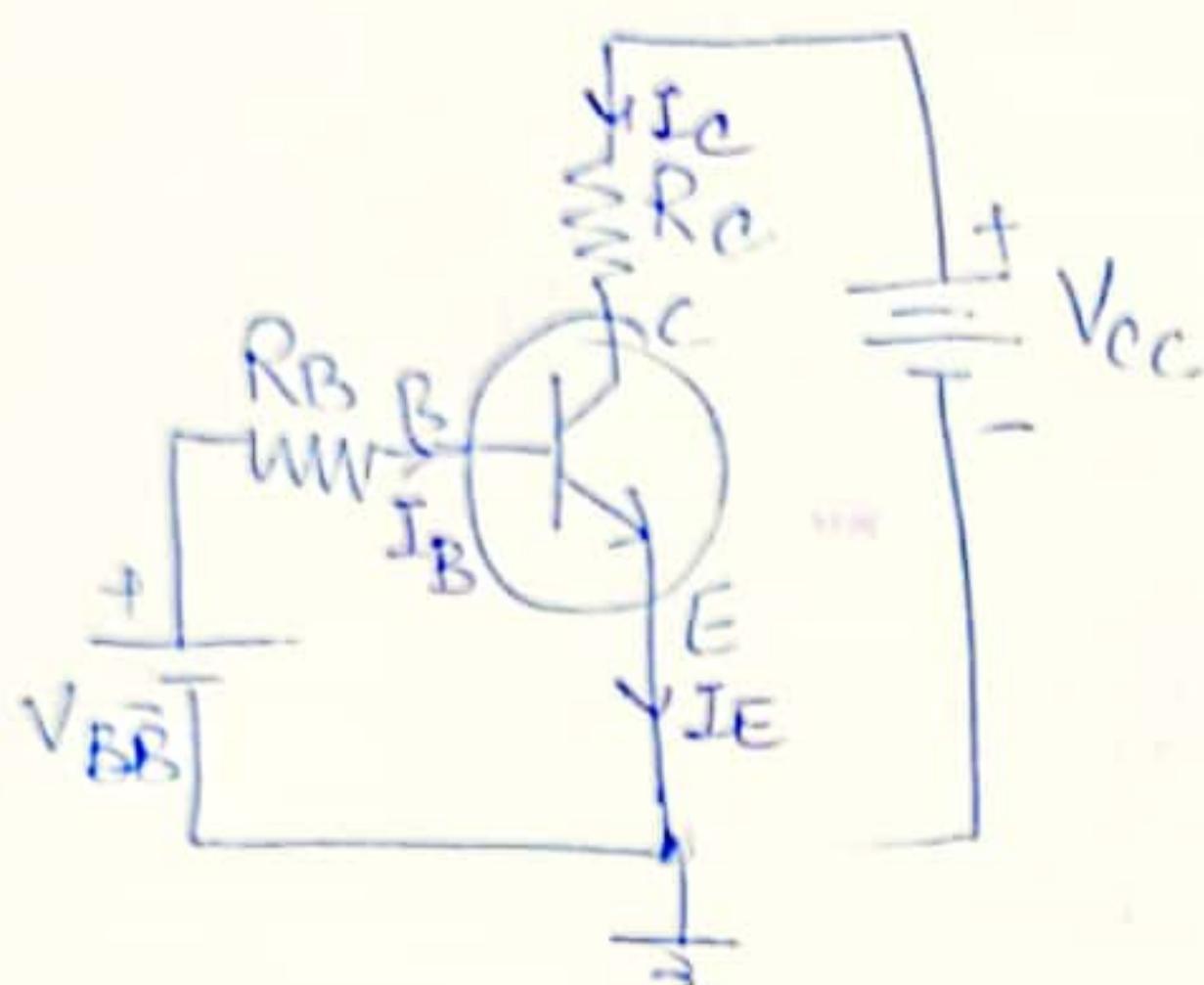
$$\alpha_{\text{d.c.}} = \frac{I_C}{I_E} = \frac{4.10}{5.18} = 0.79$$

$$\boxed{\alpha_{\text{dc}} = 0.79}$$

ac current gain is defined as a ratio of Change in collector current ( $\Delta I_C$ ) to change in emitter current ( $\Delta I_E$ ) for constant  $V_{CB}$ .

$$\boxed{\alpha_o = \alpha_{\text{ac}} = \frac{\Delta I_C}{\Delta I_E}}$$

Current gain ( $\beta$ ) of a transistor in CE (Common Emitter) Configuration:-



Input  $\rightarrow$  Base current  
O/P  $\rightarrow$  Collector current.

In CE configuration current gain is defined as the ratio of collector current to the base current.

DC current gain in CE config.

$$\beta_{dc} = \beta = \frac{I_c}{I_B}$$

$\because I_c \gg I_B \therefore \beta$  may be range from 20 to 300.

Typical Range of  $\beta = 20$  to  $300$   
d is always less than unity

AC current gain is CE config.

$$\beta_0 = \frac{\Delta I_c}{\Delta I_B}$$

For all practical purpose

$$\beta = \beta_0 \text{ & } d = d_0$$

Relation between current gain  $\alpha$  &  $\beta$ .

We know that  $I_E = I_C + I_B$ .

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1 \quad \textcircled{2}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \textcircled{1}$$

$$\beta = \alpha(1 + \beta)$$

$$\alpha = \frac{\beta}{1 + \beta}$$

where  $I_E \rightarrow$  emitter current

$I_C \rightarrow$  collector current

$I_B \rightarrow$  base current

again for eqn ①

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$
 ~~$\frac{1}{\alpha} = \frac{1 + \beta}{\beta}$~~

$$\alpha = \frac{\beta}{1 + \beta}$$

again write eq<sup>n</sup> ①

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} - 1 = \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Question If value of  $\alpha = 0.950$   
Find the value of  $\beta$ .

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.950}{1-0.950} = \frac{0.950}{0.050}$$

$$\boxed{\beta = 19}$$

Question :- For CE configuration, for which  $I_E = 10\text{mA}$  &  $\beta = 100$ .  
Determine the value of  $I_C$  &  $I_B$ .

$$\beta = \frac{I_C}{I_B}, \quad \alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{\beta}{1+\beta} = \frac{100}{101} = 0.99$$

$$I_C = \alpha I_E = 0.99 \times 10\text{mA}$$

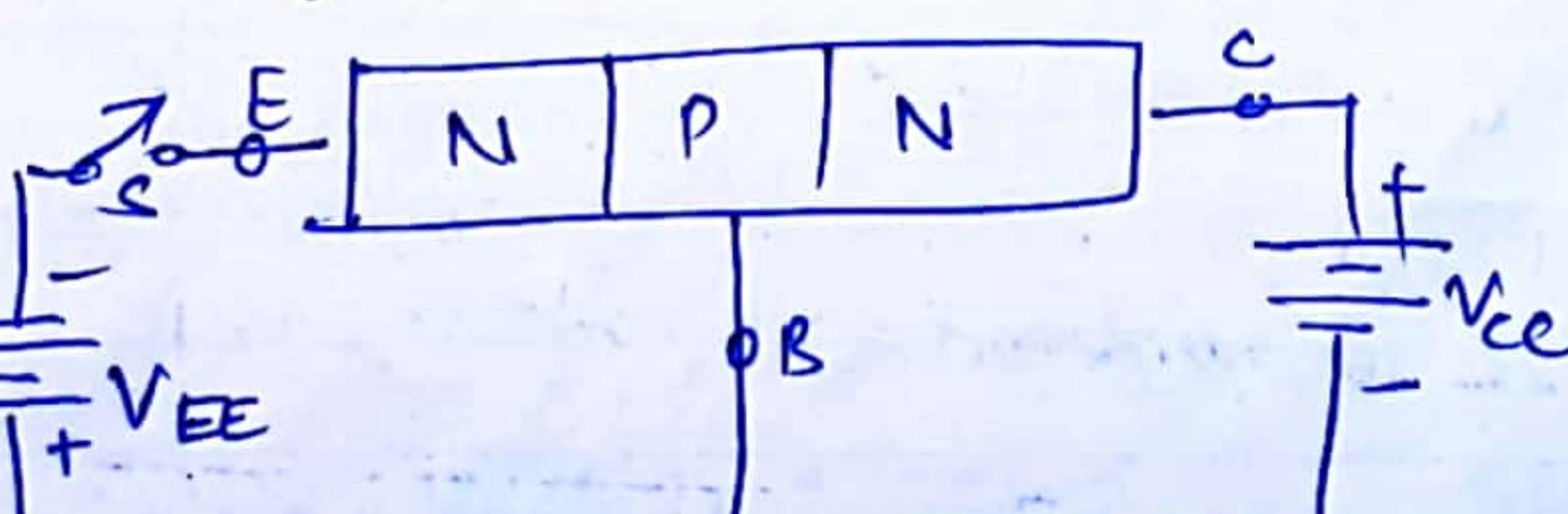
$$\boxed{I_C = 9.9\text{mA}}$$

$$I_B = \frac{I_C}{\beta} = \frac{9.9\text{mA}}{100}$$

$$= 0.099\text{ mA}$$

$$\boxed{I_B = 99\mu\text{A}}$$

Leakage current in CB Transistor.



Question  $\beta = 100$ . If the value of  $I_E = 10\text{mA}$ . Then determine the value of  $I_C$  &  $I_B$ .

$$\text{Soln} \quad \beta = \frac{I_C}{I_B} \quad \alpha = \frac{I_C}{I_E}$$

$$100 I_B = I_C \quad \alpha = \frac{\beta}{1+\beta}$$

$$I_C = \alpha I_E \quad \alpha = \frac{100}{101} = 0.99 \\ = 0.99 \times 100\text{mA}$$

$$\boxed{I_C = 99\text{mA}}$$

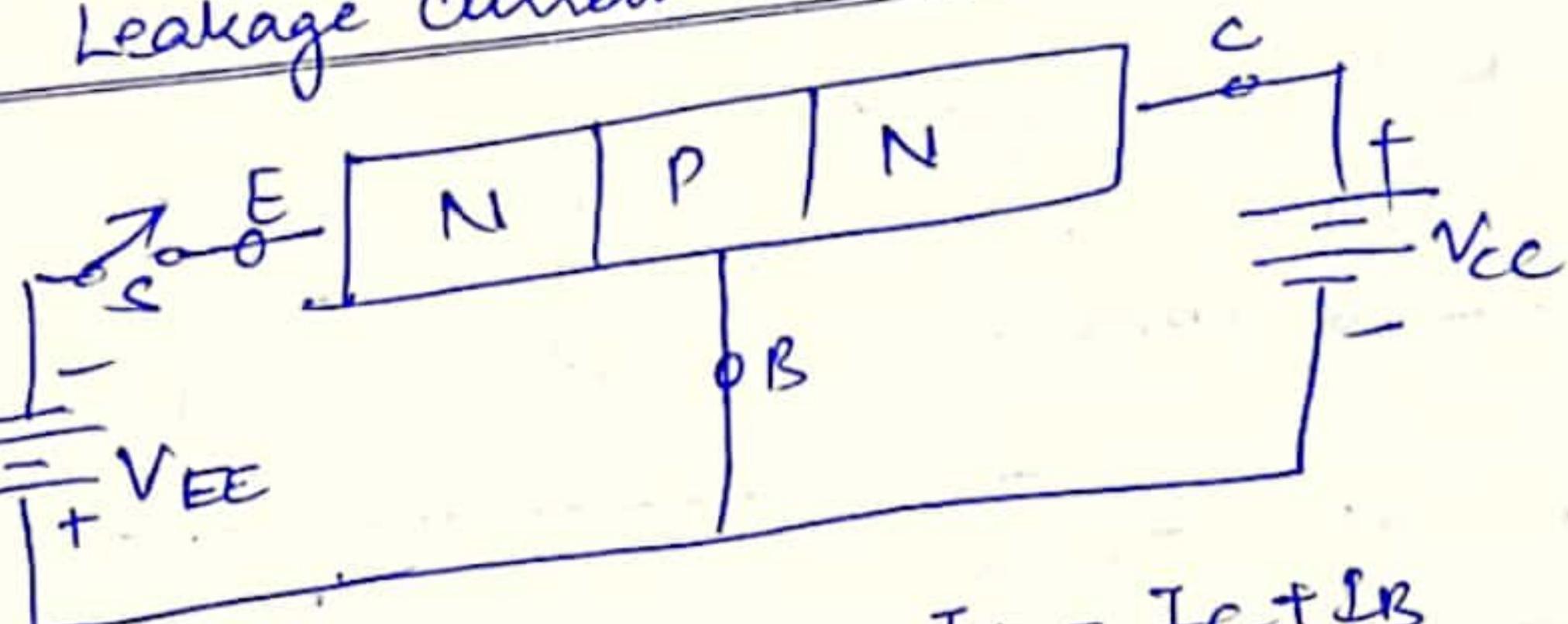
$$\boxed{\alpha = 0.99}$$

$$I_B = \frac{I_C}{100}$$

$$I_B = \frac{99 \times 100\text{mA}}{100}$$

$$\boxed{I_B = 0.99\text{mA}}$$

## Leakage current in CB Transistor



$$\text{when } S \text{ is closed, } I_E = I_C + I_B$$

when  $S$  is open, EB junction of transistor is open circuit  
 means  $I_B = 0$  &  $I_C = 0$  but CB junction is R.B  
 ∵ minority carriers diffuse into across CB junction  
 & produce small current which is called as leakage current  $I_{CBO}$  or  $I_{CO}$ .

$I_{CBO}$  or  $I_{CO}$  → leakage current b/w collector and base with emitter open.

(like reverse saturation current in pn junction)

Collector current of transistor contains :-

- ① Injected current due to majority carriers ( $\alpha I_E$ )
- ② Leakage current produced by minority carriers  $I_{CBO}$  or  $I_{CO}$ .

$$I_C = \alpha I_E + I_{CBO}$$

$$\alpha I_E = I_C - I_{CBO}$$

$$\alpha = \frac{I_C - I_{CBO}}{I_E} = \frac{I_C - I_{CBO}}{I_B + I_C}$$

$$\alpha I_B + \alpha I_C + I_{CBO} = I_C$$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

Leakage current in CE configuration:-

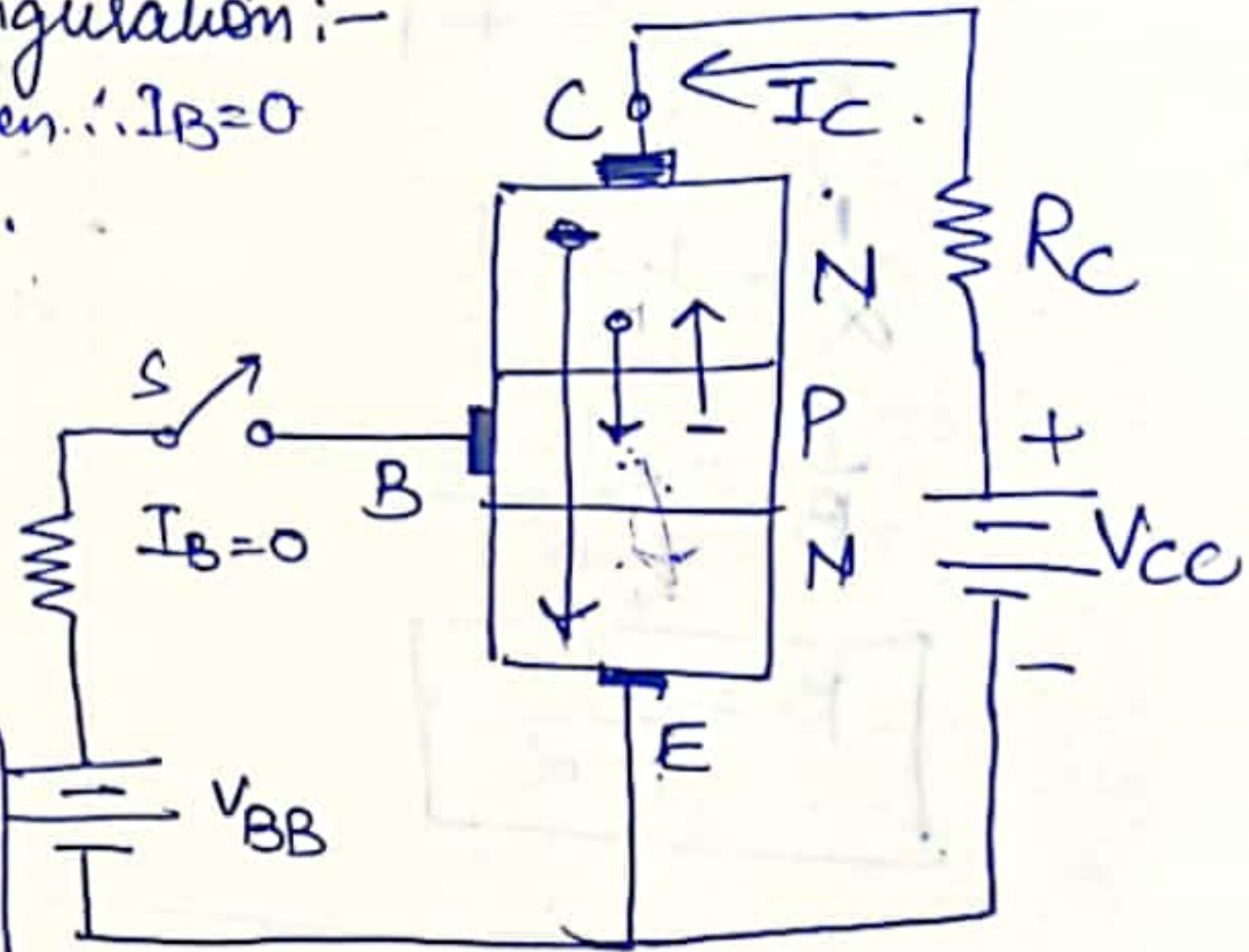
When S is open, EB junction open.  $\therefore I_B = 0$

But  $I_{CEO}$  flows between C & E.

Leakage current  $I_{CEO}$  is not only due to minority carriers  $I_{CBO}$  but also due to hole flow across junction EB. Which make it little F.B.

$$\therefore I_{CEO} = I_{CBO} + \beta I_{CBO}$$

due to minority  
due to F.B - EB junction



$$I_E = I_C + I_B \quad \text{for CB config: } I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

We know that,  $\beta = \frac{\alpha}{1-\alpha}$  and  $\frac{I_{CBO}}{1-\alpha} = I_{CEO}$   
(Leakage current in CE config)

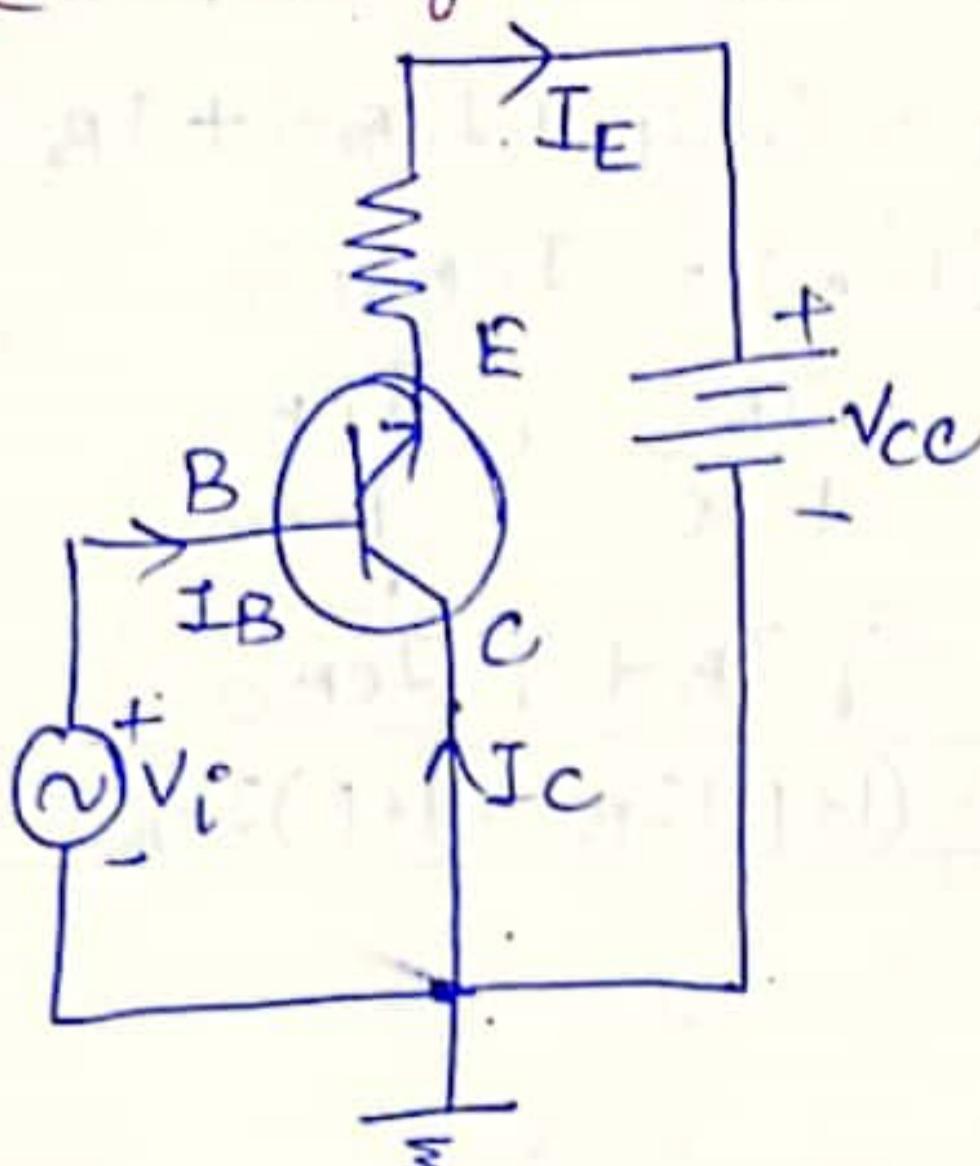
$$I_C = \beta I_B + I_{CEO}$$

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \frac{I_{CBO}}{1-\left(\frac{\beta}{1+\beta}\right)} = \frac{(1+\beta) I_{CBO}}{1+\beta-\beta}$$

$$I_{CEO} = (1+\beta) I_{CBO}$$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

## Common Collector (CC) Configuration : Collector feedback (Emitter follower)



I/p current  $\rightarrow I_B$

O/p current  $\rightarrow I_E$

current gain is ratio of change in I<sub>emitter</sub> current to change in base current.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relation between  $\alpha$ ,  $\beta$ ,  $\gamma$

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} + 1$$

$$\boxed{\gamma = \beta + 1}$$

$$\text{put } \beta = \frac{\alpha}{1-\alpha}$$

$$\gamma = \frac{\alpha}{1-\alpha} + 1$$

$$\gamma = \frac{\alpha + 1 - \alpha}{1-\alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

Note: \* Value of  $\gamma$  is approximately equal to  $\beta$ . This shows that current gain in CC configuration is very high as in CE config. but it is rarely used for amplification purpose because voltage gain is 1. It is mainly used for impedance matching.

\* It is used as emitter follower because O/p (emitter) is following the input (gain  $\approx 1$ ).

~~leakage~~  
Collector current in CC config:-

$$I_E = I_C + I_B$$

$$I_C = \alpha I_E + I_{CBO} \quad \therefore I_E = (\alpha I_E + I_{CBO}) + I_B$$

$$I_E(1-\alpha) = I_{CBO} + I_B$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$\frac{1}{1-\alpha} = \gamma$$

$$\gamma = 1+\beta$$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

$$\text{or } I_E = (1+\beta) I_B + (1+\beta) I_{CBO}$$

Table 5.2. shows the comparison of the characteristics of three configurations

Table 5.2. Comparison between the three configurations

S.No.	Characteristics	CB configuration	CE configuration	CC configuration
1.	Input resistance	Very low ( $40\Omega$ )	Low ( $50\text{ k}\Omega$ )	Very high ( $750\text{ k}\Omega$ )
2.	Output resistance	Very high ( $1M\Omega$ )	High ( $10\text{ k}\Omega$ )	Low ( $50\Omega$ )
3.	Current Gain	Less than unity (0.98)	High (100)	High (100)
4.	Voltage Gain	Small (150)	High (500)	Less than unity
5.	Leakage Current	Very small ( $5\mu\text{A}$ for Ge and $1\mu\text{A}$ for Si)	Very large ( $500\mu\text{A}$ for Ge and $20\mu\text{A}$ for Si)	Very large ( $500\mu\text{A}$ for Ge and $20\mu\text{A}$ for Si)
6.	Applications	For high-frequency applications	For audio freq. applications	For impedance matching

### 5.19 CE Configuration is Most Widely Used in Amplifier Circuits

For an ideal amplifier circuit, the input impedance should be as high as possible and the output impedance should be as low as possible. Although the input impedance for CC configuration is highest but gain for CC configuration is less than unity. So generally this is not preferred for amplifier circuits.

The input impedance of CE configuration is much higher than CB configuration since

$$r_i \text{ for CB} = \left. \frac{\Delta V_{EB}}{\Delta i_E} \right|_{V_{CE}=\text{Const.}} \quad \dots(5.29)$$

## common - collector

## Transistor Characteristics

for Common base config:-

Input Ch.

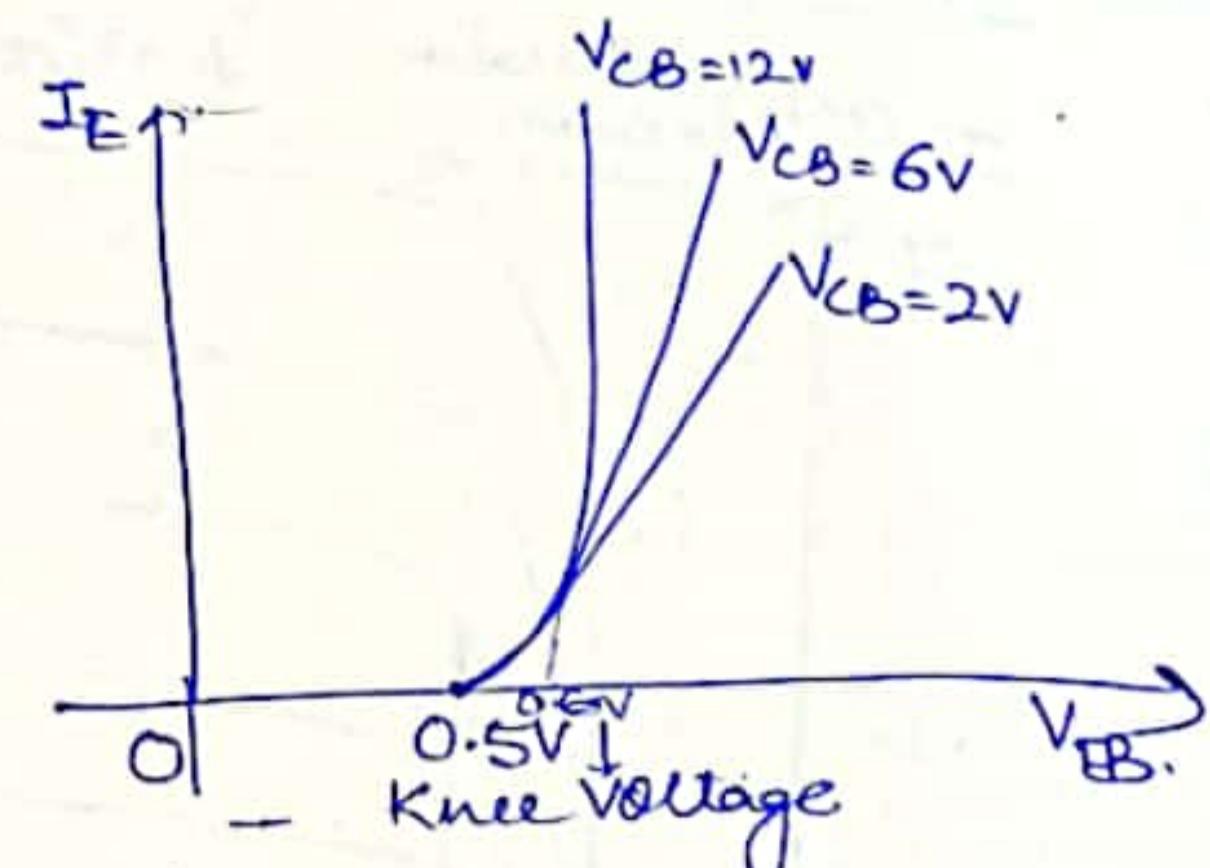
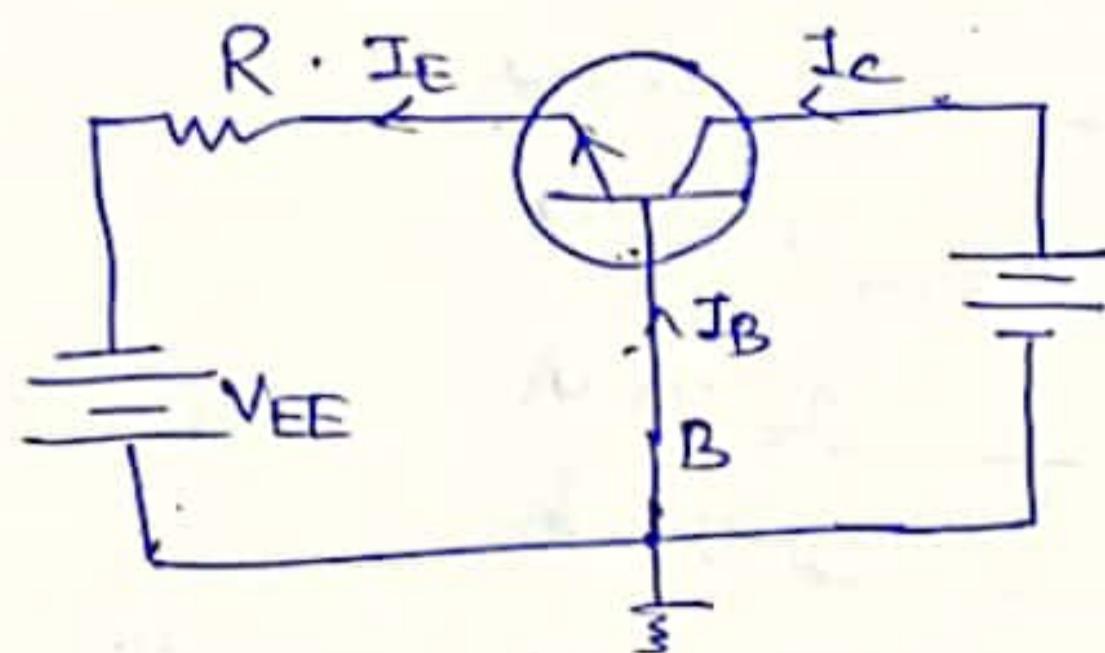


fig:- Input Ch. of CB Config.

- ① Below cut-in voltage or knee voltage  $I_E$  is negligible.
- ② After knee voltage  $I_E$  increases rapidly with small increase in  $V_{EB}$ . This shows I/P resistance is very low.

dynamic  
I/P  
resistance

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E} \quad | V_{CB} = \text{constant}$$

- ③ With increase in  $V_{CB}$ , curve shifts upwards or become vertical.

### 5.21.2. The Early Effect or Base Width Modulation

Considering figure 5.28 and the width of the EB junction region, the total base width is equal to the sum of the widths of the depletion regions extended into the base region from the collector and emitter side and the width of the region occupied by the free charge particles. But as the EB junction is forward biased, the width of its depletion region is very narrow. As the CB junction is reverse biased, the width of its depletion region is much larger. Thus neglecting the width of depletion region at the EB junction we can write :

Total base width = Width of depletion region at the CB junction inside the base region + width of the region containing free charge particles

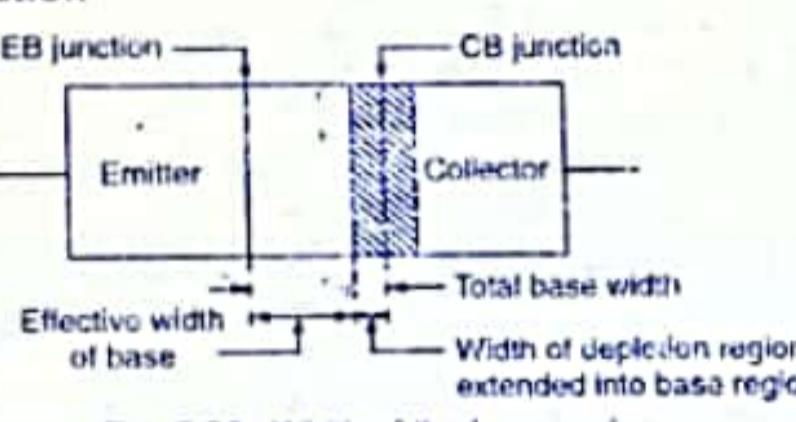


Fig. 5.28. Width of the base region

- Now as  $V_{CB}$  is increased, the reverse voltage applied to the CB junction increases. This widens the depletion region at the collector junction. Due to this, effective width of the base region decreases as shown in figure 5.28.
- This will increase the charge concentration gradient in the base region. Due to increased charge carrier concentration, more number of electrons diffuse from the emitter to base i.e., emitter current increases.
- Thus with increase in  $V_{CB}$  the input current  $I_E$  increases slightly.

- ④  $\beta$  &  $\alpha$  will increase with  $V_{CB}$ .

- ⑤ Minority current increases at CB junction.

James M Early

$V_{CB} \uparrow \Rightarrow W \uparrow \Rightarrow W_{eff}$

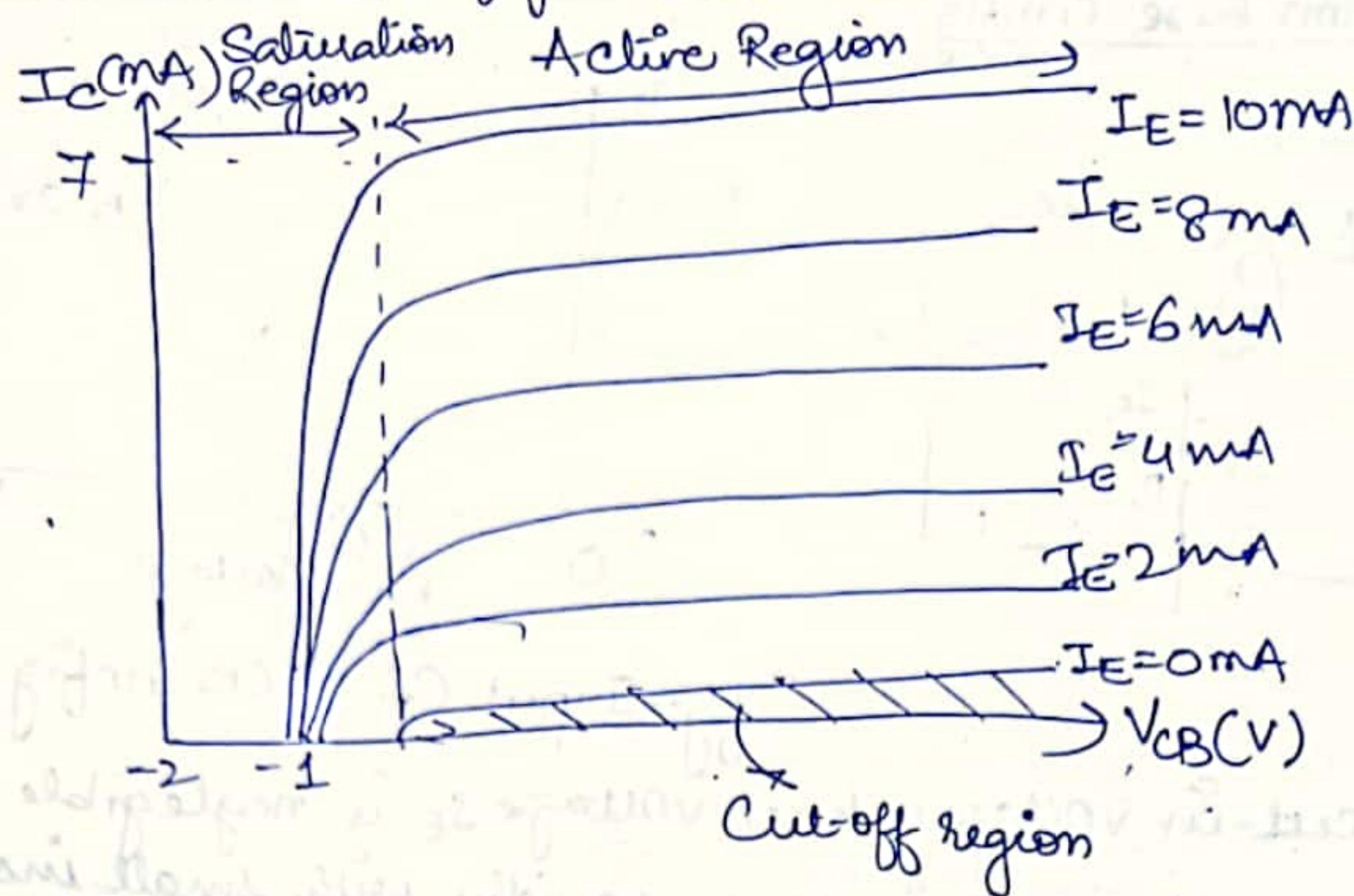
- Recombination ↓

or  
Conc' gradien↑

$E$  will start moving towards base  $I_E \uparrow$

$I_B \downarrow \rightarrow I_C \uparrow$   
 $I_E \uparrow$

## O/p Ch. in CB configuration



It has three regions :-

- 1) Active Region      2) Saturation      3) Cut-off

1) Active region:-  $I_E \approx I_C$

$I_E$  increases very slowly with  $V_{CB}$ .  
 O/p resistance = very large.

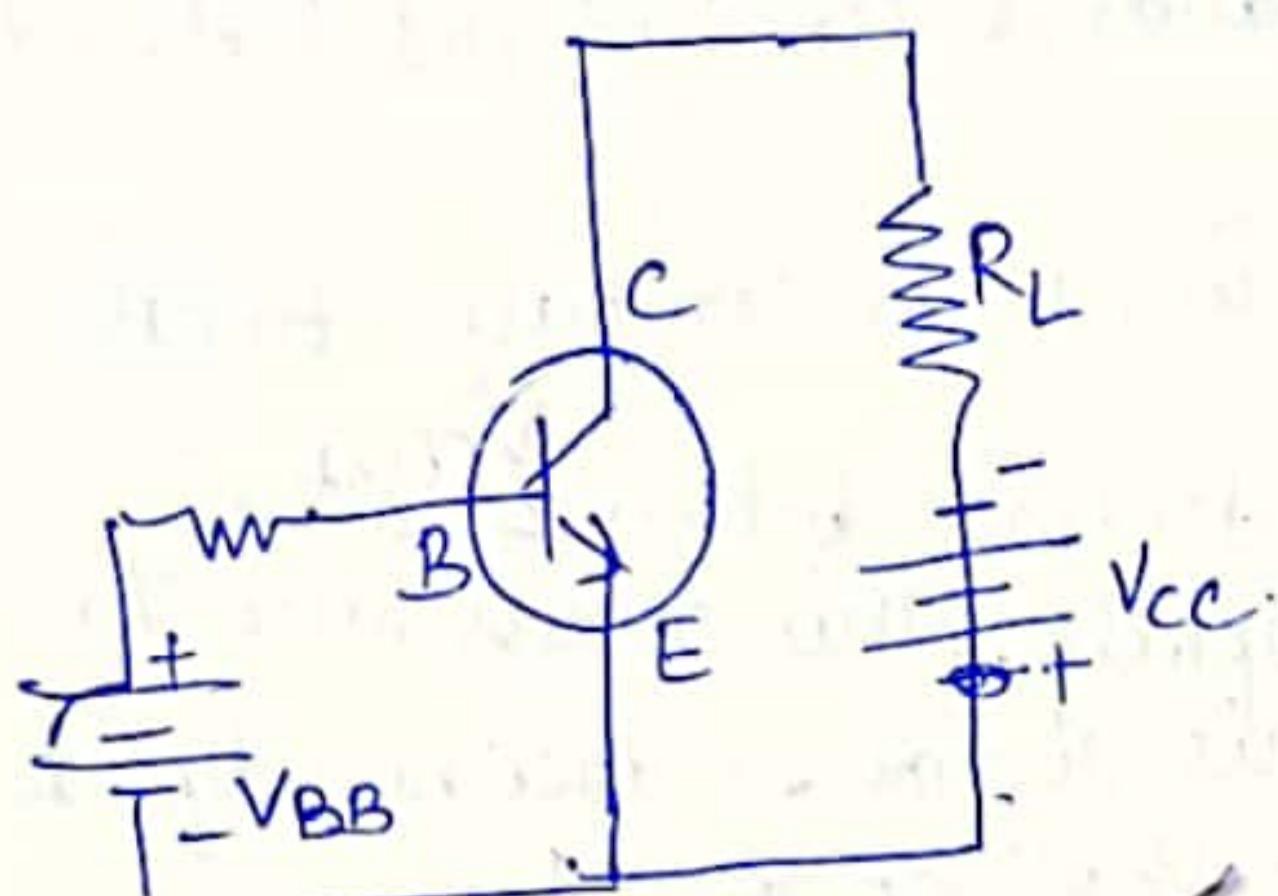
2) Saturation Reg:- If  $V_{CB}$  become large negative, CB junction set to F.B. which causes  $I_C$  decreases rapidly. In this region,  $I_C$  does not depends on  $I_E$  [CB  $\rightarrow$  F.B]  $\therefore I_C$  increases rapidly

3) Cut-off region:- when  $I_E = 0$ ,  $I_C$  is not zero. Both junctions are reverse bias.

$$4) h_o = \frac{\Delta V_{CB}}{\Delta I_C} \Big|_{I_E = \text{const}}$$

$$5) \alpha = \frac{I_C}{I_E} \quad \alpha_{dc} = \frac{I_C}{I_E}$$

## Input Ch. for CE Configuration :-



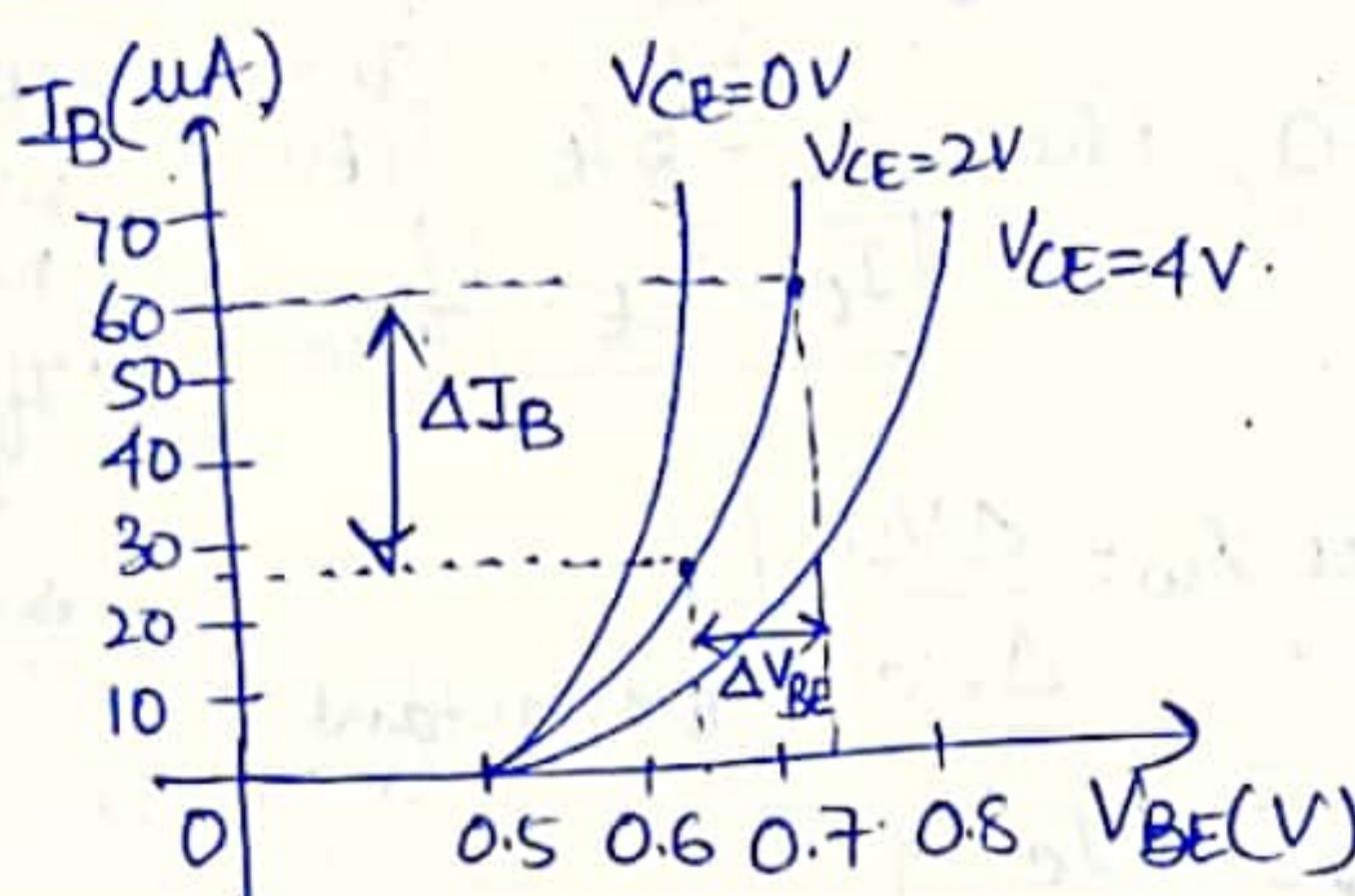
I/P Current  $\rightarrow I_B$

I/P Voltage  $\rightarrow V_{BE}$

Controlling Voltage  $\rightarrow V_{CE}$

Typical I/P Ch. Curves

Relate  $I_B$  &  $V_B$  for various values of  $V_{CE}$



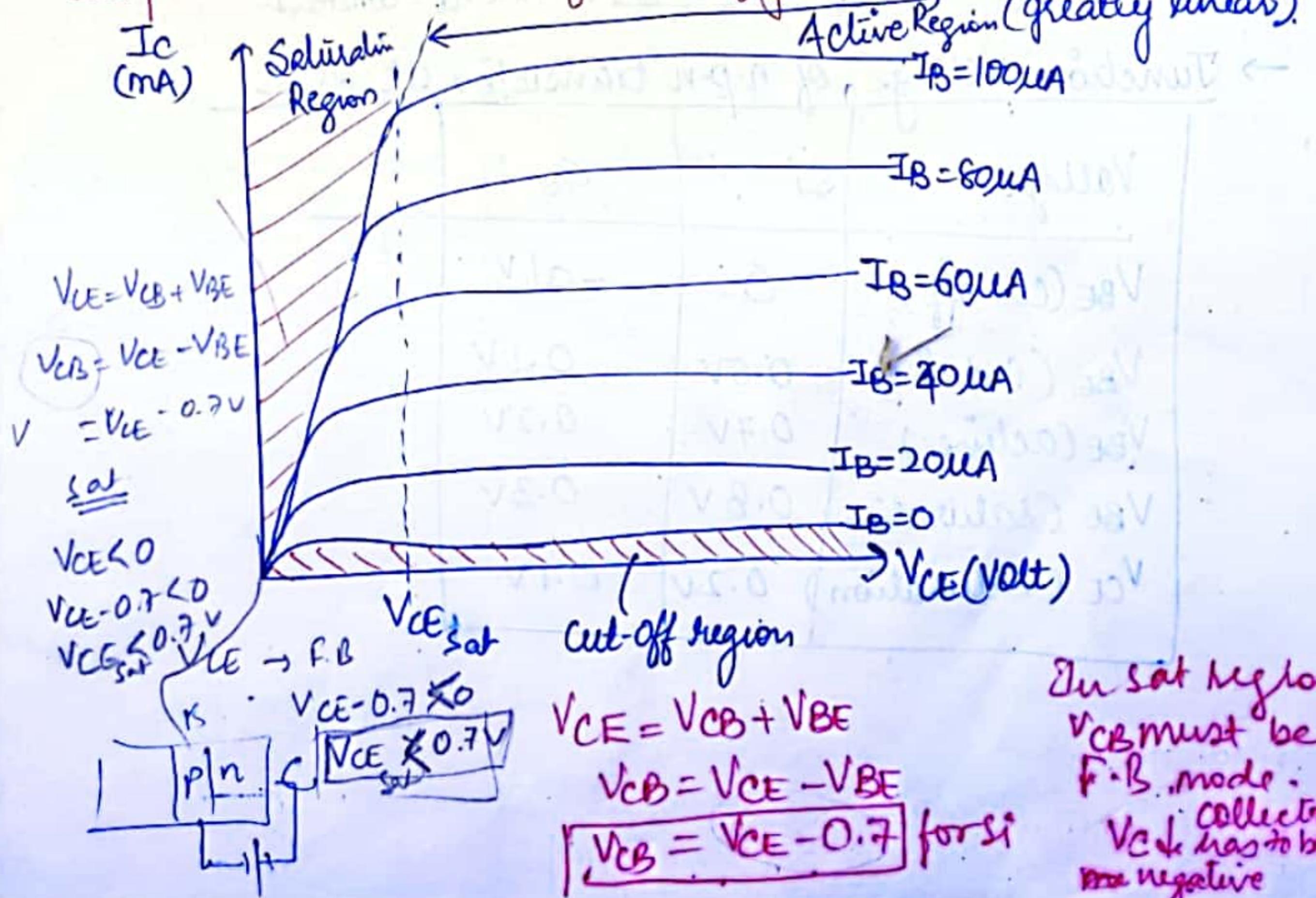
$$\text{dynamic I/P (R_i)} = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE}(\text{const.})}$$

$$V_{CE} = V_{CB} + V_{BE}$$

at const  $V_{BE}$ ,

fig: Input Ch. of CE Configuration

## Output Characteristic of CE Configuration:-



\* In active region:-  $I_C$  increases slowly with  $V_{CE}$ .  $\Delta V_{CE} \propto \Delta I_C$   
 in CE configuration is less horizontal than those  
 in CB Config.

Q.P Resistance is too small in CE as compared to CB.

\* In saturation  $\rightarrow$  when  $V_{CE}$  decrease below zero,  $I_C$   
 decreases rapidly. This occurs due to  
 F.B & CE junction. In this region  $I_C$  does not depends  
 on  $I_B$ .  $V_{CE} = V_{CB} + V_{BE} \Rightarrow V_{CB} = V_{CE} - V_{BE}$   
 $= V_{CE} - 0.7 \text{ V}$

\* Cut-off Region:- If  $I_B = 0$ , then  $I_C = \beta I_B + I_{CEO}$

$$I_C = I_{CEO} \quad | I_B = 0$$

$V_{CB} \rightarrow R_B$

means negative

If  $V_{CE} < 0.7$   
 then in sat region

\* Q.P dynamic resistance  $R_D = \frac{\Delta V_{CE}}{\Delta I_C} \quad | I_B \rightarrow \text{constant}$

\* dc current gain  $B_0 = \frac{\Delta I_C}{\Delta I_B}$

ac current gain  $B_0 = \frac{\Delta I_C}{\Delta I_B} \quad | \text{ when } V_{CE} = \text{constant}$

→ Junction Voltage of n-p-n transistor at 25°C

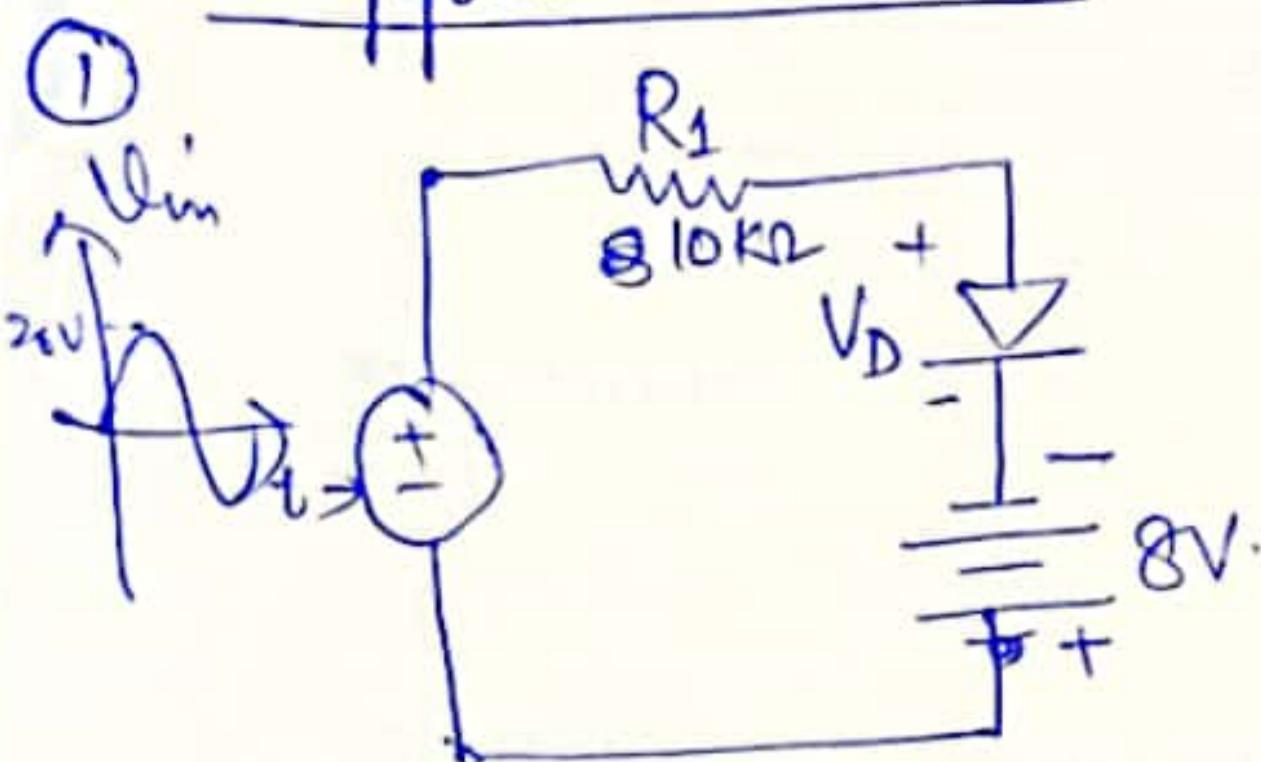
Voltage	$S_i$	$G_e$
$V_{BE}(\text{cut-off})$	0	-0.1V
$V_{BE}(\text{cut-in})$	0.5V	0.1V
$V_{BE}(\text{active})$	0.7V	0.2V
$V_{BE}(\text{saturation})$	0.8V	0.3V
$V_{CE}(\text{saturation})$	0.2V	0.1V

$$38V + 80V = 35V$$

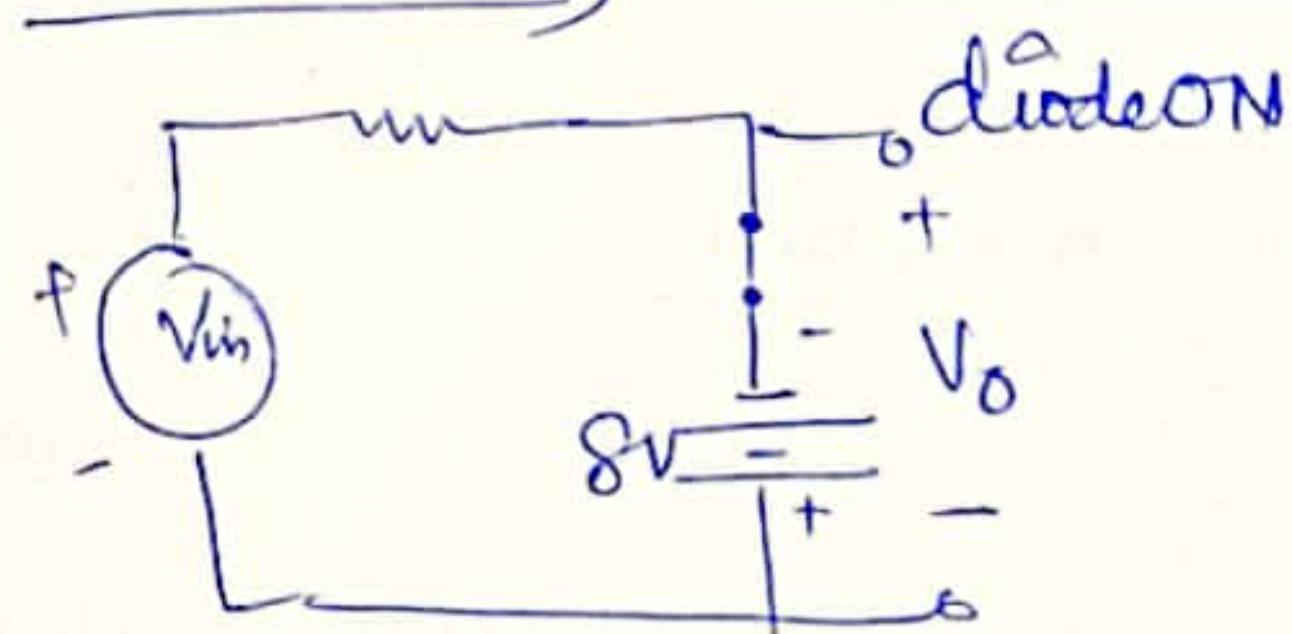
$$38V - 35V = 3V$$

$$12V \quad [F.O - 35V = 3V]$$

## Clipper Questions :-



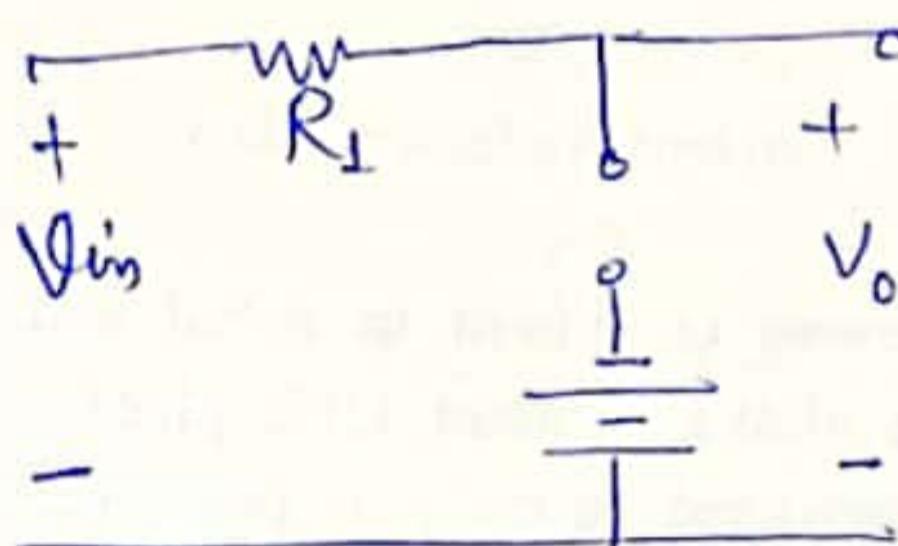
for Positive HC,



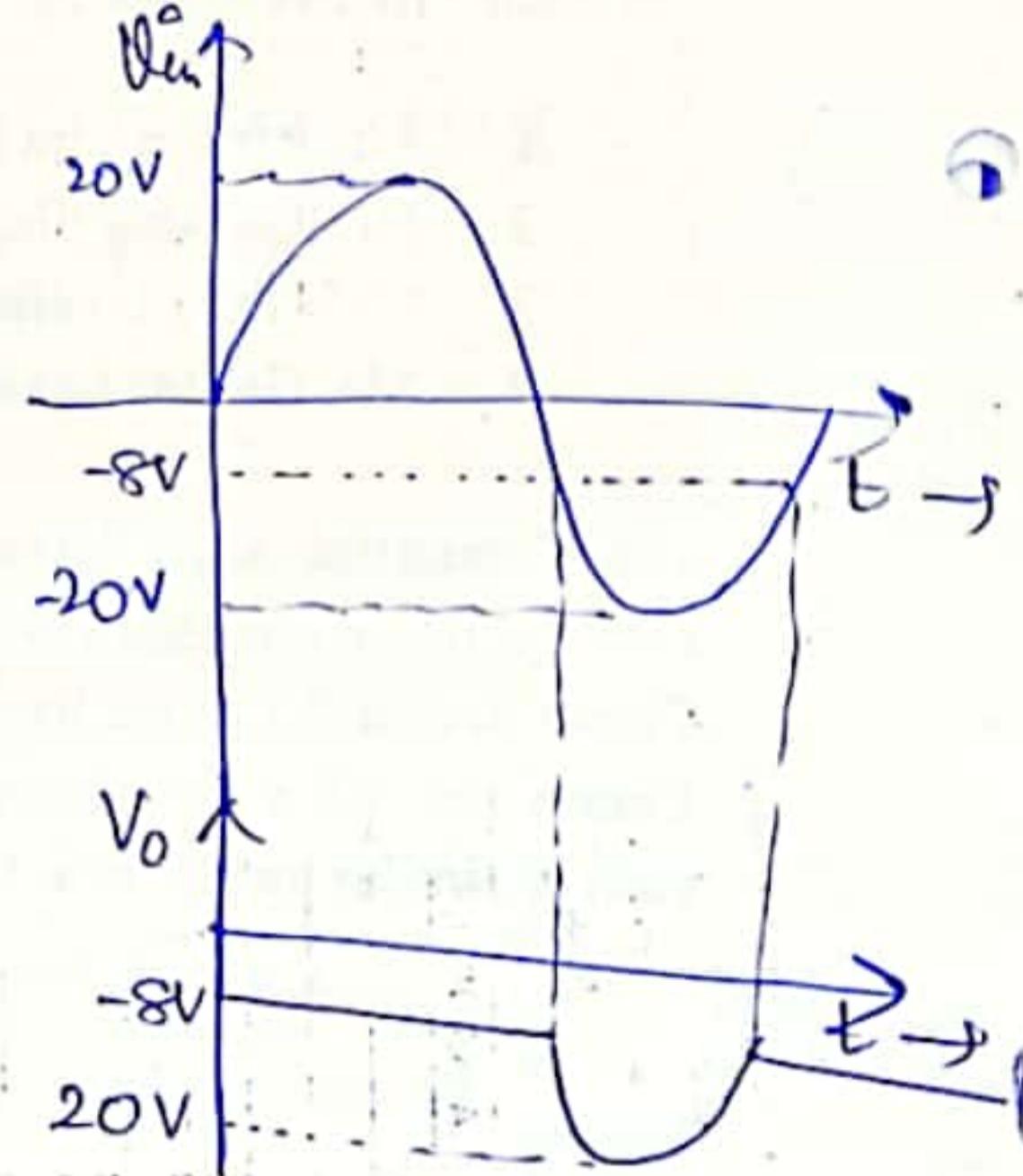
$$V_o = -8V$$

for NHC

If  $V_{in} > -8V$  diode ON  
Otherwise OFF



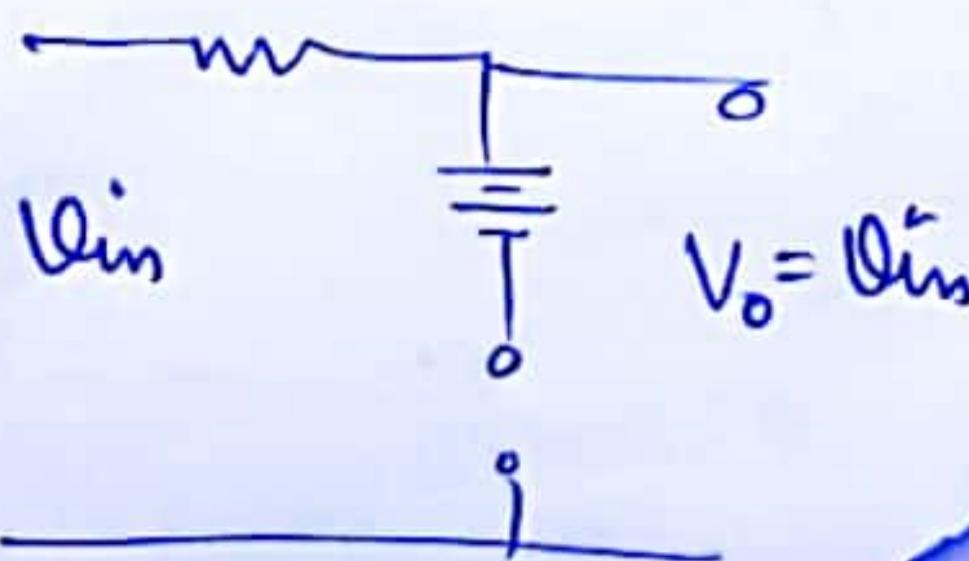
$$V_o = V_{in}$$



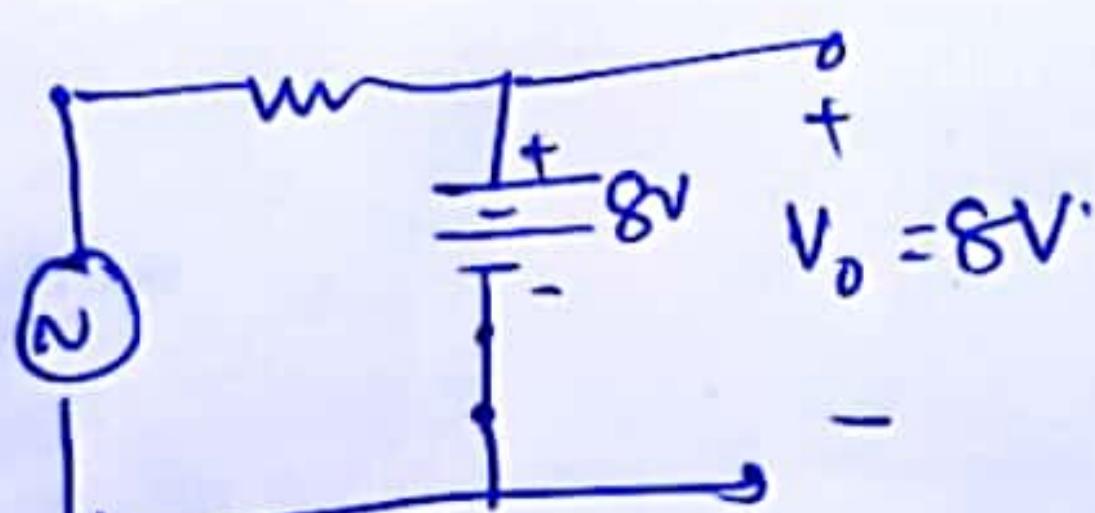
for PHC,

If  $V_{in} < 8V$  diode ON.  
Otherwise diode is OFF

when diode OFF



when diode ON



October 04, 2018

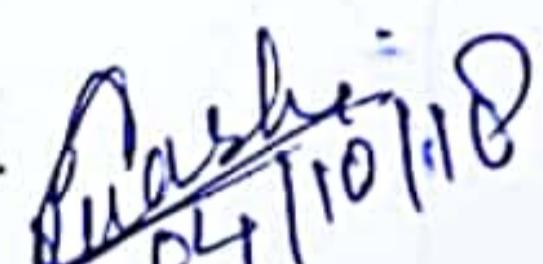
No. PSIT/2018-19/290

ORDER

A complaint has been lodged by a female student Taskeen Owasi of PSITCHE-BBA-I-D (Id. No.22993) against a male student Ravi Ranjan of ME-I-B Mechanical Engineering (PSIT). Therefore, an Inquiry Committee comprising of the following Members under the supervision of the undersigned is being constituted to investigate the causes of said complaint:

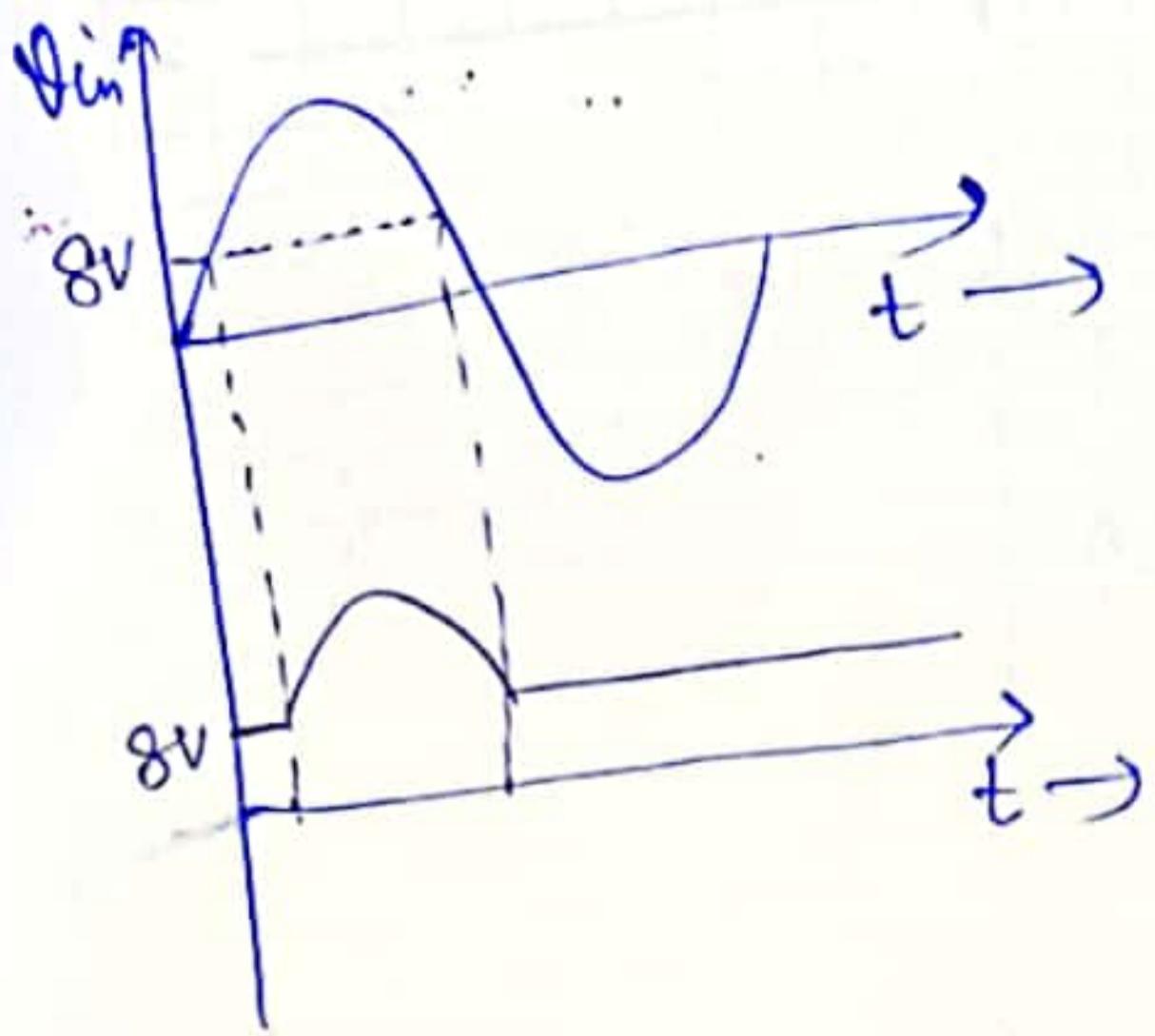
1	Mr. Raghvendra Singh	Member, WWC
2	Dr. Raghuraj Singh Suryavanshi	Member, WWC
3	Ms. Nidhi Shukla	Member, WWC
4	Ms. Garima Gupta	Assistant Professor, BBA

The Committee shall investigate into the above complaint in detail and will identify the circumstances under which the above incident took place. The Committee will submit its report to the undersigned as early as possible. The Committee will also recommend remedial measures so as to prevent recurrence of such or similar incidents in the Institute.

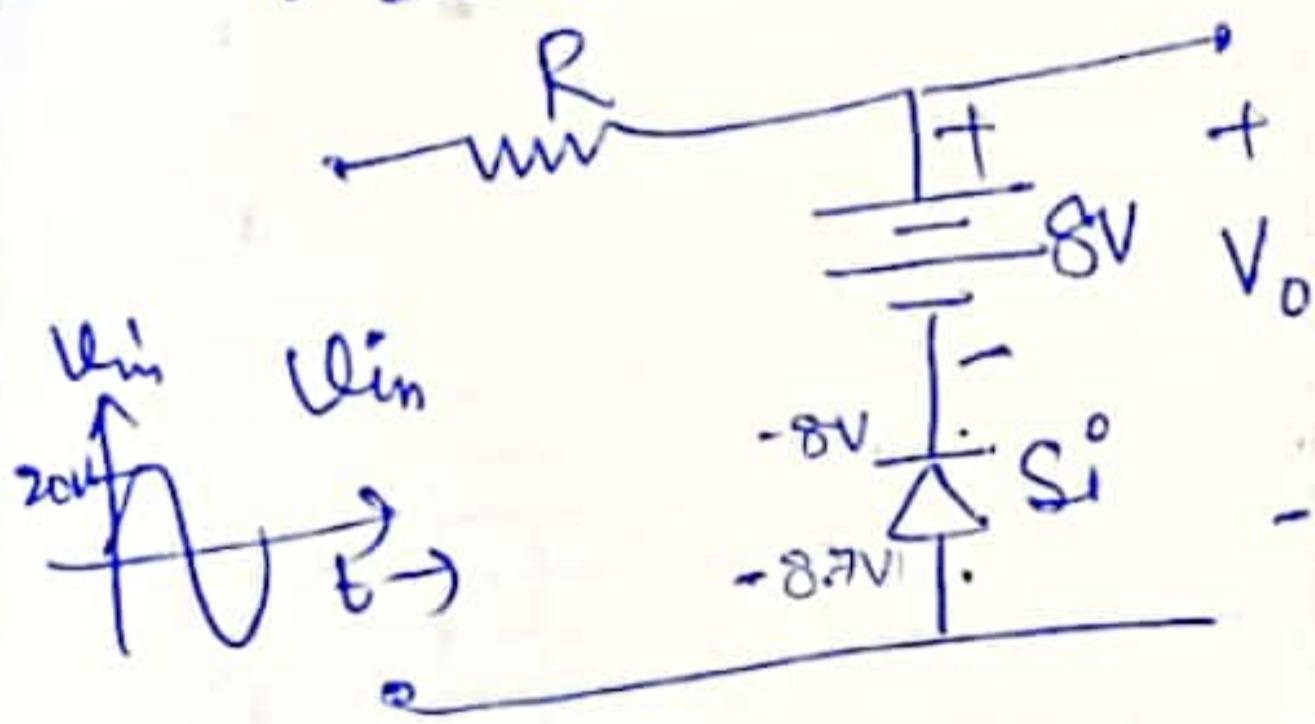
  
Dr. Urvashi Srivastava  
Convener - WWC

Copy for information to :

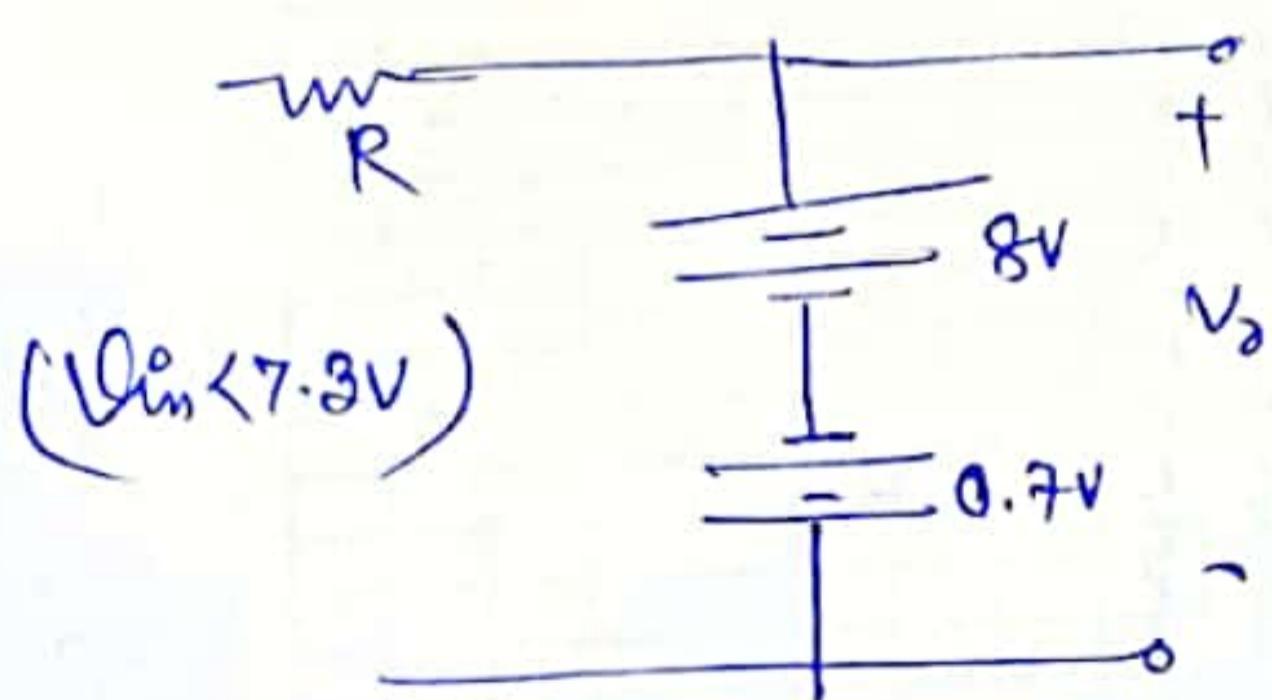
- 1 Director (PSIT)
- 2 Chief Proctor
- 3 Committee Members as above.



If diode is Si,



diode ON



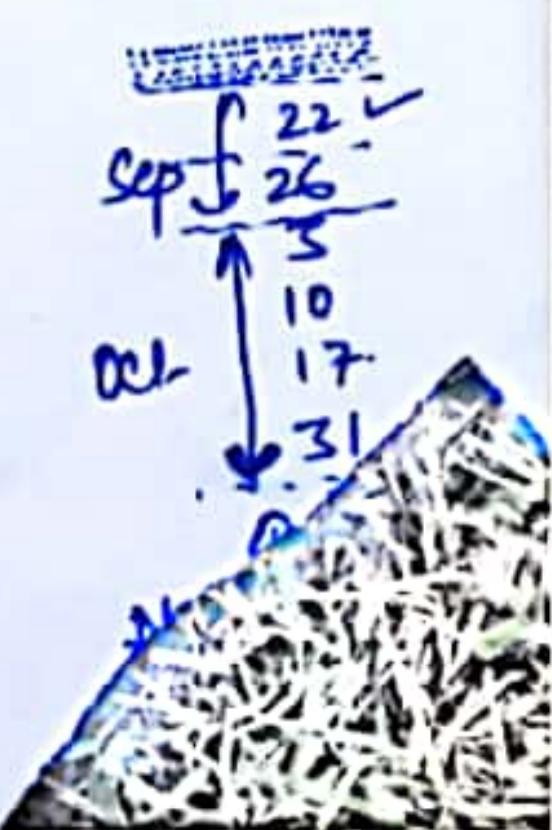
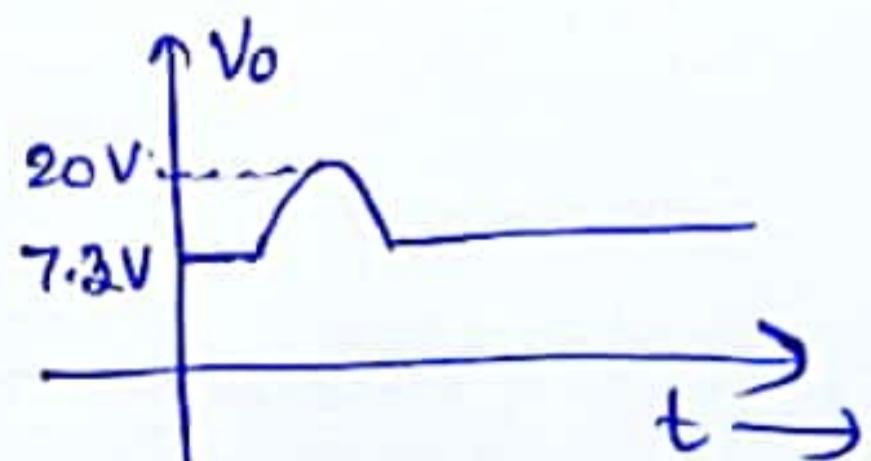
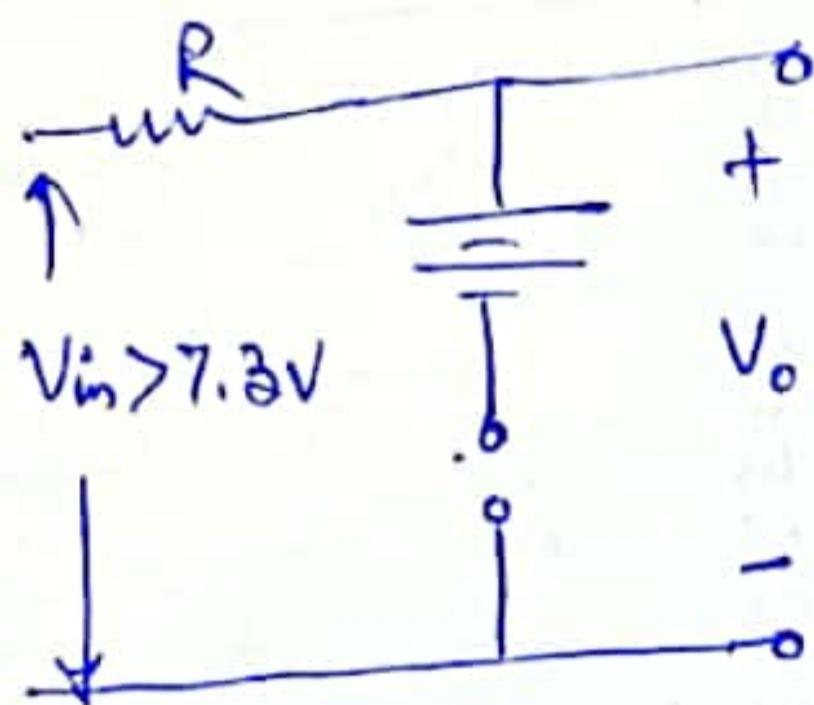
$(V_o < 7.3V)$

diode is ON.

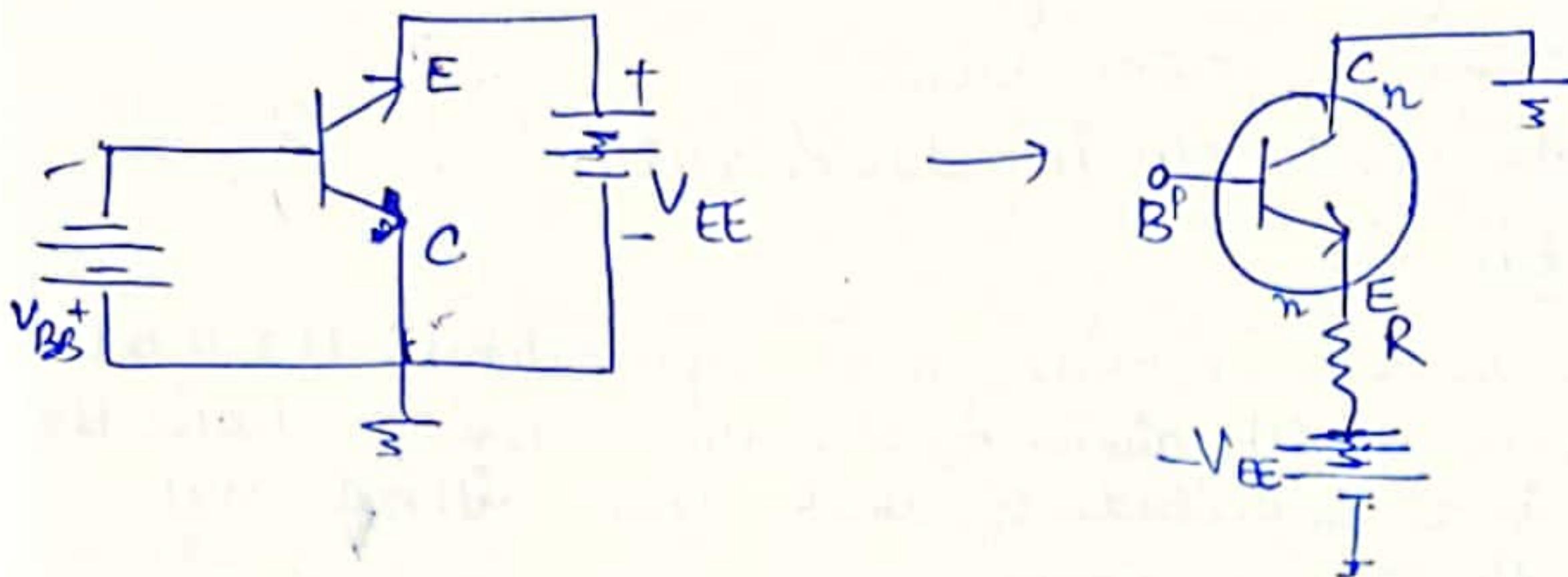
when  $V_{in} < (8 - 0.7V)$   
 $V_{in} < 7.3V$ .

Otherwise OFF.

diode OFF

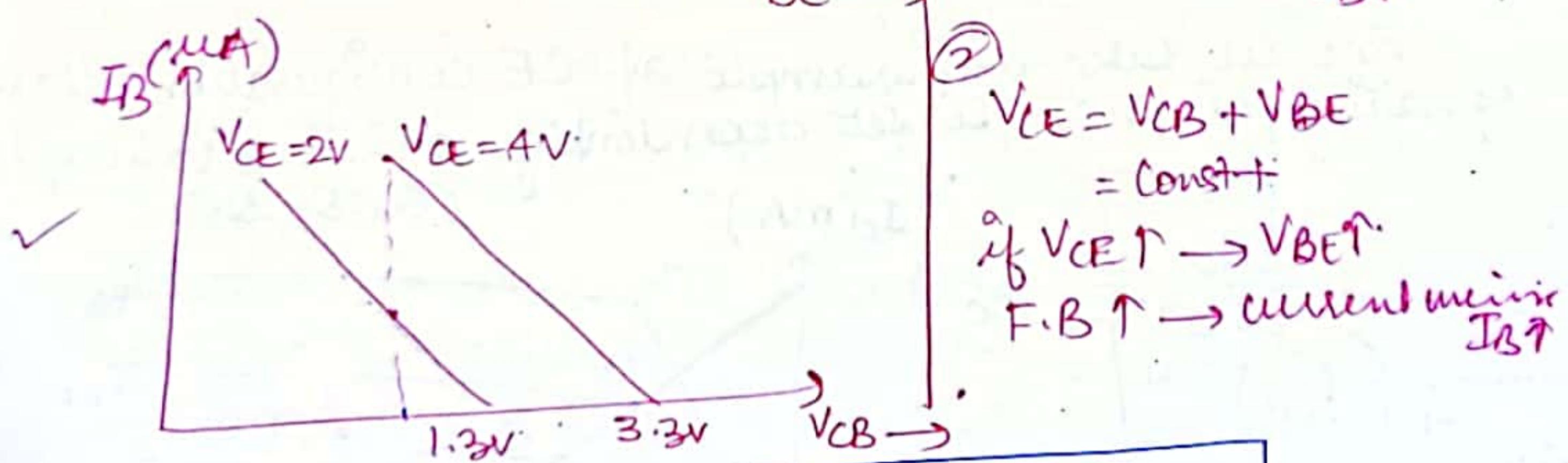
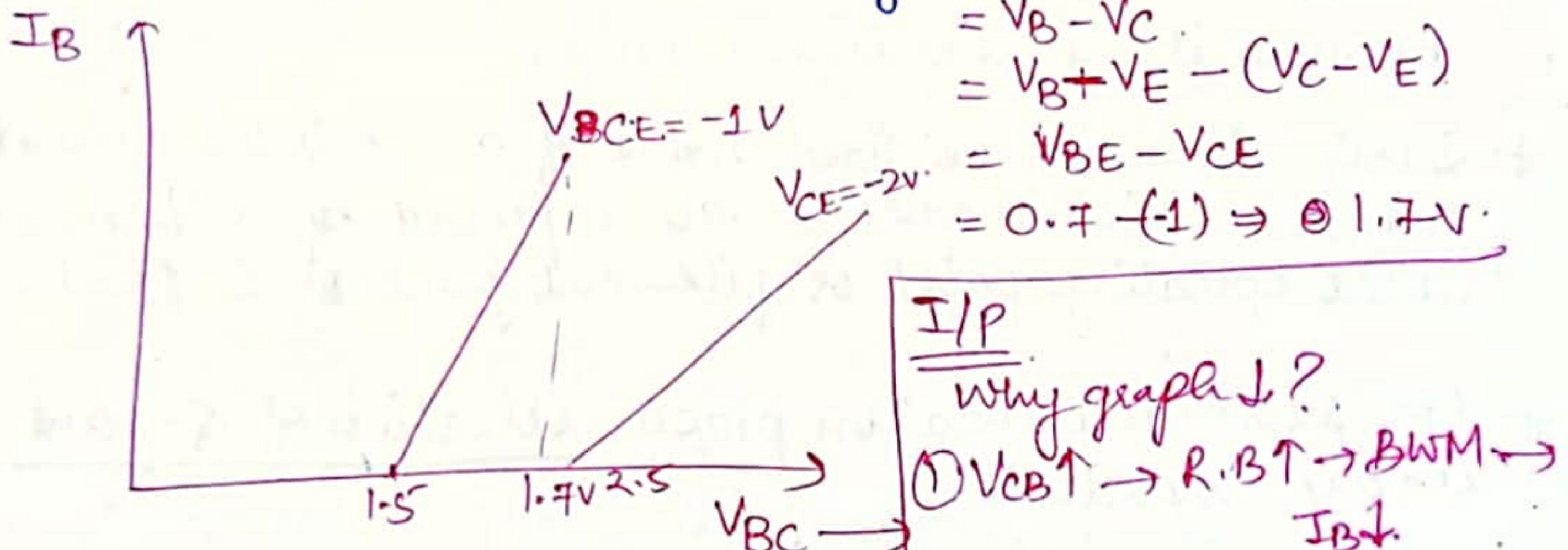


## Common collector Input Ch.

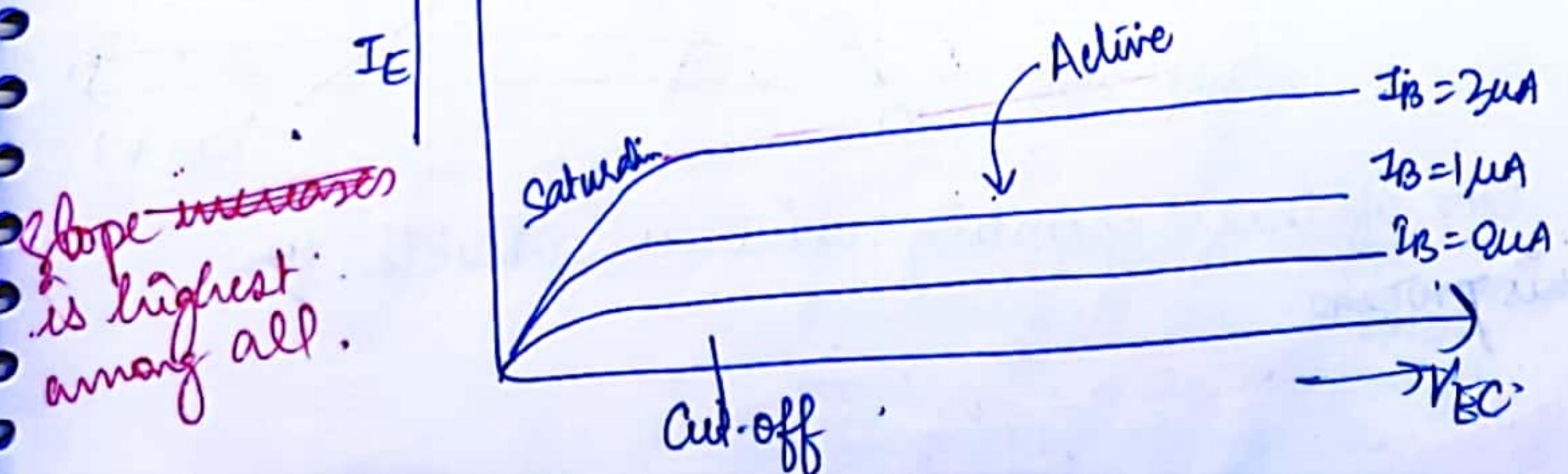


$$\text{I/P current} = I_B \quad \text{I/P Voltage} = V_{BC}.$$

$$= V_B - V_C \\ = V_B + V_E - (V_C - V_E) \\ = V_{BE} - V_{CE} \\ = 0.7 - (-1) \Rightarrow 1.7 \text{ V}$$



$$\boxed{I_E = (1 + \beta) I_B + (1 + \beta) I_{CBO}}$$



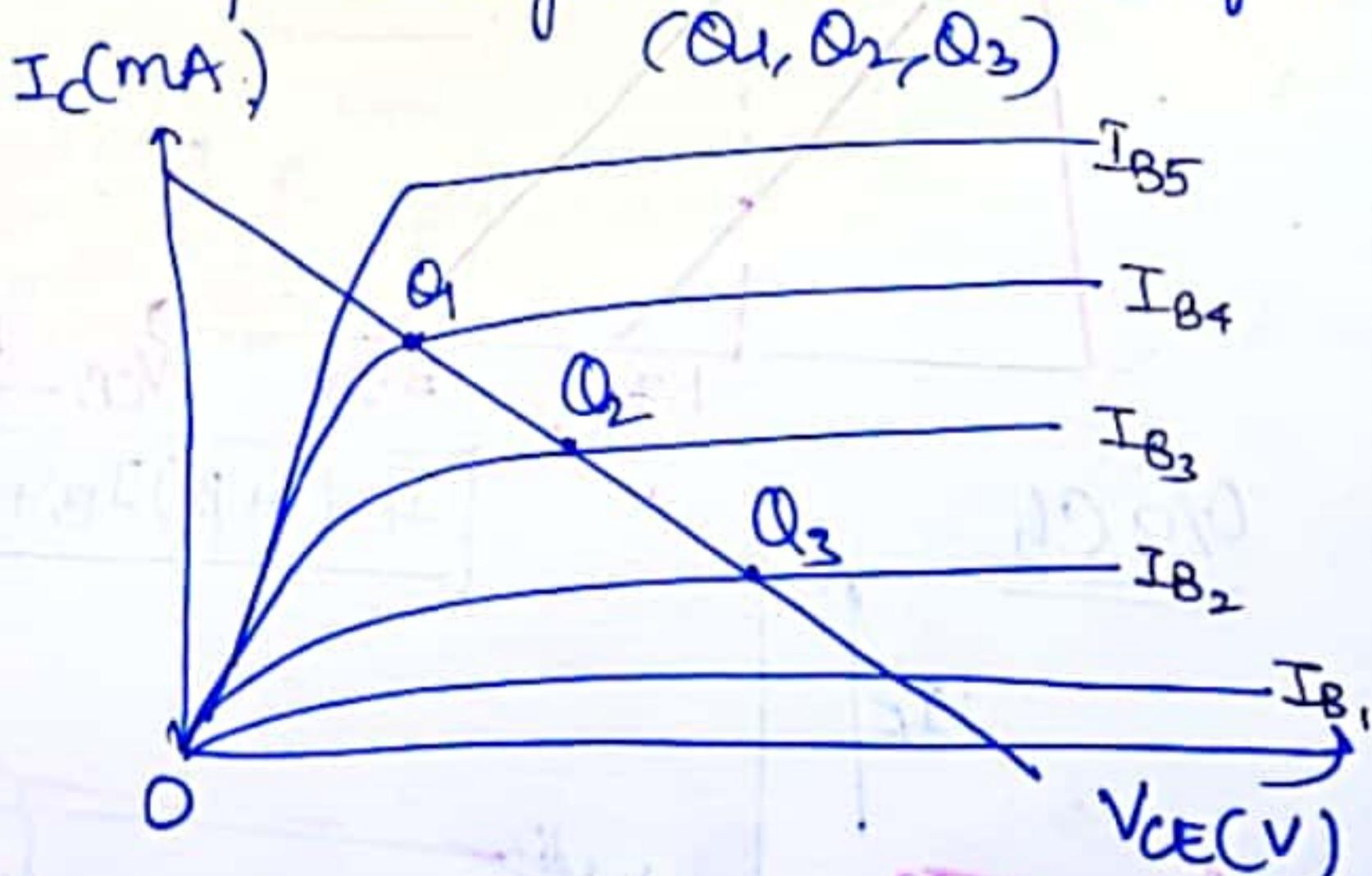
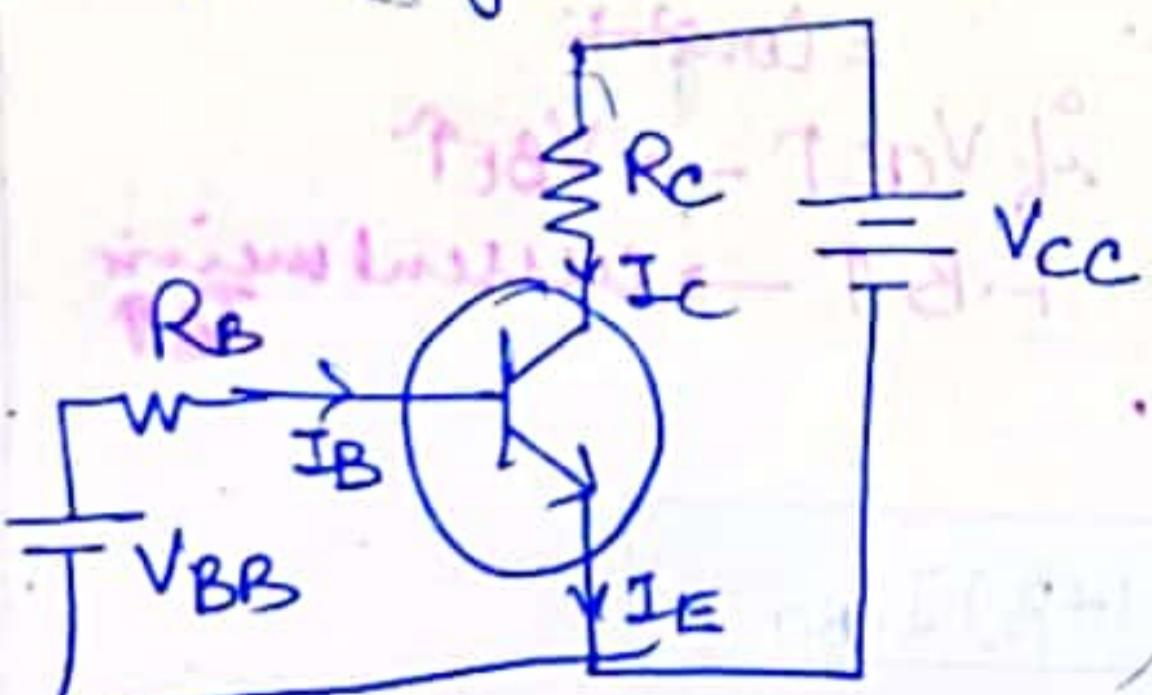
## Why we use CE Configuration :-

- ① due to high current gain
- ② high voltage & power gain
- ③ Moderate O/P to I/P impedance ratio

## Transistor Biasing =

- \* Transistor is used in wide no. of applications, the most basic one is amplification. Amplification means to raise the strength and amplitude of weak signal without any change in its original shape.
- \* Transistor must be in active region while amplification. Because it is linear process.
- \* During biasing, the fixed value of d.c collector current and d.c collector voltage are expressed by a term called operating point or quiescent point or Q-Point.
- \* For proper amplification proper selection of Q-point is very important.

Let us take an example of CE configuration, three operating points can be set depending on the value of  $I_B$ .



One of three operating point is suitable.

Output graph  
with diode  
in forward bias

- Q<sub>1</sub> lies near saturation region therefore for positive half cycle the signal will be clipped off.
- Q<sub>3</sub> lies near cut-off region, ∴ negative half cycle will be clipped off.
- If Q<sub>2</sub> is chosen then it will lie <sup>a middle of</sup> ~~in~~ <sup>in active</sup> region. Therefore signal will not be clipped off. Hence no distortion. ∴ Q-point is suitable operating point.

For faithful amplification, the operating point must lie in the middle of active region.

### Bias stabilization or Need of Stabilization

\* For proper transistor operation, only fixing of operating point is not sufficient. The operating point must remain stable throughout the operation where it is fixed originally.

Following factors are responsible for shift of operating point.

(i) Temperature dependence of transistor parameters  
 $I_C = \beta I_B + I_{CBO}(1+\beta)$

All three parameters  $\beta$ ,  $I_B$ ,  $I_{CBO}$  are temp dependent. hence with variation in temp it will vary.

(ii) Variation in parameters b/w transistor of same type  
 Even after advancement in SC technology, transistor parameters  $\beta$  vary widely with transistor of same type.

(iii) Thermal-runaway:-  
 $I_C = \beta I_B + (1+\beta) I_{CBO}$  (  $T \uparrow$ ,  $I_{CBO} \uparrow$ ,  $I_C \uparrow$ , operating point heat at junction  $\uparrow \rightarrow I_{CBO} \uparrow$ ,  $I_C \uparrow$  )

Temp change,  $I_{CBO}$  changes,  $I_C$  changes thus the operating point vary. flow of increased collector current produces heat at junction. which further raise the temperature. hence again  $I_{CBO} \uparrow$ ,  $I_C \uparrow$  and whole process repeat again. Successive increase in  $I_C$  will drive Q-point in saturation region. This is called thermal runaway.

due to this transistor may burn-out.

define of stabilization :-

The process of making operating point independent of temperature and changes or inherent variation in transistor is called as stabilization.

Stability factor

The stability factor is expressed as rate of change of  $I_c$  w.r.t the reverse saturation current while keeping CE current gain  $\beta$  and  $I_{B0}$  as constant.

$$S = \frac{dI_c}{dI_{CBO}}$$

We know that  $I_c = \beta I_B + (1+\beta) I_{CBO}$

differentiate above eqn w.r.t  $I_c$

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{dI_{CBO}}{dI_c}$$

$$1 - \beta \frac{dI_B}{dI_c} = (1+\beta) \frac{1}{S}$$

$$S = \frac{1+\beta}{1 - \beta \left( \frac{dI_B}{dI_c} \right)}$$

For common Base configuration,  $I_c = \alpha I_E + I_{CBO}$

$$\frac{dI_c}{dI_{CBO}} = 0 + 1$$

For CE Config:-  $I_c = \beta I_B + (1+\beta) I_{CBO}$

$$\frac{dI_c}{dI_{CBO}} = 1 + \beta$$

$$S = 1 + \beta$$

## Methods of Transistor Biasing

**Fixed Biased.**

**Self or Emitter Biased.**

**Voltage divider or Potential Divider**

BJT Biased in active region when,

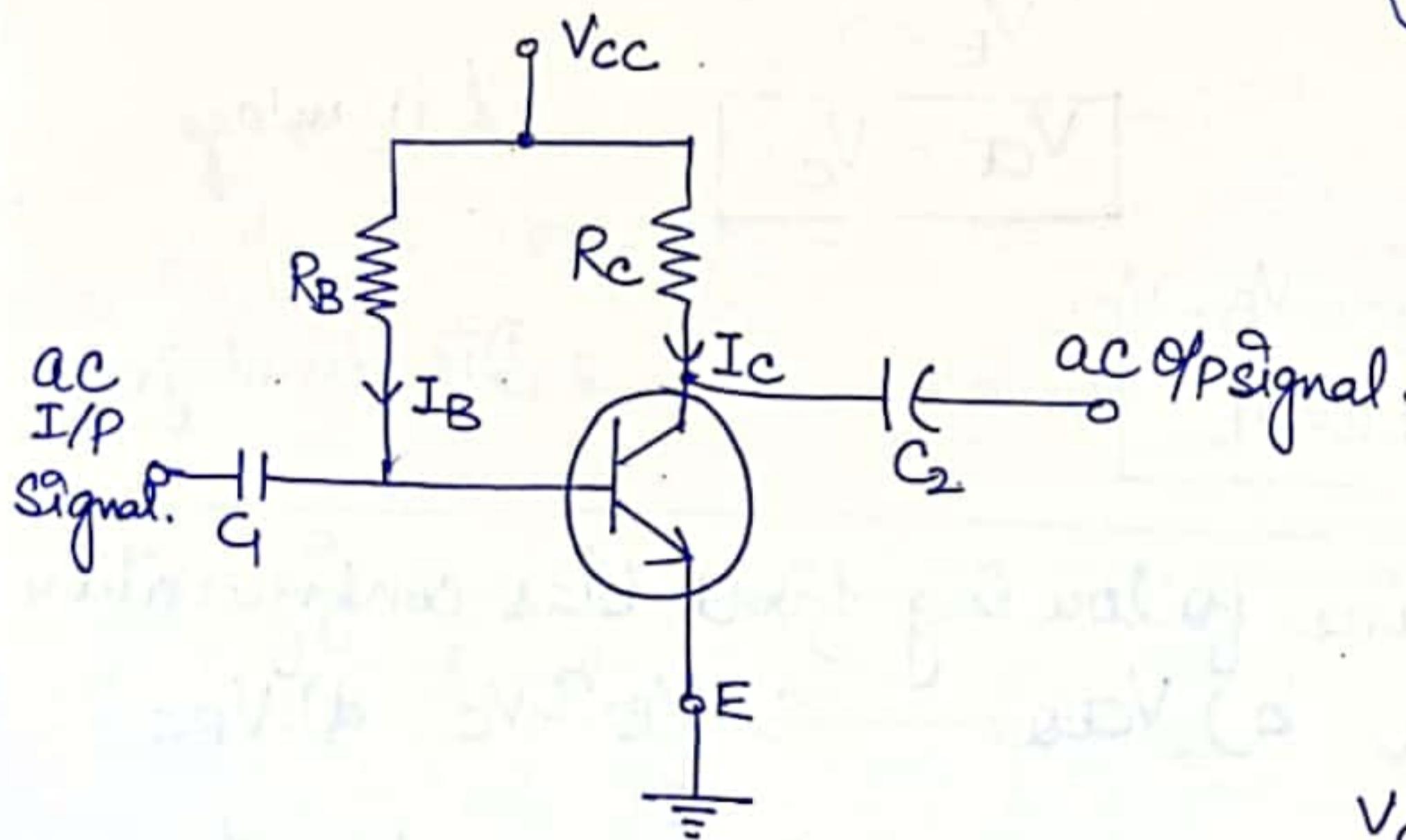
$$\textcircled{1} \quad V_{BE} = 0.6 \text{ or } 0.7 \text{ V (Junction EB \(\rightarrow\) F.B)}$$

$$\textcircled{2} \quad V_{CB} \text{ could have any reverse value within}$$

or limit  
maximum range of device

**① Fixed Biased**

It is simplest dc bias configuration.



**Collector to Base Biased or  
Collector Feedback Biased.**

**Emitter Follower (or)**

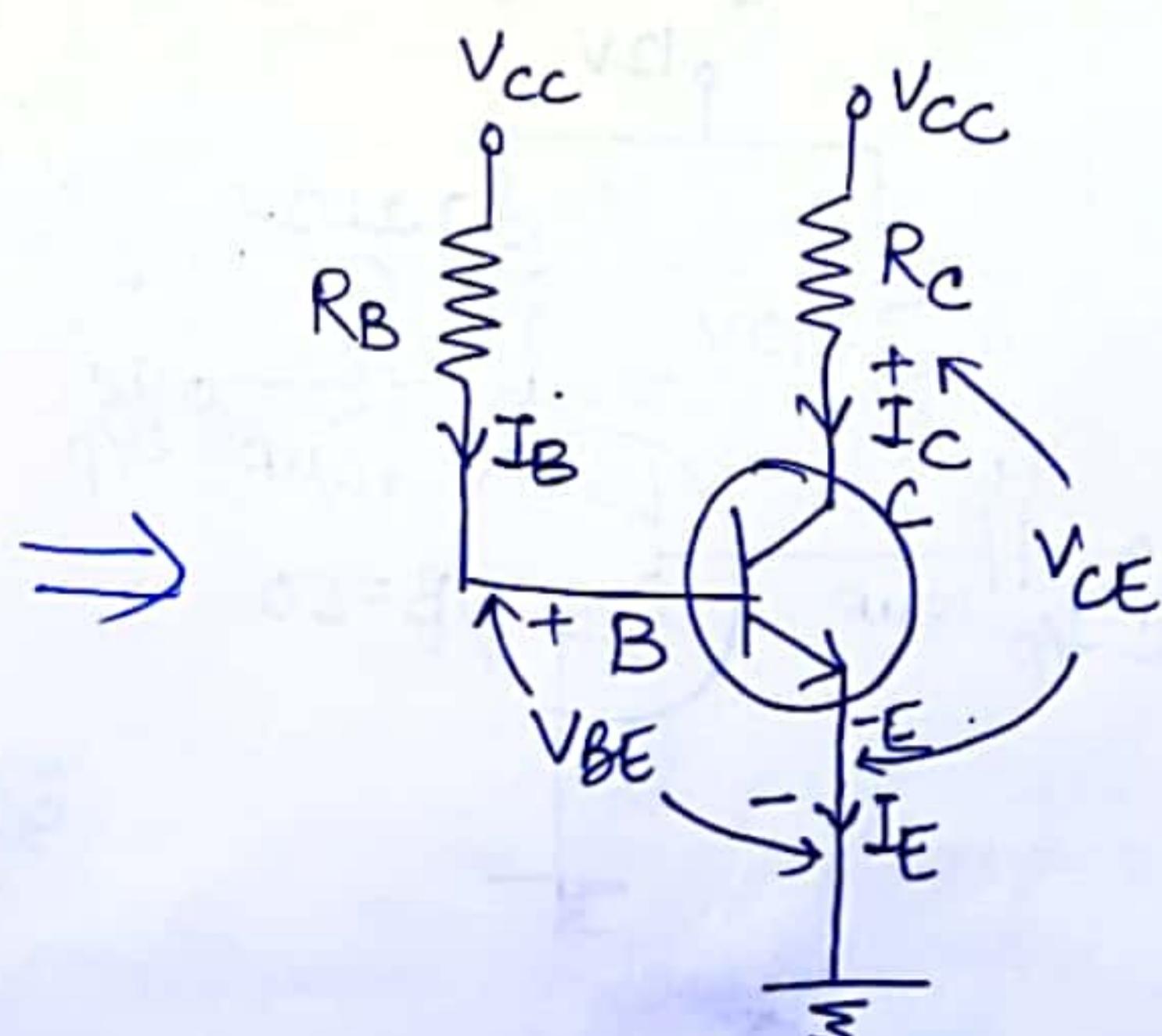
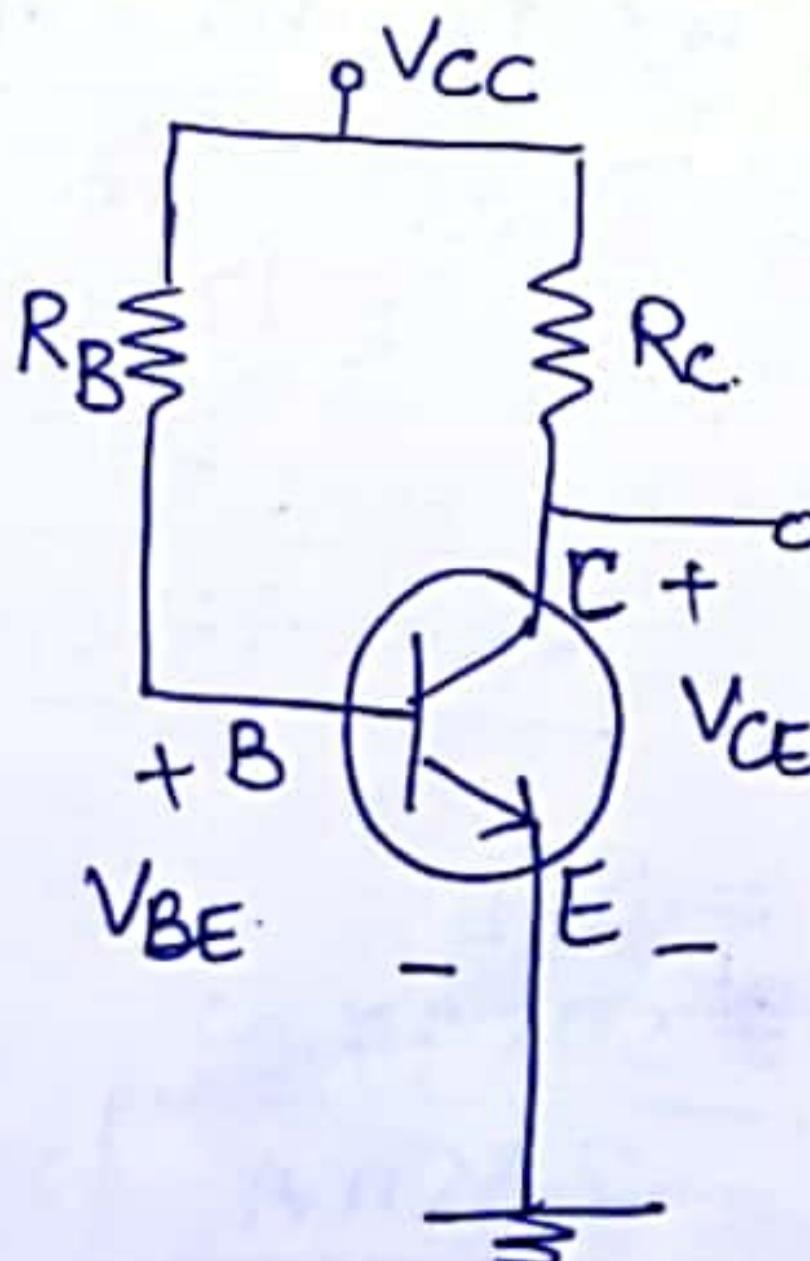
$$X_C = \frac{1}{2\pi f C}$$

for dc analysis

$$f = 0$$

$$X_C = \infty$$

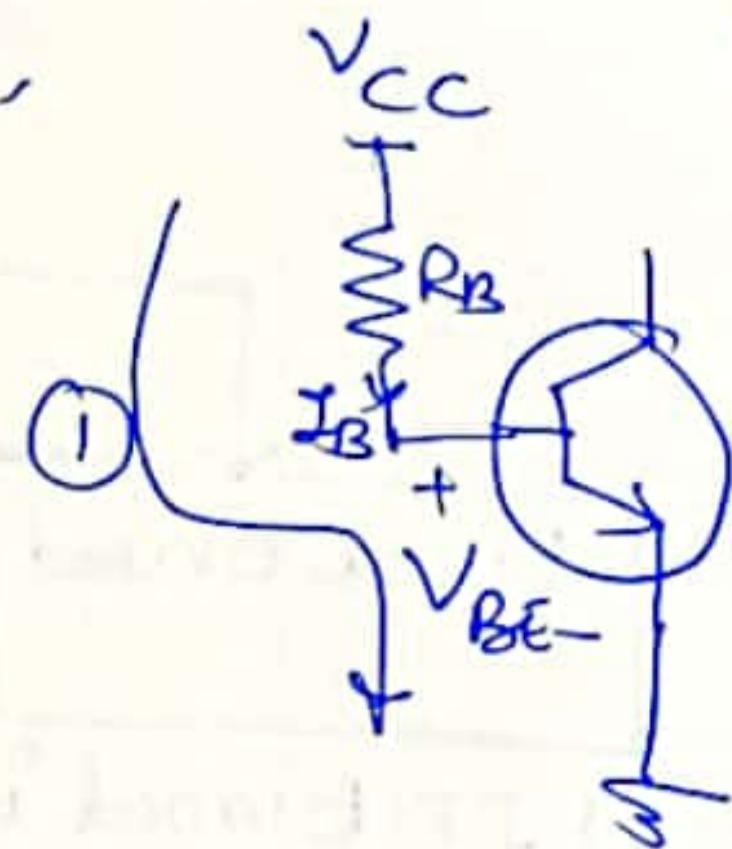
$\Rightarrow$  Open circuit equivalent



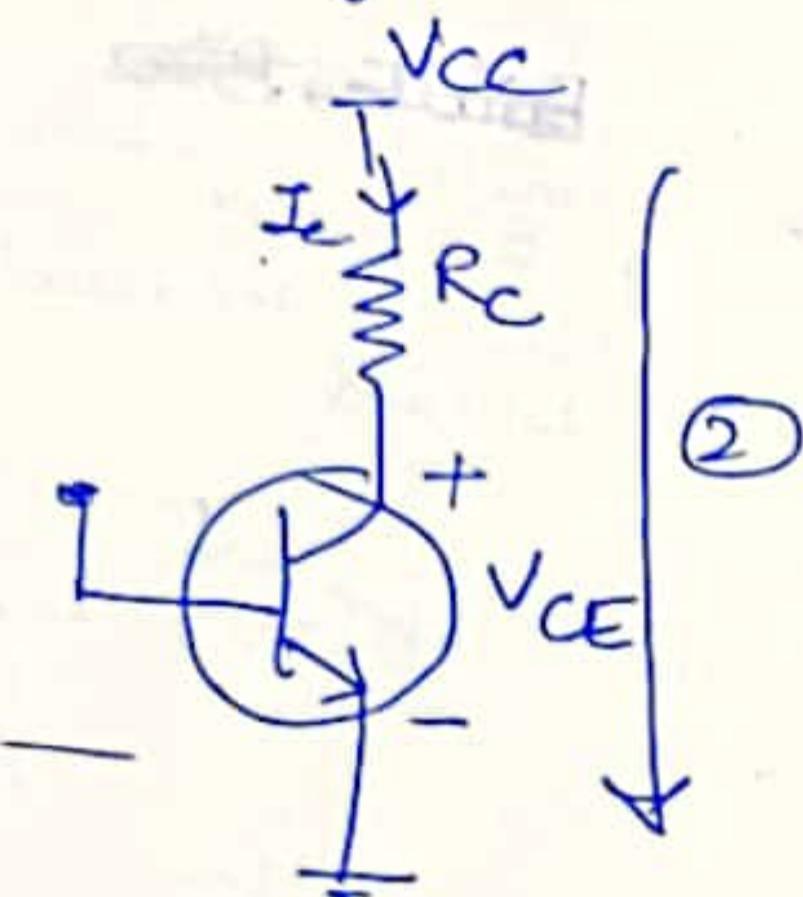
apply KVL for Fwd bias B-E junction,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



apply KVL to ... in loop ②



$$I_C = \beta I_B$$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_E = 0$$

$$V_{CE} = V_C$$

Advantage

Similarly

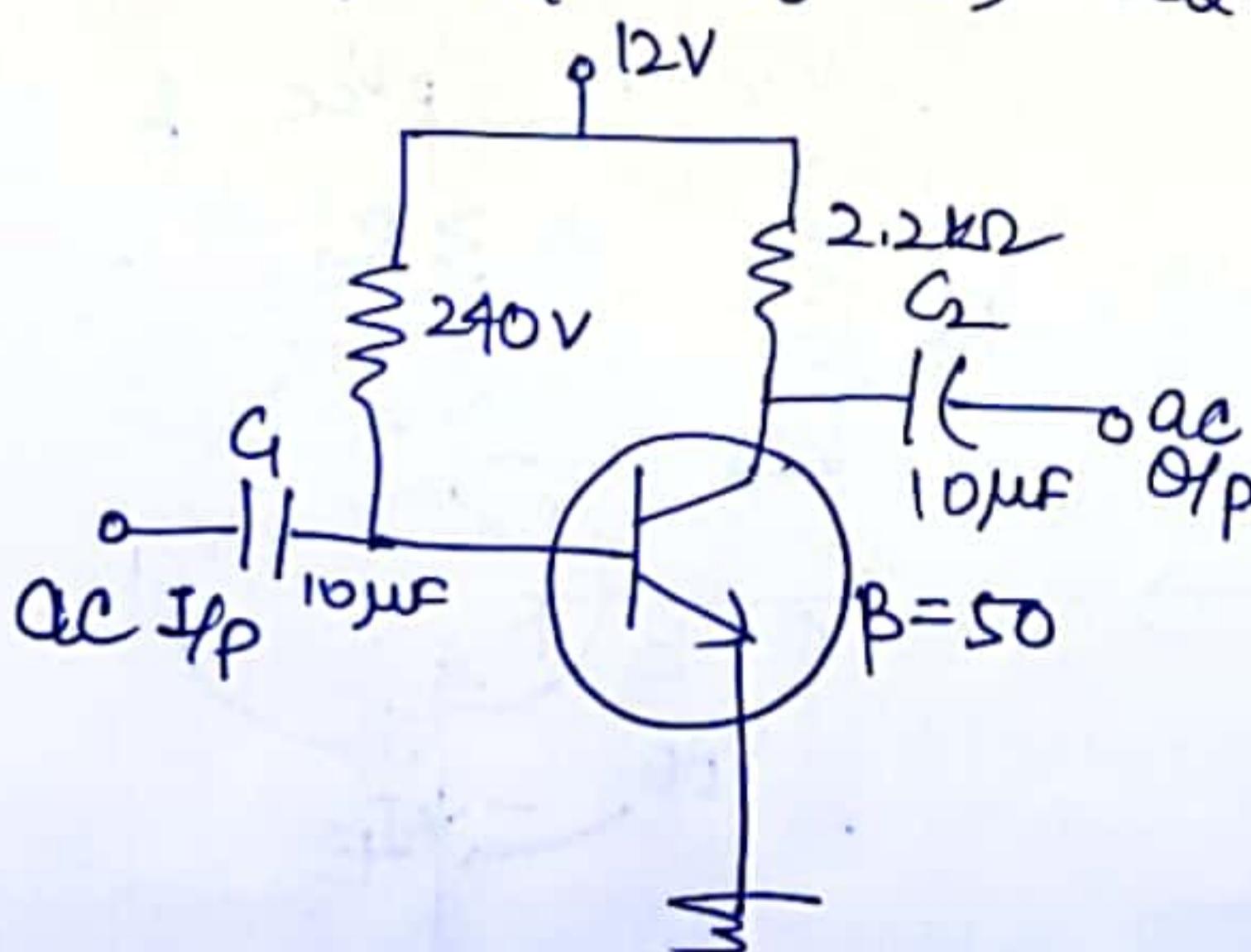
$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

Disadvantage

Question determine following fixed bias configuration

- a)  $I_{BQ}$  &  $I_{CQ}$
- b)  $V_{CEQ}$ .
- c)  $V_B$  &  $V_C$ .
- d)  $V_{BC}$



$$\text{Solt} a) I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12 - 0.7}{240}$$

$$I_B = 47.08 \mu A$$

$$\Rightarrow I_C = \beta I_B$$

$$= 50 \times 47.08$$

$$I_C = 2.35 \text{ mA}$$

$$b) V_{CEQ} = V_{CC} - I_C R_C \\ = 12 - 2.35 \times 2.2 = \underline{6.83V}$$

$$c) V_B = V_{BE} = 0.7V \\ V_C = V_{CE} = 6.83V$$

$$d) V_{BC} = V_B - V_C \\ = 0.7 - 6.83 \\ \boxed{V_{BC} = -6.13V}$$

Advantage

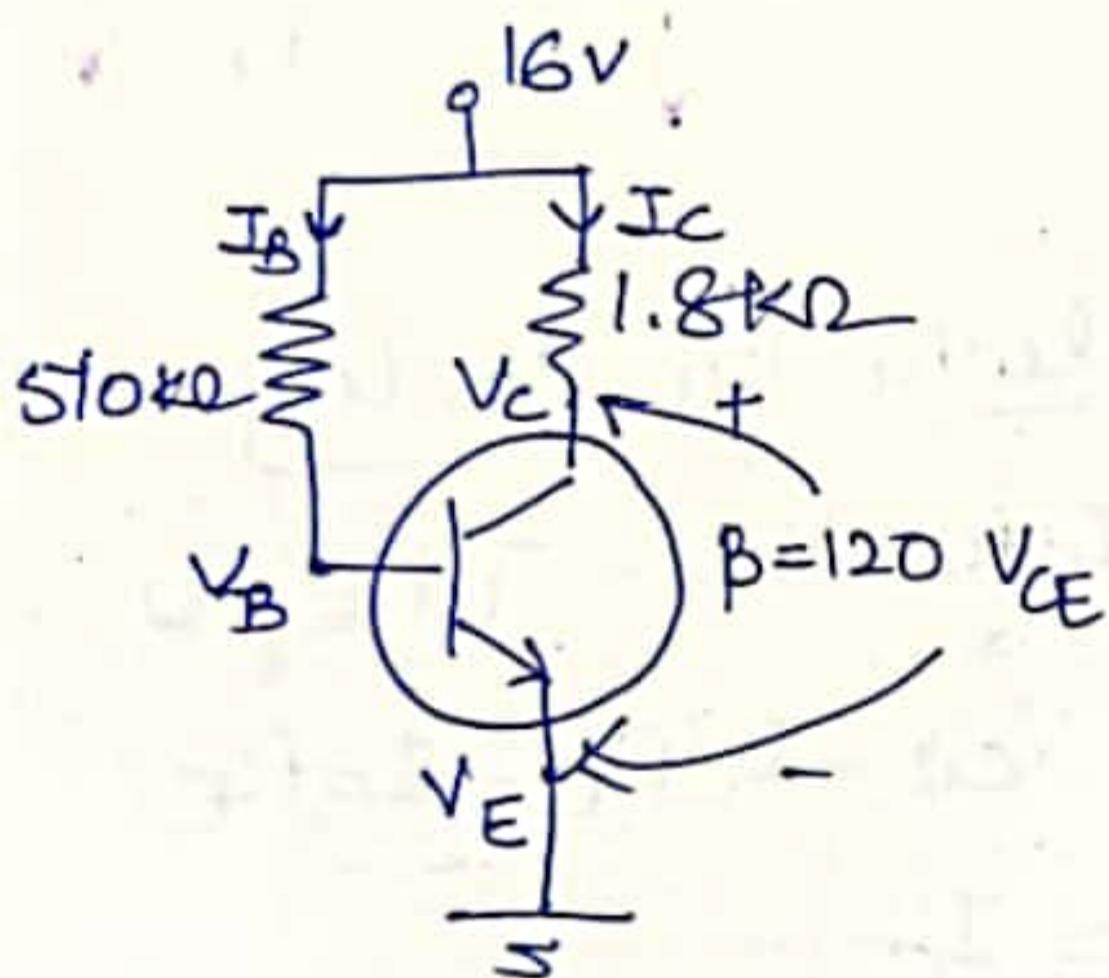
- ① Simplicity
- ② Small no. of components
- ③ If supply is very large then  $I_B$  will be independent of  $V_{BE}$

Disadvantage

- ① Poor Thermal stability

Q For given fixed bias configuration determine:

- a)  $I_{BQ}$
- b)  $I_{CQ}$
- c)  $V_{CEQ}$
- d)  $V_C$
- e)  $V_B$
- f)  $V_E$



Stability Factor of Fixed bias

$$V_{CC} - I_B R_B - V_{BE} = 0$$

diff w.r.t  $I_C$

$$0 - \frac{dI_B}{dI_C} R_B - 0 = 0$$

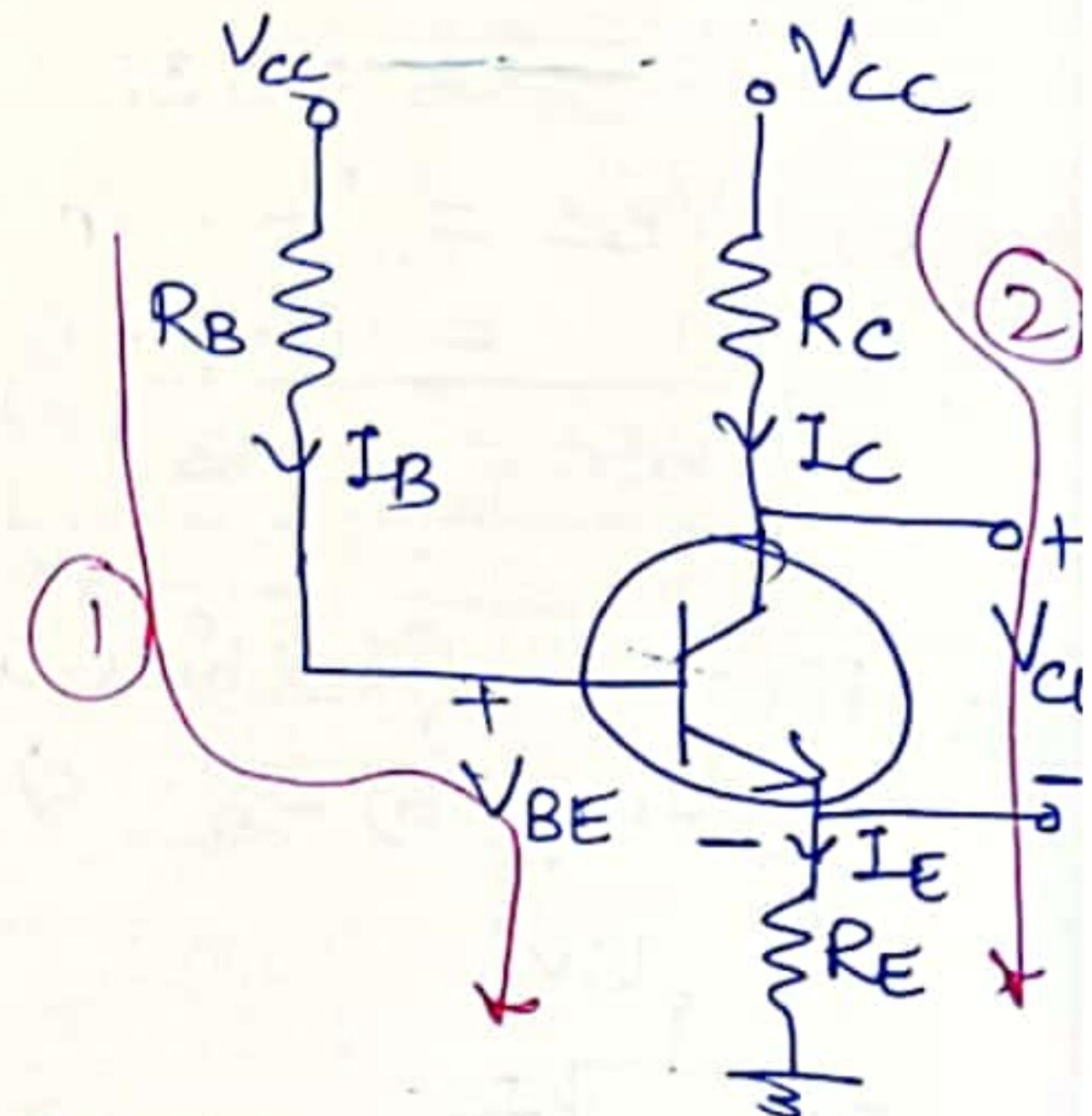
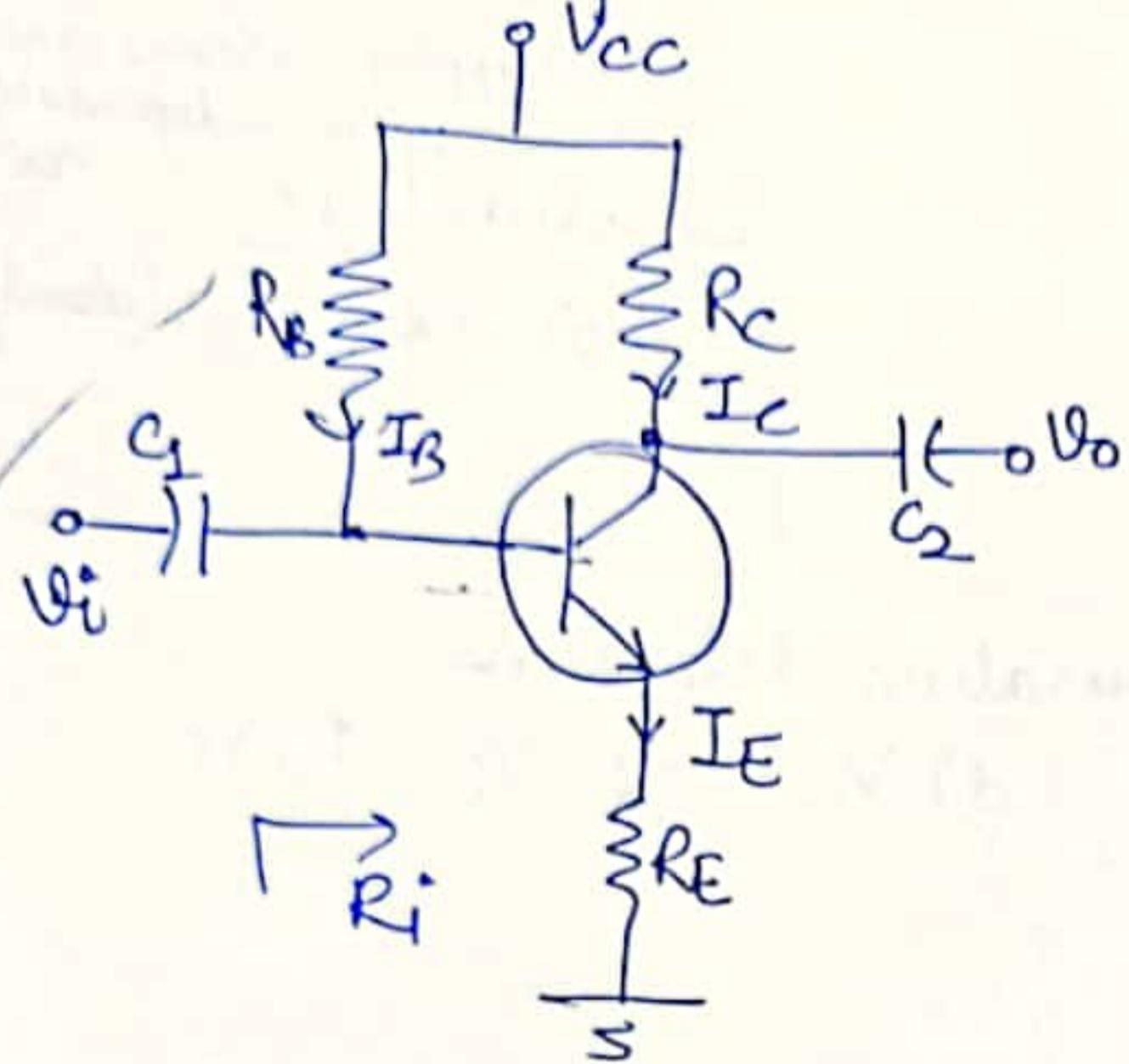
$$\frac{dI_B}{dI_C} = 0$$

$$S = \frac{(1 + \beta)}{1 - \beta \times 0}$$

$$\boxed{S = 1 + \beta}$$

## Emitter Bias Configuration

It is a more stable configuration; emitter resistor is used to improve the stability.



### Emitter Base Loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E}$$

$$R_i = (1 + \beta) R_E$$

$$V_{CE} = V_C - V_E$$

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

### Collector Emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\therefore I_E \approx I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

$$= V_{CC} - I_C R_C - I_C R_E - I_E R_E$$

$$\therefore R I_C \approx I_E$$

$$\therefore V_C = V_{CC} - I_C R_C$$

Advantage :-

① Provide better stabilization as compared to fixed bias.

Disadvantage :-

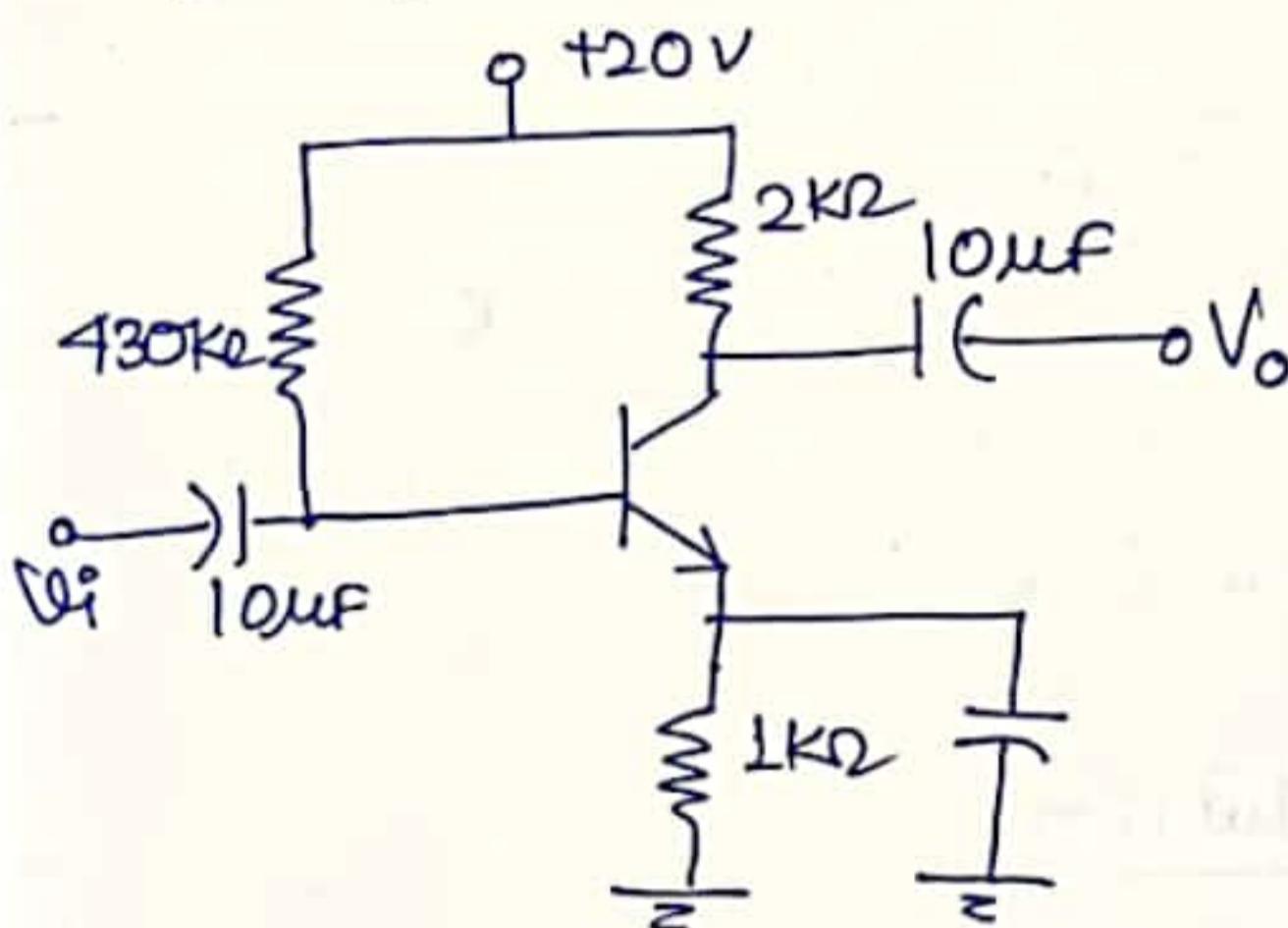
1) Circuit Complicated

2) lengthy calculations

3) Number of components are more than fixed bias circuit

2) Question. For emitter bias N/W. determine

$\Rightarrow I_B, I_C, V_{CE}, V_C, V_E, V_B, V_{BC}$ .



$$I_B = \frac{20 - 0.7}{430 + 50 \times 1} = \frac{19.3}{481} = 40.1 \text{ mA}$$

$$I_B = 40.1 \text{ mA}$$

$$I_C = \beta I_B = 50 \times 40.1 = 2.01 \text{ mA}$$

$$I_C = 2.01 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20 - (2.01)(2k + 1k) = 20 - 6.03 \text{ V}$$

$$V_{CE} = 13.97 \text{ V}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20 - 2.01 \times 2 = 15.98 \text{ V}$$

$$V_C = 15.98 \text{ V}$$

$$V_B = V_{BE} + V_E$$

$$= 0.7 + 2.01$$

$$V_B = 2.71$$

$$V_E = V_C - V_{CE}$$

$$V_E = 15.98 - 13.97 = 2.01 \text{ V}$$

$$V_E = 2.01 \text{ V}$$

$$V_{BC} = V_B - V_C$$

$$= 2.71 - 15.98 \text{ V}$$

$$V_{BC} = -13.27 \text{ V}$$

Stability factor :-  $V_{CC} - I_B R_B - V_{BE} - \frac{(I_C + I_B)}{I_C} R_E = 0$

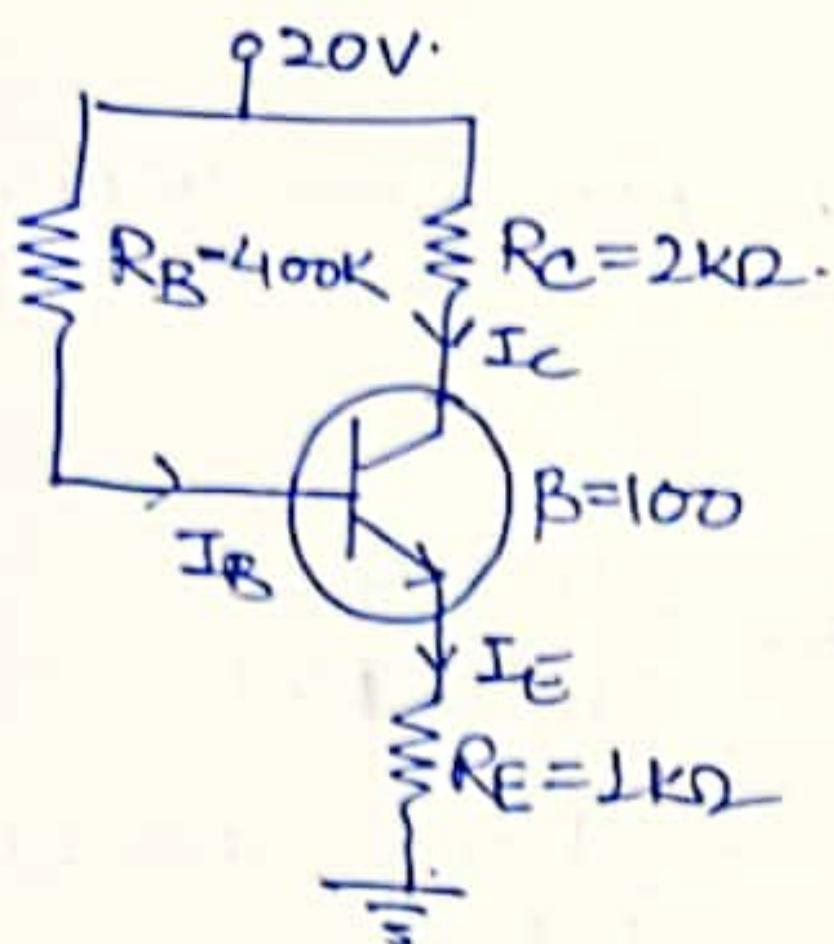
diff w.r.t  $I_C$

$$0 - \frac{dI_B}{dI_C} R_B - 0 = -R_E - \frac{dI_B}{dI_C} R_E$$

$$\frac{dI_B}{dI_C} (R_B + R_E) = -R_E$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

Q. Determine all DC bias voltage configuration and currents in the circuit. If  $R_B = 400\text{ k}\Omega$ ,  $R_C = 2\text{ k}\Omega$ ,  $R_E = 1\text{ k}\Omega$ ,  $V_{CC} = 20\text{ V}$  and  $\beta = 100$ .



$$S = \frac{(1+\beta)}{1 + \frac{\beta R_E}{R_B + R_E}}$$

DC Load Line

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

at Y axis  $V_{CE} = 0$      $I_C = \frac{V_{CC}}{R_C + R_E}$

at X axis  $I_C = 0$      $V_{CE} = V_{CC}$

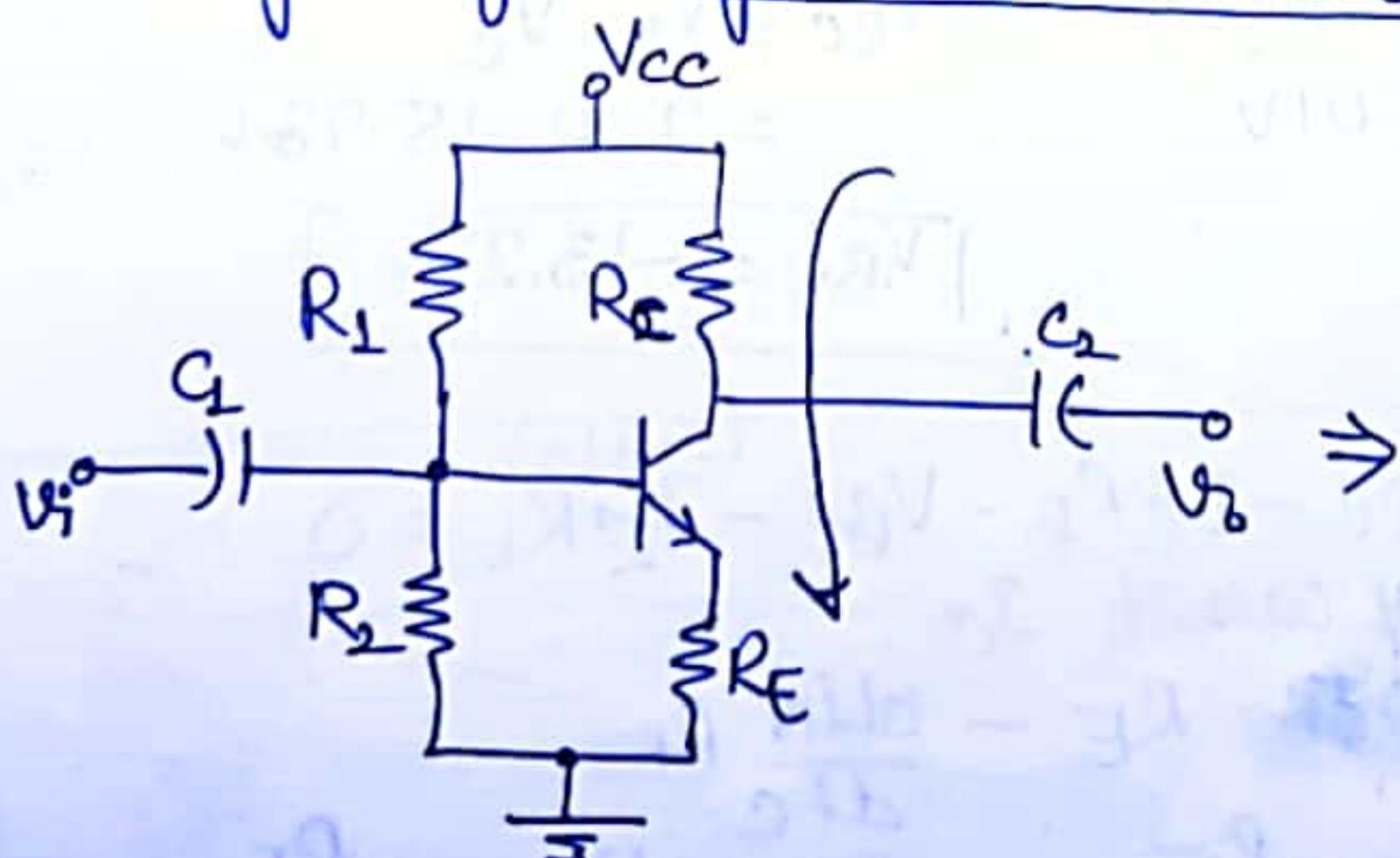
### Voltage divider Bias Configuration:-

In previous configurations  $I_{CQ}$  &  $V_{CEQ}$  were functions of current gain  $\beta$ . However  $\beta$  is temp sensitive & its value is not well defined.

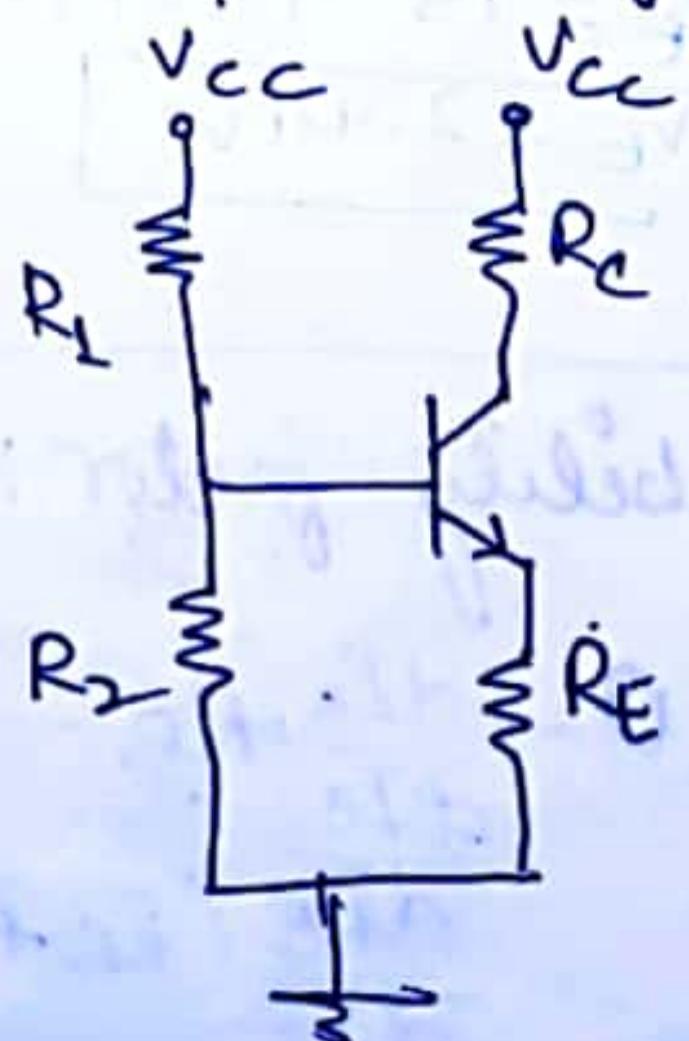
Hence it would be desirable to develop a bias circuit that is less dependent on  $\beta$ . Voltage divider configuration follows is such network. In this  $I_{CQ}$  &  $V_{CEQ}$  can be almost totally independent of  $\beta$ .

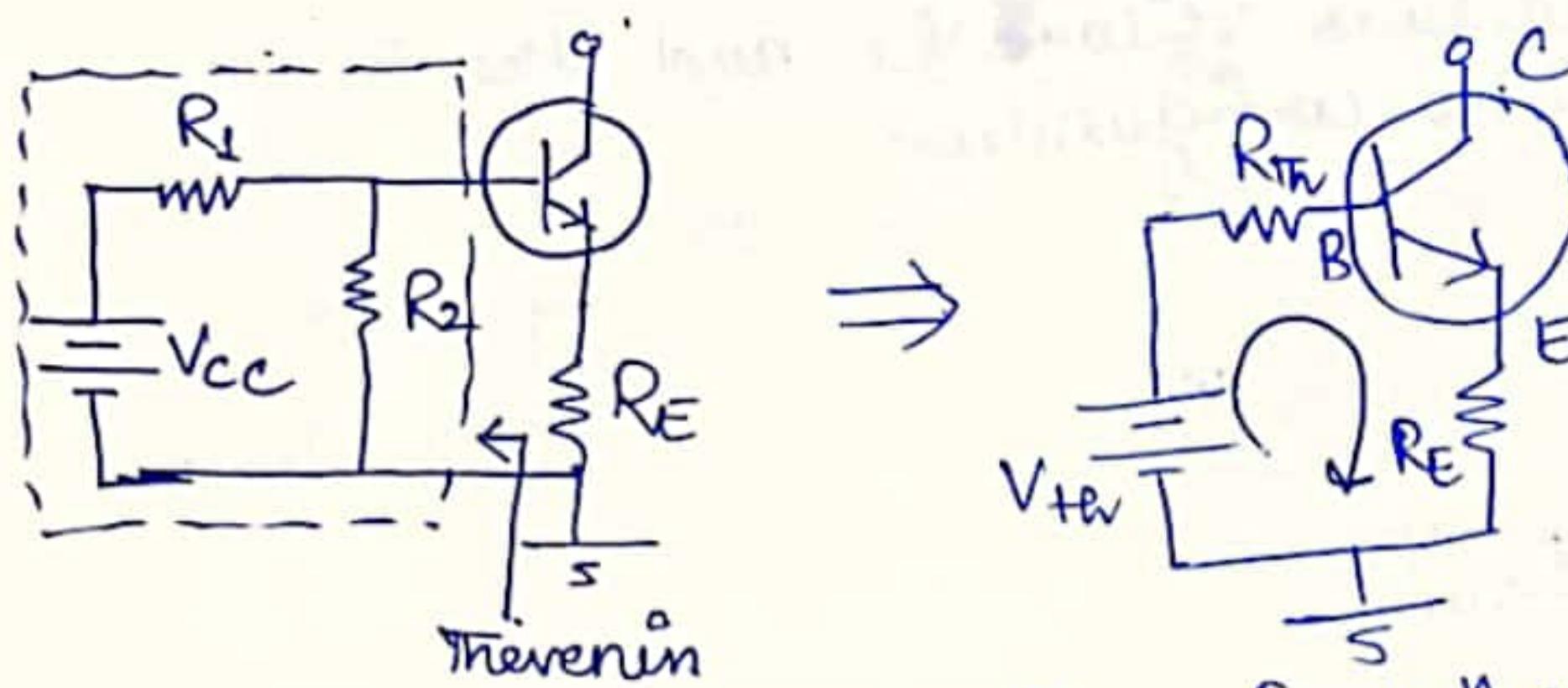
Stability factor of this circuit is lowest.

### Analysis of voltage divider bias circuit.

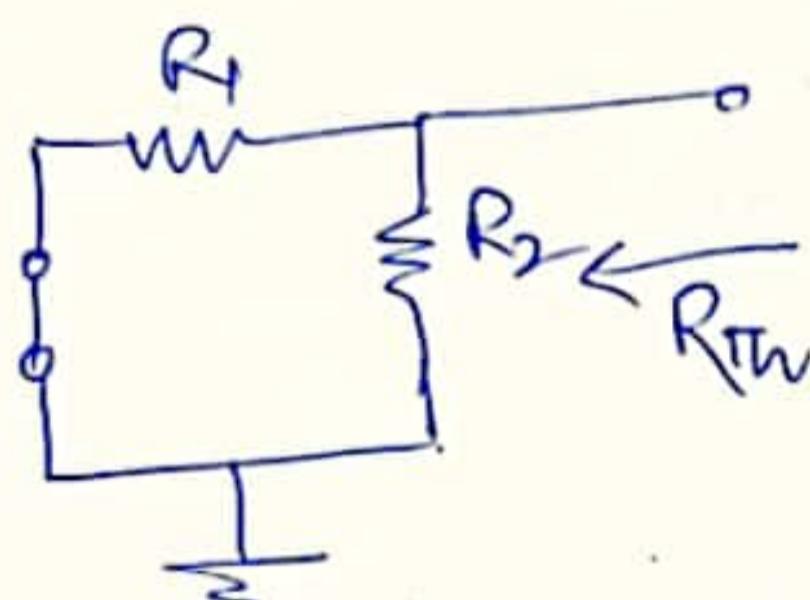


DC components of this config:





Thevenin eq<sup>n</sup> circuit



$$R_{TH} = R_1 \parallel R_2$$

$V_{TH}$  is voltage across  $R_2$ .  $R_2 = \frac{R_2 \times V_{CC}}{R_1 + R_2}$

$$V_{TH} = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

### Emitter Base loop

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$I_E = (1+\beta) I_B$$

$$V_{TH} - I_B R_{TH} - V_{BE} - (1+\beta) I_B R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta) R_E}$$

### Collector Emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\& I_C \approx I_E$$

$$\therefore V_{CC} - V_{CE} - I_C (R_E + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C (R_E + R_E)$$

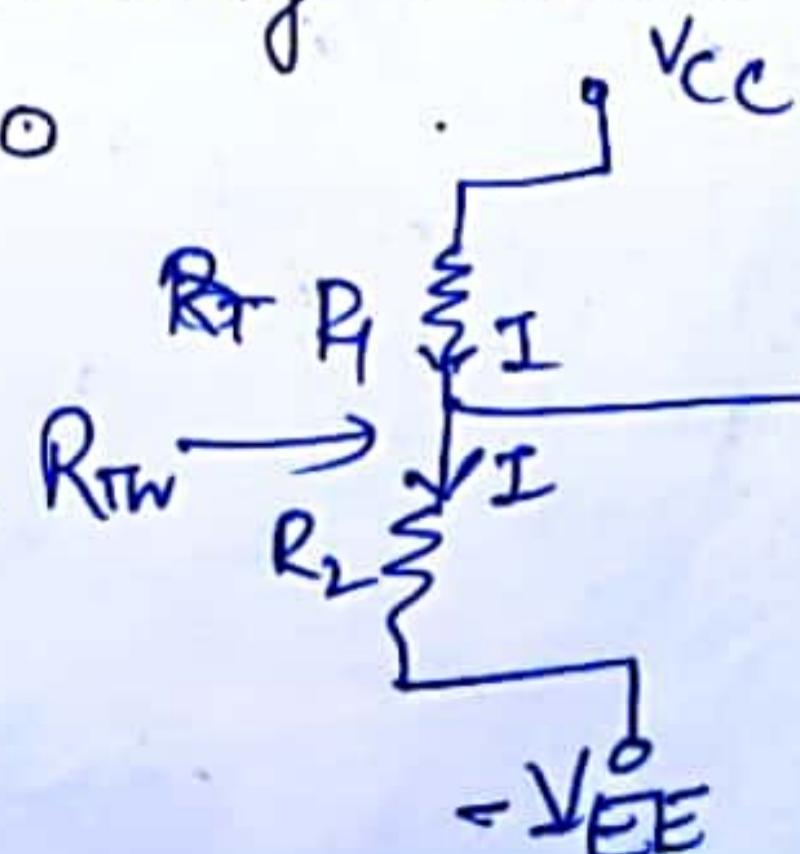
Case: When an additive battery is attached

$$V_{CC} - I_R_1 - I_R_2 + V_{EE} = 0$$

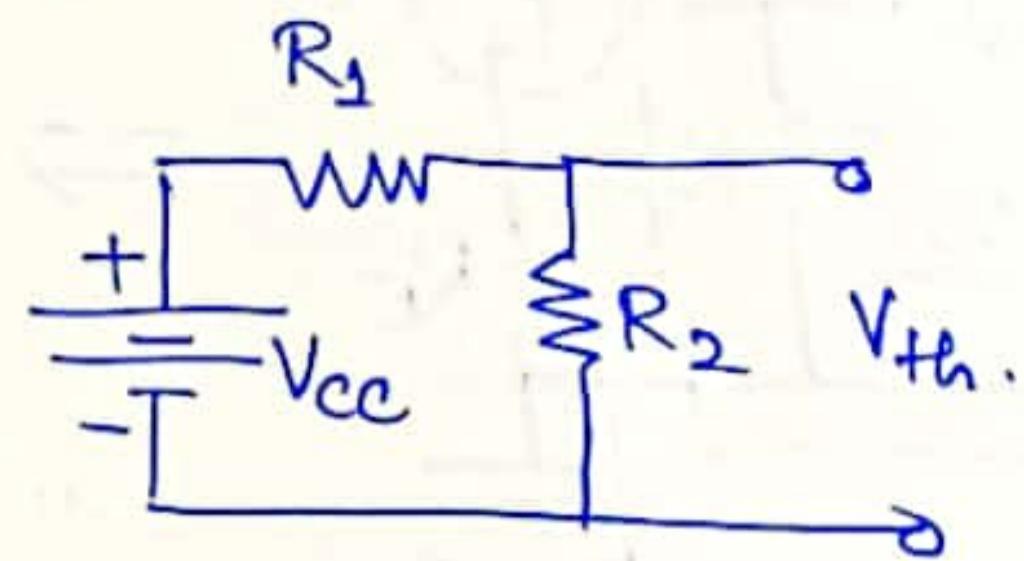
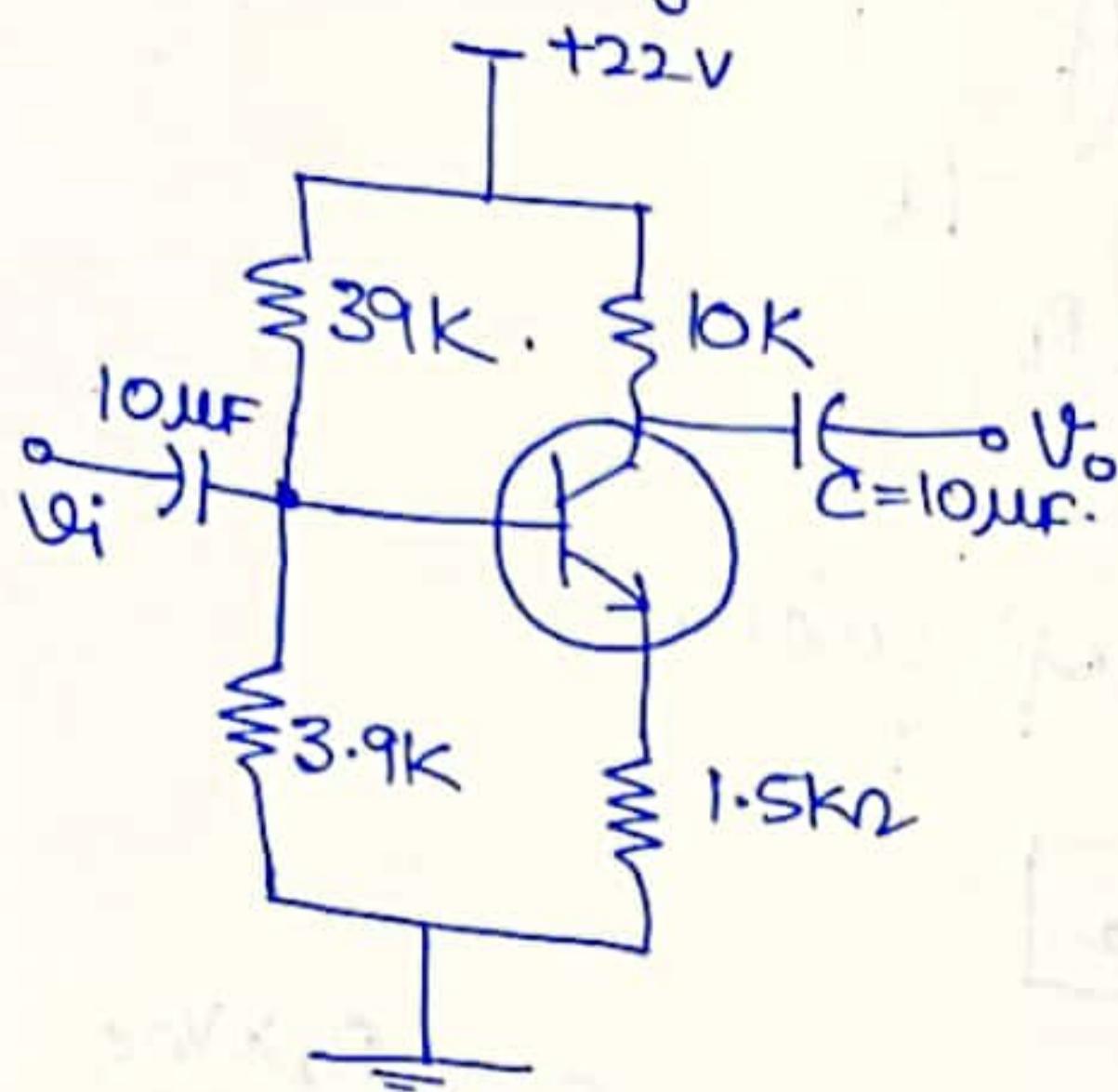
$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2}$$

$$V_{TH} = I R_2 - V_{EE}$$

$$R_{TH} = R_1 \parallel R_2$$



Determine the dc bias voltage  $V_{CE}$  and the  $I_C$  for given voltage divider configuration.



$$V_{th} = \frac{R_2}{R_1 + R_2} V_{cc}$$

$$= \frac{3.9}{39+3.9} \times 22 = 2V$$

$$\boxed{V_{th} = 2V}$$

$$R_{th} = R_L \parallel R_2$$

$$= \frac{39k \times 3.9}{39k + 3.9} = 3.55k\Omega$$

$$\boxed{R_{th} = 3.55k\Omega}$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta)R_E}$$

$$\boxed{I_B = 8.38\mu A}$$

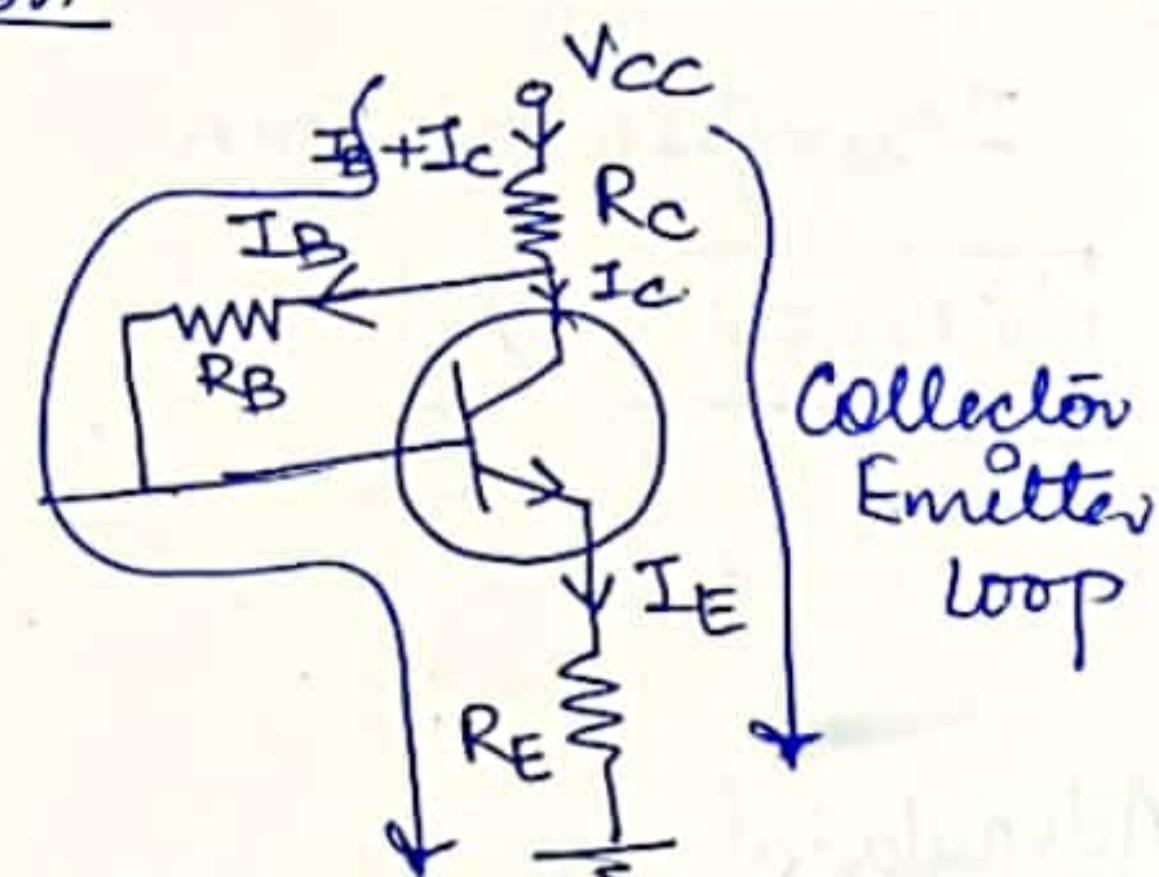
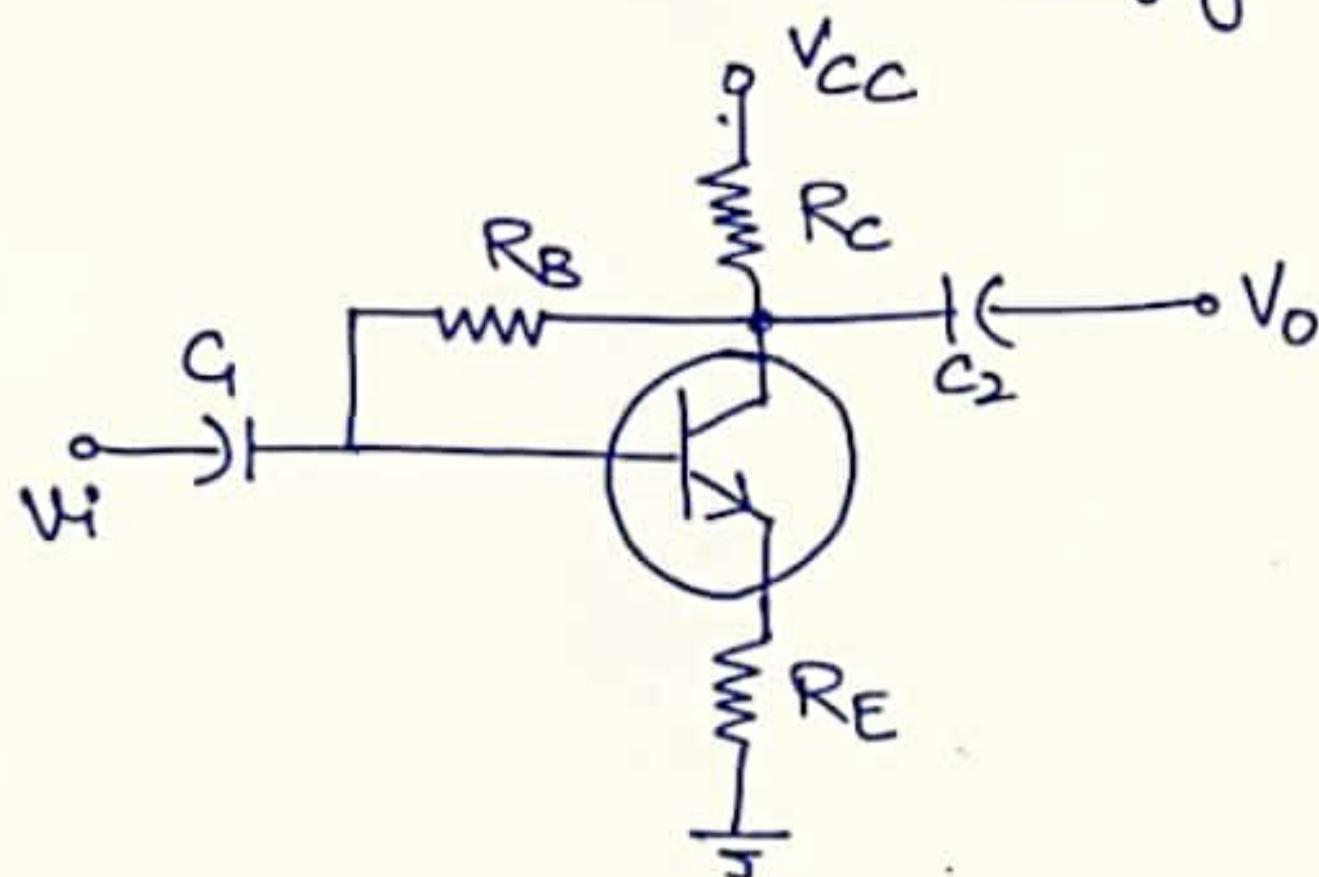
$$I_C = \beta I_B$$

$$\boxed{I_C = 0.84mA}$$

$$\boxed{V_{CE} = 12.34V}$$

181

Collector to Base configuration or  
Collector Feedback configuration



Base-Emitter Loop

$$V_{CC} - (I_c + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B [(1+\beta)R_C + R_B + (1+\beta)R_E] - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B + (1+\beta)R_E}$$

If  $R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B}$$

$$I_{CQ} = \beta I_B$$

Collector Emitter Loop

$$(I_c + I_B) \approx I_c$$

$$V_{CC} - I_c R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow I_c \approx \frac{V_{CC} - I_c(R_C + R_E)}{R_C + R_E} - I_B R_C$$

Ques Determine  $I_{CQ}$  &  $V_{CEQ}$ .

Ans

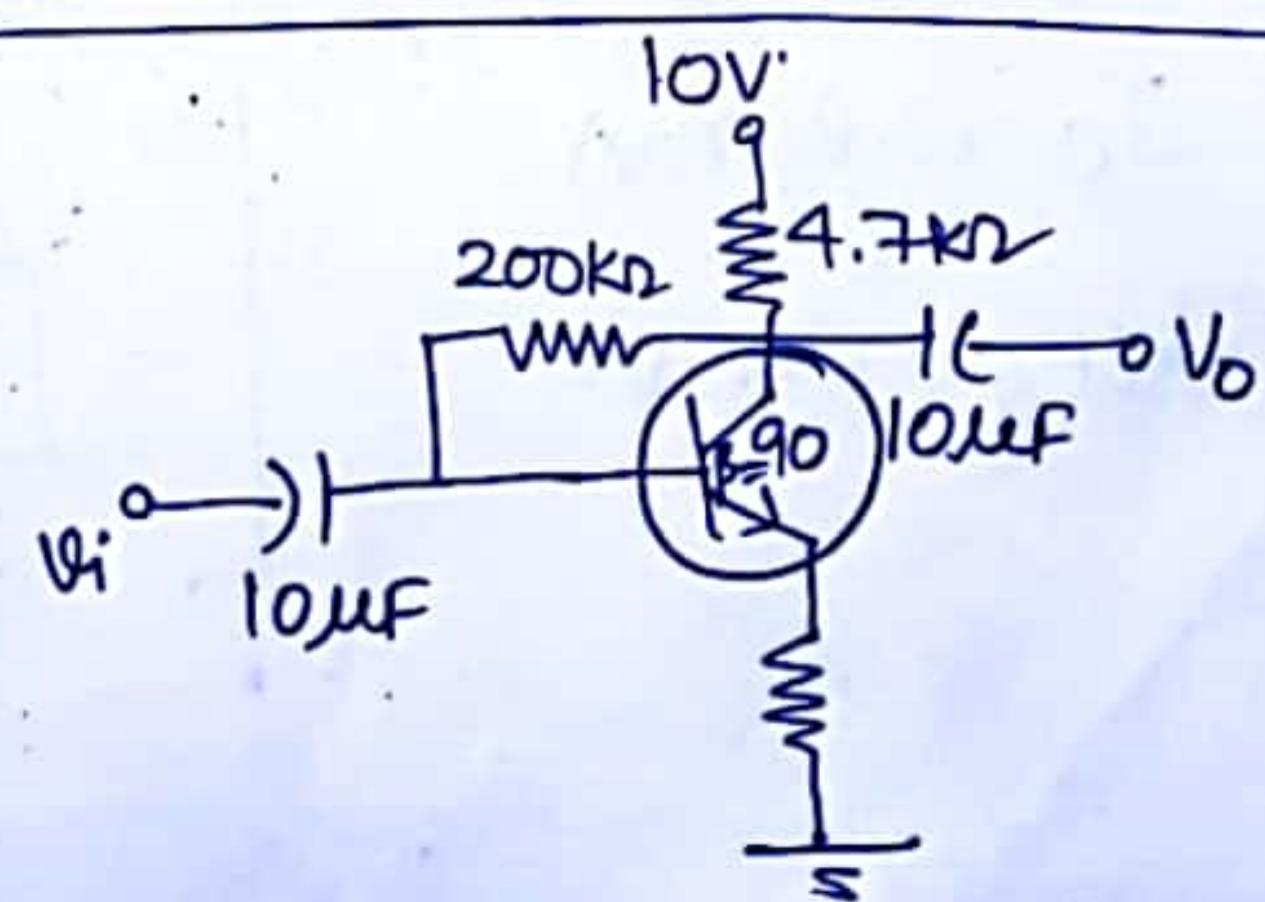
$$I_B = 11.91 \mu A$$

$$I_{CQ} = \beta I_B$$

$$I_{CQ} = 1.07 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_c(R_C + R_E)$$

$$V_{CEQ} = 3.09 \text{ V}$$



! Determine  $V_{CEQ}$  &  $I_{CEQ}$  for same circuit with  $\beta = 135$ .

Sol<sup>n</sup>

$$I_B = 8.69 \mu A$$

$$I_{CQ} = \beta I_B = 1.2 \text{ mA}$$

$$V_{CEQ} = 2.92 \text{ V}$$

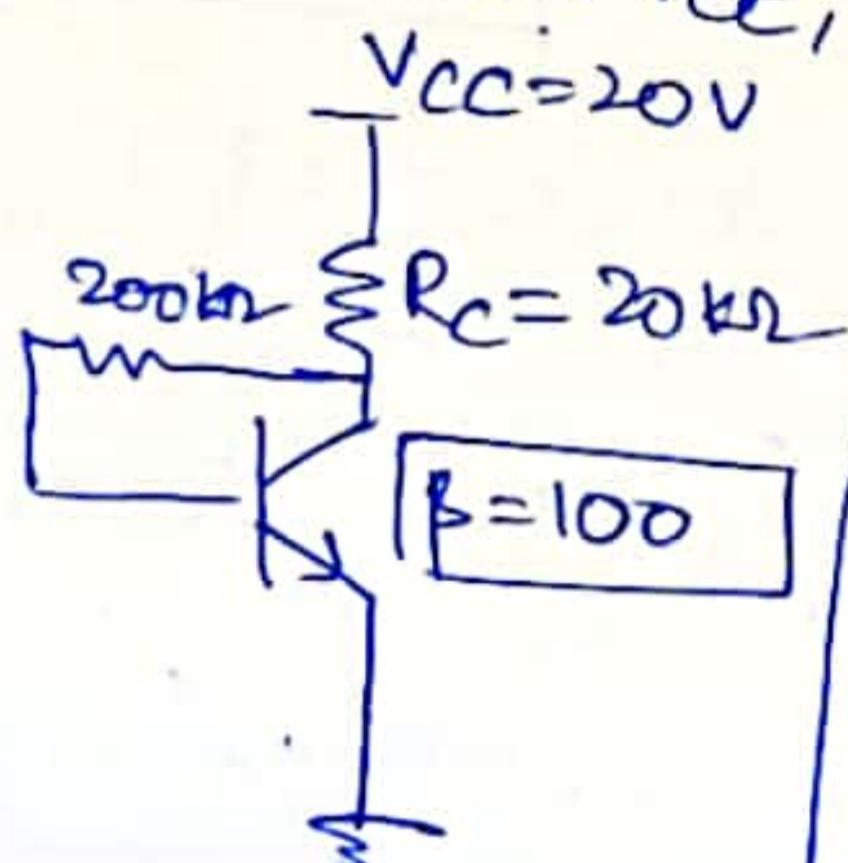
Advantage:-

- 1) Simple biasing arrangement.
- 2) Circuit has stabilized operating pt.
- 3) Disadvantage:-

→  $R_B$  cause ac feedback which reduces voltage gain of amplifier.

Ques

③ Determine  $V_{CE}$ ,  $I_C$ .

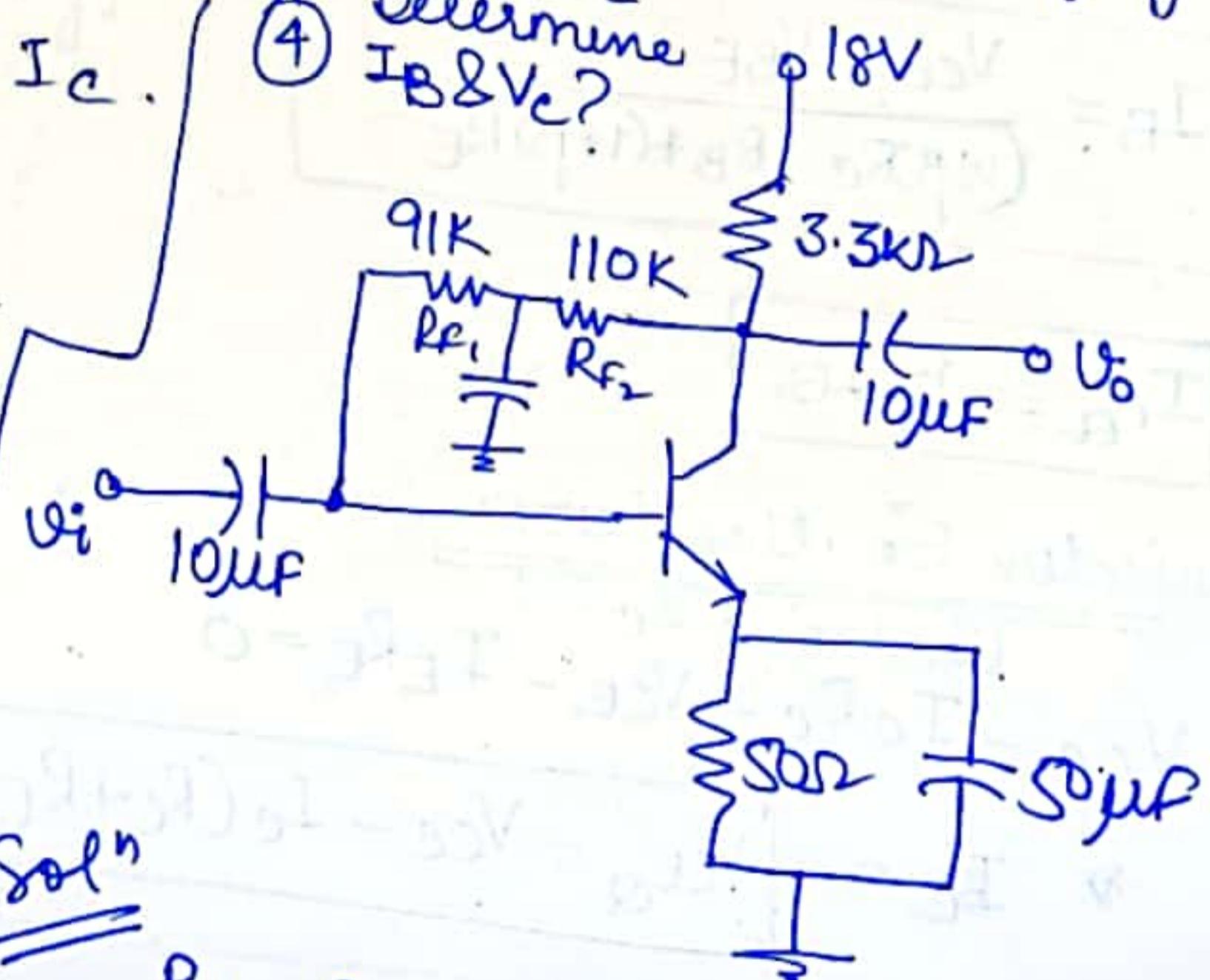


$$I_B = 8.6 \mu A$$

$$I_C = 0.86 \text{ mA}$$

$$V_{CEQ} = 2.6 \text{ V}$$

④ Determine  $I_B$  &  $V_C$ ?



Sol<sup>n</sup>

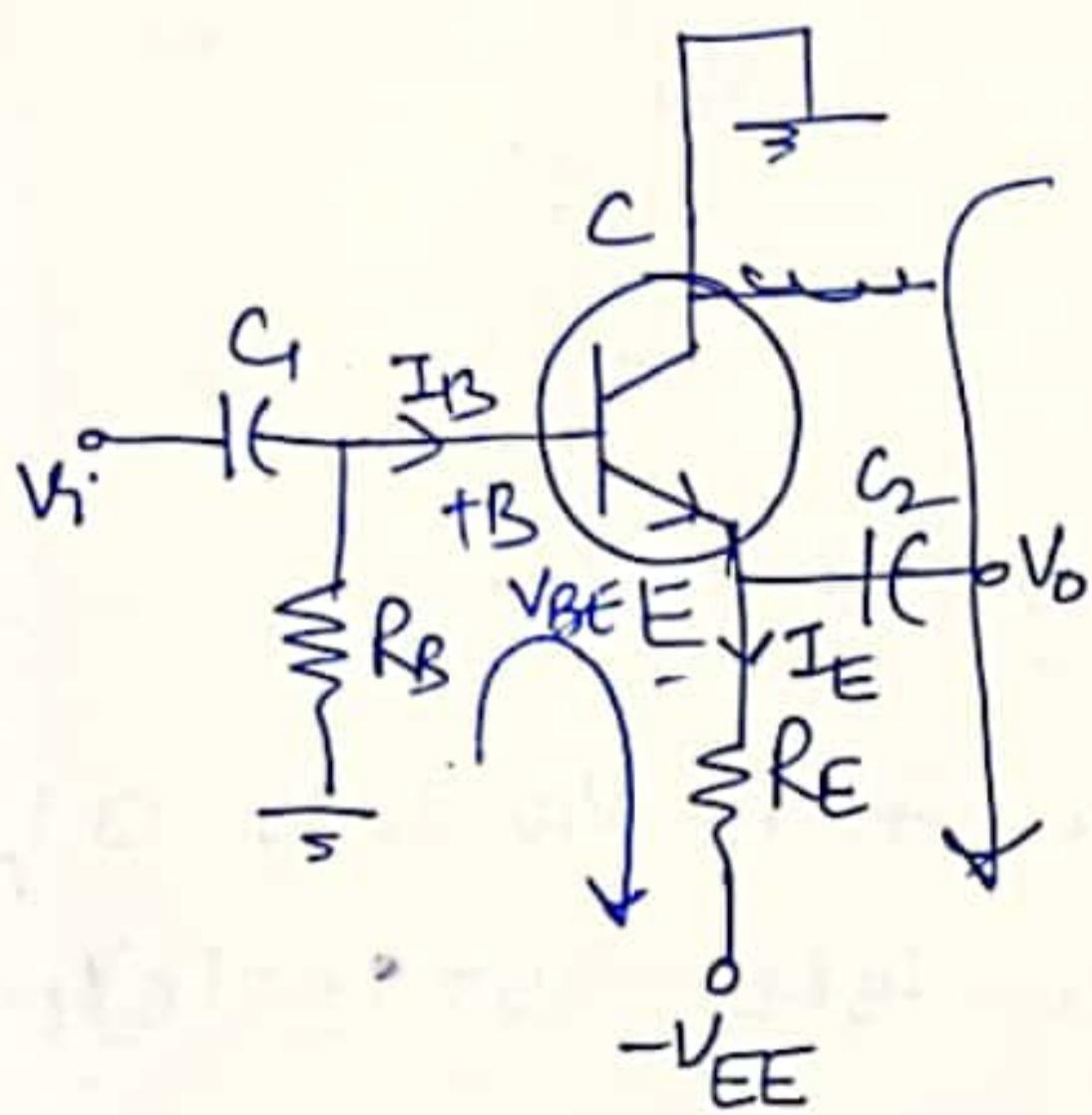
$$R_B = R_{F_1} + R_{F_2}$$

$$I_B = 35.5 \mu A$$

$$I_C = 2.66 \text{ mA}$$

### Emitter follower configuration:-

This is the only configuration where  $\text{Q}_P$  is applied at emitter terminal.



KVL at I/P loop -

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

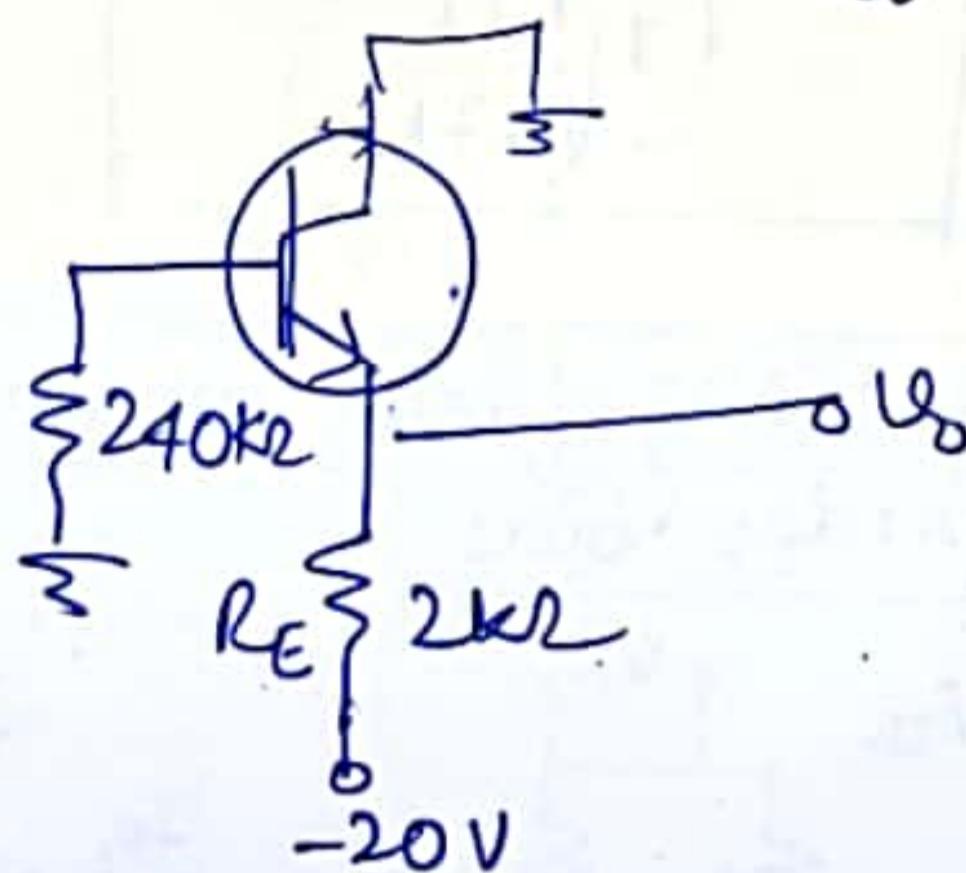
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

KCL at O/P loop,

$$0 - V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

Ques Determine  $V_{CEQ}$  &  $I_{EQ}$ . for given N/w.



$$I_B = 45.73 \mu\text{A}$$

$$I_{EQ} = (1 + \beta) I_B$$

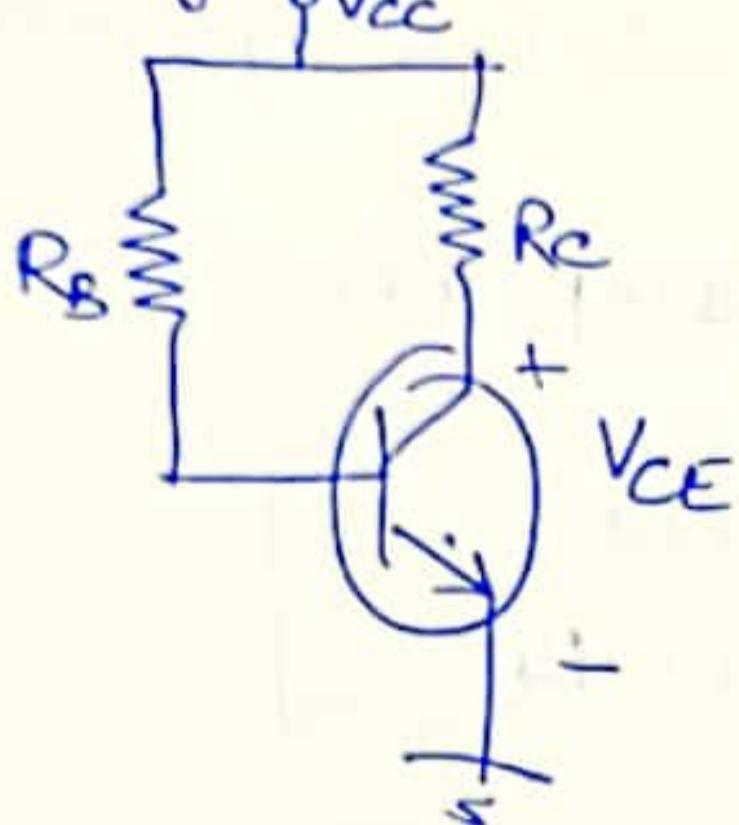
$$I_{EQ} = 4.16 \text{ mA}$$

$$V_{CE} = 11.68 \text{ V}$$

## Stability factor

$$S = \frac{1+\beta}{1-\beta \left( \frac{\Delta I_B}{\Delta I_C} \right)}$$

## Stability factor for fixed bias Configuration:-



$$V_{CC} - I_B R_B - V_{BE} = 0$$

differentiate  $I_B$  w.r.t  $I_C$ .

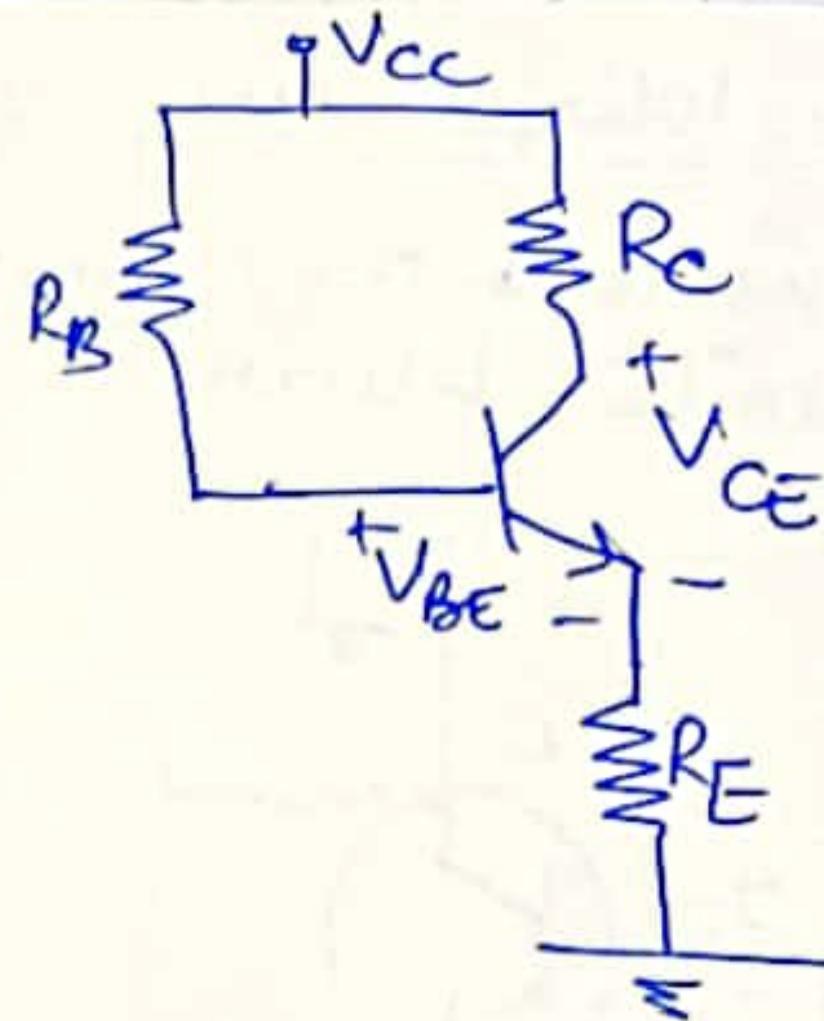
$$0 - R_B \frac{dI_B}{dI_C} - 0 = 0$$

$$\frac{dI_B}{dI_C} = 0$$

$$S = \frac{1+\beta}{1-\beta \times 0}$$

$$\therefore S = 1+\beta$$

## Stability factor of self bias or emitter bias circuit



## KVL at B-E Loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$$

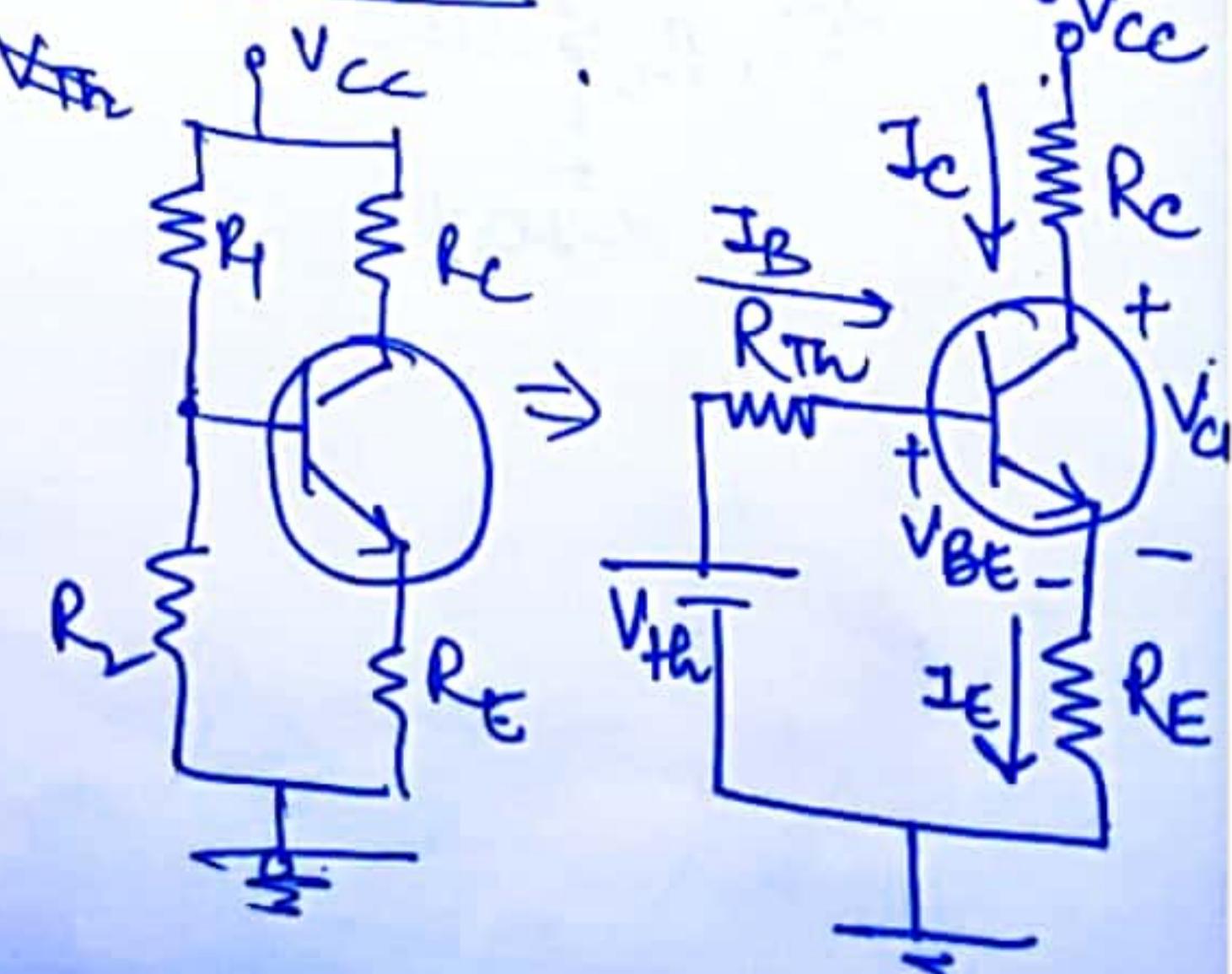
$$0 - \Delta I_B R_B - 0 - (\Delta I_C + \Delta I_B) R_E = 0$$

$$- \Delta I_B (R_B + R_E) = + \Delta I_C R_E$$

$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_E}{(R_B + R_E)}$$

$$S = \frac{1+\beta}{1 + \left( \frac{R_E}{R_B + R_E} \right)}$$

## Stability factor for voltage divider bias



$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_C + I_B) R_E = 0$$

$$0 - \frac{\Delta I_B}{\Delta I_C} R_{Th} - \left(1 + \frac{\Delta I_B}{\Delta I_C}\right) R_E = 0$$

$$\frac{\Delta I_B}{\Delta I_C} (R_{Th} + R_E) = - R_E$$

$$\boxed{\frac{\Delta I_B}{\Delta I_C} = \frac{-R_E}{R_{Th} + R_E}}$$

$$\boxed{S = \frac{1 + \beta}{1 + \left(\frac{\beta R_E}{R_{Th} + R_E}\right)}}$$

$$\frac{R_{Th}}{R_E} \ll \ll 1.$$

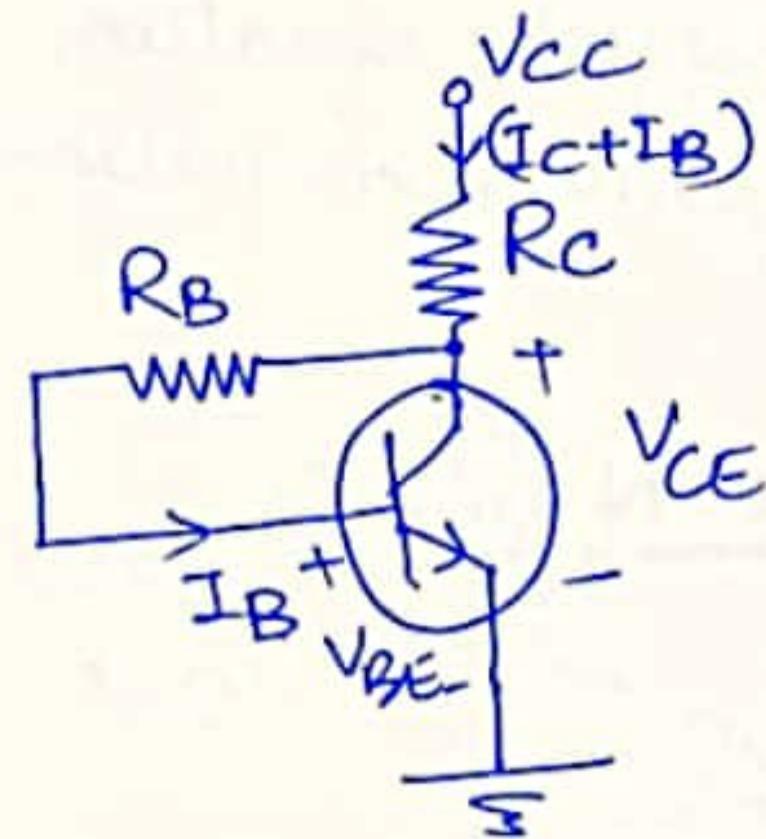
$$\begin{aligned} S &= \frac{(1 + \beta)(R_{Th} + R_E)}{R_{Th} + R_E + \beta R_E} \\ &= \frac{(1 + \beta)\left(\frac{R_{Th}}{R_E} + 1\right)}{\frac{R_{Th}}{R_E} + (1 + \beta)} \end{aligned}$$

$(R_{Th} \ll R_E)$

$$\therefore S = \frac{1 + \beta}{1 + \beta}$$

$$\boxed{S \approx 1}$$

### Stability factor of collector to base bias circuit



$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$0 - \left(1 + \frac{\Delta I_B}{\Delta I_C}\right) R_C - \frac{\Delta I_B}{\Delta I_C} R_B = 0$$

$$- \frac{\Delta I_B}{\Delta I_C} (R_B + R_C) - R_C = 0$$

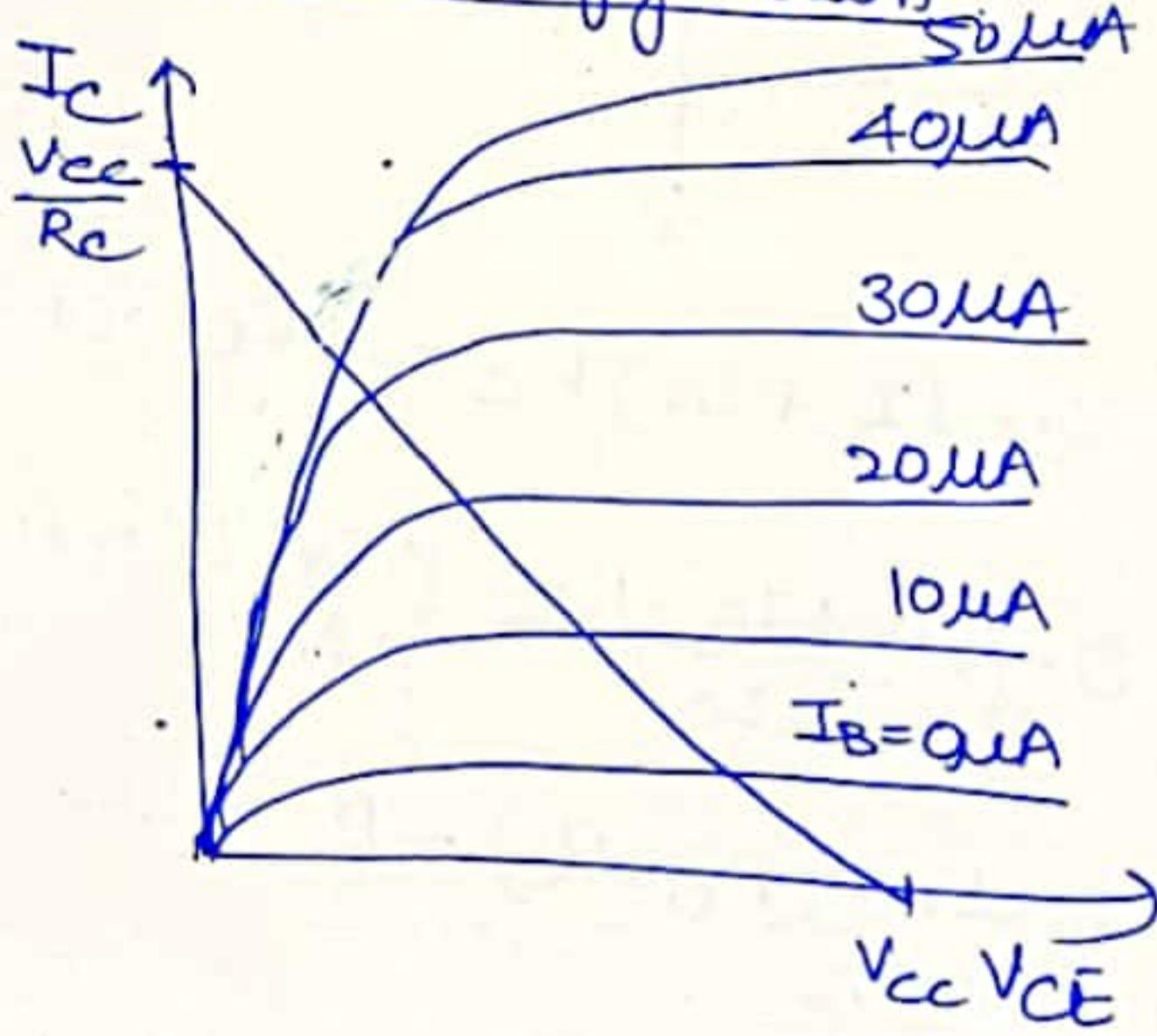
$$\boxed{\frac{\Delta I_B}{\Delta I_C} = \frac{-R_C}{R_C + R_B}}$$

$$\boxed{\text{Stability Factor} = \frac{(1 + \beta)}{1 + \beta \left(\frac{R_C}{R_C + R_B}\right)}}$$

## DC Load Line

O/P Ch. of BJT: Superimposed.  
On the plot of N/w equation  
defined by same axis parameters:

### Fixed bias configuration



$$V_{CE} = V_{CC} - I_C R_C \quad \text{---(1)}$$

at y-axis  $V_{CE} = 0$

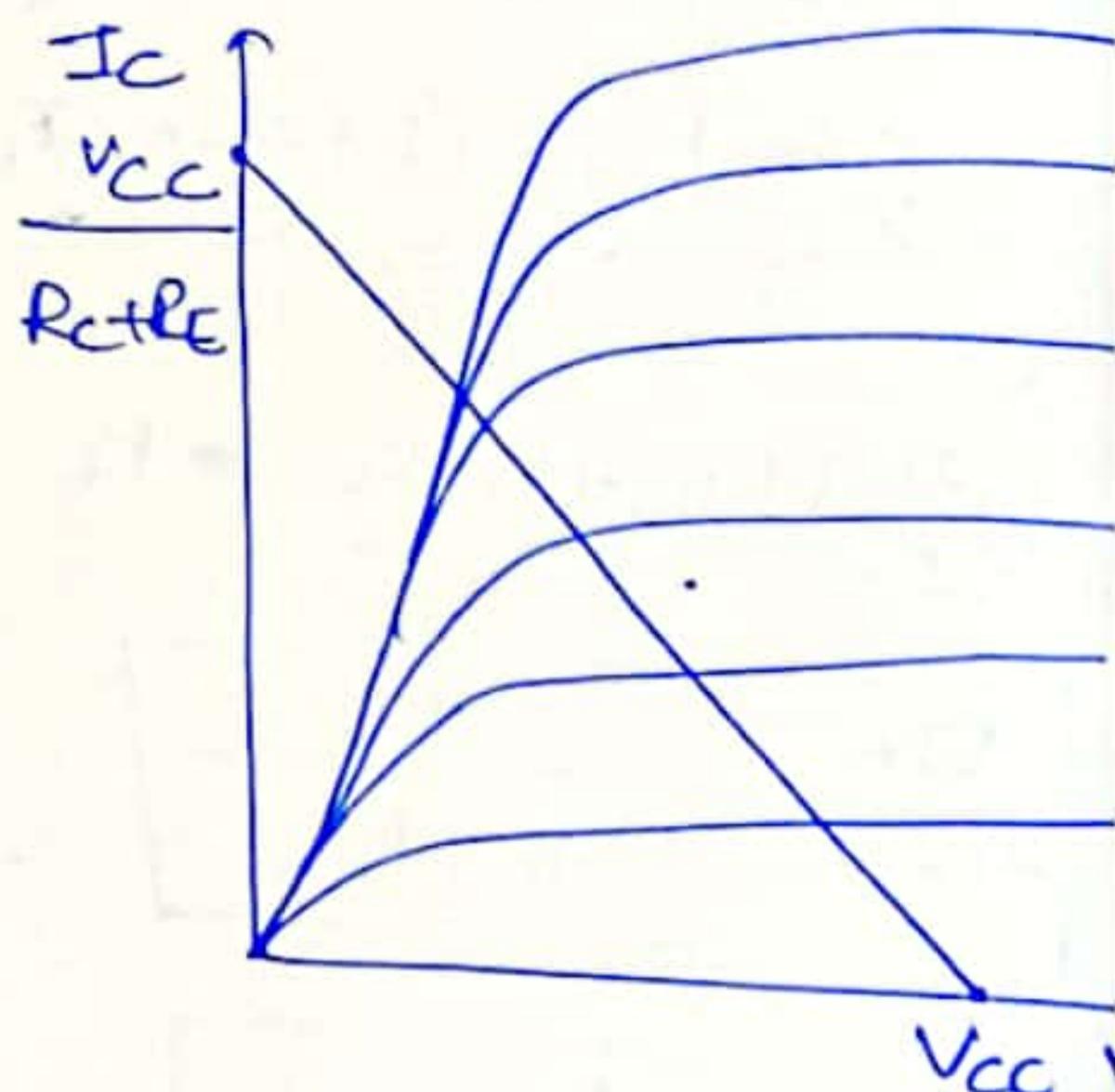
$$I_C = \frac{V_{CC}}{R_C}$$

at x-axis  $V_{CE} = 0 \Rightarrow I_C = 0$

$$V_{CE} = V_{CC}$$

Superimpose IV Ch. by  
line having eq (1)

## Emitter bias configuration



$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \text{---(2)}$$

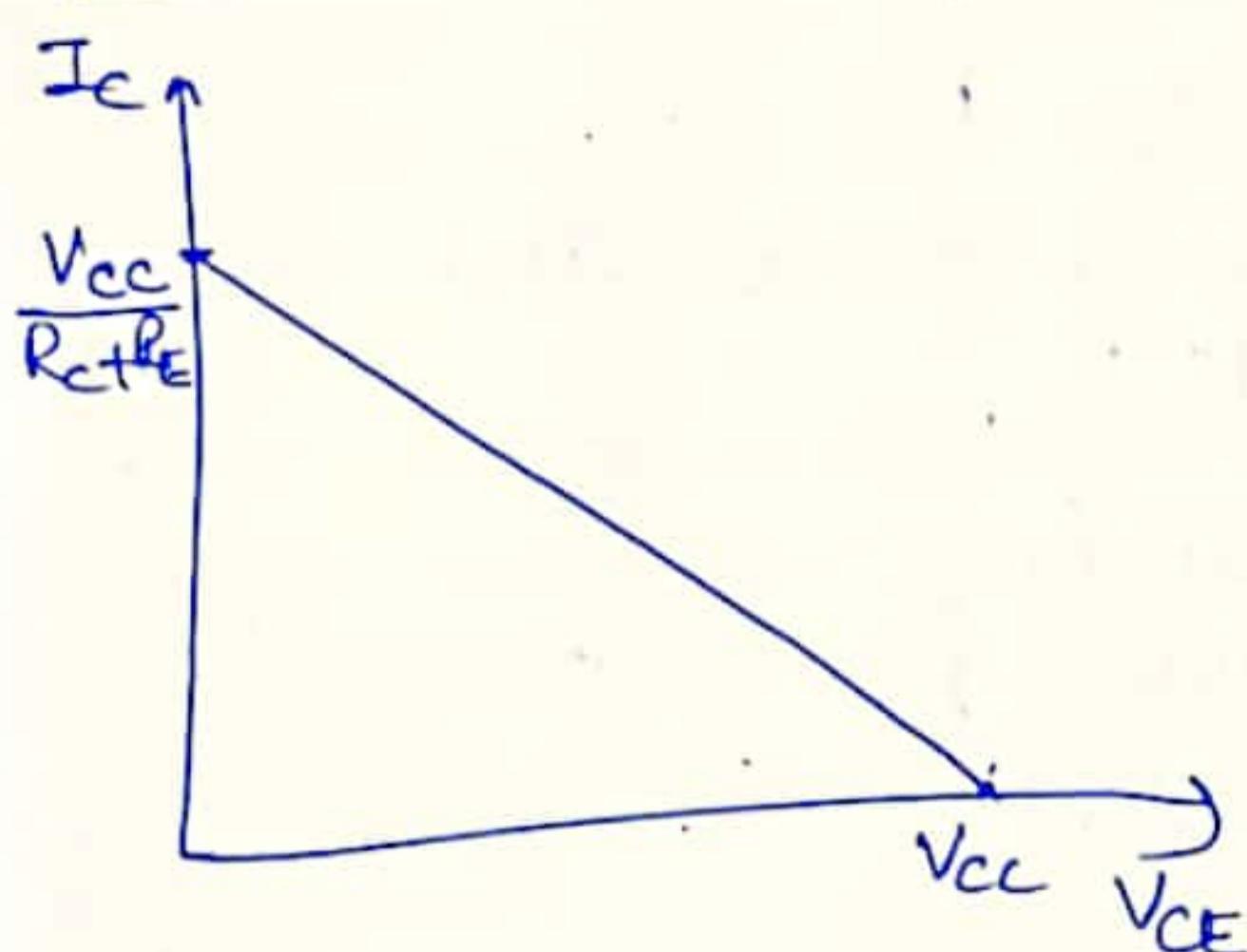
when  $I_C = 0$

$$V_{CE} = V_{CC}$$

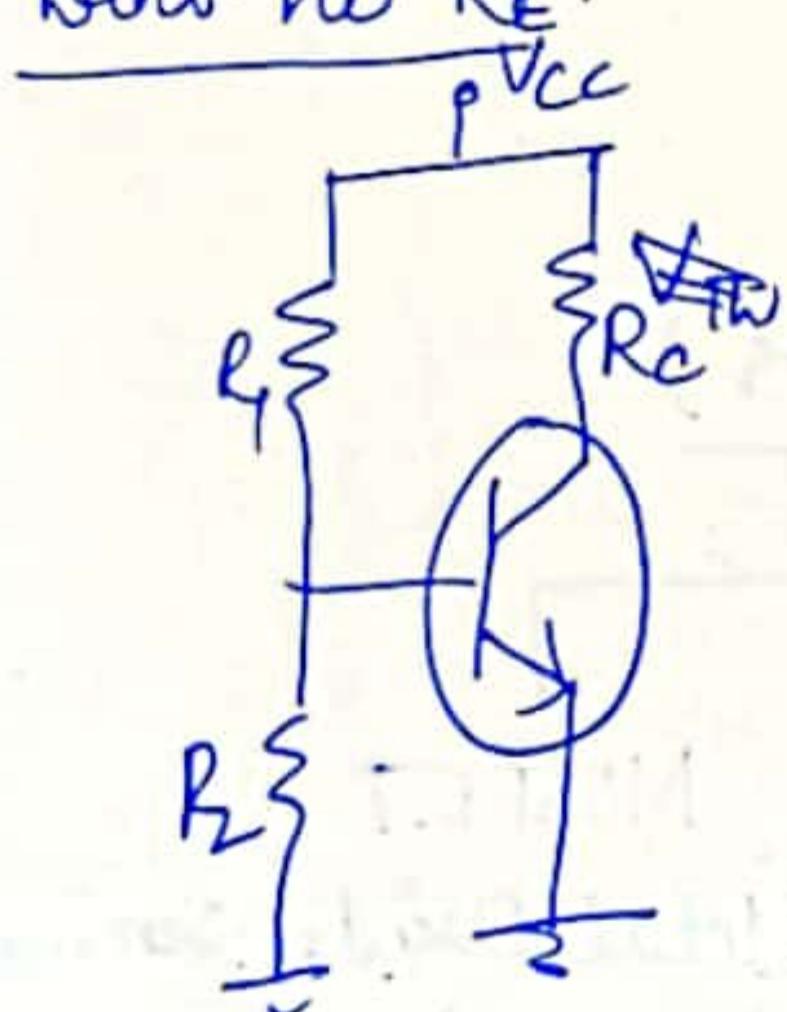
when  $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

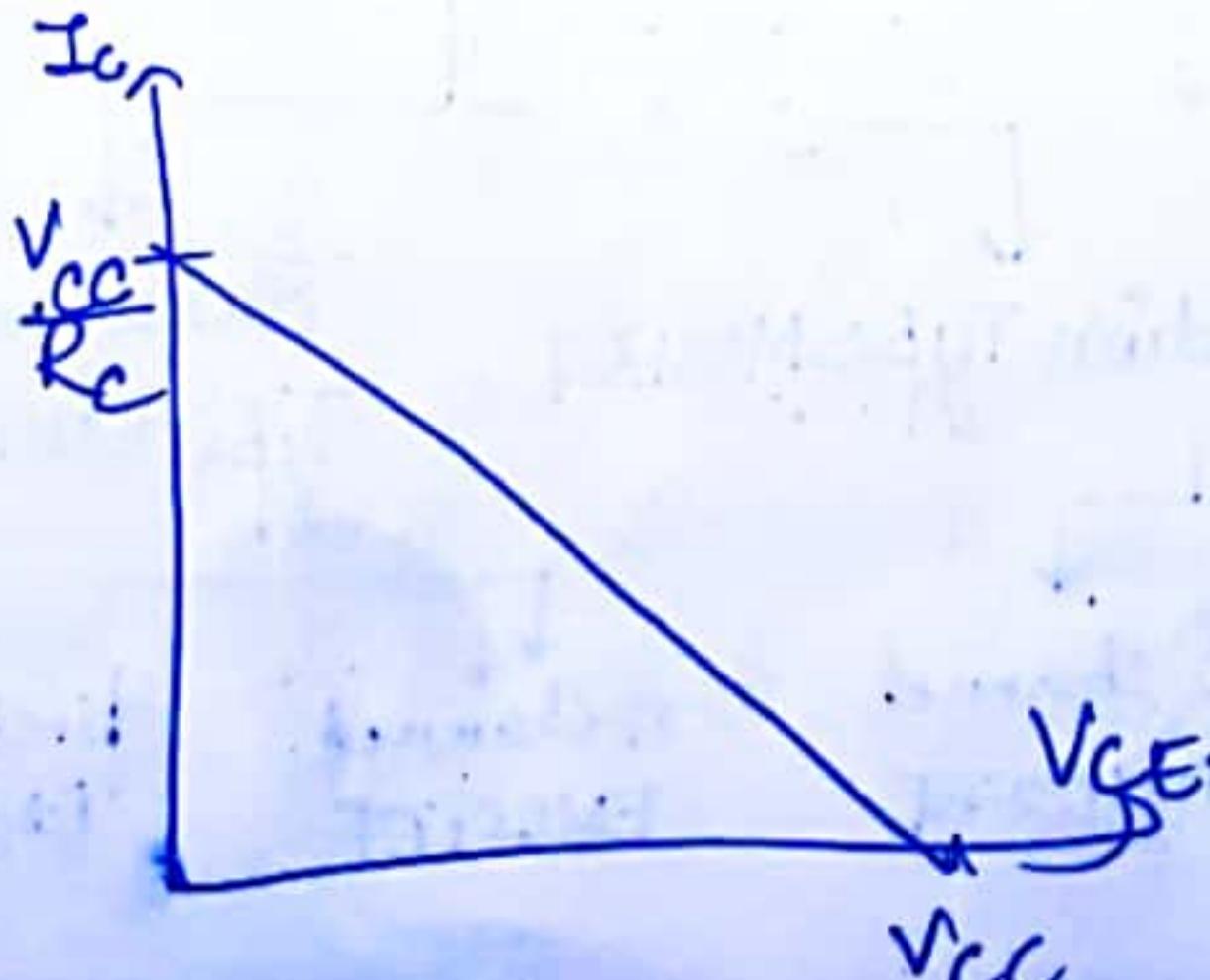
DC Load Line for  
Voltage Divider circuit  
with RE



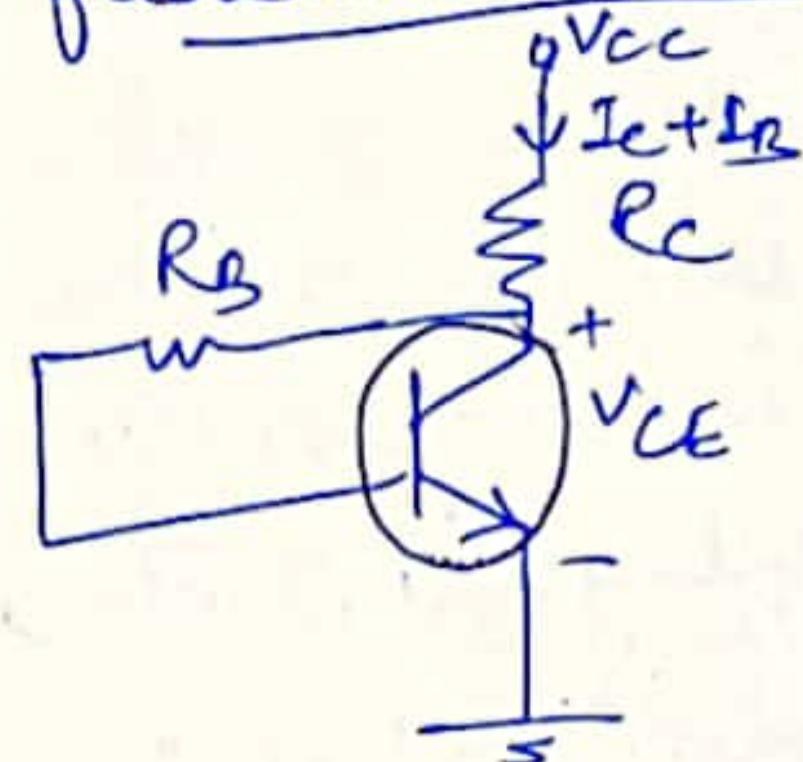
DC Load Line for  
Voltage divider configuration  
with no RE



$$V_{CC} - I_C R_C - V_{CE} = 0$$



DC Load Line to collector  
feedback circuit



$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CC} - \left( I_C + \frac{I_C}{B} \right) R_C - V_{CE} = 0$$

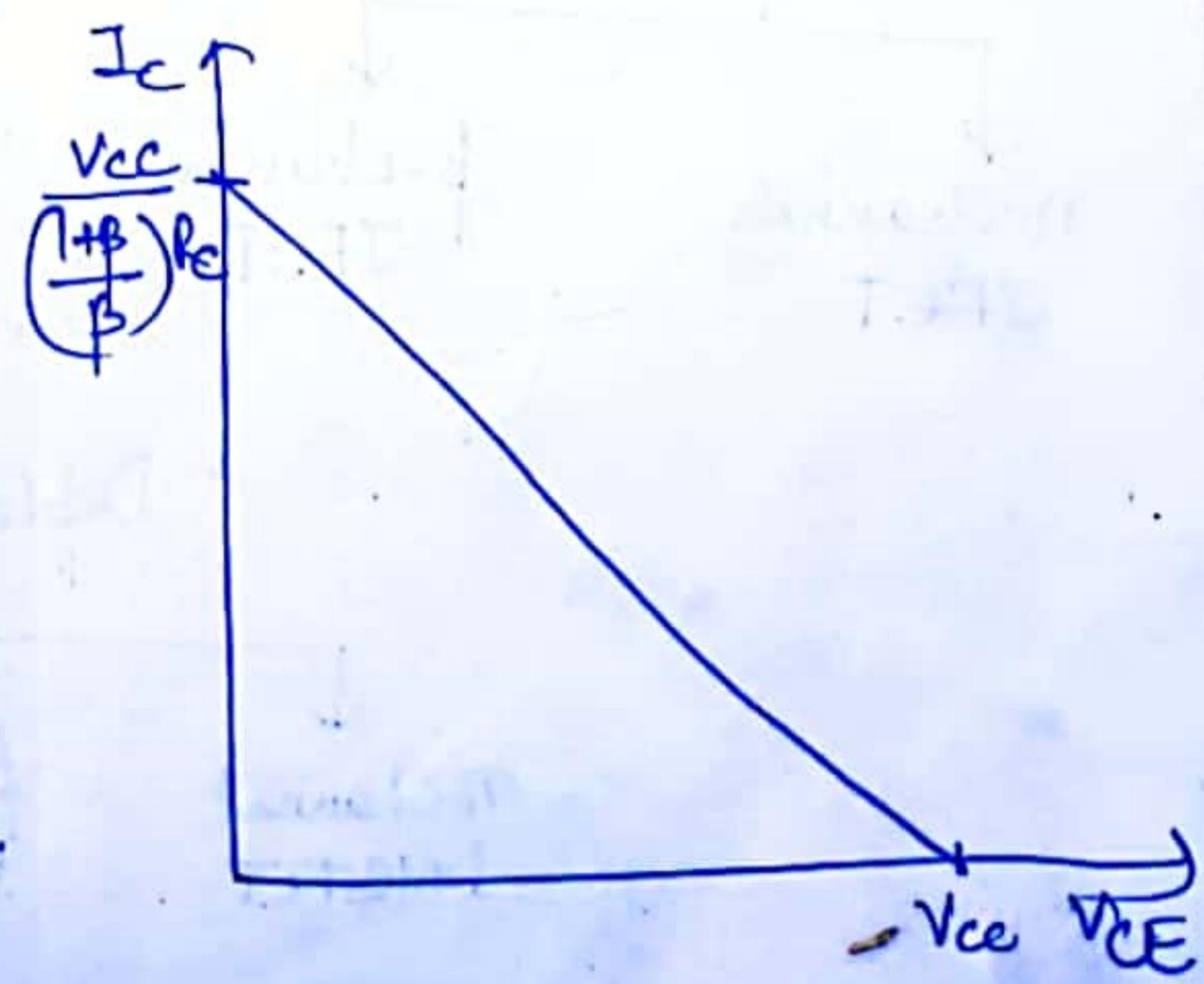
When  $V_{CE} = 0$

$$I_C \left( \frac{1+B}{B} \right) R_C = V_{CC}$$

$$I_C = \frac{V_{CC}}{\left( \frac{1+B}{B} \right) R_C}$$

When  $I_C = 0$

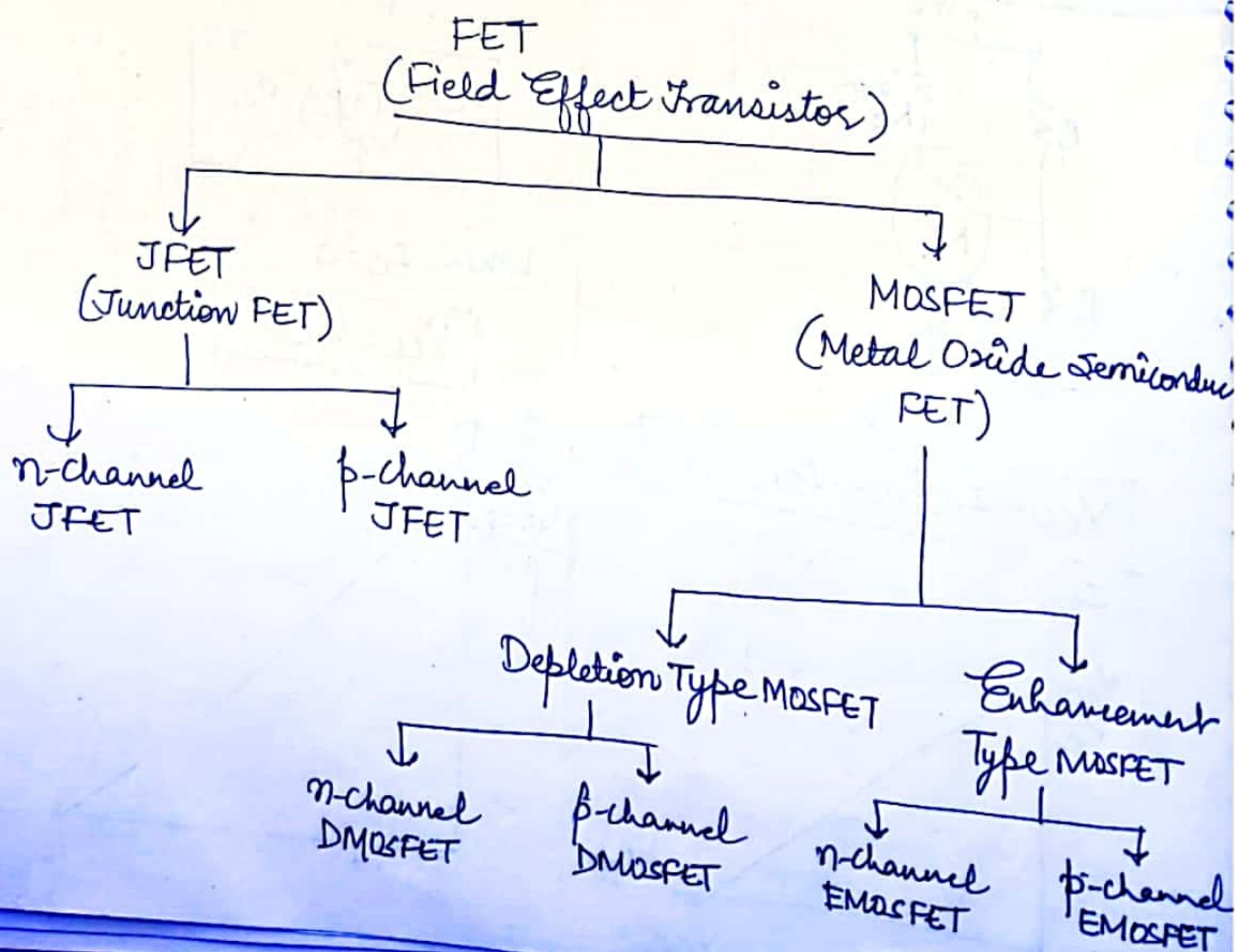
$$V_{CE} = V_{CC}$$



## Field Effect Transistor

- 1) It is three terminal device.
- 2) FET is much less noisy than BJT.
- 3) BJT is current controlled device and FET is voltage controlled device.
- 4) Terminals of FET
  - Drain (D)
  - Source (S)
  - Gate (G)
- 5) In FET drain current  $I_D$  depends on the control voltage  $V_{GS}$  applied between gate & source.

## Classification of FET

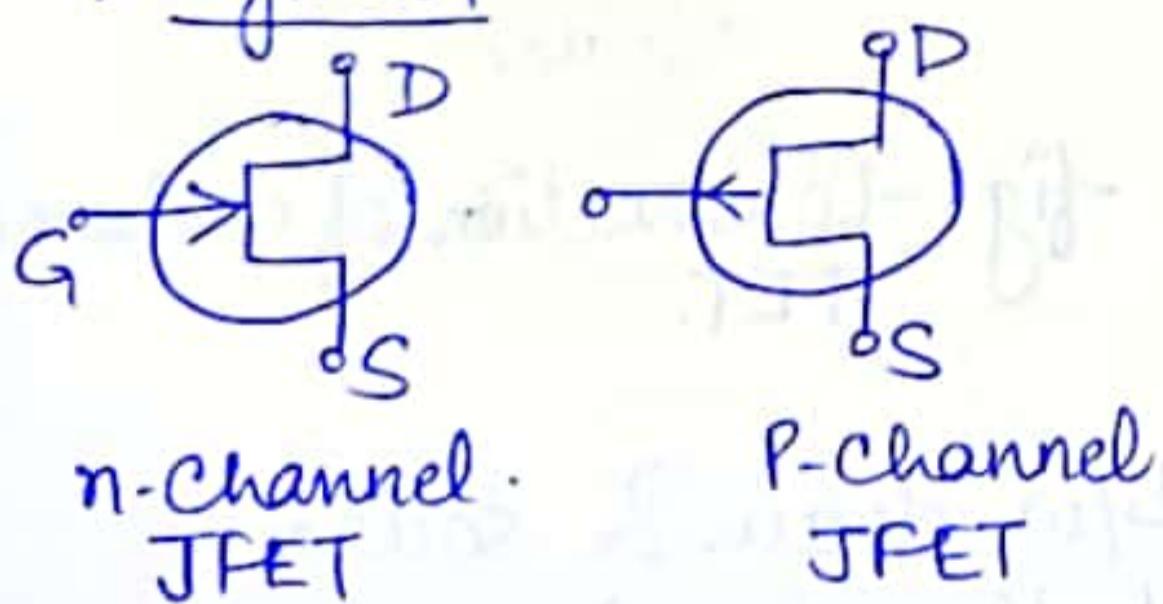


## Compare BJT & FET

### FET

- 1) It is an unipolar device i.e. current is carried by either electrons or holes.
- 2) It is voltage controlled device i.e. voltage at gate terminal controls the current flow through device.
- 3) Input impedance is very high. (in order of  $M\Omega$ )
- 4) Negative temp coefficient i.e.  $I \downarrow T \uparrow$   
This prevent thermal breakdown.
- 5) It has higher switching speed & cut-off frequencies.
- 6) ~~BJT~~ FET is smaller in size

### Symbol



- 8) It is much simpler to fabricate as an IC (Integrated circuits). It occupies a less space on IC chip than a BJT.

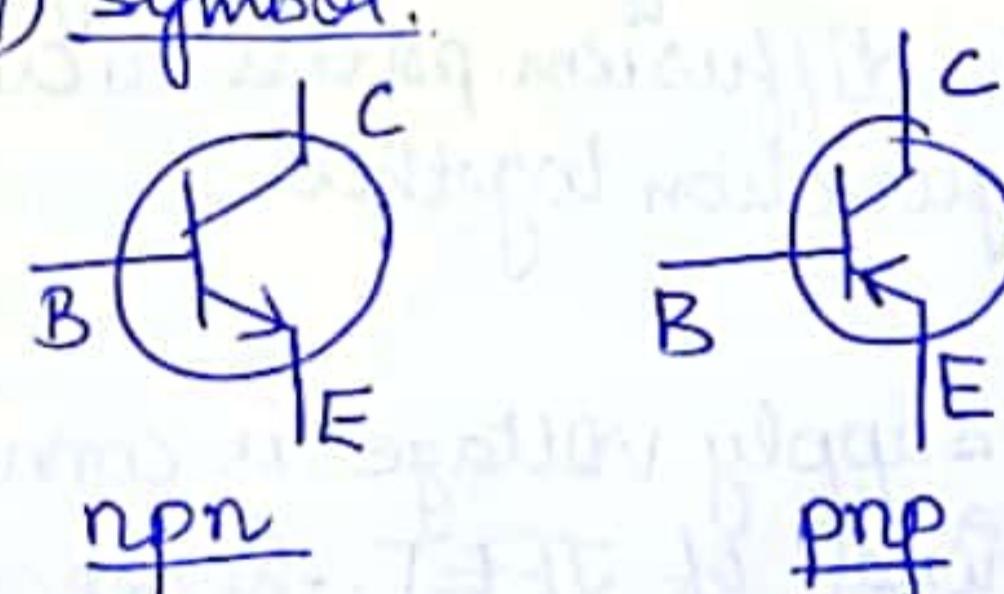
$$\begin{aligned} I_C &= \beta I_B \\ I_C &= \alpha I_E \\ I_E &= I_C + I_B \end{aligned}$$

## FET (Field Effect Transistor)

### BJT

- 1) It is a bipolar device current is carried by both holes & electrons.
- 2) It is current controlled device i.e. base current controls the amount of collector current.
- 3) Input resistance is low compared to FET (in  $k\Omega$ )
- 4) It has PTC i.e.  $T \uparrow I_C \uparrow$  that is why BJT can be damaged due to thermal breakdown.
- 5) It has lower switching speed and cut-off frequencies
- 6) BJT is larger in size.

### Symbol



- 7) It is difficult to fabricate IC. It occupies more space.

$$\begin{aligned} I_C &= 0 \\ I_D &= I_S \\ I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \end{aligned}$$

## Advantage of JFET over BJT.

- ① FET is unipolar hence operation depends on flow of majority carrier only.
- ② It is relatively immune to radiation.
- ③ FET has a very high SLP resistance (in few M $\Omega$ ).
- ④ FET is less noisy.
- ⑤ It does not exhibit any offset voltage to zero drain current.
- ⑥ FET has a better thermal stability.

## Disadvantage

FET has a relatively small gain-bandwidth product as compared with that of a conventional transistor.

### Construction of n-channel FET

- A SC bar of n-type material is taken & Ohmic contacts are made to the ends of the bar. These terminals are named as drain & source.
- On both sides of n-type bar heavily doped ( $P^+$ ) p-region have been formed by alloying and diffusion process to create p-n junction together.

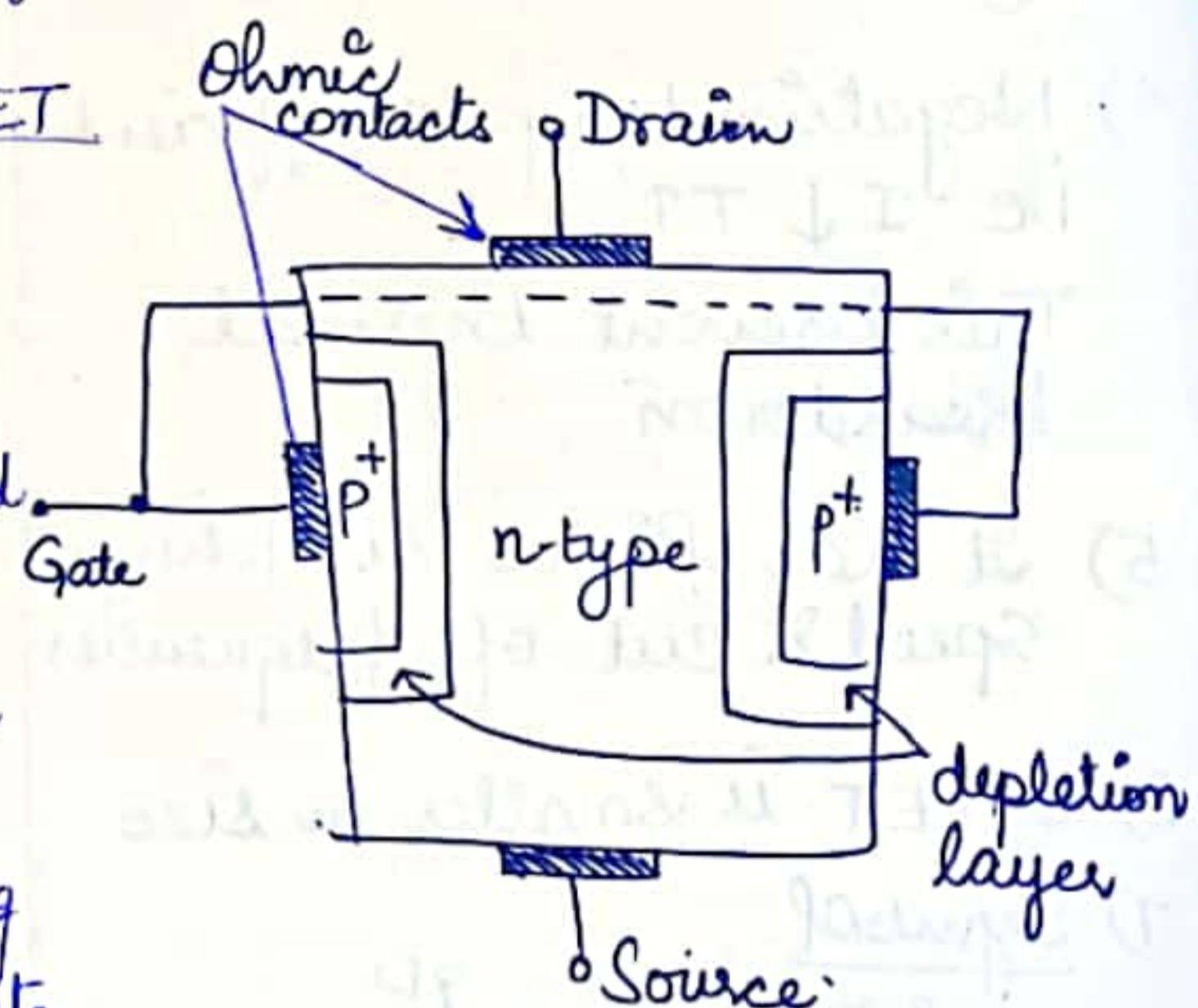
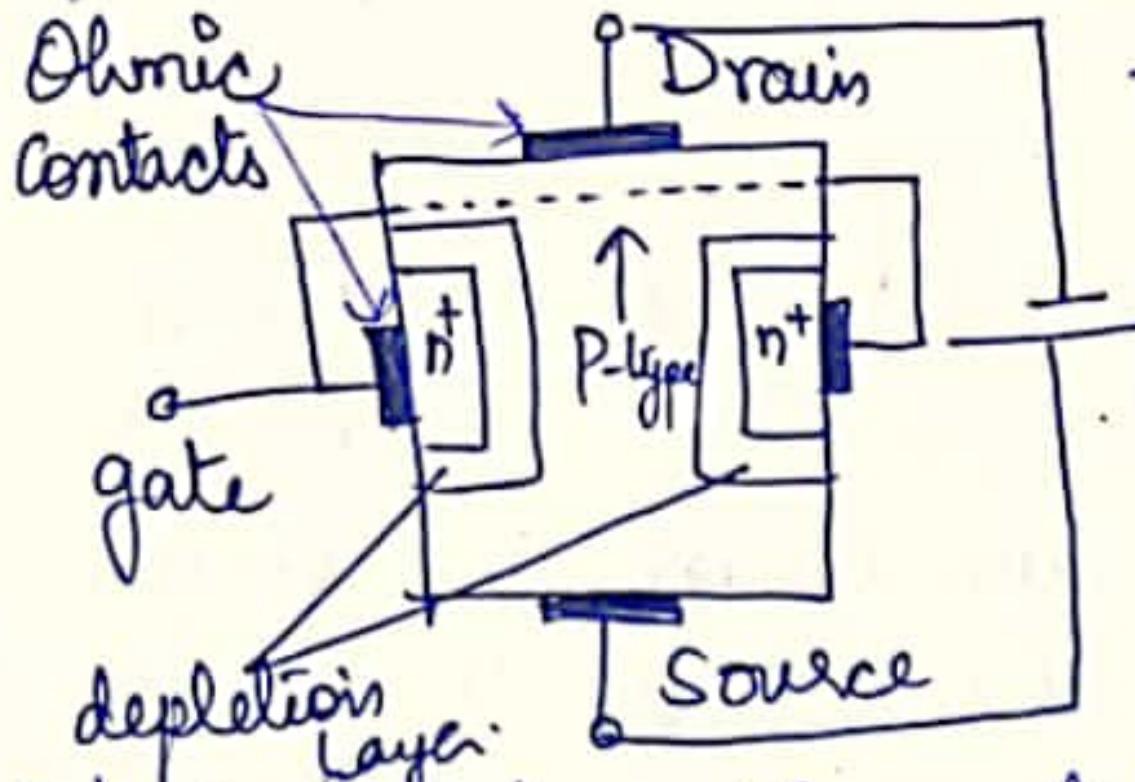


fig:- Construction of n-channel FET.

- The supply voltage is connected b/w drain & source terminal of JFET. hence current flow is along the length of n-type bar. This current is due to majority carrier.

### Construction of p-channel FET :-

- A SC bar of p-type material is taken & ohmic contacts are made to the ends of the bar. These terminals name drain & source.



- On both sides heavily doped n-regions have been formed by alloying & diffusion process.
- Supply connected b/w D & S.
- Current flow is along the length of p-side type bar.

### Working of n-channel FET :-

Case 1  $V_{GS} = 0$ ,  $V_{DS} > 0$

When  $V_{DS}$  is applied to channel & Gate terminal is connected directly to source.

Gate & source terminal has same potential hence depletion region in the lower end of p-material is similar to no-bias condition.

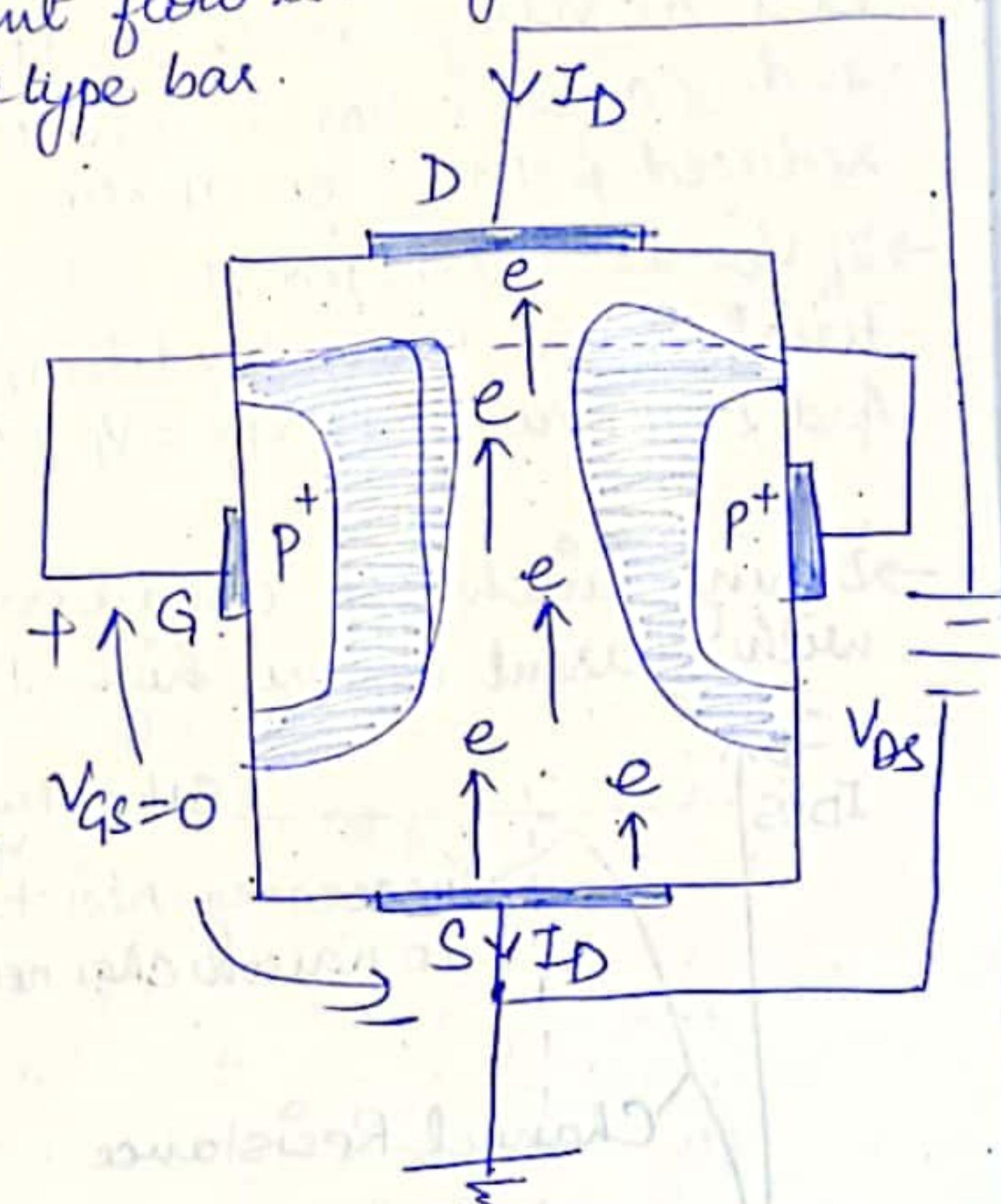


fig1:- JFET as  $V_{GS} = 0V$  &  $V_{DS} > 0V$

When  $V_{DS}$  is applied then electrons are drawn from drain terminal which establish conventional current in defined direction as shown in fig 1.

From figure it is clear that  $I_D = I_S$

\* Why depletion region is wider near top of both p-type material (Near drain)?

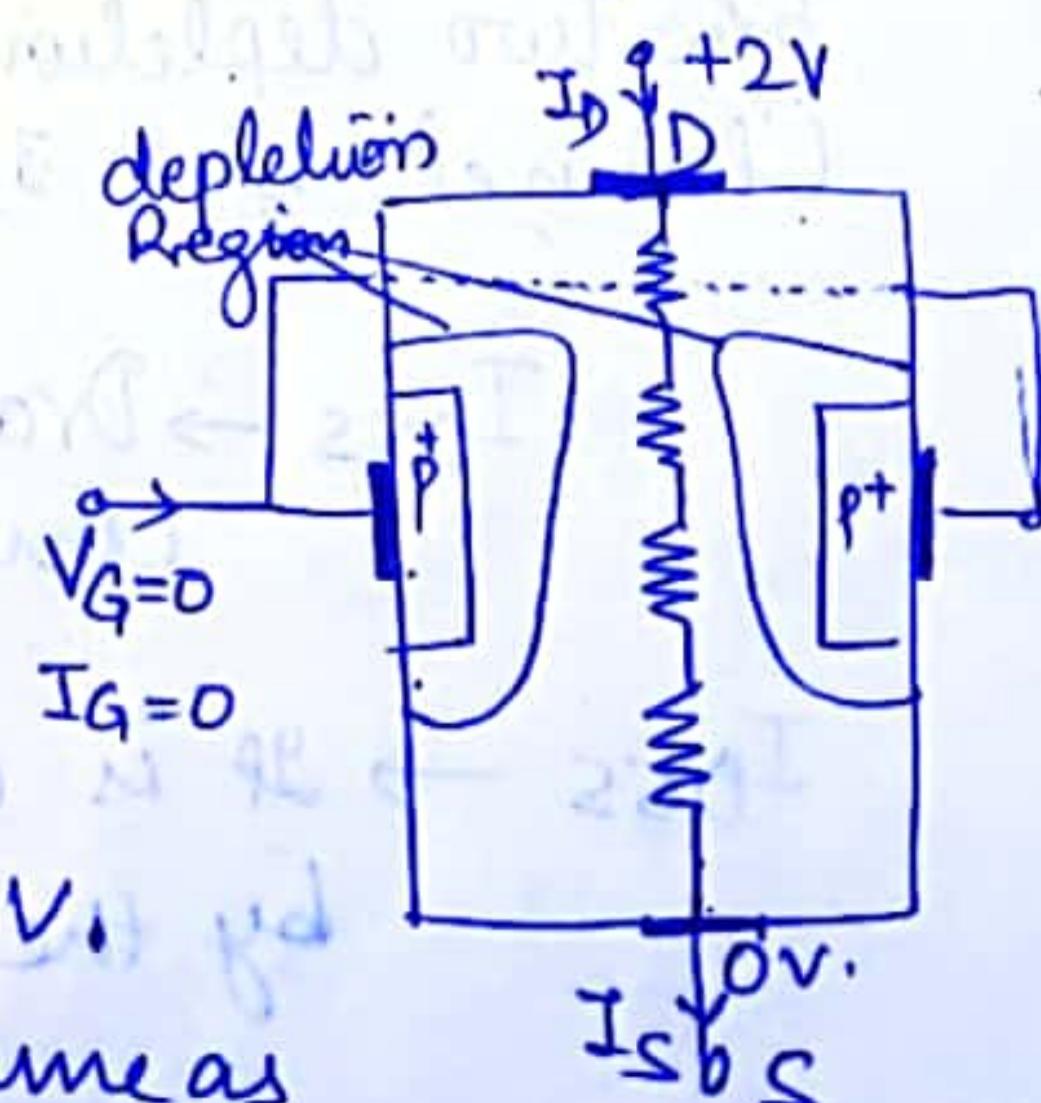
Since current  $I_D = I_S$ . This means current is uniform across channel, but voltage is variable.

For Example  $V_D = 2V$ . And  $V_G = 0$ .

This means junction is reverse biased hence depletion region is wide.

But near Source terminal  $V_G = V_D = 0V$ .

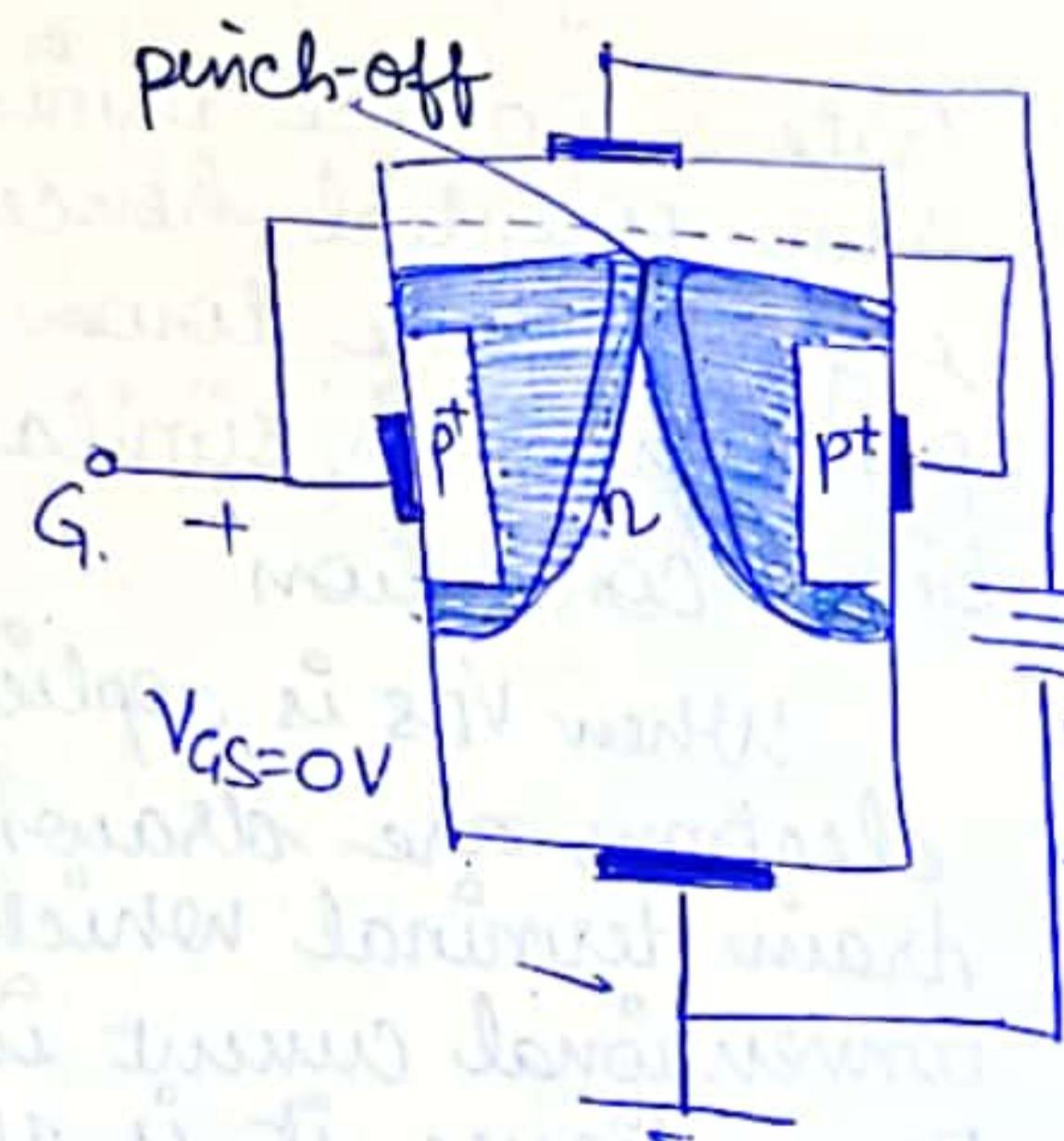
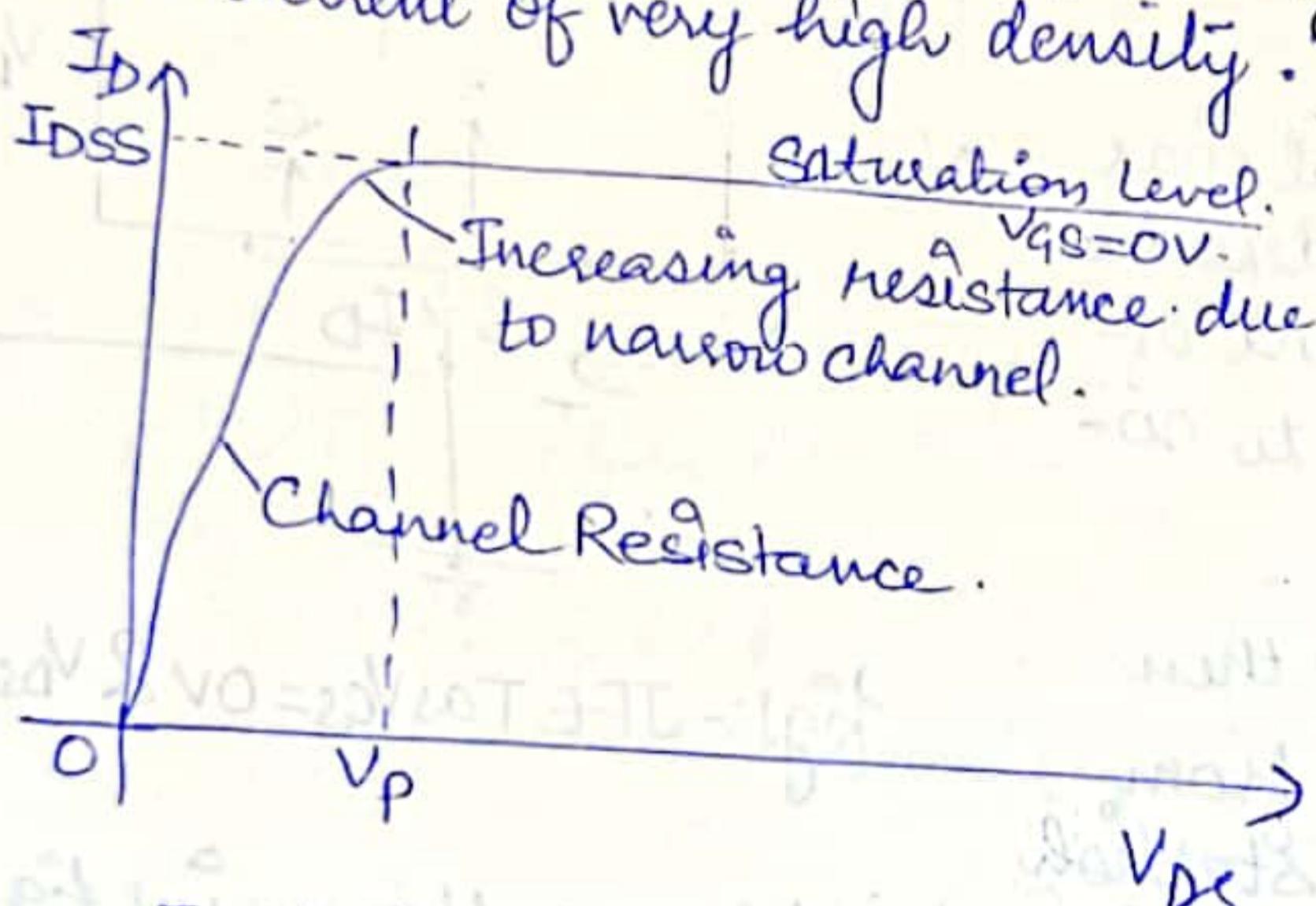
Therefore here depletion region is same as in ~~no~~ reverse bias condition.



## Pinch-off condition :-

As  $V_{DS}$  is increased from 0V to few volts, the current will increase as per Ohm's law (As shown in given plot). But As voltage increases to  $V_p$ , depletion region will widen and cause noticeable reduction in channel width. This reduced path of conduction will cause increase in resistance. → If  $V_{DS}$  is increased to a level where two depletion regions touch. Then that condition is known as pinch-off condition. And that value of  $V_{DS} = V_p$  (Pinch off voltage).

→ During pinch-off condition, a very small channel still exists with current of very high density.



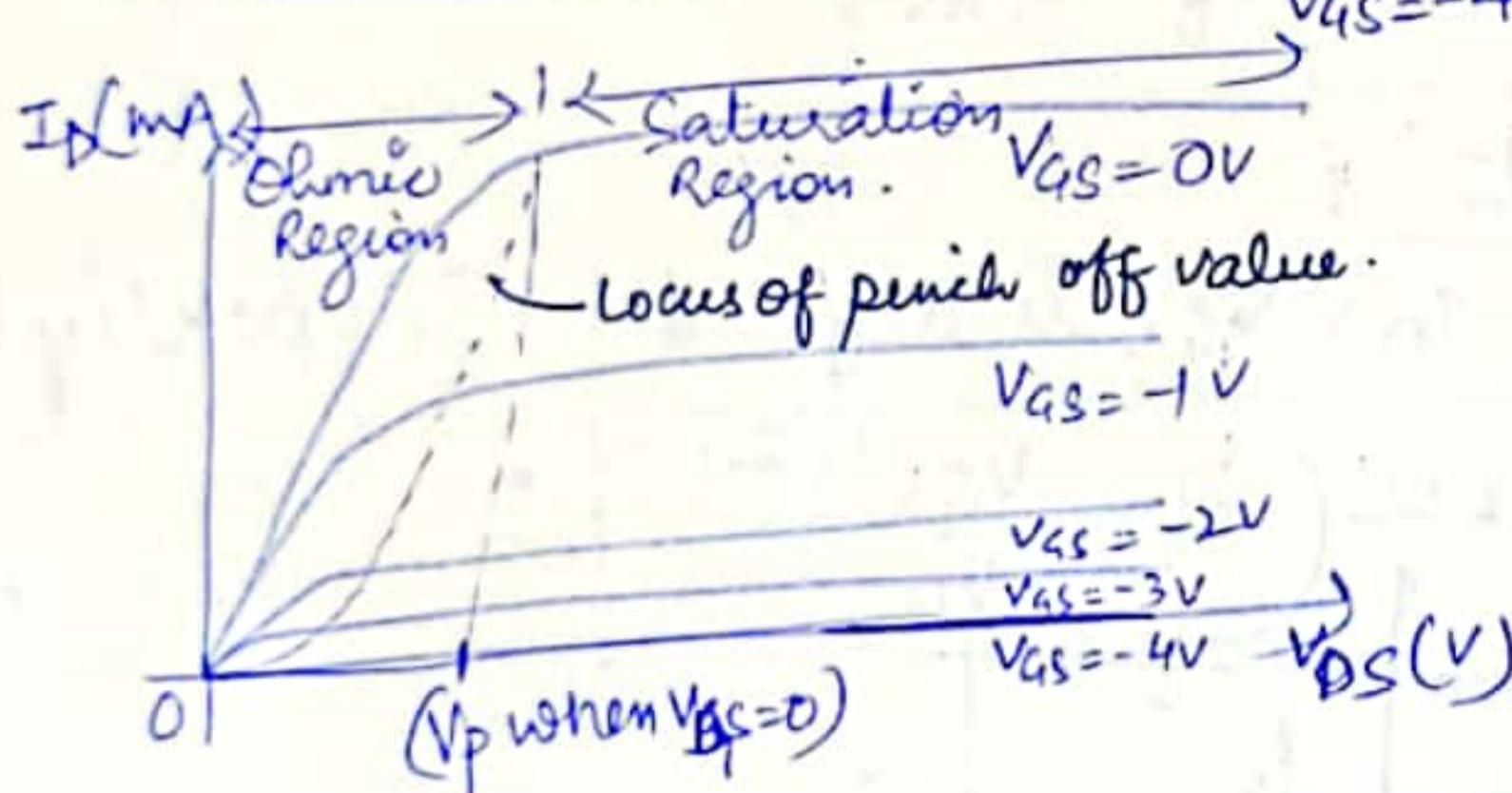
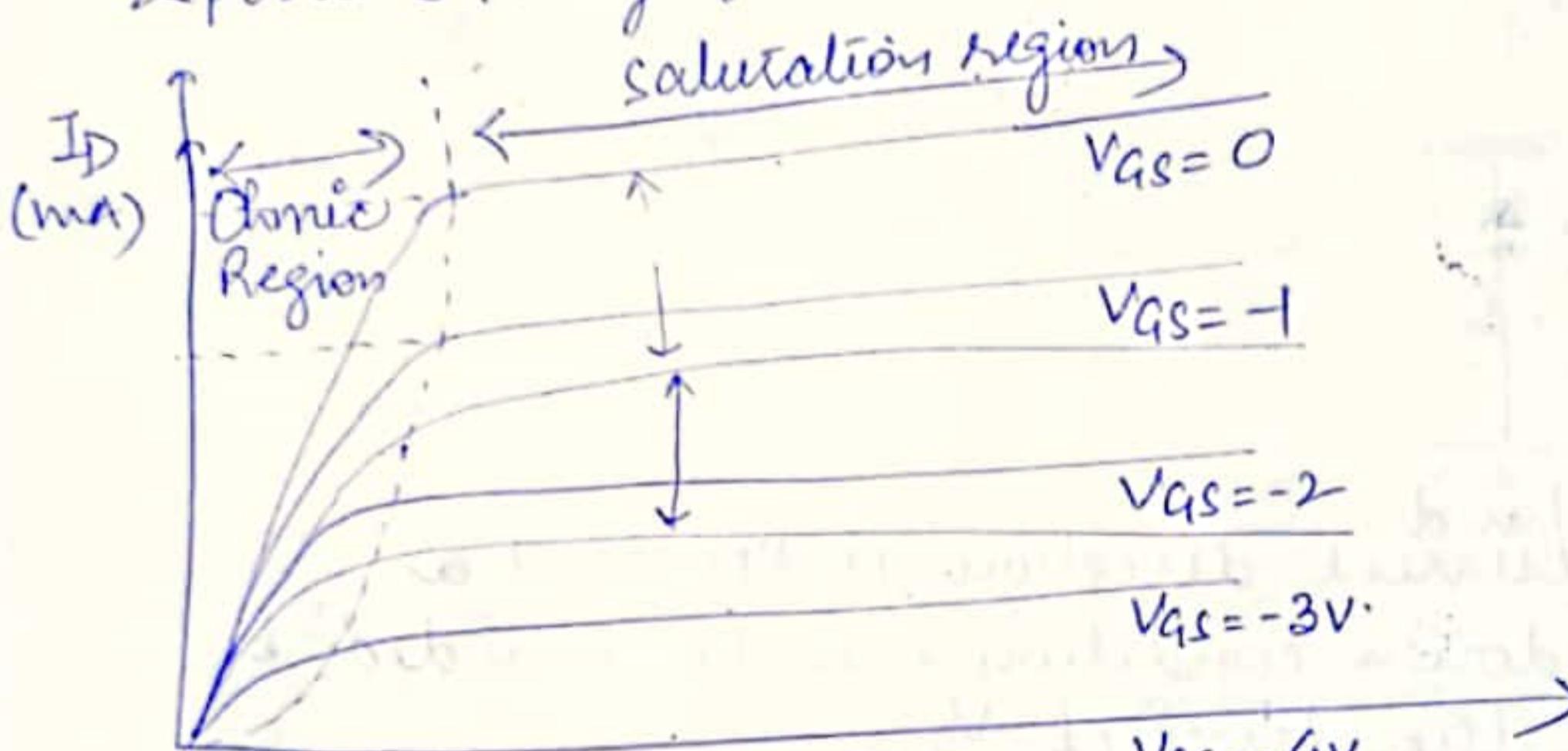
As  $V_{DS}$  increased beyond  $V_p$ , the region of close encounter between two depletion regions increases along the channel, but  $I_D$  remains constant ( $I_D = I_{DSS}$ ). fig:- pinch off. ( $V_{GS}=0, V_D > V_p$ )

$I_{DSS} \rightarrow$  Drain to source current when S/cut connection from G to S.

$I_{DSS} \rightarrow$  It is a max drain current and is defined by the condition  $V_{GS}=0$  &  $V_D > |V_p|$ .

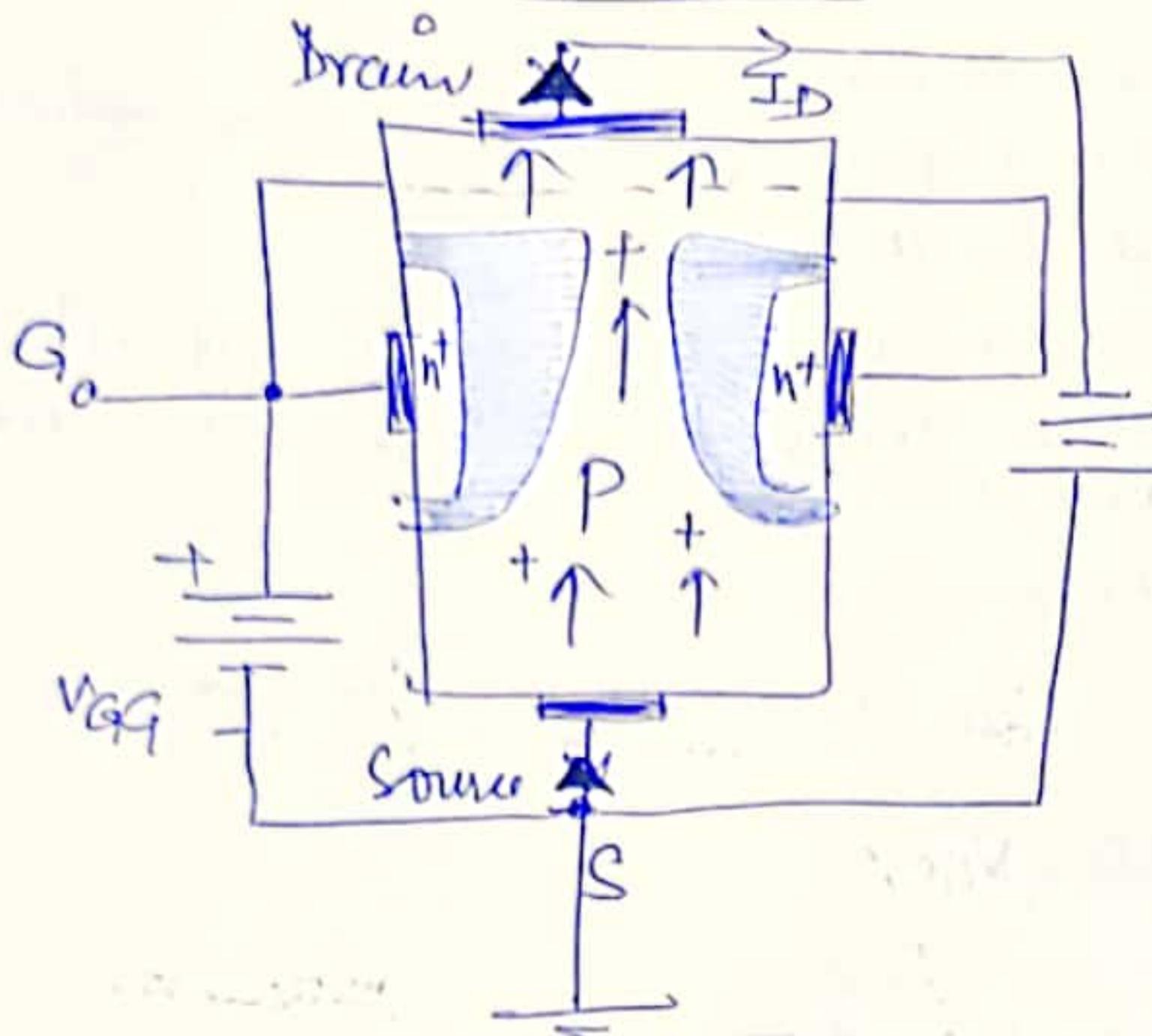
## Case-2. When $V_{GS} < 0V$ .

- 1)  $V_{GS}$  is controlling voltage of JFET
- 2) As  $V_{GS}$  decreases,  $V_p$  continues to drop in parabolic path and become more & more negative.
- 3) The level of  $V_{GS}$  that results in  $I_D = 0mA$  is defined by  $V_{GS} = V_p$ , with  $V_p$  being a negative voltage for n-channel & positive voltage for p-channel.



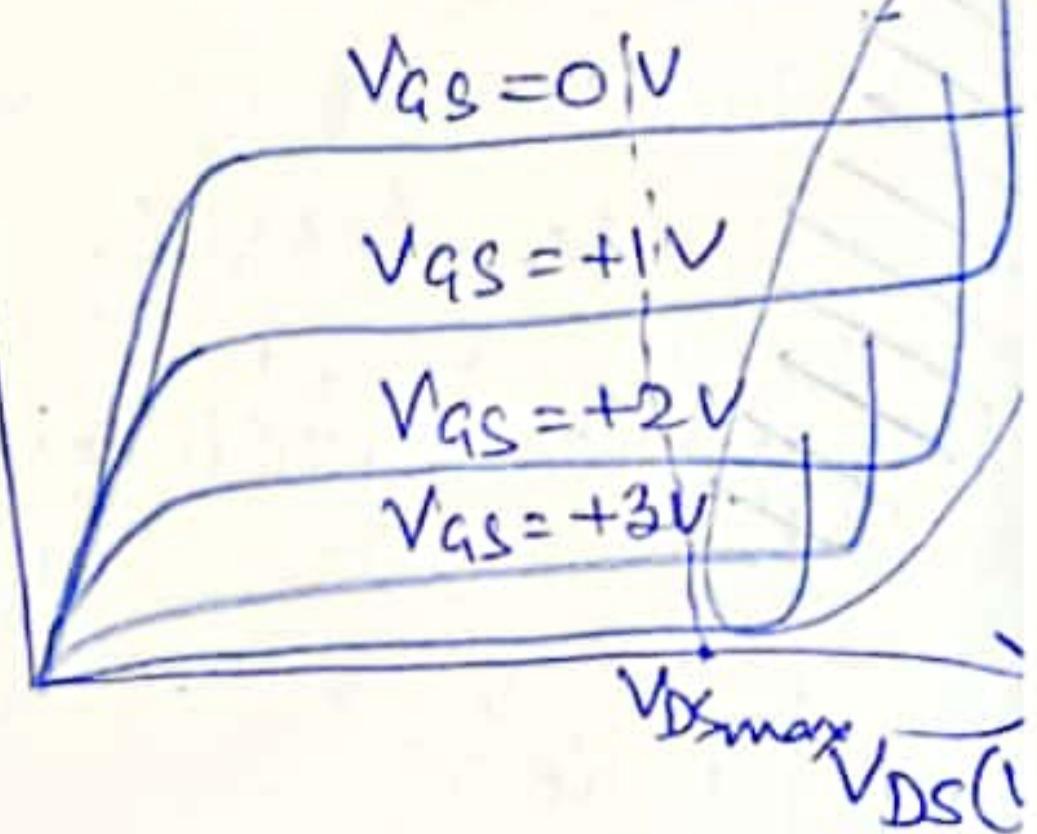
- Info
- 4) Region to the right of pinch off locus is referred to Ohmic or voltage controlled resistance region.
  - 5) As  $V_{GS}$  becomes more & more negative, the slope of each curve becomes more & more horizontal, correspondingly to an increasing resistance level.

For P-channel device



$I_D(\text{mA})$

Breakdown  
Regions



- In this <sup>is defined</sup> current direction is reversed
- The breakdown condition can be avoided by selecting the level of  $V_{DS\max}$ .

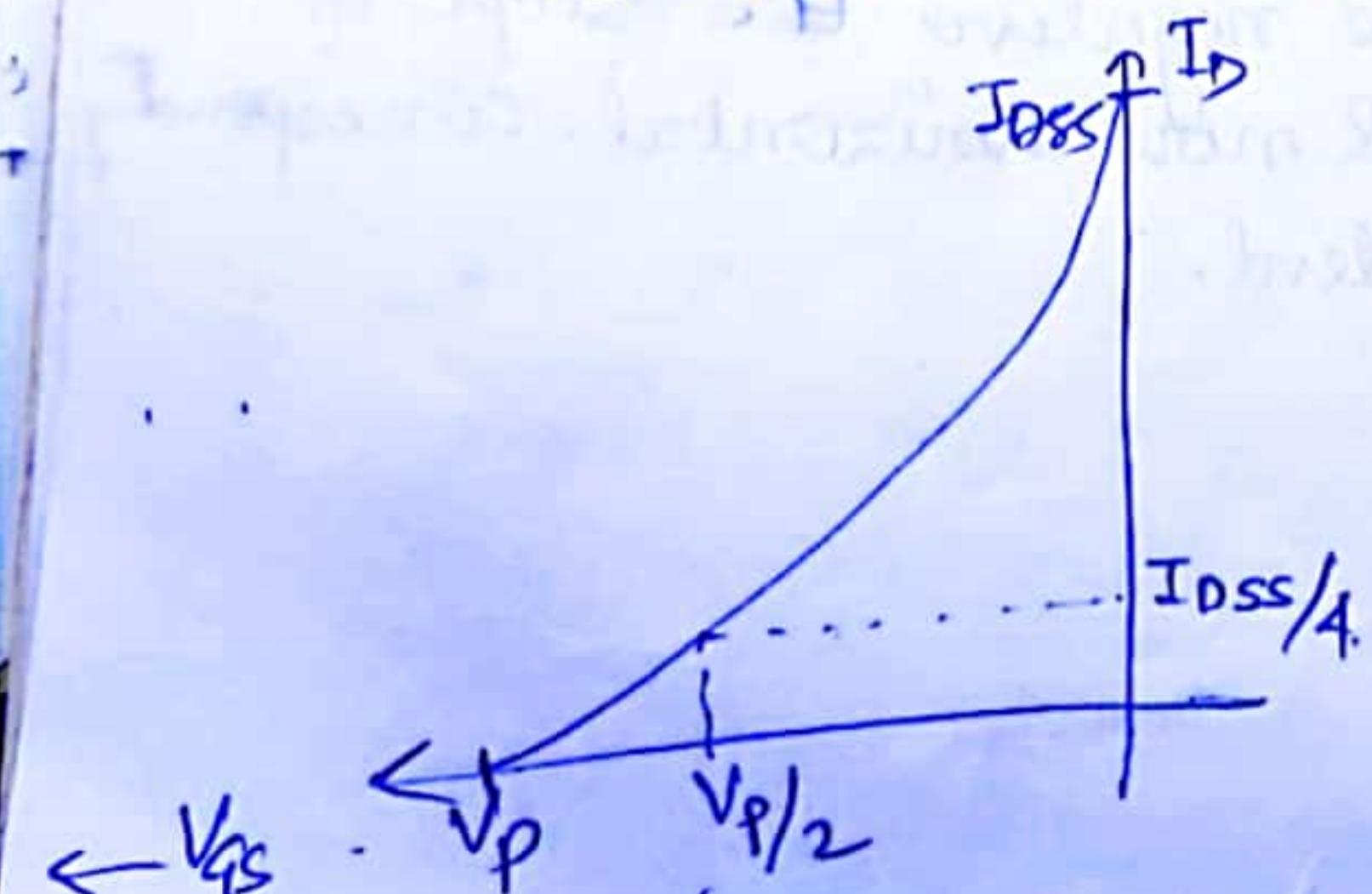
Transfer characteristics

Relationship b/w  $I_D$  &  $V_{GS}$  is defined by "Shockley's eq"

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

Constants

This shows non-linear relationship b/w  $V_{GS}$  &  $I_D$



a)  $V_{GS} = 0$

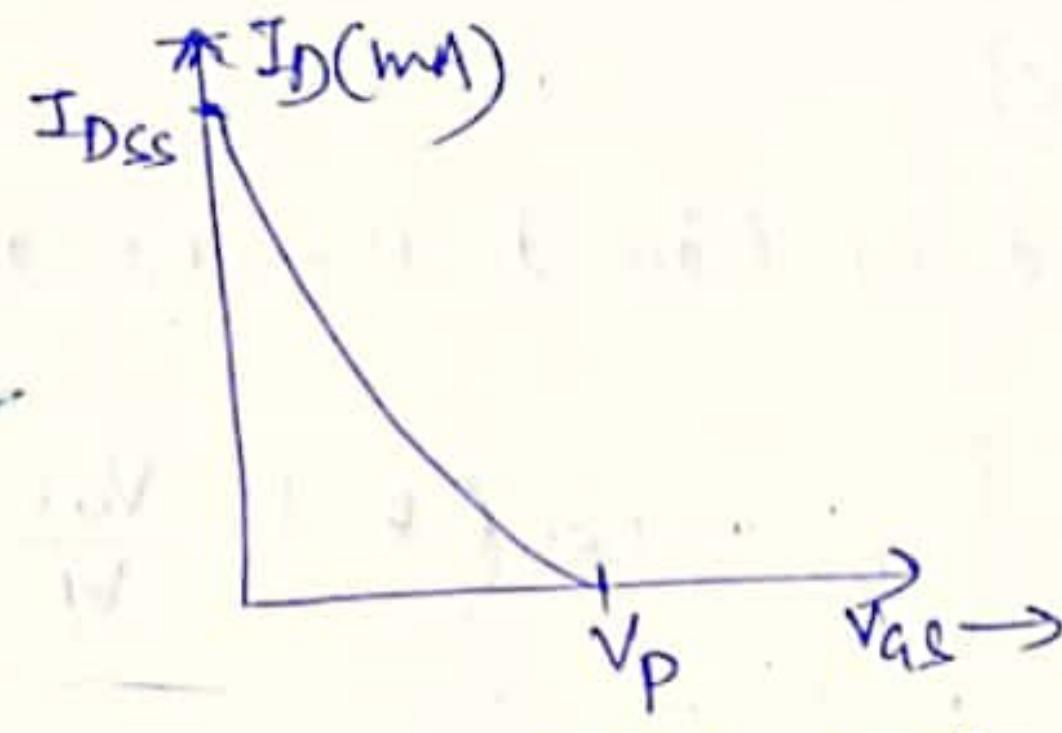
$I_D = I_{DSS}$

b)  $I_D = 0$

$V_{GS} = V_p$

c)  $I_D = I_{DSS}/4$

$V_{GS} = V_p/2$



Transfer Ch. for p-Channel JFET

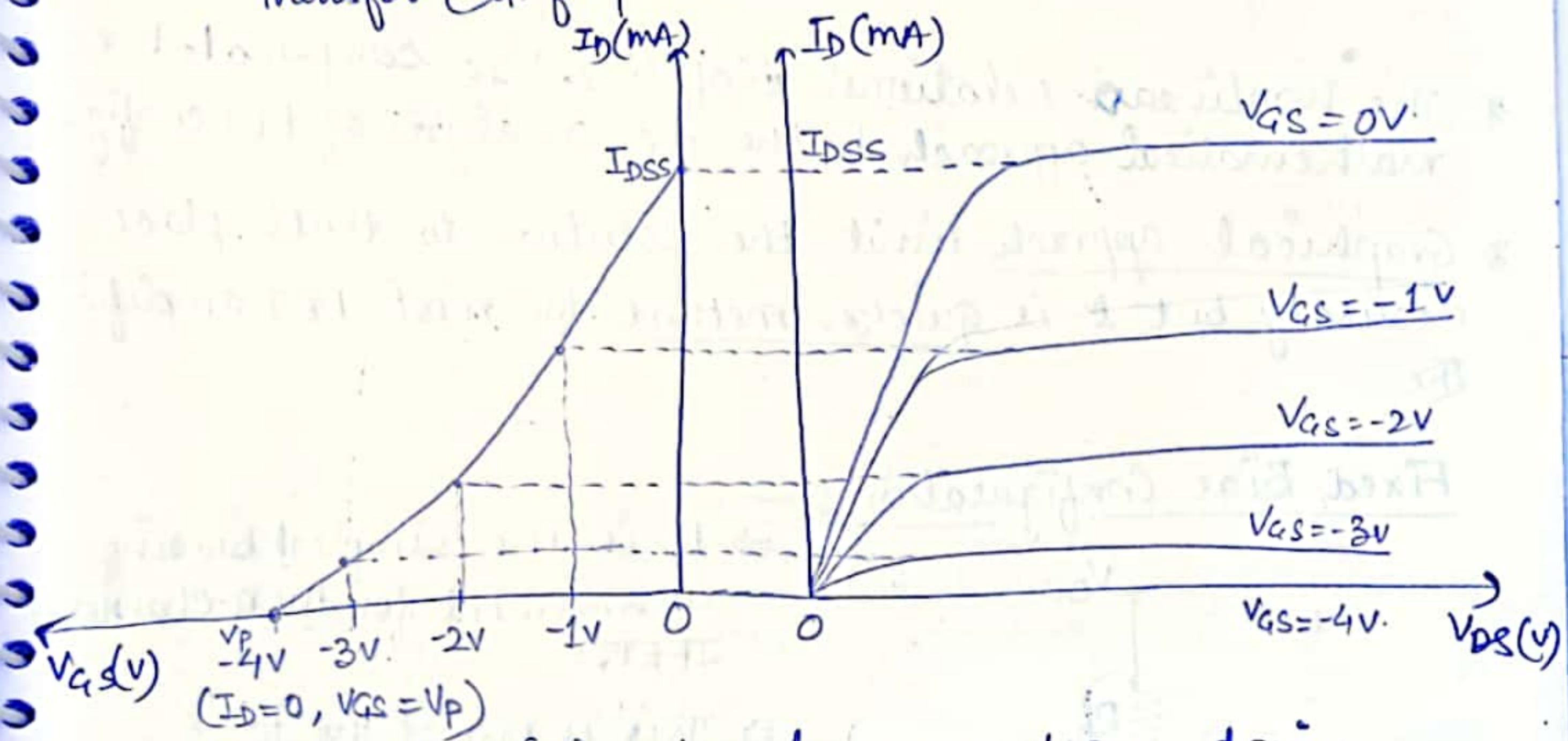


Fig: Obtaining transfer curve from drain characteristic

$$V_{GS} = V_p \left( 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

Q1)  $I_{DSS} = 15\text{mA}$ ,  $V_{GS(\text{off})} = -5\text{V}$ . Find drain current at  $0\text{V}, -1\text{V}$  &  $-4\text{V}$ .

② For following information of N-channel JFET :  $I_{DSS} = 20\text{mA}$ ,  $V_p = -8\text{V}$  &  $g_m = 5000\mu\text{s}$ .

③  $V_p = -2\text{V}$ ,  $I_{DSS} = 1.55\text{mA}$ . It is biased at  $I_D = 0.8\text{mA}$ ,  $V_{DD} = 24\text{V}$ . Find  $V_{SS}$  &  $g_m$ .

④ Determine the transconductance of FET. When  $I_D$  changes from  $1\text{mA}$  to  $1.9\text{mA}$  with change in  $V_{GS}$  is from  $-3.3$  to  $-3\text{V}$

## FET Biasing

- \* General Relationship that can be applied to the dc analysis of FET amplifiers are:

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

## Parameters of JFET

- \* The nonlinear relationship of  $I_D$  &  $V_{GS}$  complicate the mathematical approach to the dc analysis of FET config.
- \* Graphical approach limit the solution to tenth place accuracy but is quicker method for most FET amplifiers.

## Fixed Bias Configuration :-

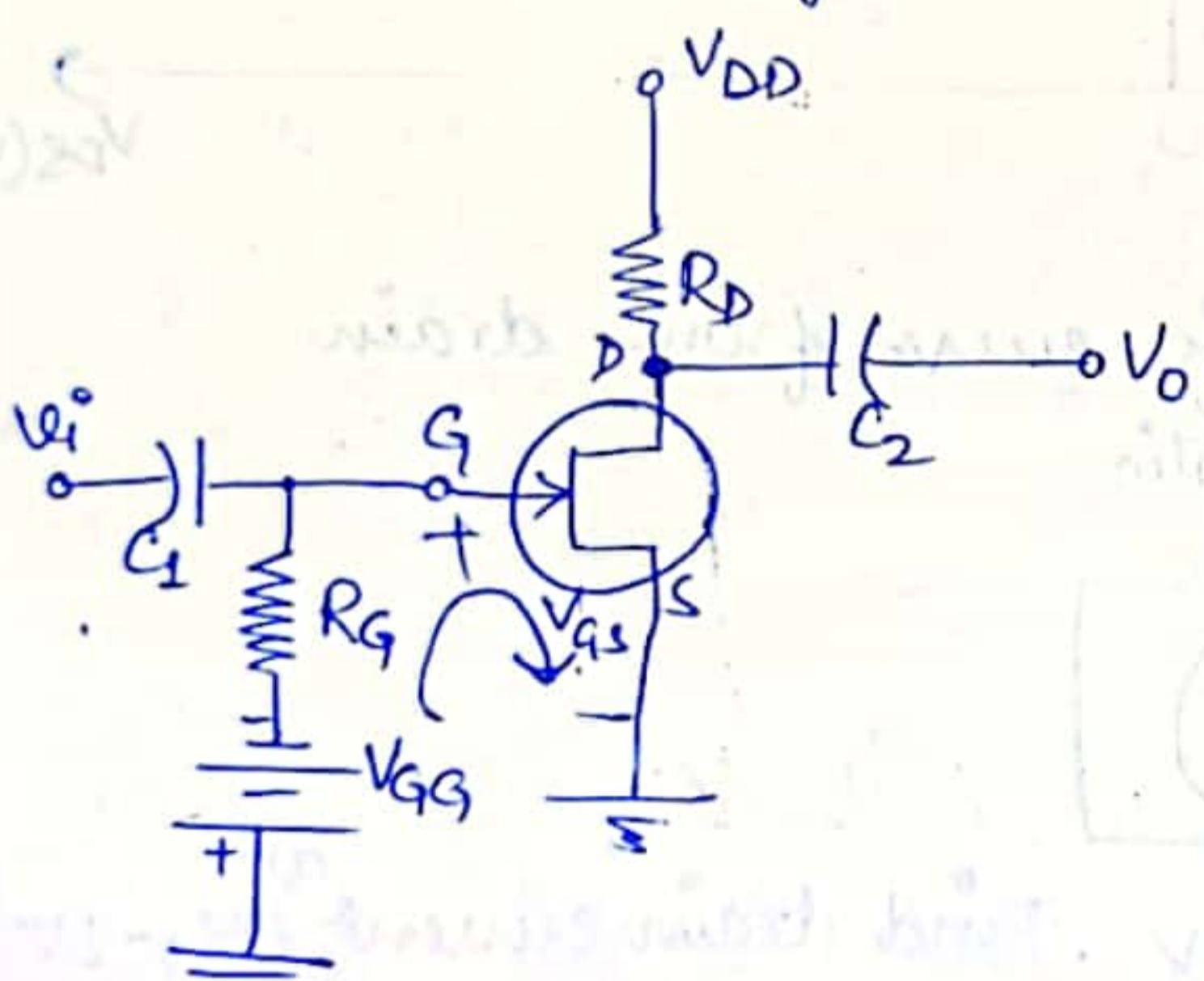


fig: Fixed bias Config.

→ It is the simplest biasing arrangement for n-channel JFET.

→ This is one of the few configurations that can be solved just as directly using either a mathematical or graphical approach.

## Mathematical approach :-

$$I_G \approx 0A$$

$$V_{RG} = I_G R_G = (0) \times (R_G) = 0V$$

$$\boxed{V_{RG} = 0V}$$

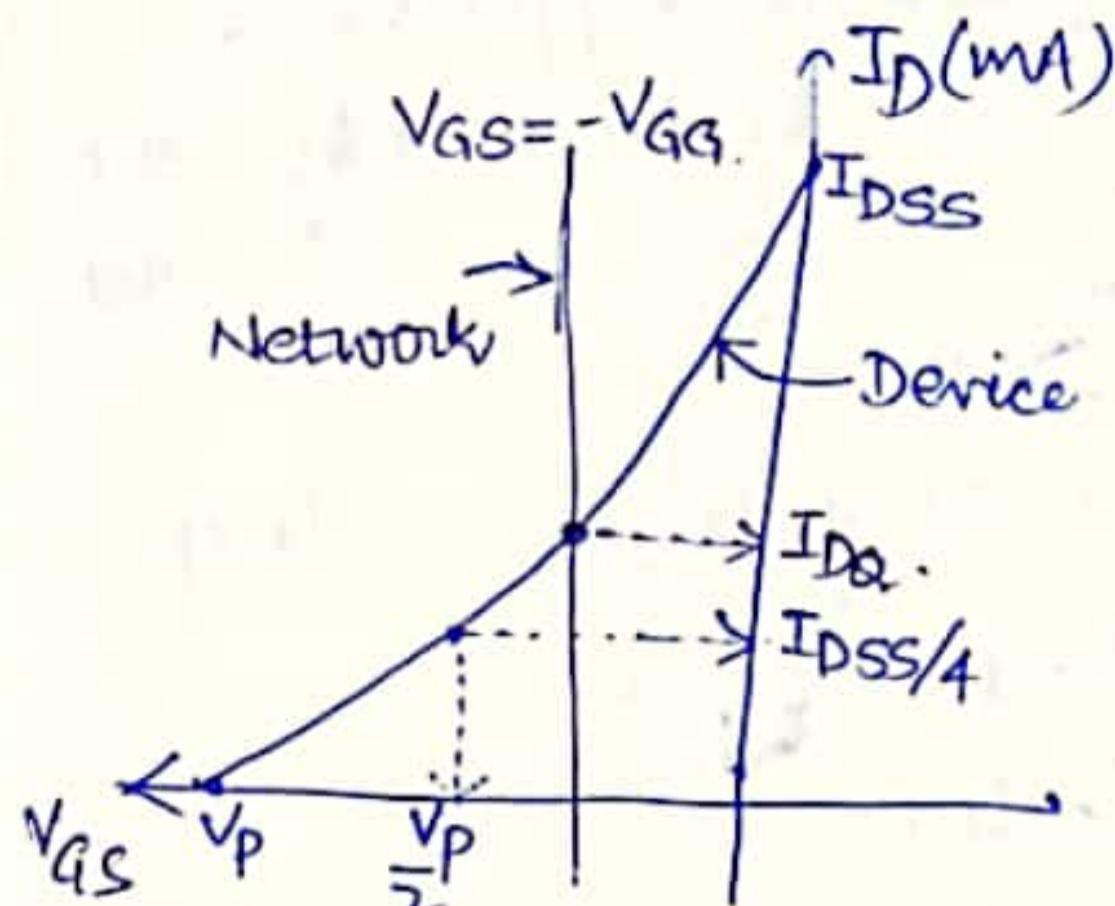
KVL in gate-source loop,

$$-V_{GG} - I_G R_G - V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$

$V_{GG}$  is fixed dc supply, the  $V_{GS}$  is fixed in mag. hence it is fixed bias config.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

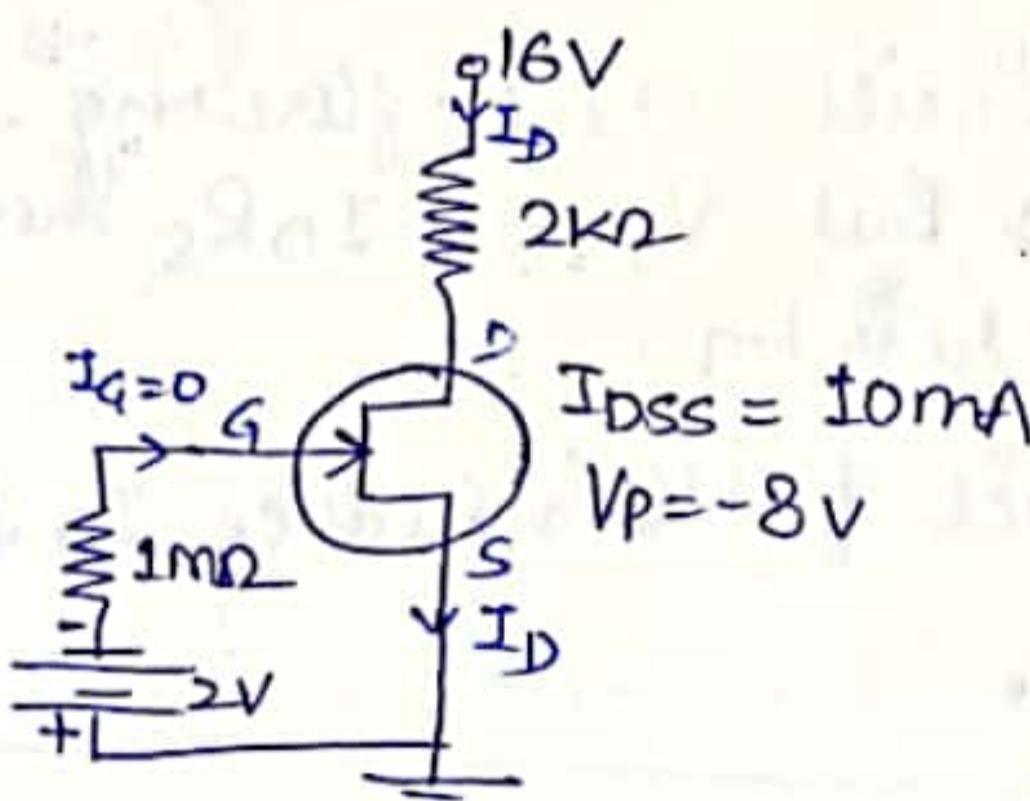


$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

Ques. Determine the following for given network.

- a)  $V_{GSQ}$
- b)  $I_{DQ}$
- c)  $V_{DS}$
- d)  $V_D$
- e)  $V_G$
- f)  $V_S$



Soln :-

$$V_{GS} = -2V$$

$$V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$\Rightarrow V_G - 0 = -2V$$

$$V_G = -2V$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10 \times 10^{-3} \left(1 - \frac{-2}{-8}\right)^2$$

$$I_{DQ} = 5.625 \text{ mA}$$

$$V_D = 16 - 5.625 \times 2$$

$$V_D = 4.75 \text{ V}$$

$$V_{DS} = V_D - V_S$$

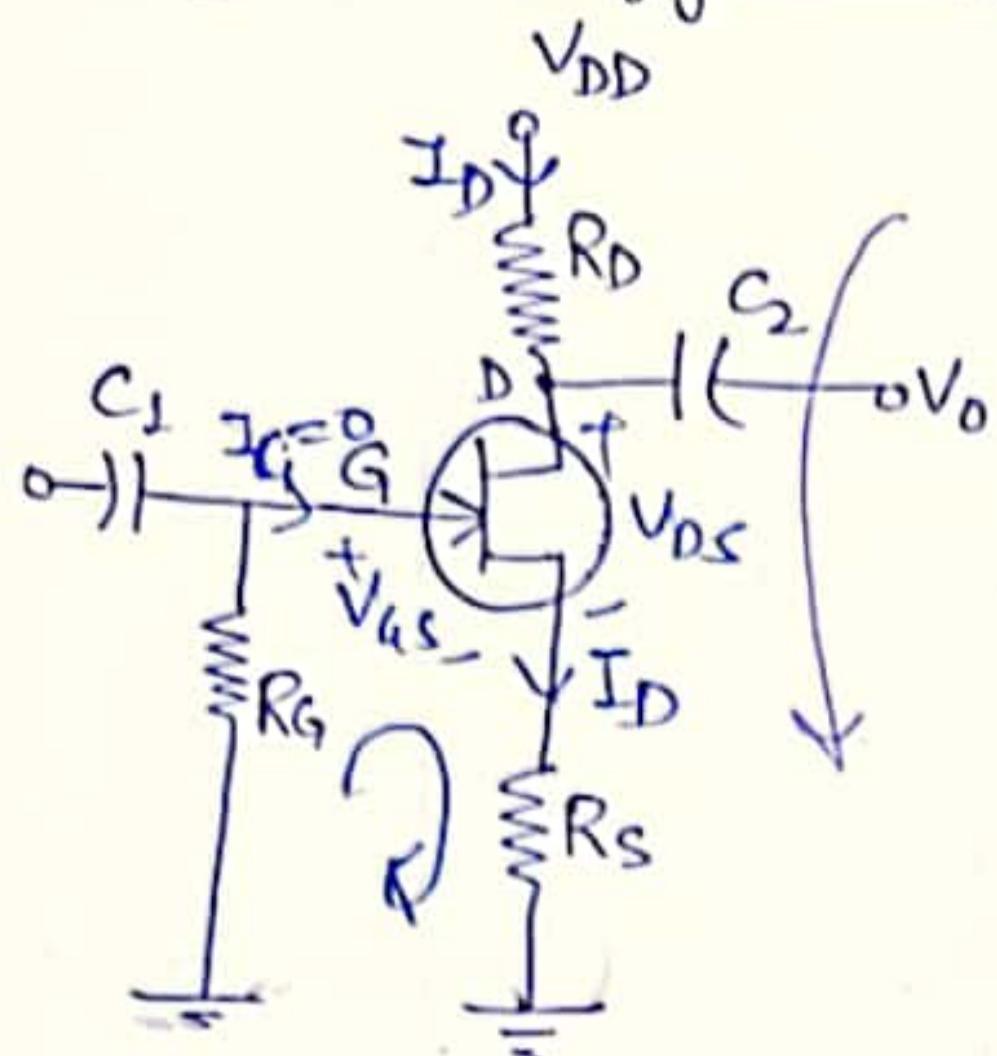
$$= 4.75 - 0 = 4.75 \text{ V}$$

$$V_{DS} = 4.75 \text{ V}$$

$$V_{DD} = 20 \text{ V}$$

$$V_{PP-EE-S} = 25 \text{ V}$$

## Self-bias configuration:-



The self bias configuration eliminates the need of two dc supplies.

$$I_{G_1} = 0$$

apply KVL at gate-source loop.

$$V_{GS} + I_D R_S = 0$$

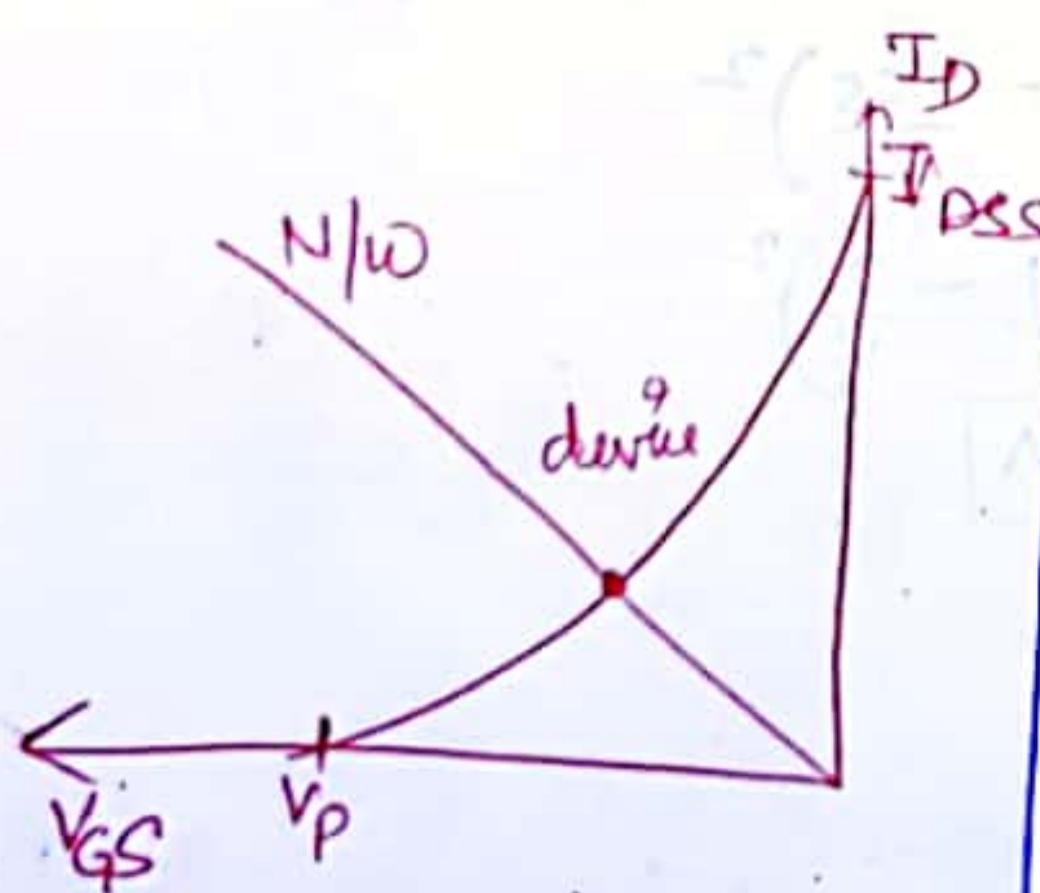
apply KVL at Drain to source loop.

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

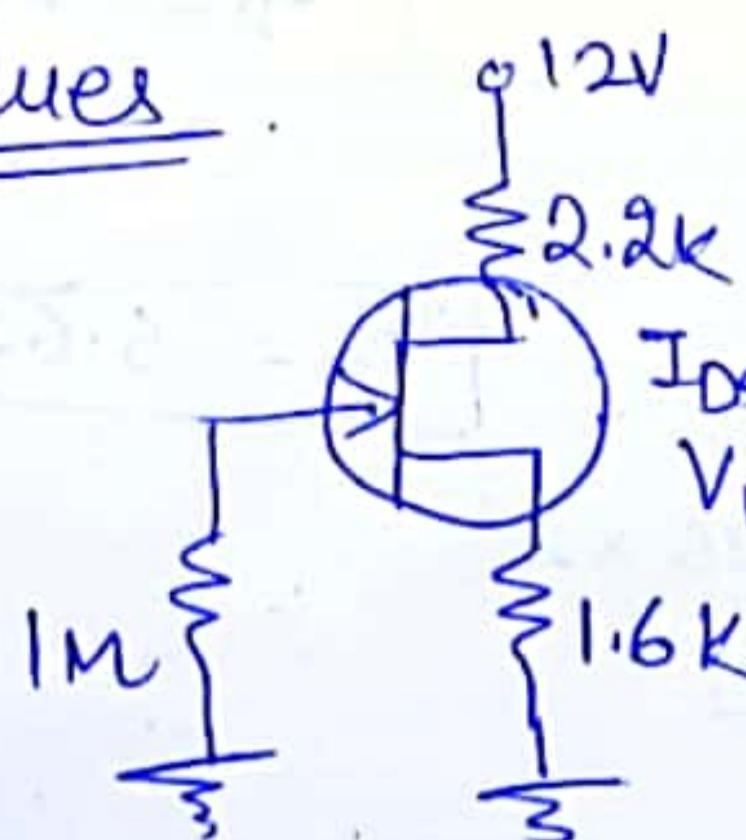
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Gate terminal connected to ground through  $R_G$  resistor  
and drain terminal is " " " ,  $R_S$  " .

$I_D \uparrow$   $V_{RS} \uparrow$   $V_{GS} \downarrow$  which further reduce  $I_D \downarrow$   
 Now reverse action takes place.



## Ques



find  
 $I_D$ ,  $V_{DS}$   
&  $V_{GS}$

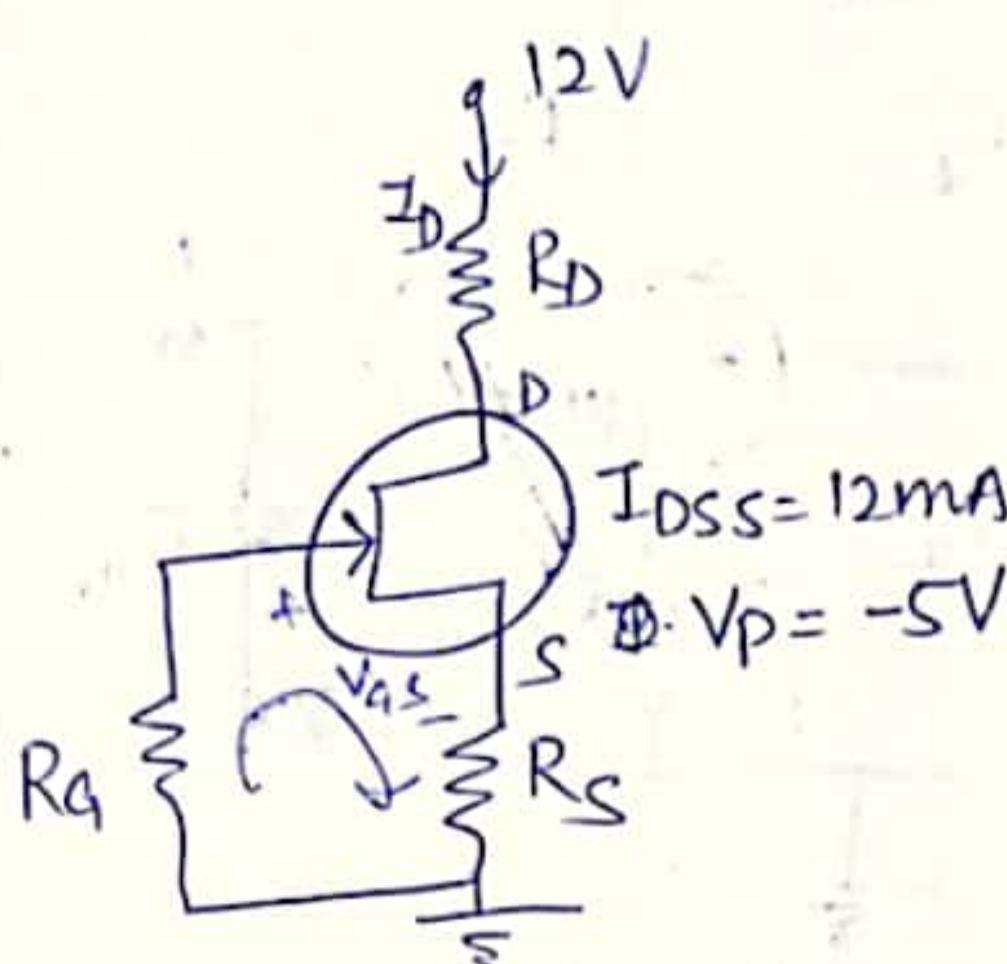
Ans

$$I_D = 1.73 \text{ mA}$$

$$V_{DS} = 5.41V$$

$$V_{GS} = -2.7744 \text{ V}$$

Ques For a self biased circuit  $V_P = -5V$ ,  $I_{DSS} = 12mA$ ,  $V_{DS} = 6V$ .  
 $V_{DD} = 12V$  Supply 12V. Find  $R_D$  &  $R_S$ .  $I_D = 5mA$



$$12 - I_D(R_D + R_S) - V_{DS} = 0 \quad (1)$$

$$I_D = I_{DSS} \left( 1 + \frac{V_{GS}}{V_P} \right)^2$$

$$5m = 12m \left( 1 + \frac{V_{GS}}{5} \right)^2$$

$$\sqrt{\left(\frac{5}{12}\right)} = \left(1 + \frac{V_{GS}}{5}\right)$$

$$0.645 = 1 + \frac{V_{GS}}{5}$$

$$\frac{V_{GS}}{5} = -0.354$$

$$\boxed{V_{GS} = -1.77V}$$

Put all values in eq "1"

$$V_{DS} = 6V$$

$$R_S = 354\Omega$$

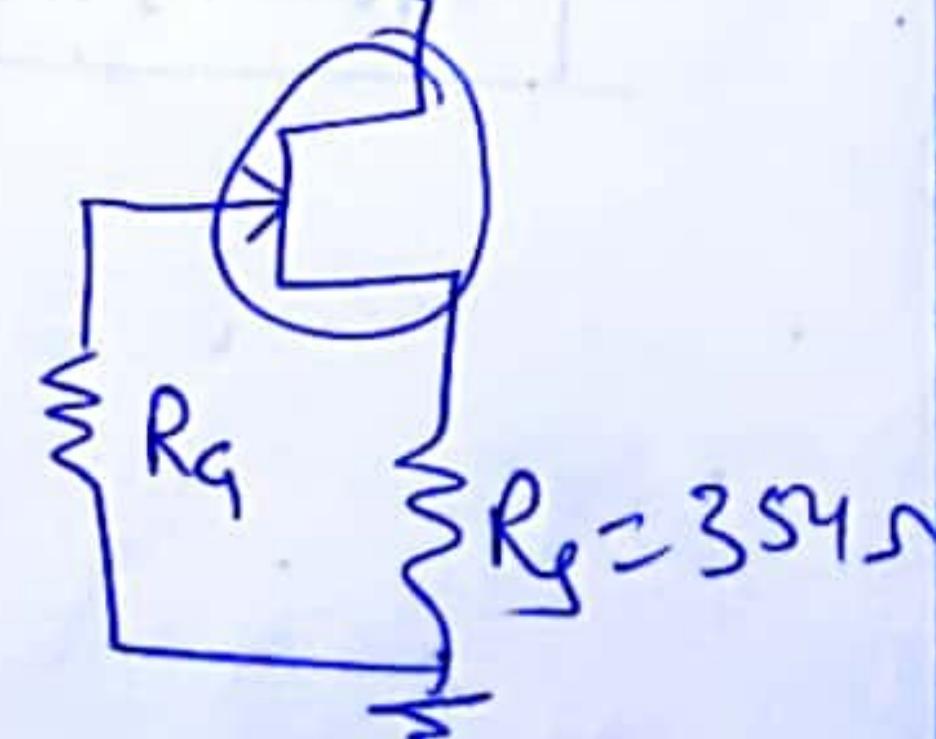
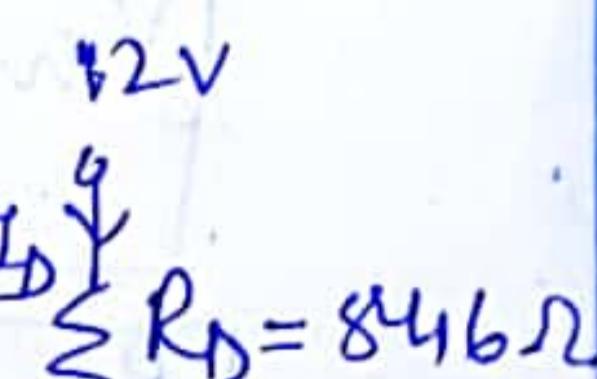
$$I_D = 5mA$$

$$12 - 5m(354 + R_D) - 6 = 0$$

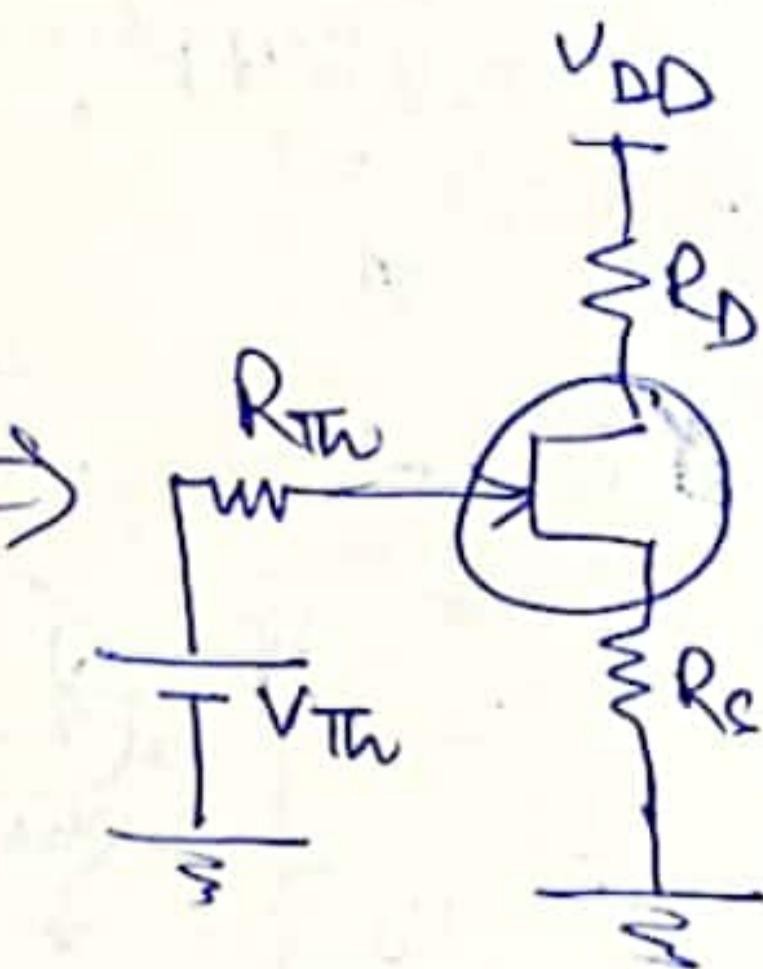
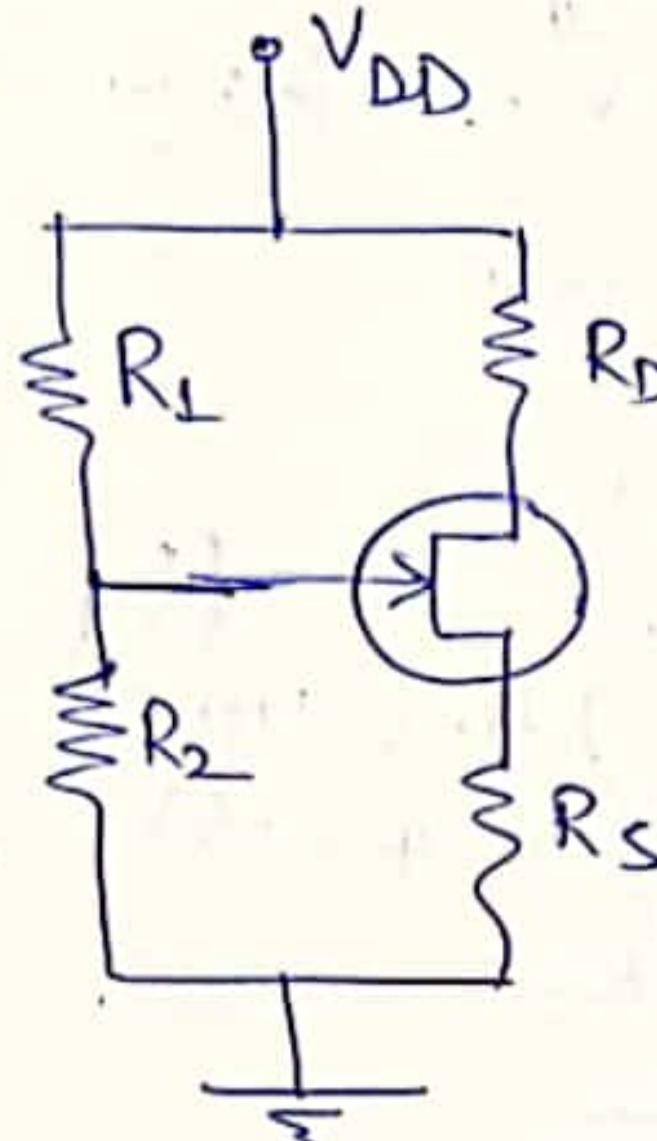
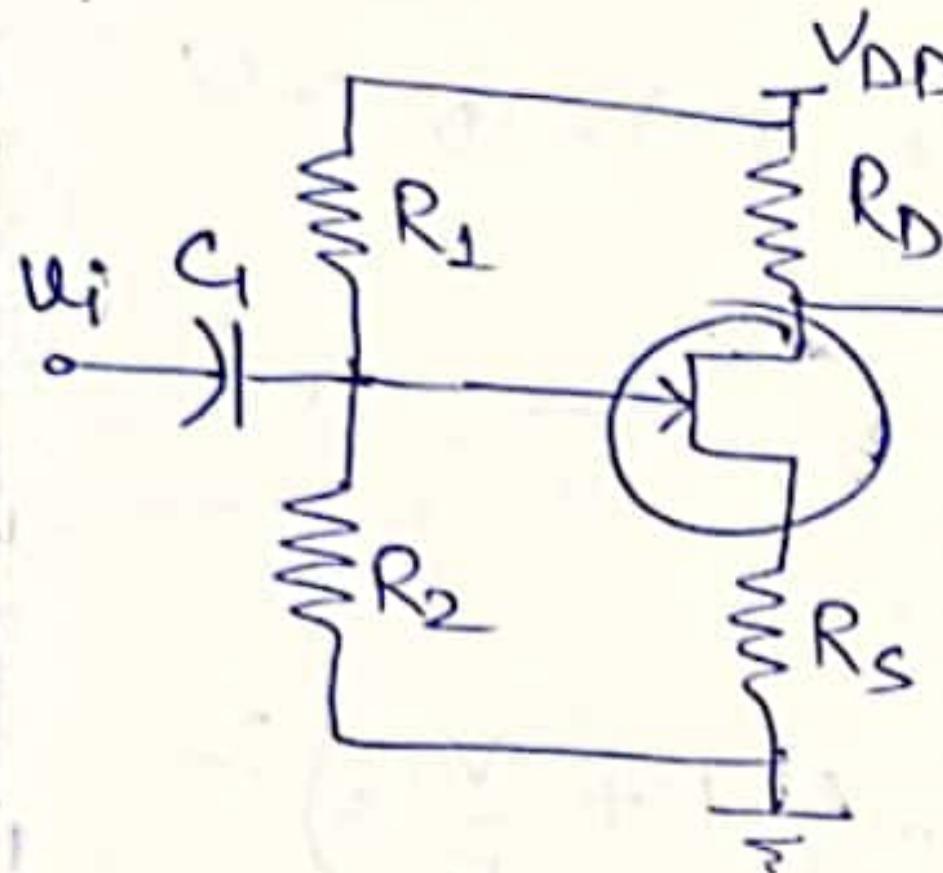
$$354 + R_D = \frac{6}{5} K$$

$$R_D = 1200 - 354$$

$$\boxed{R_D = 846\Omega}$$



## Voltage divider biasing



apply KVL from drain to source

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$I_S = I_D$$

$$\boxed{V_{DD} - I_D (R_D + R_S) - V_{DS} = 0} \quad (1)$$

at Gate to Source

$$V_{Th} - I_G R_{Th} - V_{GS} - I_D R_S = 0$$

$$I_G = 0$$

$$\boxed{V_{Th} - I_D R_S = V_{GS}} \quad (2)$$

Shockley's eq"

$$\boxed{I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2} \quad (3)$$

$$\boxed{V_{Th} = \frac{R_2 V_{DD}}{R_1 + R_2}} \quad (5)$$

$$\boxed{R_{Th} = R_1 \parallel R_2} \quad (6)$$

Ques Determine following for given network

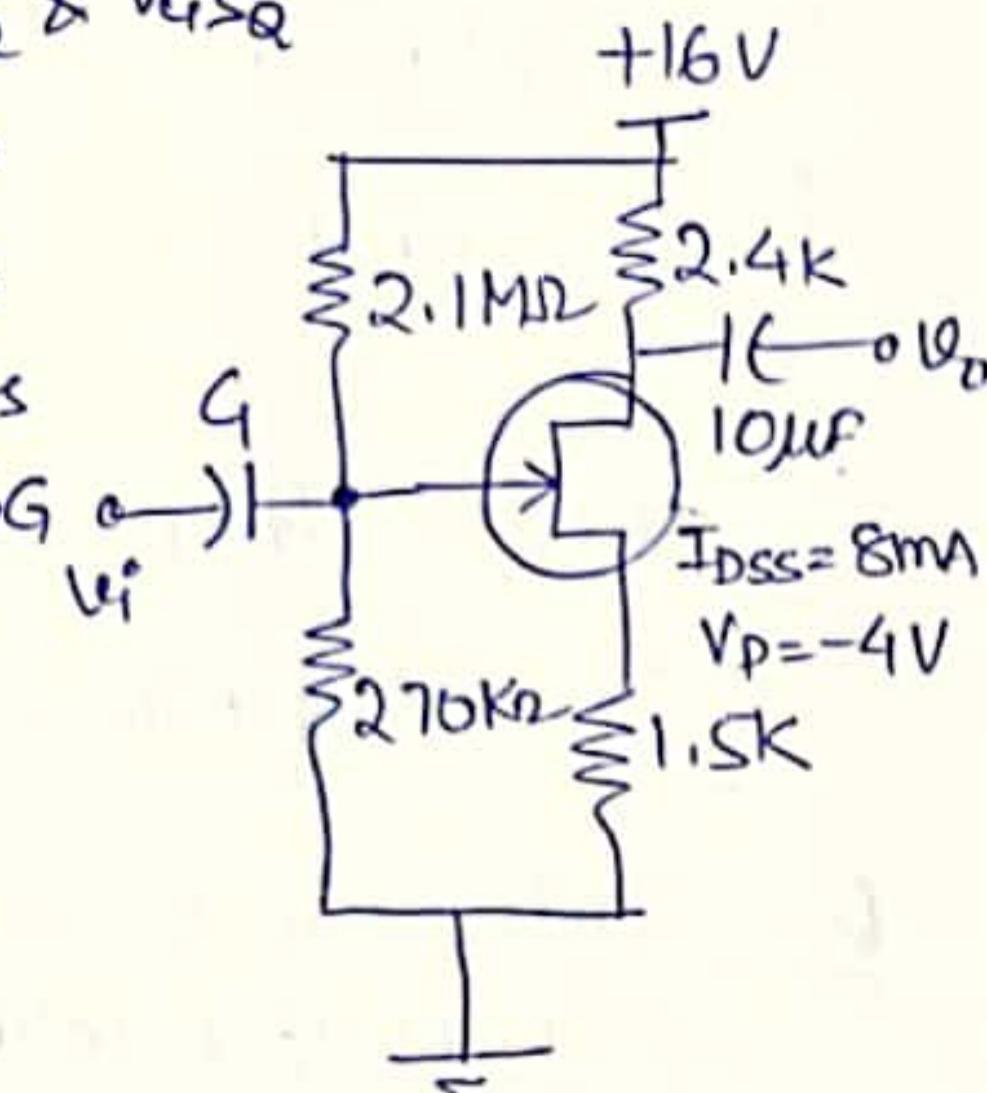
a)  $I_D$  &  $V_{GSQ}$

b)  $V_D$

c)  $V_S$

d)  $V_{DS}$

e)  $V_{DG}$



$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 8m \left(1 + \frac{1.82 - 1.5KID}{4}\right)^2$$

$$ID = \frac{8m}{162} (5.82 - 1.5KID)^2$$

$$2KID = (5.82 - 1.5KID)^2$$

$$2.25MID^2 + 33.87$$

$$-17.46KID - 2KID = 0$$

$$2.22MID^2 + 33.87 - 19.42KID = 0$$

$$ID = \frac{19.42K - \sqrt{(19.42)^2 - 4 \times 2.22M \times 33.87}}{2 \times 2.22M}$$

$$ID = 2.42mA$$

$$V_{GS} = 1.82 - 2.42 \times 1.5$$

$$\boxed{V_{GS} = -1.81V}$$

$$V_S = ID \times R_S$$

$$= 2.42mA \times 1.5K$$

$$\boxed{V_S = 3.63V}$$

apply KVL at Drain to Source loop,

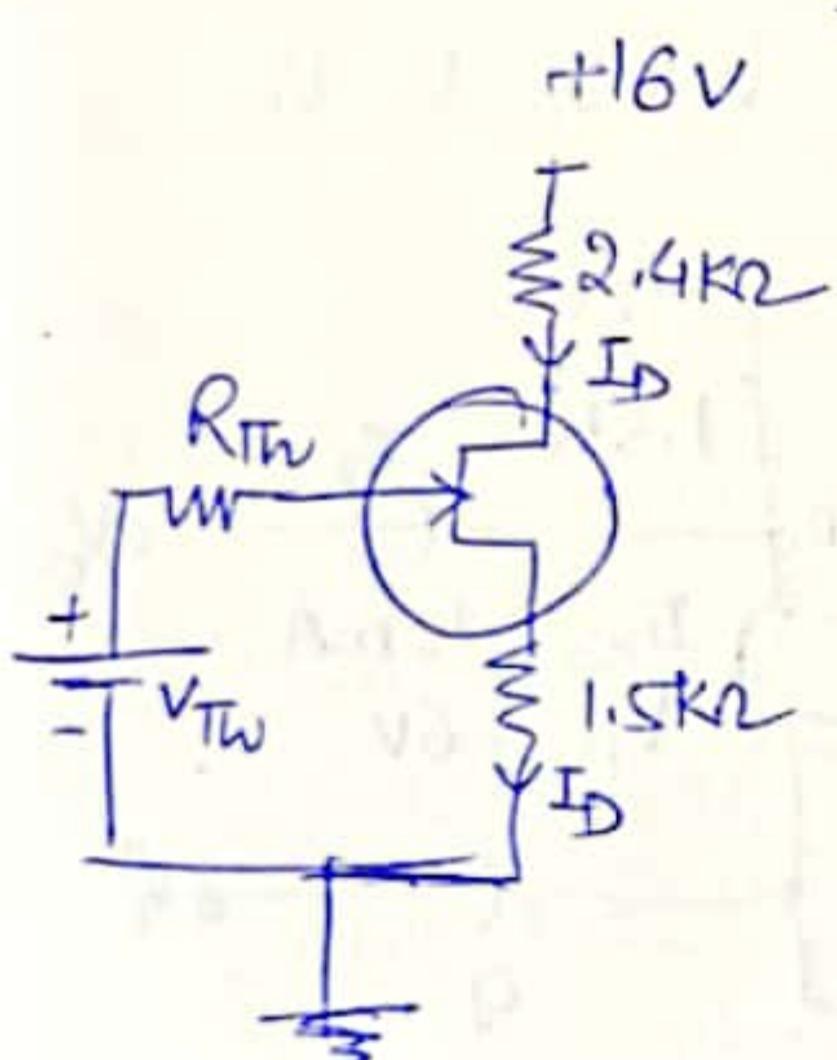
$$16 - (2.4 + 1.5)ID - V_{DS} = 0$$

$$V_{DS} = 16 - 3.9 \times 2.42$$

$$\boxed{V_{DS} = 6.56V}$$

$$\boxed{V_D = 2.93V}$$

$$\frac{V_{DG} = 2.93 - 1.82}{M_{DG} = 1.11V}$$



$$V_{Th} = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{270 \times 16}{(2100 + 270)} K$$

$$V_{Th} = \frac{4320}{2370} = 1.822V$$

$$\boxed{V_{Th} = 1.822V}$$

apply KVL at gate source loop,

$$V_{Th} - V_{GS} - ID R_S = 0$$

$$1.82 - V_{GS} - ID \times 1.5K = 0$$

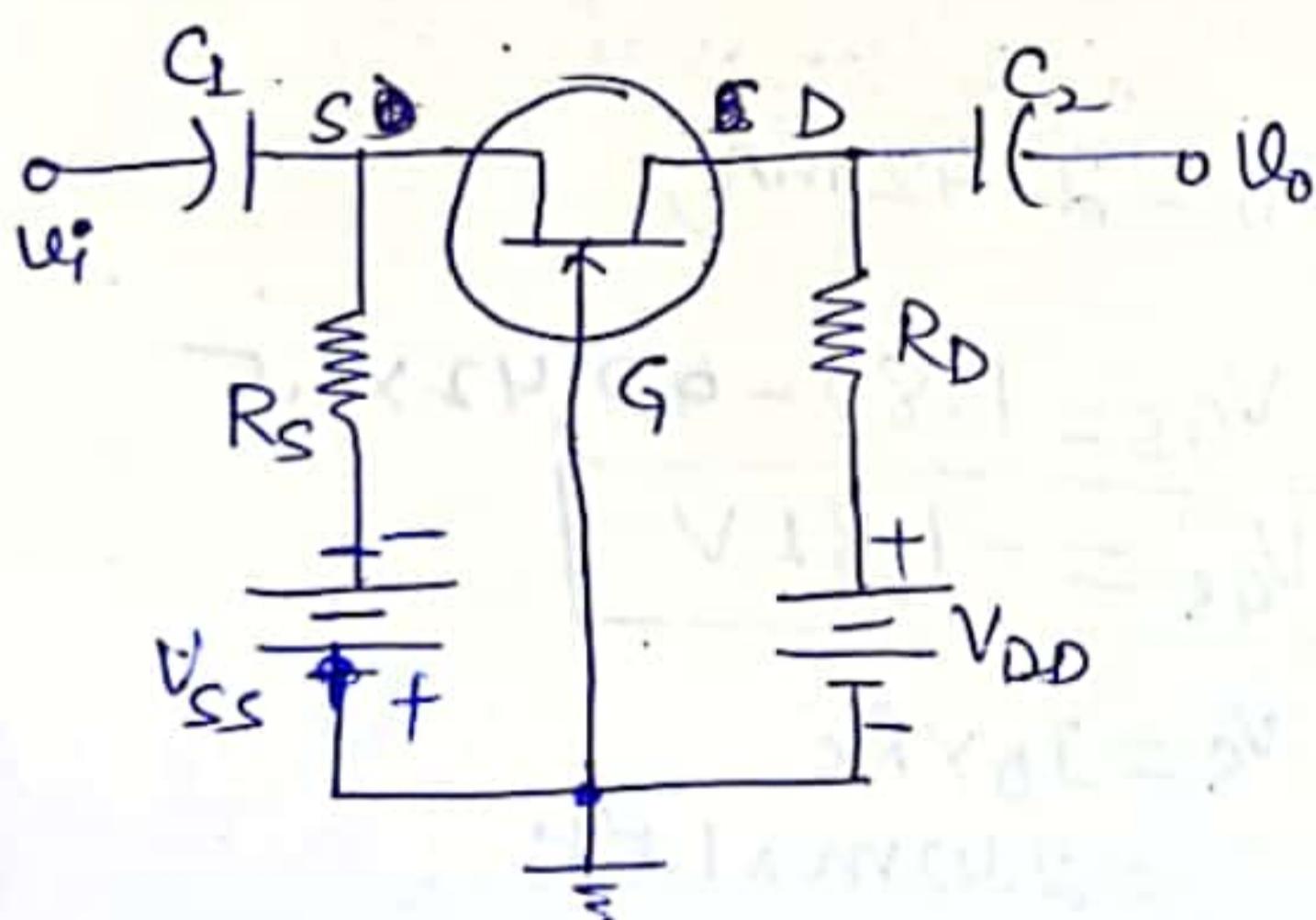
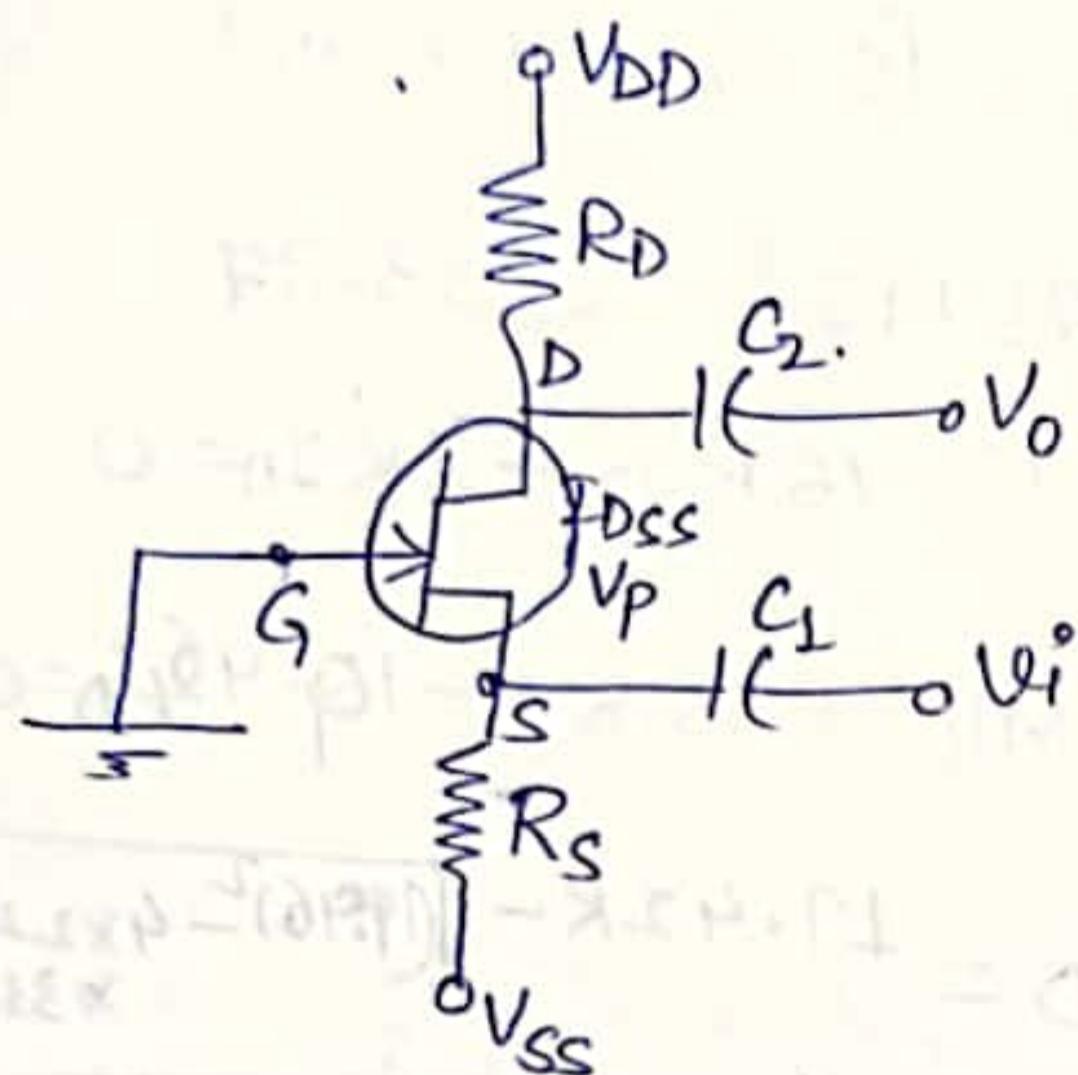
$$V_{GS} = 1.82 - ID \times 1.5K$$

## Common Gate Configuration

In this configuration, gate terminal is grounded.

I/P → source terminal

O/P → ~~Gate~~ Drain-terminal



$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_D R_S$$

~~VDS~~

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

apply KVL to drain to gate loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S - V_{SS} = 0$$

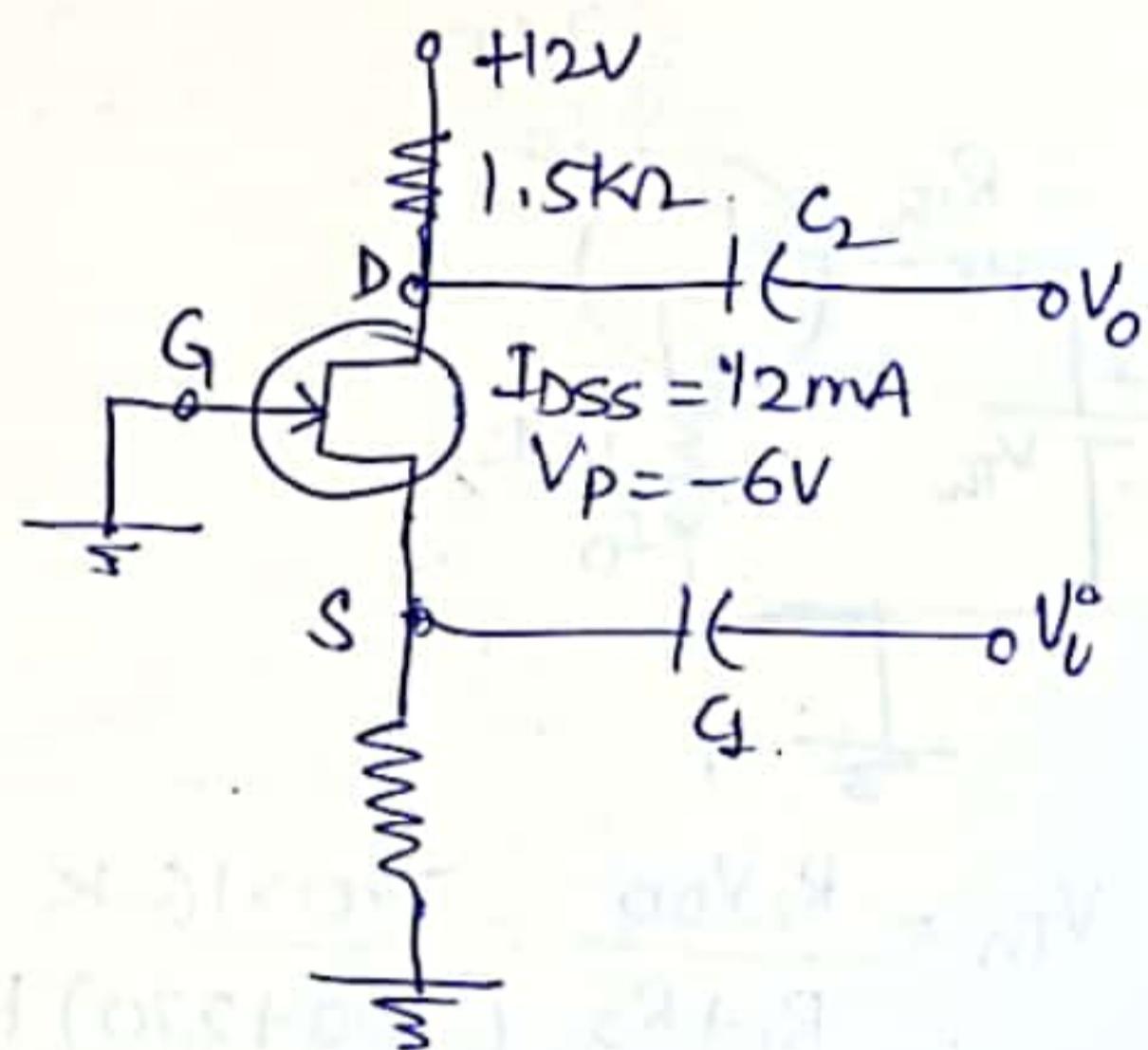
$$V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = -V_{SS} + I_D R_S$$

Ques Determine the following in CG configuration.

$$V_{GS}, I_{DQ}, V_D, V_G, V_S, V_{DS}$$



$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = 3.8 \text{ mA}$$

$$V_{GS} = -2.6 \text{ V}$$

$$V_{DS} = 3.7$$

$$V_D = V_{DD} - I_D R_D \\ = 12 - 3.8 \times 1.5$$

$$V_D = 6.3 \text{ V}$$

$$V_G = 0 \text{ V}$$

$$V_S = I_D R_S \\ V_S = 2.58 \text{ V}$$

## Parameters of JFET:-

### 1) ac Drain or dynamic drain Gate resistance

It is a ratio of change in drain to source voltage w.r.t Change in drain current when  $V_{GS}$  is constant.

$$R_d = \frac{\Delta V_{ds}}{\Delta I_d} \quad \text{at } V_{GS} = \text{constant}$$

### 2) Transconductance ( $g_m$ )

It is a ratio of change in drain current w.r.t change in gate to source voltage when change in  $V_{de}$  is constant.

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}} \quad \text{at } \Delta V_{ds} \rightarrow \text{constant}$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

### 3) Amplification Factor ( $\mu$ ):-

It is the ratio of change in drain to source voltage w.r.t gate to source voltage when Change in drain current is constant.

$$g_m = \frac{\Delta V_{ds}}{\Delta V_{GS}} \quad \Delta I_d \rightarrow \text{constant}$$

$$\mu = g_m \times R_d$$

Prove that  $g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = -2 \frac{I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right) \quad \text{--- (1)}$$

but  $g_m = \cdot$  at  $V_{GS} = 0$

$$g_m = g_{m0} = -2 \frac{I_{DSS}}{V_p}$$

$\therefore$  eq<sup>n</sup> can be written as,

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

Question ① If an N-channel JFET has  $I_{DSS} = 20 \text{ mA}$  &  $V_p = -8 \text{ V}$  &  $g_{m0} = 5000 \mu\text{s}$ . Then find  $I_D$  & transconductance at  $V_{GS} = -4 \text{ V}$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 20 \text{ m} \left(1 - \frac{-4}{-8}\right)^2 \Rightarrow 20 \times \frac{1}{4}$$

$$I_D = 5 \text{ mA}$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

$$= 5000 \mu \left(1 - \frac{1}{2}\right) \Rightarrow 2500 \mu\text{s}$$

$$g_m = 2500 \mu\text{s}$$

$$9V - 2V = 7V$$

$$(2+2)- = 2V$$

$$V_E =$$

$$V_E = 2m 2V$$

>Show that if  $|V_{GS}| \ll |V_P|$   
then  $I_D = I_{DSS} - g_m V_{GS}$

Soln:-

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = I_{DSS} \left[ 1 - 2 \frac{V_{GS}}{V_P} + \left( \frac{V_{GS}}{V_P} \right)^2 \right]$$

$\because |V_{GS}| \ll |V_P|$

$$\therefore I_D = I_{DSS} \left[ 1 - 2 \frac{V_{GS}}{V_P} \right]$$

$$I_D = I_{DSS} - 2 I_{DSS} \frac{V_{GS}}{V_P}$$

we know that  $V_{GS} = -2V$

$$g_m = -\frac{2 I_{DSS}}{V_P}$$

$$\therefore I_D = I_{DSS} + g_m V_{GS}$$

(Proved)

Q3) For n-channel JFET,  
if  $I_{DSS} = 1.55 \text{ mA}$ ,  $V_P = -2V$ .  
find  $V_{DSmin}^2$  &  $I_D$  for  $V_{GS} = -2V$ .

Soln

$$V_{GS} = -2V$$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$\boxed{I_D = 0.8 \text{ mA}}$$

$$V_{DSmin} = V_{GS} - V_P$$

(at pinchoff) = (-2) - (-5)

= 3V

$$\boxed{V_{DSmin} = 3V}$$

Q4)  $V_P = -2V$ ,  $I_{DSS} = 1.55 \text{ mA}$ . If  
 $I_D = 0.8 \text{ mA}$ ,  $V_{DD} = 24V$ .  
Find (i)  $V_{GS}$  (ii)  $g_m$

$$V_{GS} = V_P \left[ 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right]$$

$$V_{GS} = -2 \left[ 1 - \sqrt{\frac{0.8}{1.55}} \right]$$

$$\boxed{V_{GS} = -0.6074V}$$

$$g_m = -\frac{2 I_{DSS}}{V_P}$$

$$= -\frac{2 \times 1.55}{(-2)}$$

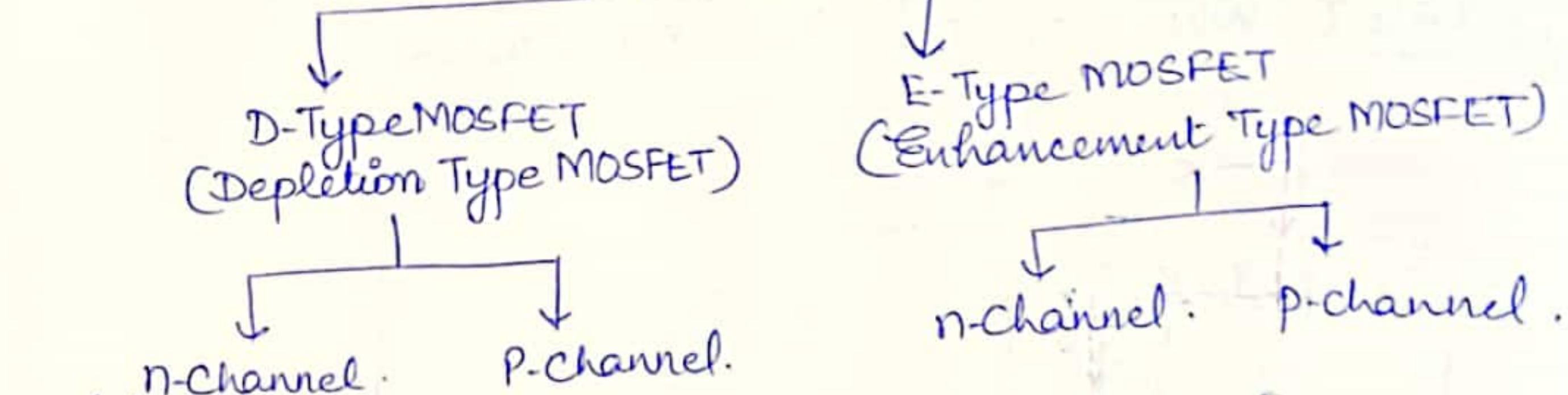
$$g_m = 1.55 \text{ m}$$

$$g_m = g_m \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$= 1.55 \left( 1 - \frac{-0.6074}{2} \right)$$

$$\boxed{g_m = 1.079 \text{ ms}}$$

## MOSFET (Metal Oxide Semiconductor FET) or IGFET (Insulated Gate FET)



### Depletion Type MOSFET

Basic Construction of n-channel depletion type MOSFET:-

- 1) A slab of p-type material is formed from a Si Base, which is referred as substrate.
- 2) In some cases source is connected with substrate.
- 3) It is four terminal device:
  - i) Drain(D)
  - ii) Source(S)
  - iii) Gate(G).
  - iv) Substrate(SS).

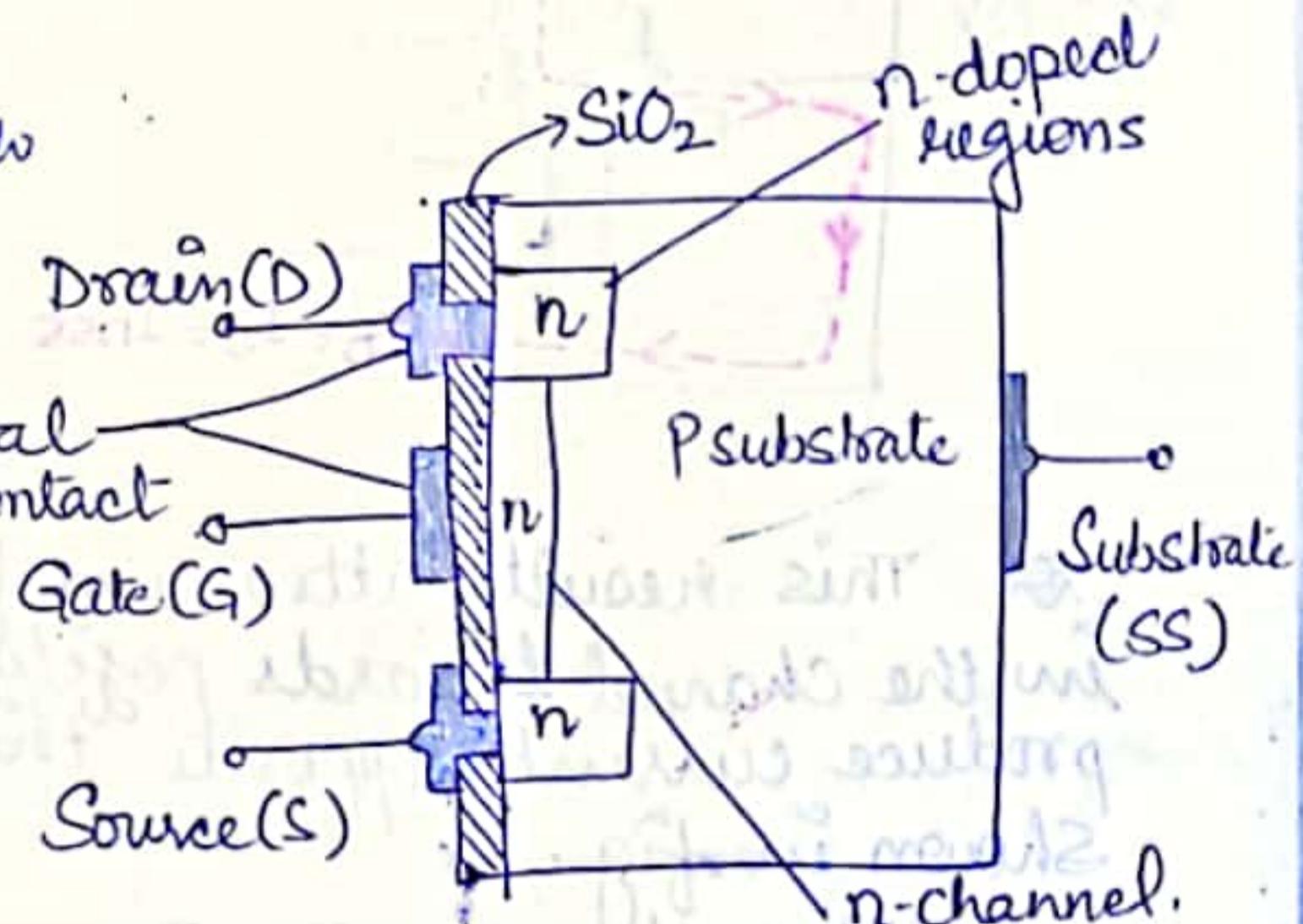
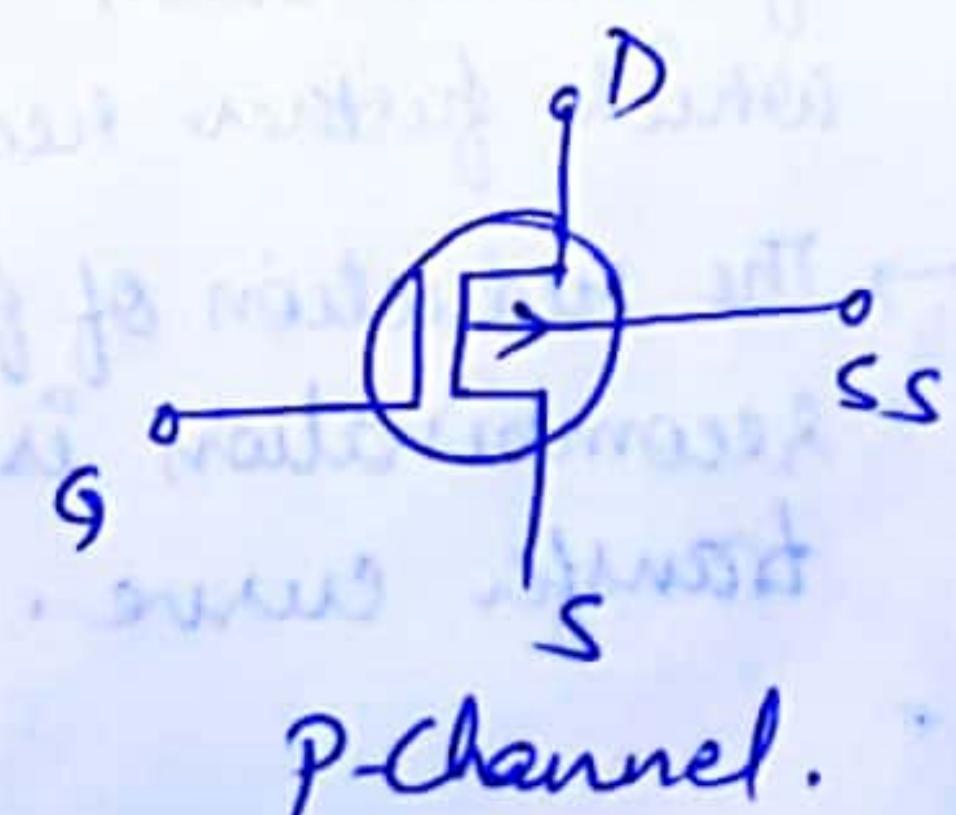
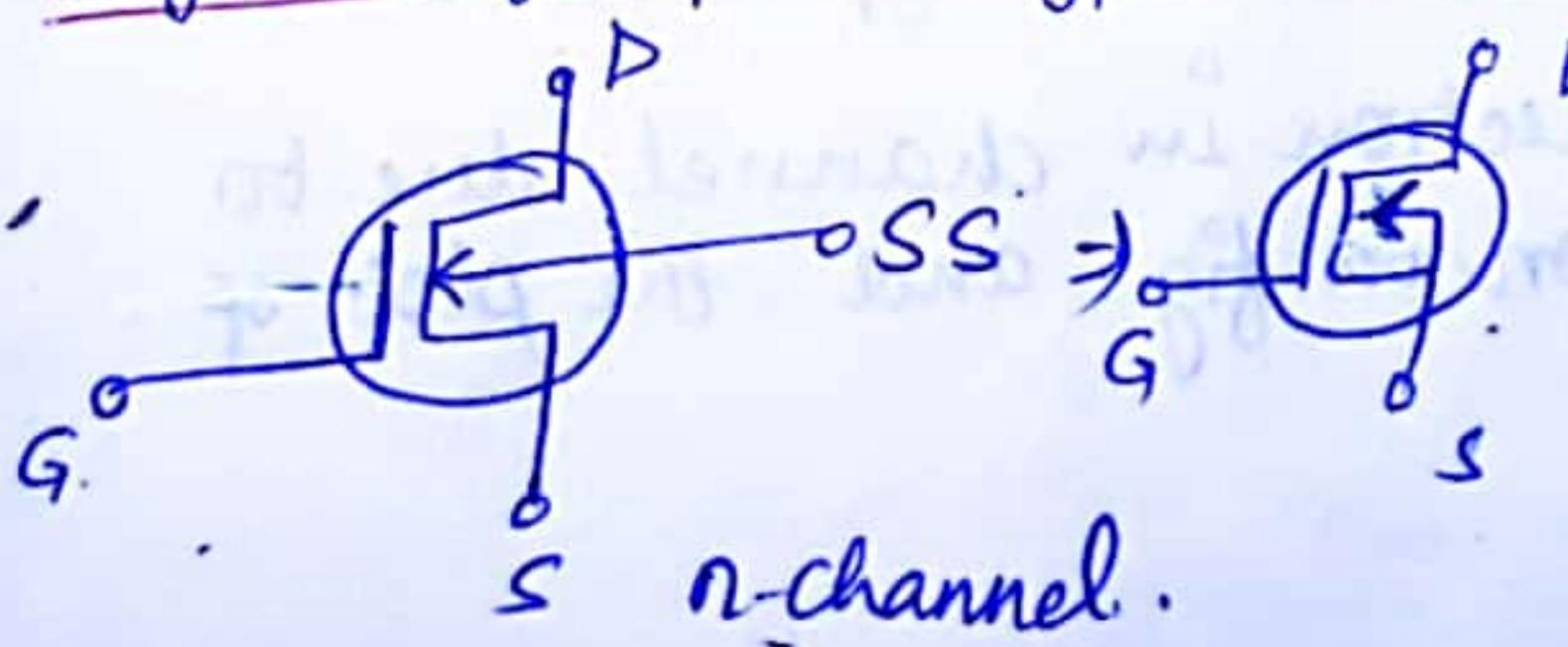


fig: n-channel Depletion type MOSFET Construction

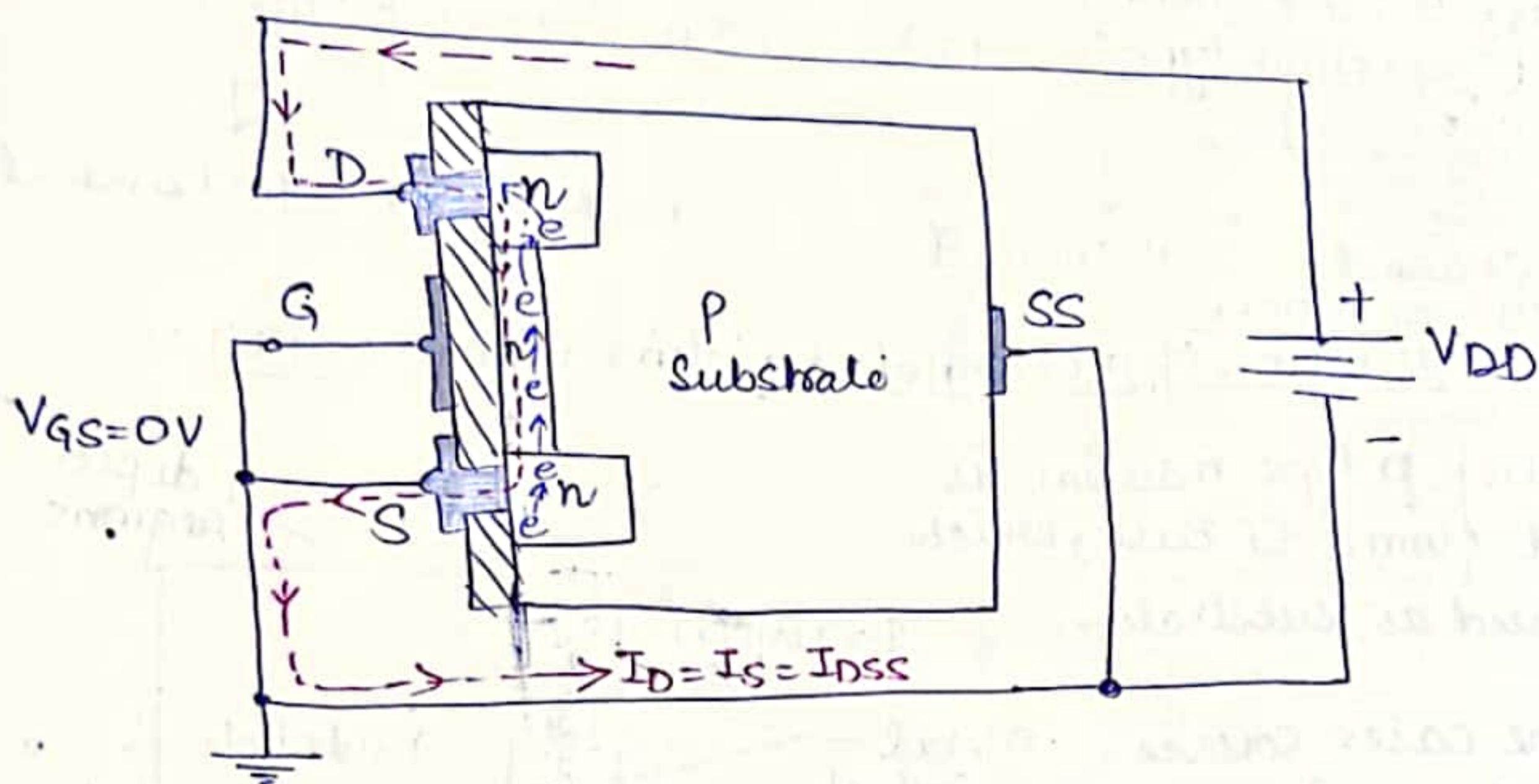
- 4) The drain & source are connected through metal contacts to n-doped regions.
- 5) Gate is also connected by metallic contact but insulated through  $\text{SiO}_2$  layer called as dielectric.
- 6) Due to the presence of  $\text{SiO}_2$  layer I/P impedance of D-type MOSFET is very high.  $|T_G| = 0$

### Symbol of depletion type MOSFET:-



## Basic operation of n-channel MOSFET (Working)

Case I When  $V_{GS} = 0$  &  $V_{DS} = V_{DD}$ ,  ~~$V_{SS} = 0$~~

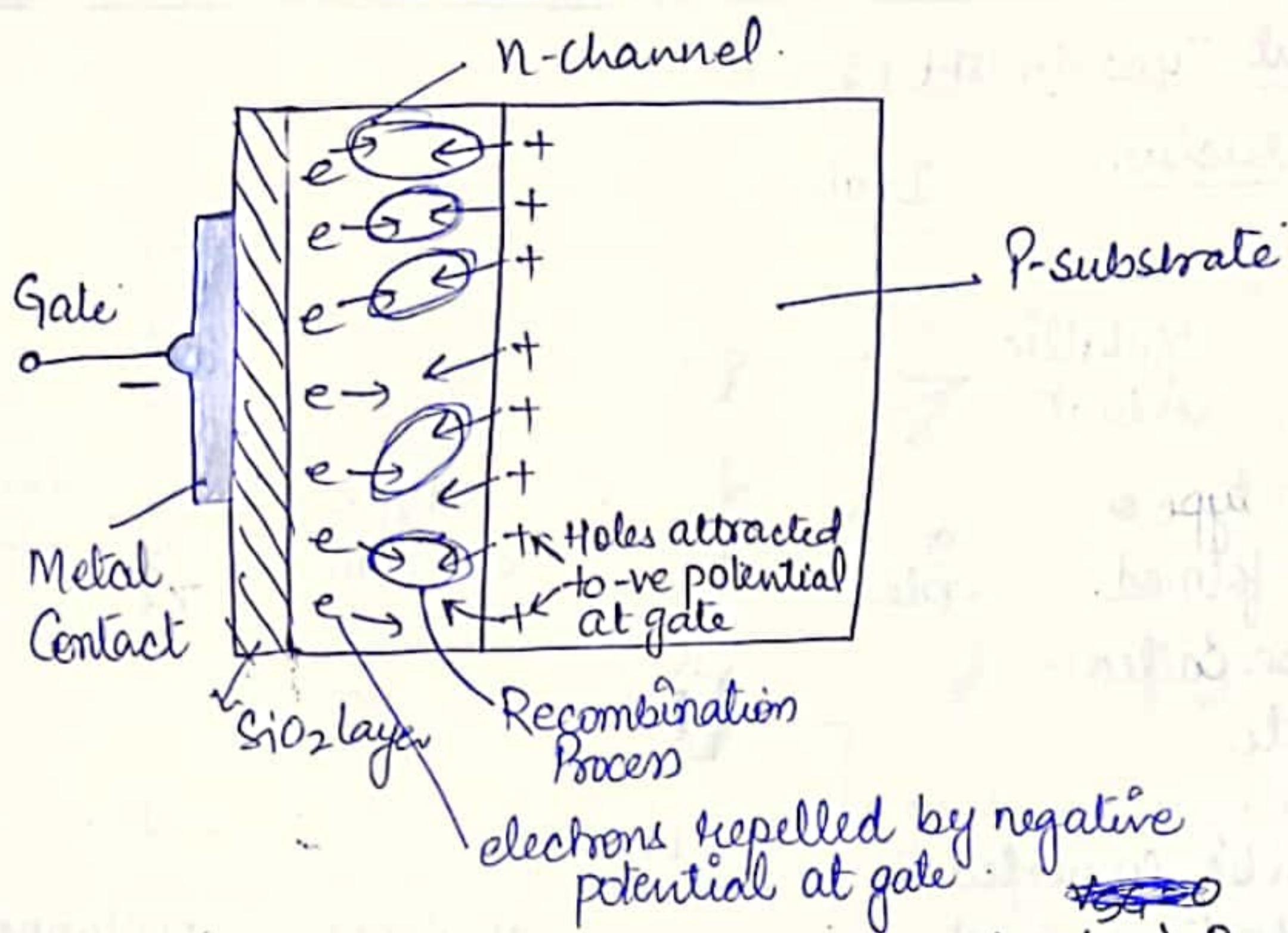


This result attraction force for free electrons present in the channel towards positive voltage at drain which produce current in opposite <sup>direction to</sup> the flow of electron. as shown in fig.

When  $V_{GS} = 0$ ,  $I_D = I_{DSS}$ .

Case 2:- Depletion Mode:-  $V_{GS} < 0V$ ,  $V_{DS} > 0V$   
(Negative) (Positive),  ~~$V_{SS} = 0$~~

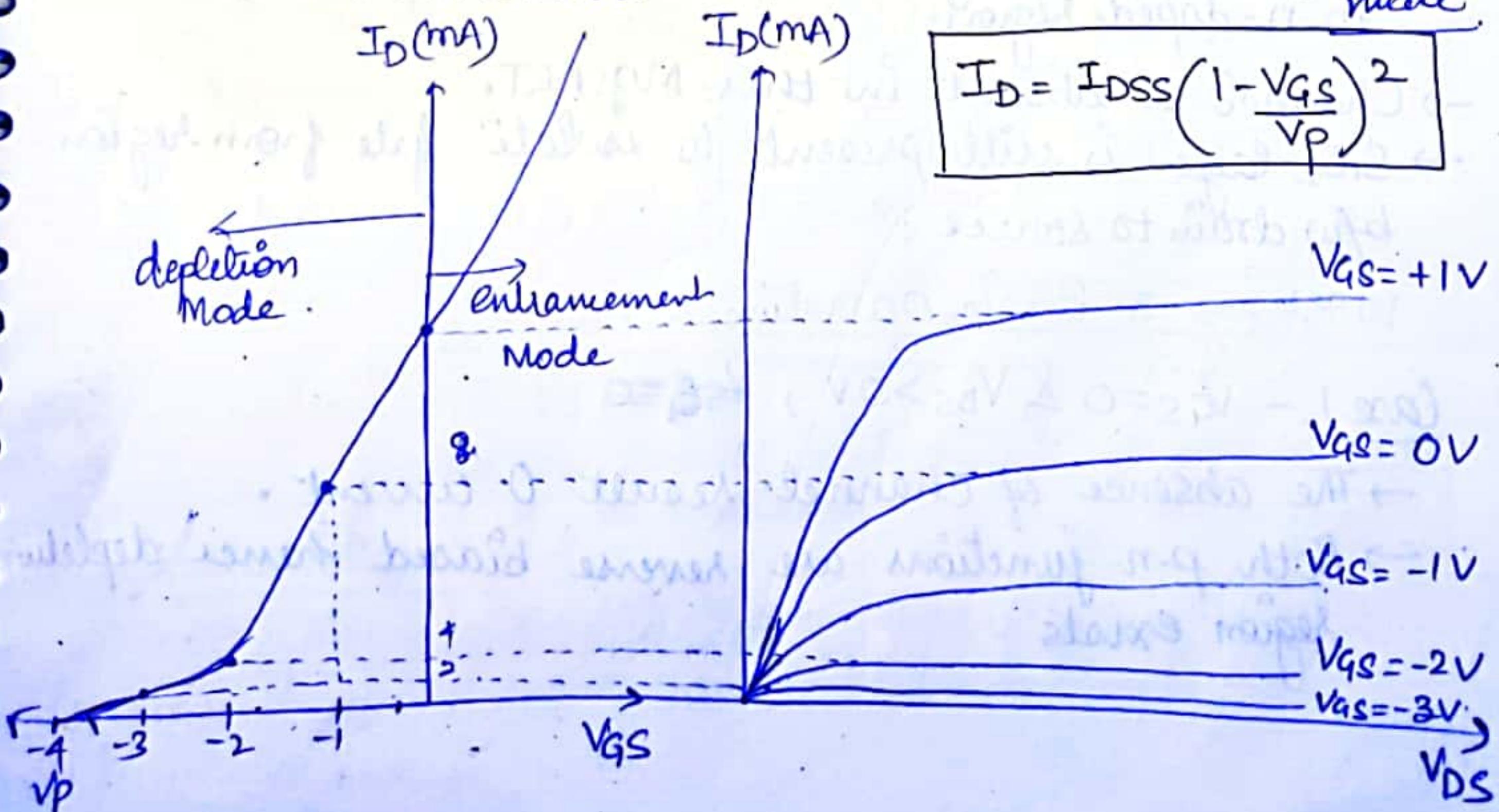
- The negative potential at gate will tend to pressure electrons towards p-substrate and attract holes of p-type substrate depending on the magnitude of  $V_{GS}$ .
- Due to increased negative biasing at  $V_{GS}$ , the level of recombination b/w electron & holes will increase which further reduce the number of electrons in channel.
- The reduction of free electron in channel due to recombination is shown in fig. and the plot of transfer curve.



~~Trans~~ Case 3: (Enhancement Mode)  $V_{GS} > 0, V_{DS} > 0.$

- Positive gate will draw additional electrons from substrate due to reverse leakage current and result new carriers through collisions b/w accelerating particles.
- Hence If  $V_{GS}$  increases then  $I_D$  will increase at rapid rate.

The application of +ve  $V_{GS}$  "enhance" the level of free carriers in channel hence this is called as enhancement mode.



## Enhancement Type MOSFET :-

### Basic Construction

→ A slab of p-type material is formed from Si base called as substrate.

→ Source can be connected with substrate in most of the cases.

→ Again this has four terminals

- i) Gate
- ii) Source
- iii) Drain
- iv) Substrate

→ Source & Drain regions are connected with metallic contact to n-doped region.

→ Channel is absent in this MOSFET.

→  $\text{SiO}_2$  layer is still present to isolate gate from region b/w drain to source.

### Working or Basic Operations

Case 1:-  $V_{GS} = 0$  &  $V_{DS} > 0V$ ,  ~~$V_G = 0$~~ .

→ The absence of channel result 0 current.

→ Both p-n junctions are reverse biased hence depletion region exists.

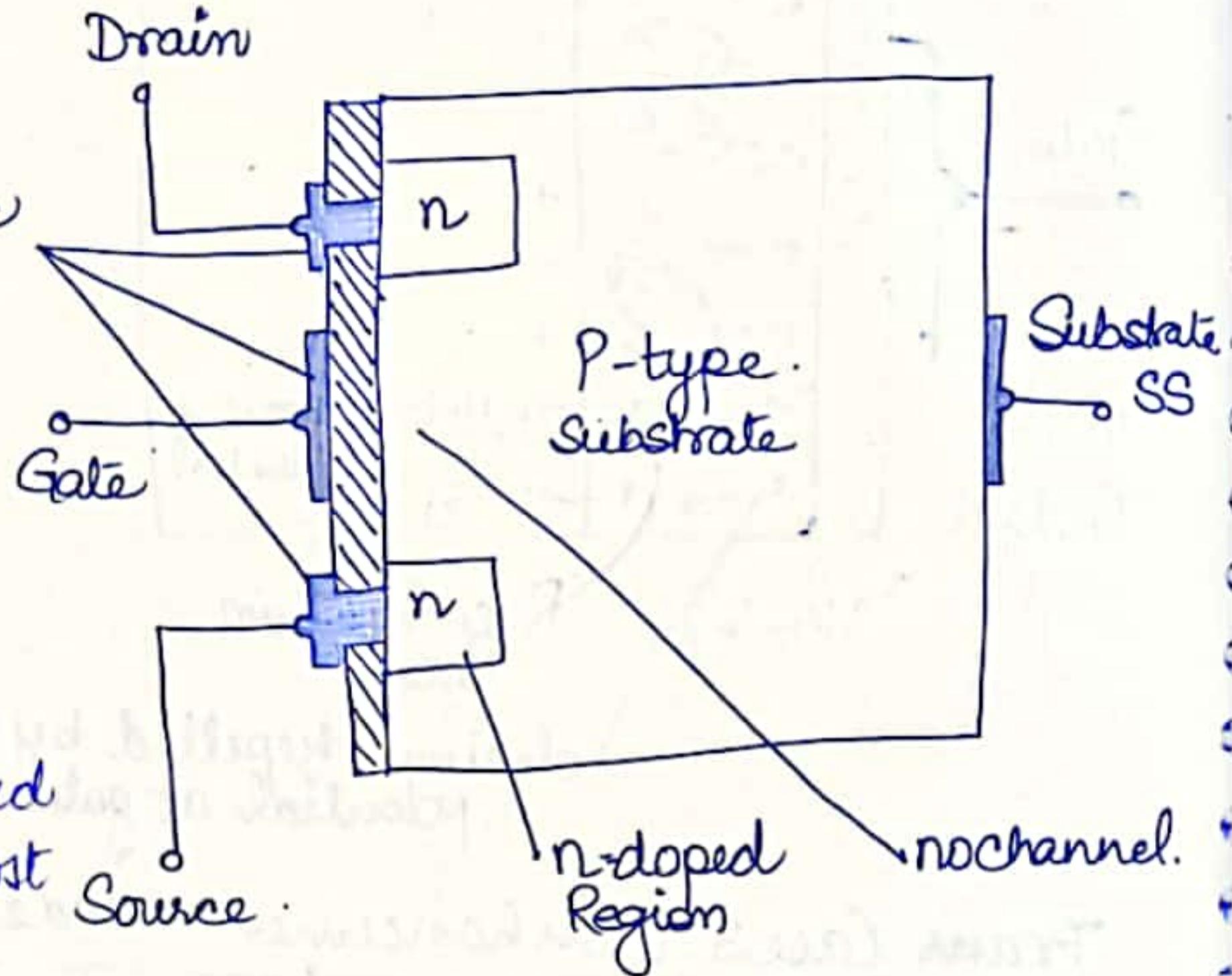


fig:- n-Channel Enhancement-Type MOSFET Construction

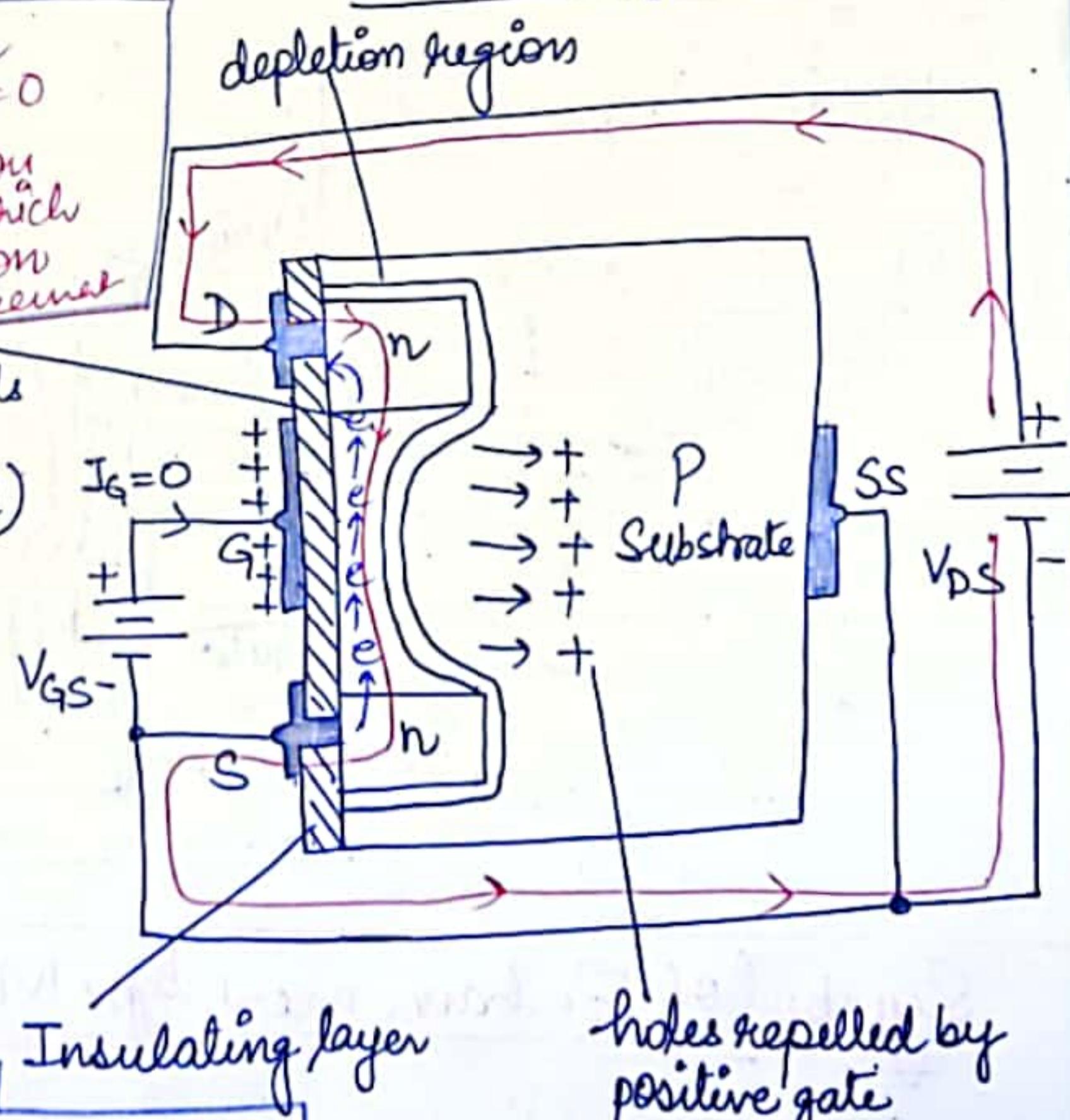
Case 2  $V_{DS} > 0V$ ,  $V_{GS} > 0V$ ,  ~~$V_{GS} = 0V$~~

- ① The positive potential at gate will pressure holes in the substrate along the edge of  $\text{SiO}_2$  layer to leave the area and enter into the deeper region of p-substrate.
- ② Hence electrons from p-substrate will accumulate at the region near the surface of  $\text{SiO}_2$  layer.
- ③ The  $\text{SiO}_2$  layer & its insulating quantity will prevent negative carriers from being absorbed at gate terminal.
- ④ As  $V_{GS} \uparrow$  the conc<sup>n</sup> of electron near  $\text{SiO}_2$  surface increases eventually until the induced n-region near can support measurable flow between drain & source.

This process is called as channel formation.

Note:- Since channel does not exist at  $V_{GS}=0$  & enhanced application of  $V_{GS}$  produce channel which further support conduction hence it is called as enhancement type MOSFET.

electron attracted towards positive gate  
(Induced channel)



Threshold Voltage:—

The value of  $V_{GS}$  at which  $I_D$  increases significantly is called as threshold voltage ( $V_{Th}$ ).

fig:- Channel Formation

Case 3 :- When  $V_{GS} > V_{Th}$  at certain constant value  
 $\text{Exp } V_{GS} = 8V$  &  $V_{DS}$  is raised from 2V to 5V.

$$\therefore V_{DG} = V_{DS} - V_{GS}$$

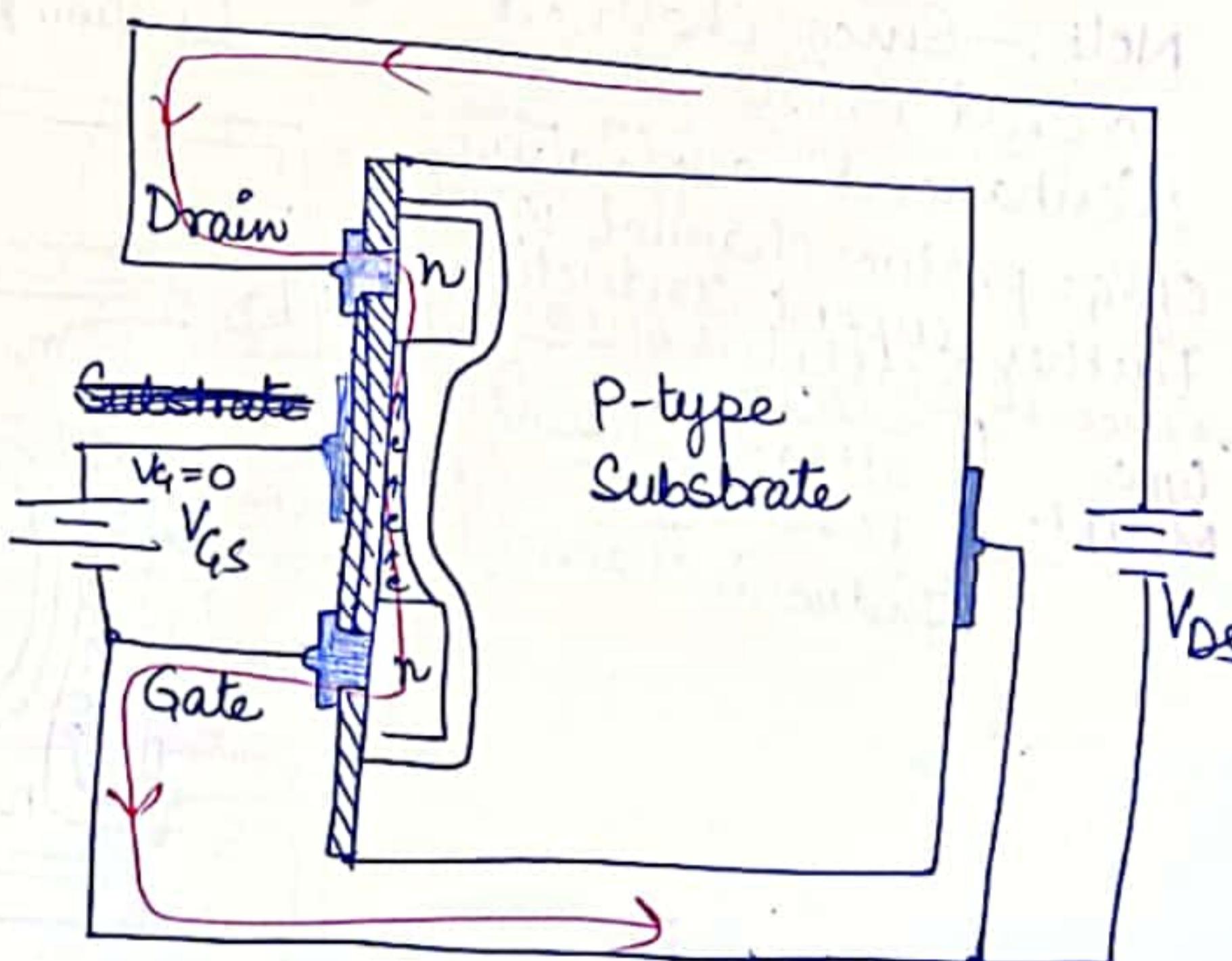
It will increase from -6V to -3V. The gate will become less positive w.r.t drain. The reduction in  $V_{GS}$  will reduce attraction force of electron to near drain side hence effective channel width will also decrease.

At certain point, Channel will reduced to pinch-off and saturation condition will be established.

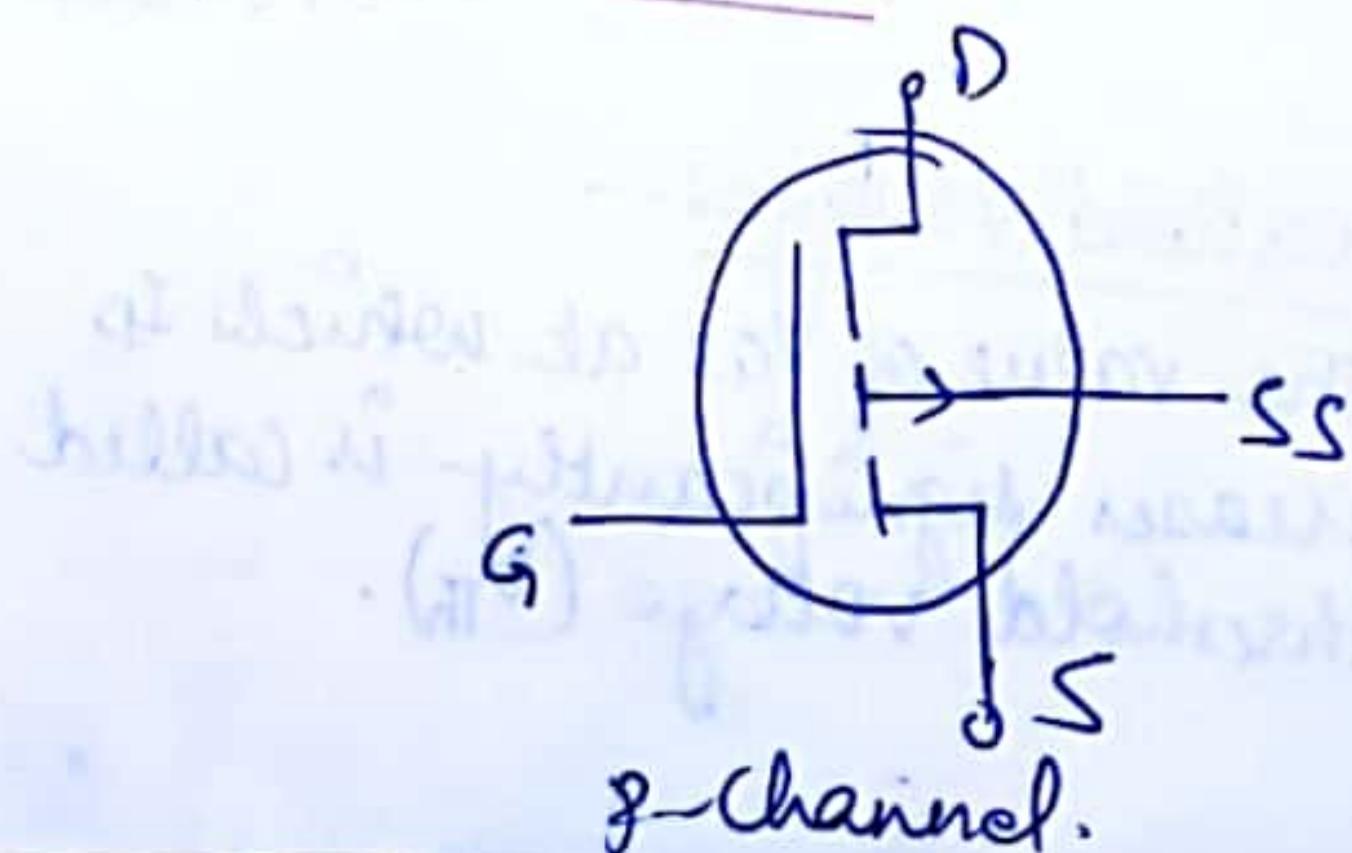
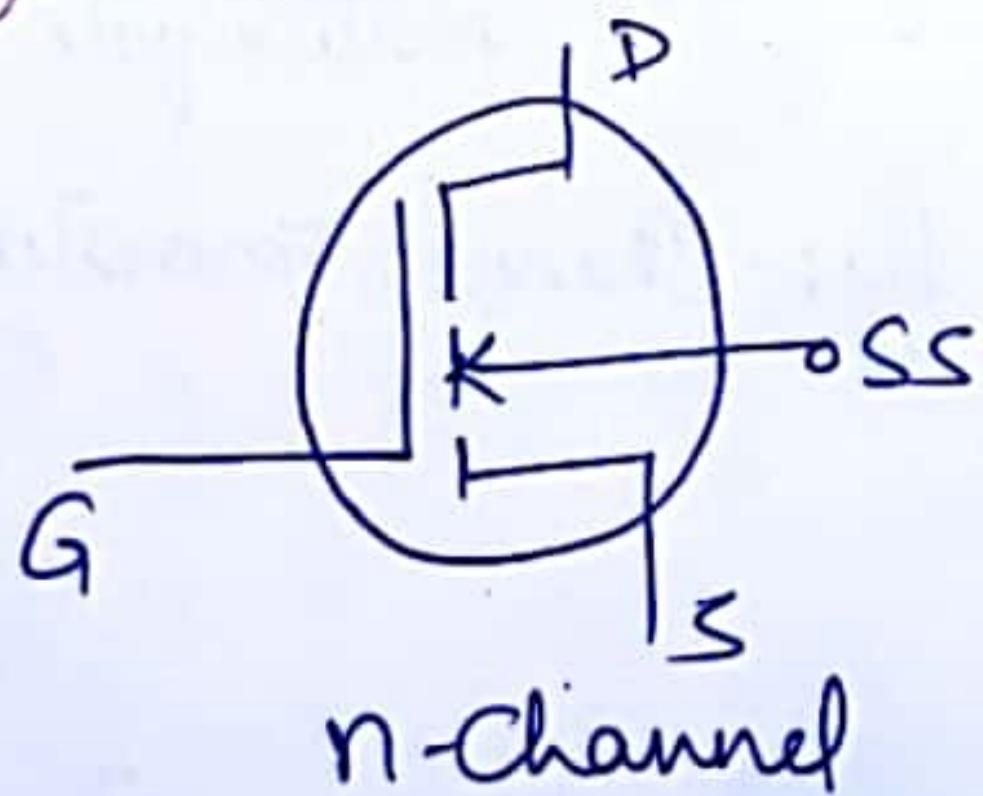
Now any further increase in  $V_{DS}$  at fixed levels of  $V_{GS}$  will not affect saturation level of  $I_D$  until breakdown conditions will encounter.

$$V_{DS_{sat}} = V_{GS} - V_T$$

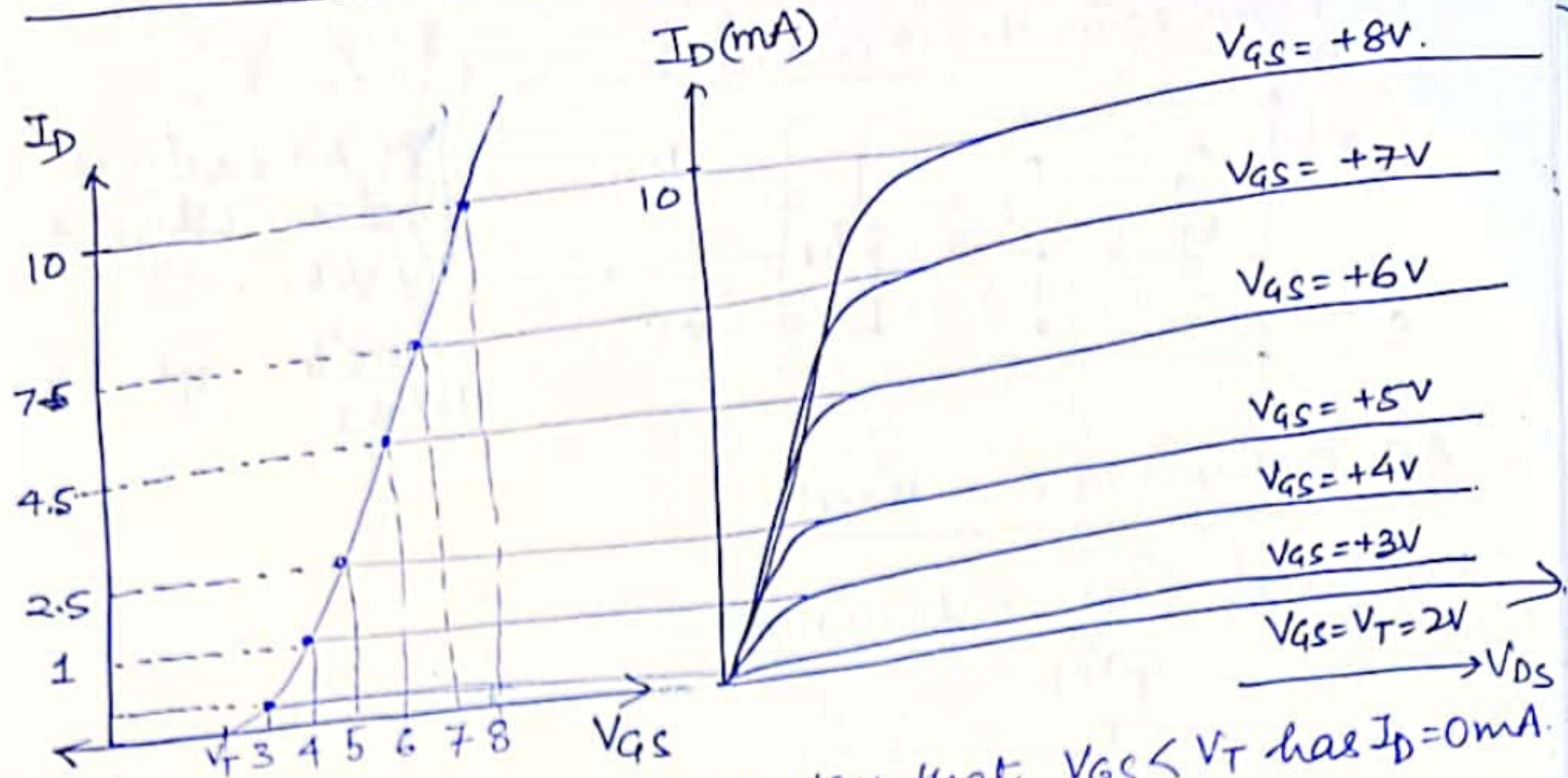
Drain



Symbol of Enhancement-type MOSFET



## Drain characteristic & transfer curve

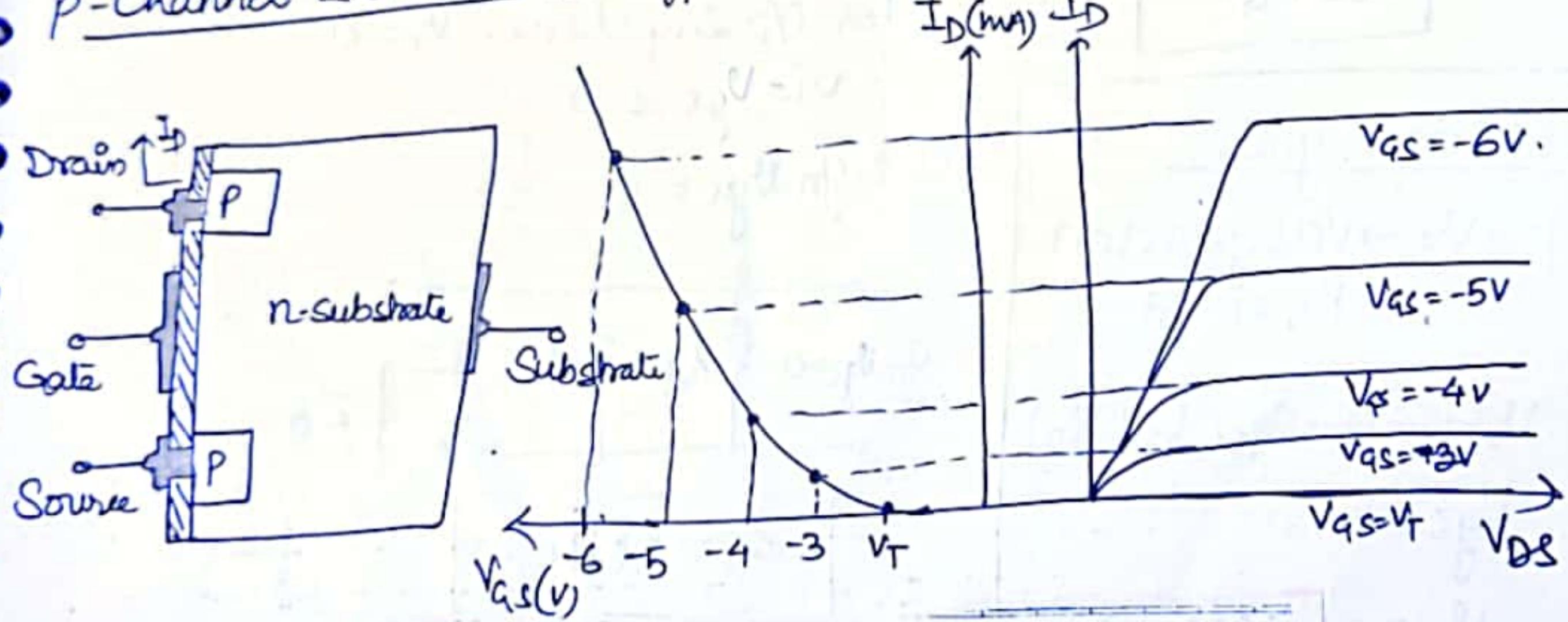


From transfer curve we can say that  $V_{GS} < V_T$  has  $I_D = 0$ .  
 For the levels of  $V_{GS} > V_T$ , drain  $I_D$  is related to  $V_{GS}$  as following non-linear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

$k \rightarrow$  Constant (material dependent) ( $\text{mA}/\text{V}^2$ )

## P-channel Enhancement type MOSFET:-

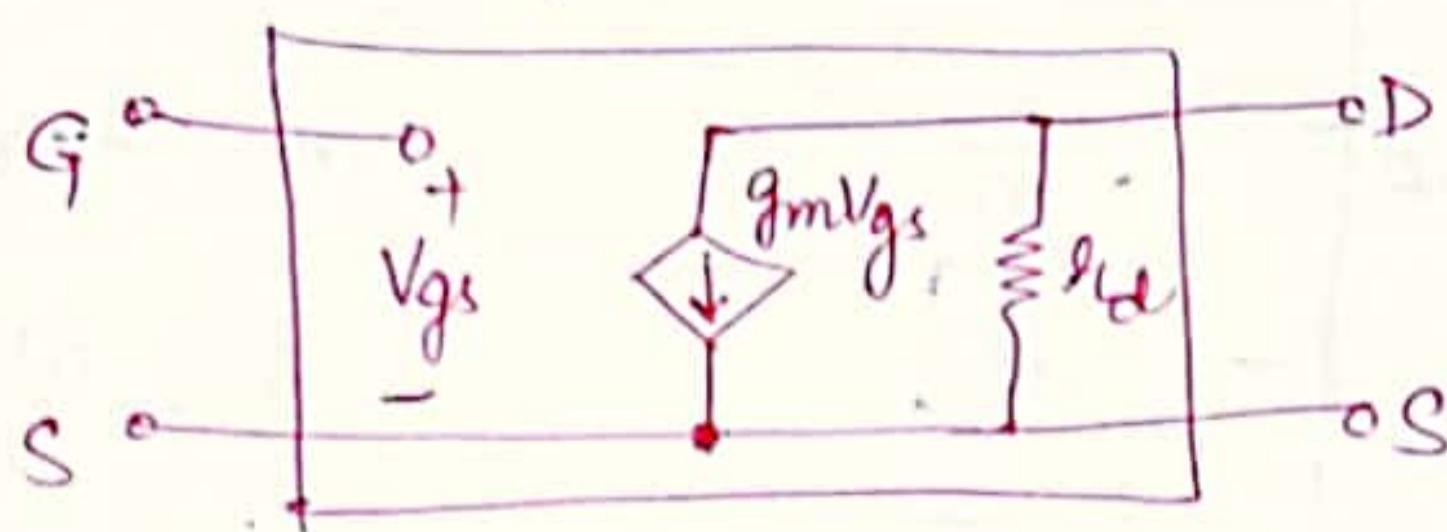


## Comparison of D-Mos and E-Mos

D-MOS	E-MOS
channel J <sub>S</sub> present in D-Mos	channel J <sub>S</sub> absent in E-Mos.
D-Mos follows Shockley eqn $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	E-Mos follows eqn $I_D = k(V_{GS} - V_{TH})^2$

## AC Analysis of JFET

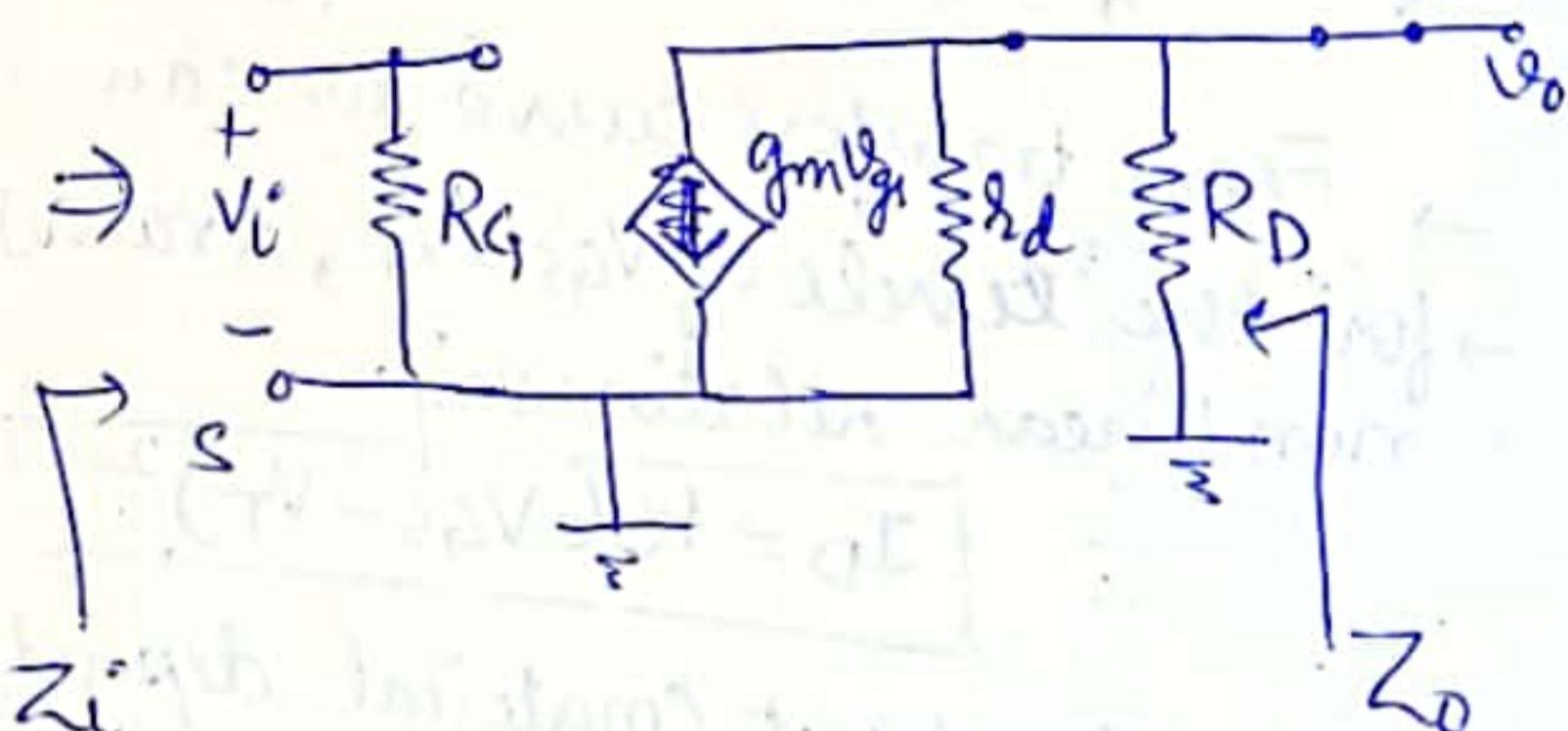
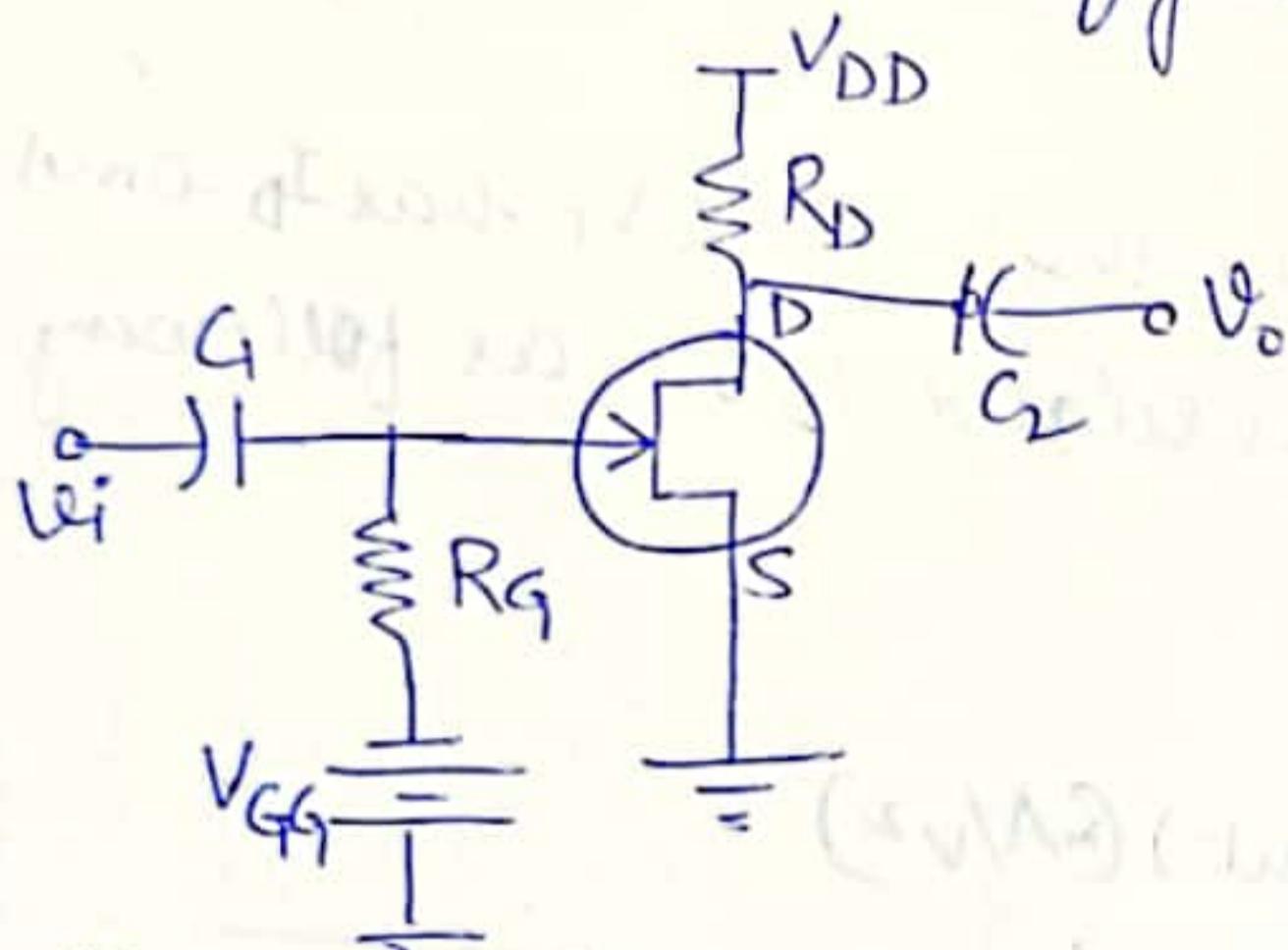
### JFET AC equivalent circuit :-



For AC analysis  
replace voltage source  
by s/ckt.  
capacitor replace by  
s/ckt

### AC Analysis of CS circuit.

#### (i) Fixed bias configuration:-



Input Impedance

$$Z_i = R_G$$

### Voltage gain

$V_o \rightarrow$  Voltage across  
 $R_D$  or  $r_d$ .

$$V_o = -g_m V_{gs} (r_d \parallel R_D)$$

$$V_{gs} = V_i$$

$$\therefore V_o = -g_m V_i (r_d \parallel R_D)$$

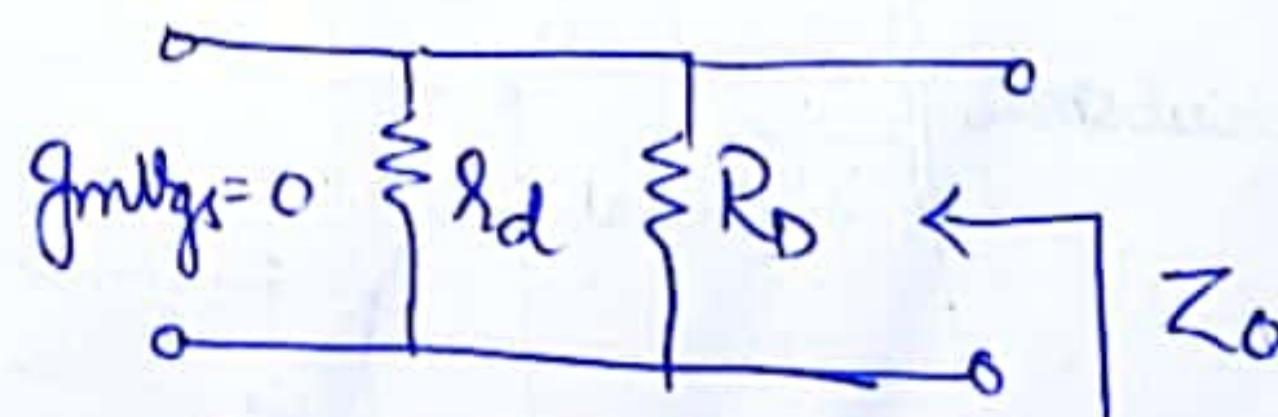
$$A_V = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)$$

### O/p Impedance

For O/P Impedance  $V_i = 0$

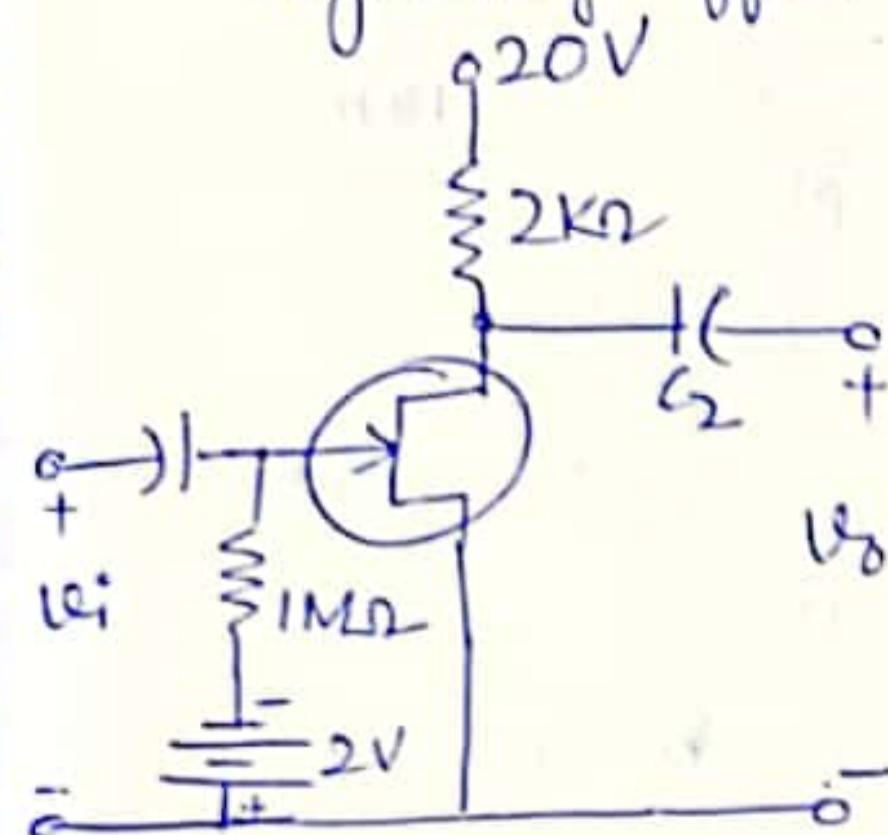
$$V_i = V_{ge} = 0$$

$$\therefore g_m V_{gs} = 0$$



$$Z_o = r_d \parallel R_D$$

Ques For given circuit  $g_m = 1.88 \text{ mS}$ ,  $r_d = 25 \text{ k}\Omega$  then calculate the value of  $Z_i$ ,  $Z_o$  &  $A_v$ , also calculate  $A_v$  ignoring effect of  $r_d$



$$Z_i^o = R_g = 1 \text{ M}\Omega$$

$$A_v = -g_m(r_d \parallel R_d)$$

$$= -1.88 \text{ mS} \times 1.88 \text{ k}\Omega$$

$$\boxed{Z_i^o = 1 \text{ M}\Omega}$$

$$Z_o = R_d \parallel r_d$$

$$= 2 \text{ k}\Omega \parallel 25 \text{ k}\Omega$$

$$\boxed{Z_o = 1.85 \text{ k}\Omega}$$

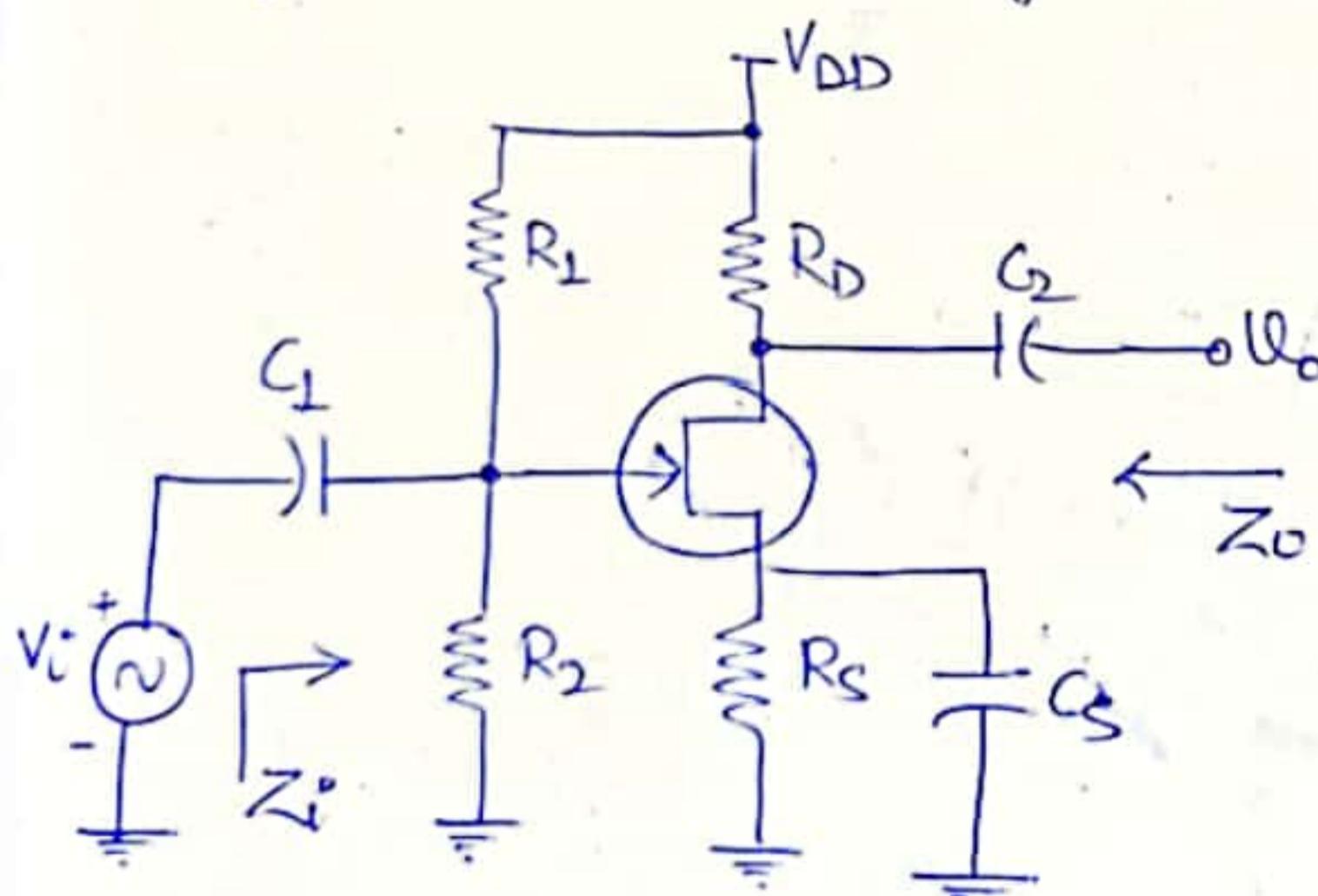
$$\boxed{A_v = -3.48}$$

$$A_v = -g_m R_d$$

$$= -1.88 \text{ mS} \times 2 \text{ k}\Omega$$

$$\boxed{A_v = -3.76}$$

### Voltage divider bias configuration



$$Z_1^o = R_1 \parallel R_2$$

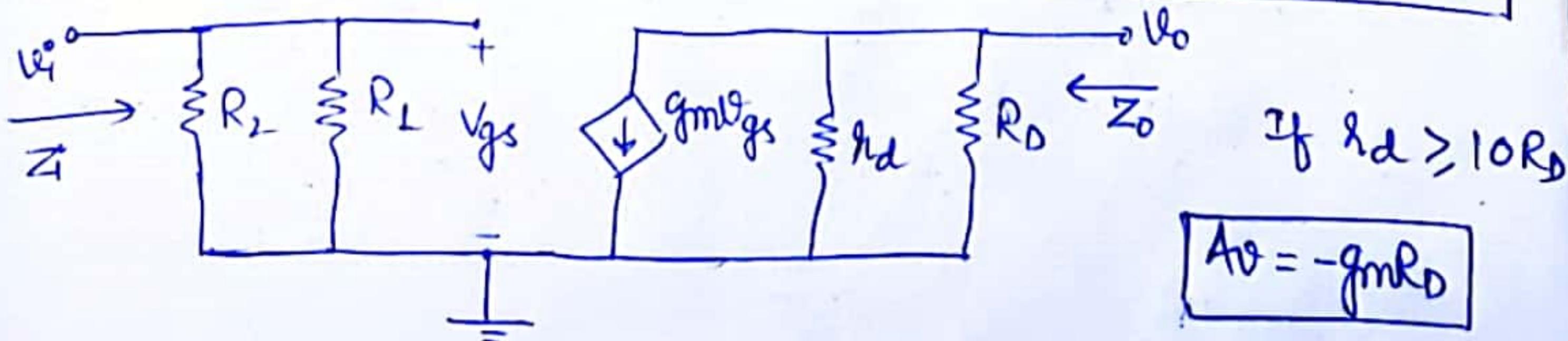
$$Z_o = r_d \parallel R_d$$

$$r_d \gg 10R_d \therefore Z_o = R_d$$

$$A_v \approx V_{gs} = V_i$$

$$V_o = -g_m V_{gs} (r_d \parallel R_d)$$

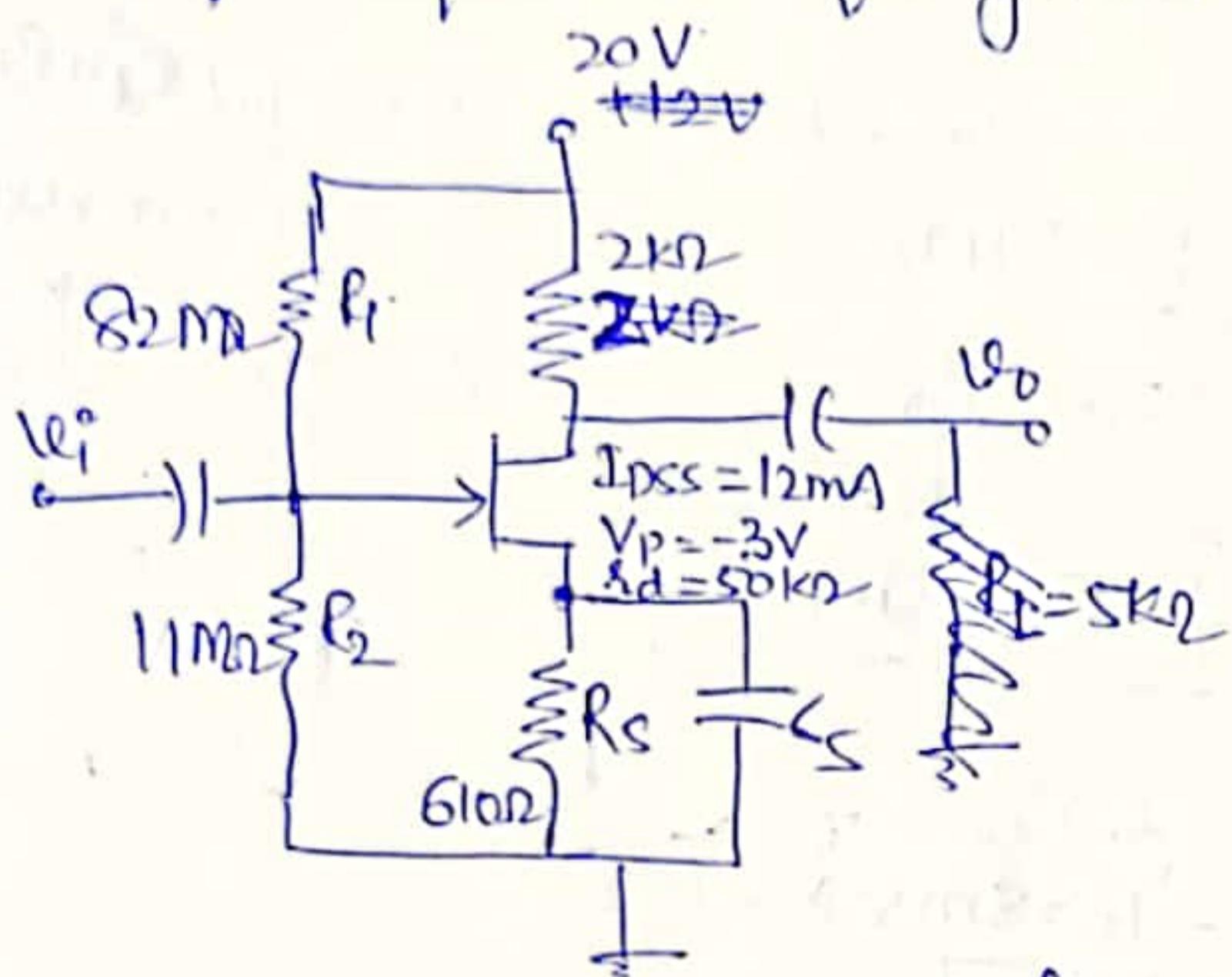
$$\boxed{A_v = -g_m (r_d \parallel R_d)}$$



$$\boxed{A_v = -g_m R_d}$$

fig : AC Equivalent Circuit

Ques for given figure determine O/P voltage and draw small signal equivalent for given circuit.  $V_i = 20mV$



$$g_{mo} = \frac{2i_{DSS}}{IV_{P1}} = \frac{2 \times 12mA}{3} \Rightarrow 8m$$

$$g_m = g_{mo} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$= 8m \left( 1 - \frac{0.02V}{20mV} \right) = 8m$$

$$= 7.94ms$$

$$Av = -g_m \times R_D$$

$$= -$$

Ans  $Z_f = 9.7M\Omega$ ,  $Z_o = 1.92k\Omega$

~~$A_v = -7.14$~~

$V_o = 210mV$

0.02

Ques Determine voltage gain

$$\alpha_{out} = 0$$