

TRAFFIC SIGNAL CONTROLLER

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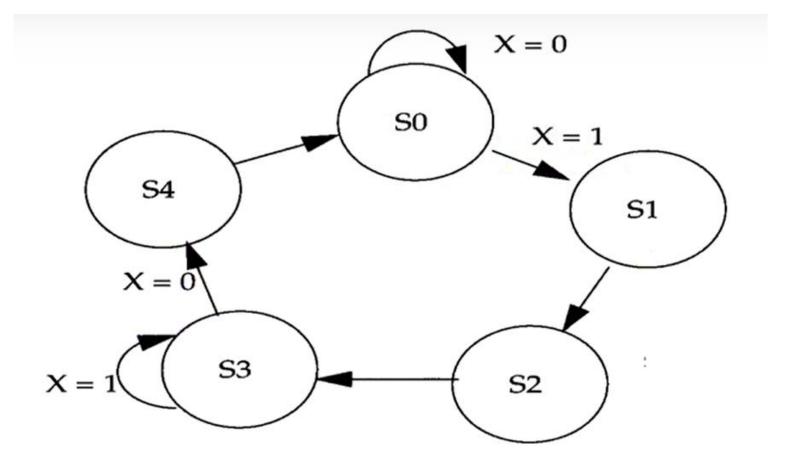
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TEAM NO:17

FINITE STATE MACHINE:



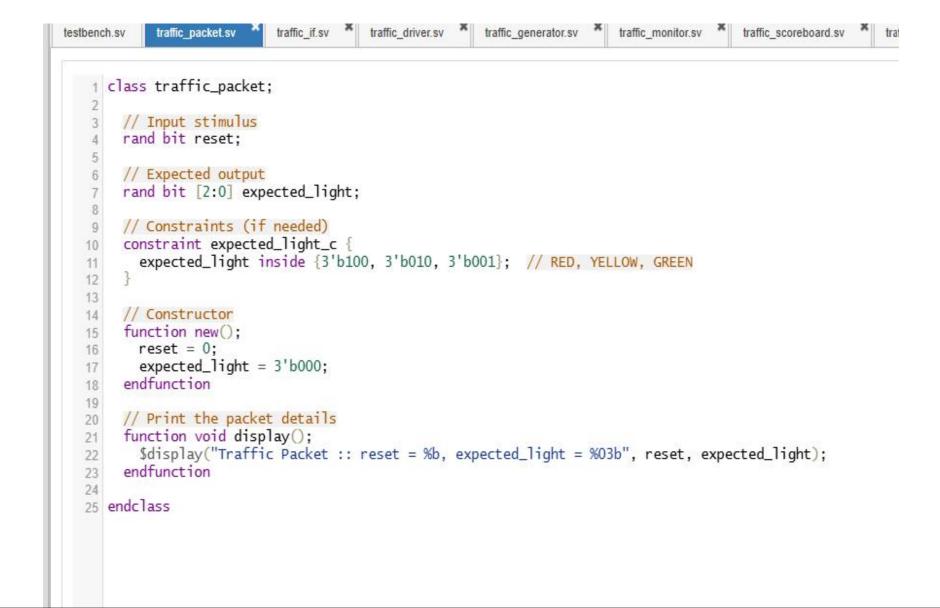


DUT CODE:

```
design.sv
     module traffic(
       input logic clk,
       input logic reset,
       output logic [2:0] light
   6
   8
       typedef enum logic [1:0] {
         S_RED = 2'b00.
  10
         S_GREEN = 2'b01,
         S_YELLOW = 2'b10
  11
  12
       } state_t;
  13
       state_t state, next_state;
  14
  15
       logic [3:0] count;
  16
  17
       always_ff @(posedge clk or posedge reset) begin
  18
  19
         if (reset)
  20
           state <= S_RED;
  21
         else
  22
           state <= next_state;
  23
       end
  24
  25
  26
       always_comb begin
  27
         next_state = state;
  28
         case (state)
           S_RED: if (count == 4'd10) next_state = S_GREEN;
  29
  30
           S_GREEN: if (count == 4'd10) next_state = S_YELLOW;
           S_YELLOW: if (count == 4'd5) next_state = S_RED;
  31
  32
           default: next_state = S_RED;
  33
         endcase
       end
  34
  35
  36
       always_ff @(posedge clk or posedge reset) begin
         if (reset) begin
  37
  38
           count <= 0;
           light <= 3'b100;
  39
  40
         end else begin
           count <= count + 1;
  41
  42
           case (state)
             S_RED: light <= 3'b100;
  43
             S_GREEN: light <= 3'b001;
  44
             S_YELLOW: light <= 3'b010;
  45
           endcase
  46
  47
         end
  48
       end
  49
  50 endmodule
```



PACKET CODE:





GENERATOR CODE:



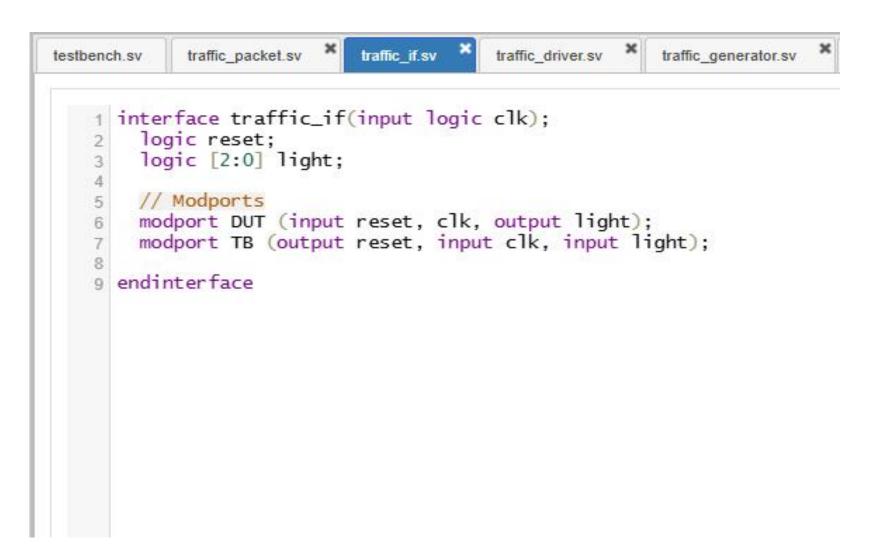


DRIVER CODE:

```
traffic_packet.sv * traffic_if.sv *
                                          traffic driver.sv
                                                          traffic generator.sv
testbench.sv
    1 class traffic_driver;
        virtual traffic_if.TB vif;
       function new(virtual traffic_if.TB vif);
          this.vif = vif;
        endfunction
       task drive(traffic_packet pkt);
          vif.reset = pkt.reset;
          @(posedge vif.clk);
   11
          vif.reset = 0; // De-assert reset after one clock cycle
       endtask
   15 endclass
```



INTERFACE CODE:



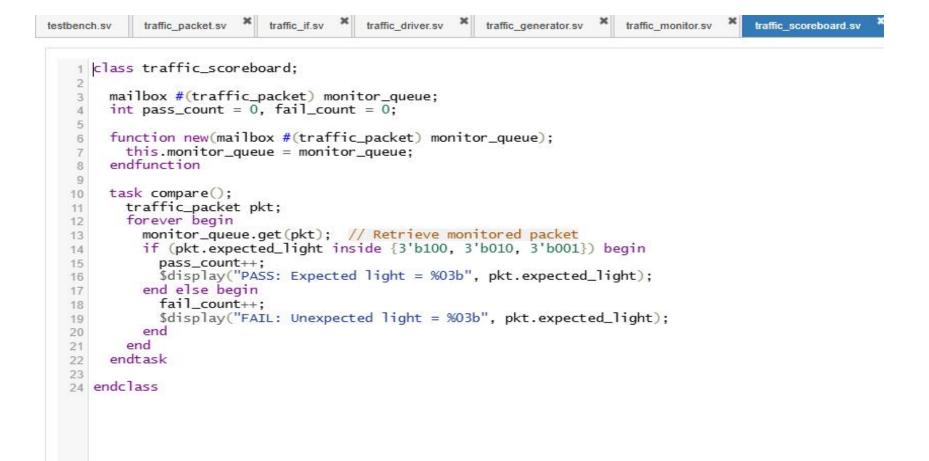


MONITOR CODE:

```
traffic_if.sv ×
testbench.sv
            traffic packet.sv
                                          traffic driver.sv
                                                          traffic generator.sv
                                                                             traffic monitor.sv
                                                                                              traffic
    1 class traffic_monitor;
       virtual traffic_if.TB vif;
        mailbox #(traffic_packet) monitor_queue;
        function new(virtual traffic_if.TB vif, mailbox #(traffic_packet) monitor_queue);
         this.vif = vif;
         this.monitor_queue = monitor_queue;
        endfunction
   10
        task monitor();
   11
          traffic_packet pkt;
          forever begin
  13
            @(posedge vif.clk);
            pkt = new();
  15
            pkt.expected_light = vif.light;
   16
            monitor_queue.put(pkt);
  17
          end
   18
  19
        endtask
  20
  21 endclass
```



SCOREBOARD CODE:





ENVIRONMENT CODE:

```
traffic monitor.sv * traffic scoreboard.sv
            traffic packet.sv * traffic if.sv *
                                         traffic_driver.sv ×
                                                          traffic_generator.sv *
                                                                                                                 traffic_env.sv
testbench.sv
      `include "traffic_packet.sv"
      include "traffic_generator.sv"
      include "traffic_driver.sv"
include "traffic_monitor.sv"
      include "traffic scoreboard.sv"
      class traffic_env;
  10
       traffic_generator generator;
       traffic driver driver:
   11
        traffic_monitor monitor:
  12
        traffic_scoreboard scoreboard;
  13
  14
        mailbox #(traffic_packet) packet_queue;
  15
        mailbox #(traffic packet) monitor queue:
  16
  17
        virtual traffic_if.TB vif;
  18
  19
        function new(virtual traffic_if.TB vif);
  20
          this.vif = vif;
  21
  22
          packet_queue = new();
          monitor_queue = new();
  23
          generator = new(packet_queue);
  24
          driver = new(vif);
  25
          monitor = new(vif, monitor_queue);
  26
          scoreboard = new(monitor_queue);
  27
  28
        endfunction
  29
       task run();
  30
  31
          fork
            generator.g1();
  32
            monitor.monitor();
  33
            scoreboard.compare():
  34
  35
            drive();
  36
          join
        endtask
  37
  38
        task drive();
  39
          traffic packet pkt:
  40
          while (packet_queue.num() > 0) begin
  41
            packet_queue.get(pkt);
  42
            driver.drive(pkt);
  43
          end
  44
  45
        endtask
  46
  47 endclass
```



TEST CODE:

```
traffic_packet.sv * traffic_if.sv * traffic_driver.sv * traffic_generate
testbench.sv
    1 | include "traffic_env.sv"
      class traffic_test;
        traffic_env env;
        function new(virtual traffic_if.TB vif);
         env = new(vif);
        endfunction
       task run();
        env.run();
        endtask
   16 endclass
```



TESTBENCH TOPLEVEL MODULE:

```
* traffic_if.sv * traffic_driver.sv *
            traffic_packet_sv
testbench.sv
                                                         traffic generator.sv
                                                                           traffic mo
      `include "traffic_if.sv"
      include "test.sv"
   6 module traffic_tb;
       logic clk;
       traffic_if tb_if(clk);
  10
       traffic dut(
  11
         .clk(tb_if.clk),
          .reset(tb_if.reset),
  13
          .light(tb_if.light)
  14
  15
  16
       // Clock generation
  17
       initial begin
  19
          c1k = 0;
         forever #5 clk = ~clk; // 10 ns clock period
  20
  21
  22
  23
        // Run the test
       initial begin
  24
         traffic_test test = new(tb_if.TB);
  25
  26
          test.run():
          #1000; // Run simulation for 1000 time units
  27
          $finish;
  28
  29
        end
  30
  31 endmodule
```



OUTPUT SNAPSHOTS:

```
PASS: Expected light = 100
PASS: Expected light = 001
```





THANK YOU