PROJECT REPORT
ON
L3 CACHE

- Durga Kundan Vanama & Vinod Sake

Portland State
UNIVERSITY

1. Introduction:

With the advent of technology, the need for higher performance in computers is increasing. To achieve the higher performance the processors are made to run at a frequency as high as thousands of Megahertz to tens of Gigahertz. Even though the processor runs at such high frequencies memory systems cannot cope up with them, due to which there has been search for alternative solution. The problem was solved by using the concept of "caching". Processor requests are routed through a small memory unit called as cache before searching the entire memory. Cache stores the necessary information i.e., might it be data or instruction, which is frequently used by processor, so that processor requests are fulfilled as quickly as possible. If the information is not present in cache, then it is fetched from the memory.

2. Applications:

The concept of caching can be applied in various computing domains such as:

- Translation Look Aside Buffers (TLB) in Virtual memory
- Caches in memory system as lower or higher level caches
- Caches in Graphics Processing Units (GPU) and Digital Signal Processors (DSP)
- Web caches, which store the websites, which are visited.

3. Technical Specification:

The L3 cache design implemented in the project has the following specifications:

- Total Capacity = 16MB
- Byte Line = 64 bytes
- Associativity = 8-way set
- Coherence Protocol = MESI
- Replacement Policy = true-LRU scheme (counter)
- Policy decisions for write = Write back
- Policy decisions for write miss = Write allocate

L2 cache specifications:

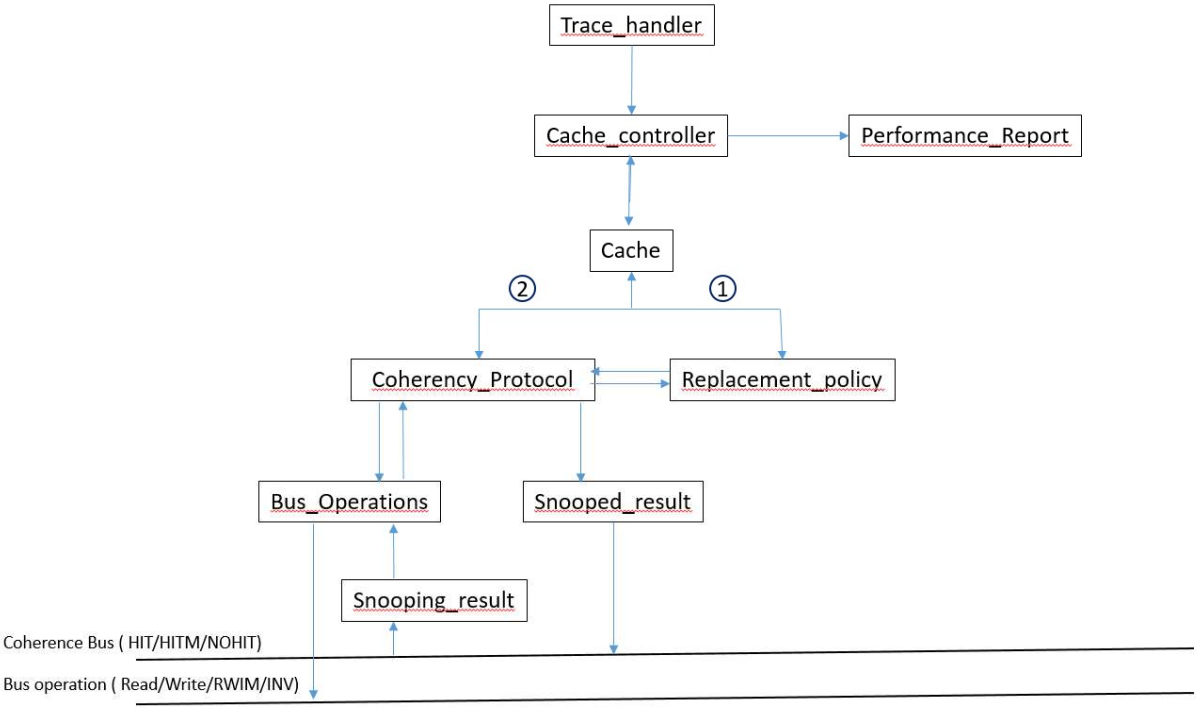
- Byte Line = 32 bytes

4. Assumptions:

We have made following assumptions in designing the L3 cache:

- All the read and write references are single byte addressable.
- L3 & L2 cache memories are line aligned
- When performing clear operation, we are performing Write bus operation if the state is in modified state and sending message to L2 cache to Invalidate if present.
- L3 cache would backoff the requested cache for snoop read of modified line, write back the cache line into memory and then allow other processor to complete it read operation.
- CPU address as 32-bits wide

5. Design Architecture:



6. Source Code:

a. Cache Package:
   All the parameterisable variables are defined in package and can be used anywhere in the project modules.
   cache_pkg.sv

b. Trace handler:
   The Trace handler reads in command and address and sends to cache controller.
   Trace_handler.sv

c. Cache Controller:
   The Cache controller reads the command from trace handler and distinguishes CPU commands, SNOOP commands, CLEAR and PRINT commands. At the end of reading trace file, we are printing the statistics of cache usage.
   Cache_controller.sv

d. L3 Cache:
   The L3 Cache reads the command and address and performs operations.
   cache.sv

7. Testing Strategies:

a. **CACHE READS:**

Test Strategy: 8 ways in Index 0 are filled with valid states by performing bus operations.

Expected Results:

CPU Reads – 8

CPU Writes –0

Hits – 0

Misses – 8

Test vector:

0 00000000

9

0 00200001

9

0 00400002

9

0 00600003

9

0 00800000

9

0 00A00001

9

0 00C00002

9

0 00E00003

9

b. **CACHE WRITE:**

Test Strategy: 8 ways in Index 0 are filled with valid states by cpu write operations.

Expected Results:

CPU Reads – 0

CPU Writes –8

Hits – 0

Misses – 8

Test vector:

1 00000000

9

1 00200001

9

1 00400002
9
1 00600003
9
1 00800000
9
1 00A00001
9
1 00C00002
9
1 00E00003
9

c. **CACHE SET FILL with HITS & MISSES:**

Test Strategy:

Expected Results:

CPU Reads – 32
CPU Writes –0
Hits – 32
Misses – 32

Test vector:

0 2123450
0 4123450
0 6123450
0 8123450
0 A123450
0 C123450
0 E123450
0 0123450
0 2123450
0 4123450
0 6123450
0 8123450
0 A123450
0 C123450
0 E123450
0 0123450
0 2123450
0 4123450
0 6123450

0 8123450
0 A123450
0 C123450
0 E123450
0 0123450
0 1123450
0 3123450
0 5123450
0 7123450
0 9123450
0 b123450
0 d123450
0 f123450
9

d. **SNOOP WRITE:**

Test Strategy: Performing a snoop write on 1246 which is not present in cache. The initial and final states will be invalidated.

Expected Results:

CPU Reads – 0
CPU Writes –0
Hits – 0
Misses – 0

Test vector:

5 1246
9

e. **SNOOP INVALIDATE:**

Test Strategy: The first address reads the data from cache line and the initial state of the address is shared (as last two bits of address according to code is HIT) and a snoop invalidate is invoked on same address. The state moves to invalidate to the address.

Expected Results:

CPU Reads – 1
CPU Writes –0
Hits – 0
Misses – 1

Test vector:

0 6000040
3 6000040
3 1234

9

f. **SNOOP RWIM:**

Test Strategy: The first address reads the data from cache line and the initial state of the address is Exclusive (as last two bits of address according to code is NO HIT) and a snoop rwim is invoked on same address. The state moves to invalidate to the address.

Expected Results:

CPU Reads – 2
CPU Writes –1
Hits – 0
Misses – 3

Test vector:

0 1239
6 1239
0 1234
6 1234
9
1 60
9
6 60
9
6 1235
9

g. **SNOOP READ:**

Test Strategy: The first address writes the data from cache line and the initial state of the address is modified and a snoop read is invoked on same address. The state moves to share on the address.

Expected Results:

CPU Reads – 2
CPU Writes –1
Hits – 2
Misses – 1

Test vector:

1 1231
9
4 1231
9
0 1234

9
4 1234
9
2 1231
9
4 1231
9
4 1243
9

h. CHECK FOR BUS OPERATIONS:

Test Strategy: Performing read and write operations and checking for busoperaions.

Expected Results:

CPU Reads – 24
CPU Writes –6
Hits – 5
Misses – 25

Test vector:

0 00000000
0 00200001
0 00400002
0 00600003
0 00800000
0 00A00001
0 00C00002
0 00E00003
9
0 01000000
9
0 01600001
9
0 01200002
9
0 01800001
9
0 02800001
9
0 02A00002
9
0 03000001

9
0 04000003
9
1 01200002
9
1 01800001
9
1 02800001
9
1 02A00002
9
1 03000001
9
1 00800000
9
0 00000000
9
0 00200001
9
0 00400002
9
0 00600003
9
0 01800000
9
0 00A00001
9
0 00C00002
9
0 05600001
9

8. Testing Results:

a. CACHE READS:

```
# ************ Valid lines in L3cache ************
#  MESI |  LRU   |  TAG   |      SET      |      WAY
#    S    |    0    |    7    | 00000000 |       0
#    S    |    1    |    6    | 00000000 |       1
#    E    |    2    |    5    | 00000000 |       2
#    S    |    3    |    4    | 00000000 |       3
#    S    |    4    |    3    | 00000000 |       4
#    S    |    5    |    2    | 00000000 |       5
#    E    |    6    |    1    | 00000000 |       6
#    S    |    7    |    0    | 00000000 |       7
# ********************* END **********************
#
# STATSITICS:
# CACHE READS|CACHE WRITES|   CACHE HITS   |CACHE MISSES|CACHE HIT RATIO
#
#         8         |         0         |         0         |         8         |    0.000000%
```

b. CACHE WRITE:

```
# ************ Valid lines in L3cache *************
#  MESI |  LRU   |  TAG |    SET      |      WAY
#    M    |    0    |    7    | 00000000 |       0
#    M    |    1    |    6    | 00000000 |       1
#    M    |    2    |    5    | 00000000 |       2
#    M    |    3    |    4    | 00000000 |       3
#    M    |    4    |    3    | 00000000 |       4
#    M    |    5    |    2    | 00000000 |       5
#    M    |    6    |    1    | 00000000 |       6
#    M    |    7    |    0    | 00000000 |       7
# ********************* END **********************
#
# STATSITICS:
#
# CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#
#          0          |          8          |         0         |          8          |        0.000000%
```

c. CACHE SET FILL with HITS & MISSES:

```
# ************ Valid lines in L3cache ************
#  MESI |  LRU  |  TAG |    SET      |      WAY
#    S    |    0    |  120  | 000048d1 |        0
#    S    |    1    |  104  | 000048d1 |        1
#    S    |    2    |   88  | 000048d1 |        2
#    S    |    3    |   72  | 000048d1 |        3
#    S    |    4    |   56  | 000048d1 |        4
#    S    |    5    |   40  | 000048d1 |        5
#    S    |    6    |   24  | 000048d1 |        6
#    S    |    7    |    8   | 000048d1 |        7
# ********************* END **********************
#
# STATSITICS:
#
# CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#
#         32          |          0          |       16        |         16          |      50.000000%
```

d. SNOOP WRITE:

```
# ************ Valid lines in L3cache ************
#  MESI |  LRU  |  TAG        |    SET    |  WAY
# ********************* END **********************
#
# STATSITICS:
#
# CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#
#          1          |          0          |       0         |          1          |      0.000000%
```

e. SNOOP INVALIDATE:

```
# ************ Valid lines in L3cache ************
#  MESI |  LRU  |  TAG        |     SET    | WAY
# ********************** END **********************
#
# STATSITICS:
#
# CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#
#          0          |          0          |        0        |          0          |       0.000000%
```

f. SNOOP RWIM:

```
#************ Valid lines in L3cache *****************
#  MESI |  LRU  |  TAG        |     SET    | WAY
# ********************** END **********************
#
# STATSITICS:
#
#CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#        2          |          1          |        0        |          3          |       0.000000%
```

g. SNOOP READ:

```
# ************ Valid lines in L3cache ************
#  MESI |  LRU  |  TAG |     SET        |  WAY
#    S    | 0      |    0   |  00000048  |         7
# ********************** END **********************
#
# STATSITICS:
# CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#        2          |          1     |          2   |          1     |    66.666667%
```

h. CHECK FOR BUS OPERATIONS:

```
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00000000 ---->
#
# BusOp: READ, Address: 0000000, TOTAL_Address: 00000000, Get Snoop Result: HIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00200001 ---->
#
# BusOp: READ, Address: 0008000, TOTAL_Address: 00200000, Get Snoop Result: NOHIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00400002 ---->
#
# BusOp: READ, Address: 0010000, TOTAL_Address: 00400000, Get Snoop Result: HITM
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00600003 ---->
#
# BusOp: READ, Address: 0018000, TOTAL_Address: 00600000, Get Snoop Result: HIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00800000 ---->
#
# BusOp: READ, Address: 0020000, TOTAL_Address: 00800000, Get Snoop Result: HIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00a00001 ---->
#
# BusOp: READ, Address: 0028000, TOTAL_Address: 00a00000, Get Snoop Result: NOHIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00c00002 ---->
#
# BusOp: READ, Address: 0030000, TOTAL_Address: 00c00000, Get Snoop Result: HITM
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00e00003 ---->
#
# BusOp: READ, Address: 0038000, TOTAL_Address: 00e00000, Get Snoop Result: HIT
#
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 01000000 ---->
#
# BusOp: READ, Address: 0040000, TOTAL_Address: 01000000, Get Snoop Result: HIT
#
# L2: Invalidate 00000000
# L2: Invalidate 00000020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 01600001 ---->
#
# BusOp: READ, Address: 0058000, TOTAL_Address: 01600000, Get Snoop Result: NOHIT
#
```

```
# L2: Invalidate 00200000
# L2: Invalidate 00200020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 01200002 ---->
#
# BusOp: READ, Address: 0048000, TOTAL_Address: 01200000, Get Snoop Result: HITM
#
# L2: Invalidate 00400000
# L2: Invalidate 00400020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 01800001 ---->
#
# BusOp: READ, Address: 0060000, TOTAL_Address: 01800000, Get Snoop Result: NOHIT
#
# L2: Invalidate 00600000
# L2: Invalidate 00600020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 02800001 ---->
#
# BusOp: READ, Address: 00a0000, TOTAL_Address: 02800000, Get Snoop Result: NOHIT
#
# L2: Invalidate 00800000
# L2: Invalidate 00800020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 02a00002 ---->
#
# BusOp: READ, Address: 00a8000, TOTAL_Address: 02a00000, Get Snoop Result: HITM
#
# L2: Invalidate 00a00000
# L2: Invalidate 00a00020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 03000001 ---->
#
# BusOp: READ, Address: 00c0000, TOTAL_Address: 03000000, Get Snoop Result: NOHIT
#
# L2: Invalidate 00c00000
# L2: Invalidate 00c00020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 04000003 ---->
#
# BusOp: READ, Address: 0100000, TOTAL_Address: 04000000, Get Snoop Result: HIT
#
# L2: Invalidate 00e00000
# L2: Invalidate 00e00020
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 01200002 ---->
#
# BusOp: INVALIDATE, Address: 0048000, TOTAL_Address: 01200000, Get Snoop Result: HITM
#
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 01800001 ---->
#
```

```
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 02800001 ---->
#
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 02a00002 ---->
#
# BusOp: INVALIDATE, Address: 00a8000, TOTAL_Address: 02a00000, Get Snoop Result: HITM
#
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 03000001 ---->
#
# <---- TRACE_CMD: CPU_WRITE_DATA :: TRACE_ADDRESS: 00800000 ---->
#
# BusOp: RWIM, Address: 0020000, TOTAL_Address: 00800000, Get Snoop Result: HIT
#
# L2: Invalidate 01000000
# L2: Invalidate 01000020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00000000 ---->
#
# BusOp: READ, Address: 0000000, TOTAL_Address: 00000000, Get Snoop Result: HIT
#
# L2: Invalidate 01600000
# L2: Invalidate 01600020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00200001 ---->
#
# BusOp: READ, Address: 0008000, TOTAL_Address: 00200000, Get Snoop Result: NOHIT
#
# L2: Invalidate 04000000
# L2: Invalidate 04000020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00400002 ---->
#
# BusOp: WRITE, Address: 0048000, TOTAL_Address: 01200000, Get Snoop Result: HITM
#
# BusOp: READ, Address: 0010000, TOTAL_Address: 00400000, Get Snoop Result: HITM
#
# L2: Invalidate 01200000
# L2: Invalidate 01200020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00600003 ---->
#
# BusOp: WRITE, Address: 0060000, TOTAL_Address: 01800000, Get Snoop Result: HIT
#
# BusOp: READ, Address: 0018000, TOTAL_Address: 00600000, Get Snoop Result: HIT
#
# L2: Invalidate 01800000
# L2: Invalidate 01800020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 01800000 ---->
#
```

```
# BusOp: WRITE, Address: 00a0000, TOTAL_Address: 02800000, Get Snoop Result: HIT
#
# BusOp: READ, Address: 0060000, TOTAL_Address: 01800000, Get Snoop Result: HIT
#
# L2: Invalidate 02800000
# L2: Invalidate 02800020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00a00001 ---->
#
# BusOp: WRITE, Address: 00a8000, TOTAL_Address: 02a00000, Get Snoop Result: NOHIT
#
# BusOp: READ, Address: 0028000, TOTAL_Address: 00a00000, Get Snoop Result: NOHIT
#
# L2: Invalidate 02a00000
# L2: Invalidate 02a00020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 00c00002 ---->
#
# BusOp: WRITE, Address: 00c0000, TOTAL_Address: 03000000, Get Snoop Result: HITM
#
# BusOp: READ, Address: 0030000, TOTAL_Address: 00c00000, Get Snoop Result: HITM
#
# L2: Invalidate 03000000
# L2: Invalidate 03000020
# <---- TRACE_CMD: CPU_READ_DATA :: TRACE_ADDRESS: 05600001 ---->
#
# BusOp: WRITE, Address: 0020000, TOTAL_Address: 00800000, Get Snoop Result: NOHIT
#
# BusOp: READ, Address: 0158000, TOTAL_Address: 05600000, Get Snoop Result: NOHIT
#
# L2: Invalidate 00800000
# L2: Invalidate 00800020
#

# ************ Valid lines in L3cache ************
#  MESI |  LRU   |  TAG   |      SET       |      WAY
#    E    |    6     |    1     |  00000000  |        0
#    S    |    1     |    6     |  00000000  |        1
#    E    |    2     |    5     |  00000000  |        2
#    S    |    3     |   12     |  00000000  |        3
#    S    |    4     |    3     |  00000000  |        4
#    S    |    5     |    2     |  00000000  |        5
#    S    |    7     |    0     |  00000000  |        6
#    E    |    0     |   43     |  00000000  |        7
# ********************* END **********************
#
```

STATSITICS:
#
CACHE READS|CACHE WRITES|CACHE HITS|CACHE MISSES|CACHE HIT RATIO
#
24 | 6 | 5 | 25 | 16.666667%