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Optimal thermal operation of liquid-cooled electronic chips

Chander Shekhar Sharma [a], Severin Zimmermann [a], Manish K. Tiwari [a], Bruno Michel [b], Dimos Poulikakos [a,*]

[a] Department of Mechanical and Process Engineering, ETH Zurich, 8092 Zurich, Switzerland
[b] Advanced Thermal Packaging, IBM Zurich Research Laboratory, IBM Research GmbH, 8803 Rueschlikon, Switzerland

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ABSTRACT

A novel framework is developed to determine the optimal operating conditions of water cooled microprocessor chips through a tradeoff between heat recovery from the coolant and the chip thermal reliability. For illustration, a manifold microchannel heat sink is evaluated experimentally and computationally. First, a single objective optimization is demonstrated by combining the heat recovery and chip reliability into a single parameter. Then, multi-objective optimizations are performed by using Pareto optimality and Multi-Criteria Design Analysis. Using conservative guidelines, these approaches suggest that for an optimal coolant flow rate of 1 l/m, optimal coolant inlet temperature lies between 40 and 50 °C.

1. Introduction

Until today the microprocessor industry has managed to keep pace with Moore's law of increasing transistor density on a single chip [1]. However, as more and more transistors are being packed in a given chip area, the heat dissipation density of a typical chip has risen dramatically. High heat density leads to high chip temperature, which adversely affects the chip performance and raises concerns about thermal reliability of electronics. Single phase liquid cooling for microprocessors has been long recognized as an effective method to replace conventional air-cooling to handle the increasing heat densities of current and future microprocessors. The liquid best suited thermally for single-phase cooling is water due to its high specific heat and thermal conductivity, as well as high availability and environmental friendliness.

Heat sinks with microchannels are now established as an effective approach to implement liquid cooling for electronics. Tuckerman and Pease [2] first reported that a heat sink with microchannels is ideal for liquid cooling of electronic chips, as the heat transfer coefficient scales inversely with the characteristic channel dimension for a fully developed laminar flow. A maximum power dissipation density of 790 W/cm^2 with a thermal resistance of 0.1 °C cm^2/W but at a high pressure drop of 2 bars was measured. Following this, many experimental and numerical studies have investigated the flow and heat transfer characteristics of microchannel heat sinks. Copeland et al. [3] undertook a numerical study of a manifold microchannel heat sink with multiple inlet and exit manifolds supplying liquid to microchannels from vertical direction. Based on the geometric and flow symmetry, they successfully used a single microchannel to represent the entire heat sink in their model. Fedorov and Viskanta [4] reported a numerical study of a manifold microchannel heat sink and analyzed the complex thermal transport inside a 3D microchannel. Their results supported the idea of using a manifold microchannel heat sink due to higher heat transfer coefficients near the channel inlets. Lee et al. [5] studied heat transfer in rectangular microchannels and concluded that conventional numerical analysis can be used to model thermal performance of microchannels.

Apart from effective cooling of high heat dissipating electronic chips, an additional important issue of concern is the increasing energy consumption by large computing systems such as data centers. Direct electricity consumption by data centers had already reached 1% of the total world electricity consumption by 2005 [6] due to increased demands for IT (Information Technology) related services such as internet and telephony. The introduction of the Green500 list for supercomputers [7,8] emphasized that performance can no longer be the sole motivation for development of microprocessors and that performance per unit energy consumption is the more appropriate metric for better computing.

Today, the energy for cooling conventional air-cooled data centers comprises almost half of the total energy consumption of such

* Corresponding author. Tel.: +41 44 632 27 38; fax: +41 44 632 11 76.
E-mail address: dimos.poulikakos@ethz.ch (D. Poulikakos).

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Nomenclature

A	area (m^2)
c_p	specific heat at constant pressure (J/kg K)
C_1, C_2	empirical constants
D_h	hydraulic diameter (m)
E_a	activation energy (eV)
Ex	flow exergy (W)
f	CFD solution on a grid
F	objective function
GCI	grid convergence index
h	specific enthalpy (J/kg), grid spacing (μm), heat transfer coefficient (W/m^2 K)
H	height, thickness (μm)
k	thermal conductivity (W/m K)
K	scaling parameter for utility function
l, L	length (μm)
$\dot{m}$	mass flow rate (kg/s)
MTTF	mean time to failure (10^6 h)
N	number of microchannels
Nu	Nusselt number
p	observed order of convergence
P	pressure (Pa)
$\dot{q}$	heat flux (W/m^2)
Q	heat dissipation (W)
R	reliability, thermal resistance (°C cm^2/W)
s	specific entropy (J/kg K)
$\dot{S}$	rate of entropy generation (W/K)
t	time (h)
T	temperature (°C, K)
U	velocity vector (m/s)
U	attribute utility
w	weight for objective function F
W	width (μm)
$\dot{w}$	power (W)

Greek letters

η	efficiency
δ	Kronecker delta
λ	instantaneous failure rate (per 10^6 h)
μ	dynamic viscosity (Pa s)
π	multiplying factors in failure rate
ρ	density (kg/m^3)
$\boldsymbol{\tau}$	stress tensor (Pa)

Subscripts

avg	average
b	base
ch	channel
elect	electrical
f	fluid
in	inlet
intf	solid–liquid interface
J	junction
max	maximum
meas	measured
min	minimum
nm	normalized
out	outlet
pump	pumping
pred	predicted
s	solid
th	thermal
tot	total
T	temperature
TIM	thermal interface material
u	utopian design
w	wall

systems. This portion of energy use can be significantly reduced by switching to liquid cooling. This is because the much lower thermal resistance inherent in liquid use enables cooling above the free cooling limit thus eliminating the need for coolant chillers. The free cooling limit represents the minimum temperature at which the coolant can effectively transport heat from a chip to ambient conditions without the need for an additional chiller. Additionally, and perhaps more importantly, if hot water in the temperature range of 50–70 °C is used to cool electronic chips, direct utilization of the collected thermal energy becomes feasible, either using synergies with district heating or specific industrial applications [9–11]. In doing so, irrespective of the cooling system being used, thermal reliability of the electronic chip must be guaranteed. This requires maintaining the chip temperature below certain upper limits as the thermal reliability of the chip reduces exponentially with chip temperature [12]. This aspect is discussed in detail in Section 2.

There are two classes of parameters that influence the performance of a cooling system for electronic chips. The first set of parameters, which are directly related to cooling system, include inlet flow rate and temperature of coolant fluid, the design of heat transfer surfaces in the heat sink, the nature of the coolant fluid (liquid or gas) and the nature of flow (single or two phase). The other category of parameters lies outside the envelope of cooling system and belongs to the design of the electronic system. These parameters include chip power dissipation, thermal reliability of chip, net wiring length on an electronic board etc. These two classes of parameters are coupled; hence, the design of a cooling system usually involves a trade-off, which can be investigated as an optimization problem.

Many studies have been reported in literature on design of electronic cooling systems. Some of them have focused on optimization of the microchannel dimensions so as to minimize the thermal resistance for the heat sink [13–16]. Shah et al. [17] proposed an exergy based figure of merit for electronic cooling systems and their work accounted for impact of high junction temperature on chip performance in term of MIPS (millions of instructions per second). However, this work was limited to air cooling; it did not consider thermal reliability issues for electronic chips and did not include multiple objective optimization to systematically determine the relative importance of competing criteria. There are, however, some examples of electronic cooling system design per se addressed using multi-objective optimization approaches. Husain and Kim [18] and Ndao et al. [19] selected the conflicting objectives of minimization of pumping power and minimization of thermal resistance, and optimized channel shape using Pareto optimality. Escher et al. [20] optimized the manifold and microchannel design of a manifold microchannel heat sink to achieve uniform fluid coolant distribution. Quepo et al. [21] presented a methodology to design a cooling system with the twin objectives of minimization of total wiring length of printed circuit board and total electronic failure rate. A Pareto front comprising of non-dominated solutions was constructed and multi-attribute utility analysis (MAUA) was used to select the optimal solution.

To the best our knowledge, no clear guideline exists in the literature for a multi-attribute optimization of water-cooled electronic systems that account for both chip reliability and exergetic efficiency. The previously reported feasibility studies on hot water cooled electronic systems are all motivated to maximize exergetic (second law of thermodynamics based) efficiency of such systems and open up novel possibilities for reuse of the energy extracted from the chip. However, we illustrate here that although the exergetic efficiency of the cooling system increases with increase in temperature of water, this gain in exergetic efficiency comes at a price of increased maximum chip temperature and thus decreased thermal reliability of the chip. It is evident that there exists a clear need to achieve an optimal trade-off between maximizing the exergetic efficiency of the cooling system and maximizing the thermal reliability of the microprocessor being cooled. Therefore, using an experimentally validated 3D conjugate heat transfer model and two different optimization approaches, the current work focuses on defining optimal operation conditions for electronic chip cooling systems using hot water as the coolant for energy reuse. Two optimization approaches, one single objective and the other multi-objective, are used. The single objective optimization is formulated by combining the two required criteria, i.e. heat recovery and thermal reliability, into a single parameter termed as net efficiency, which is then maximized. This parameter is a product of normalized MTTF (Mean Time to Failure) for the chip and exergetic efficiency of the overall system. The multi-objective optimization approach employs the concept of Pareto optimality and two different methodologies from Multi-Criteria Design Analysis (MCDA), namely TOPSIS (Technique for Order Preference by Similarity to Ideal Solutions) and MAUA (Multi-Attribute Utility Analysis), to achieve an optimal trade-off between the two criteria. Our primary aim is to provide a fundamental methodology to obtain optimal operating conditions for water cooled electronic chips. The proof of concept is therefore developed on an exemplary manifold microchannel heat sink.

The paper is organized as follows. Section 2 discusses the thermal reliability of electronic chips and its quantification, Section 3 details the experimental set-up and measurements, Section 4 presents the formulation of a 3D conjugate heat transfer model and grid convergence check, Section 5 discusses the formulation and the solution methodology for the optimization problem and lastly, Section 6 presents the validation of the numerical model, analysis of the results and the optimal solutions.

2. Reliability of electronic devices

With large scale integration in microprocessor chips, the reduction in transistor switching and signal transmission energies have not kept pace with the increasing gate densities. The resulting non-ideal scaling of supply and threshold voltages has led to increase in power dissipation (heat) densities. In addition, miniaturized transistors in deep submicron complementary metal oxide semiconductor (CMOS) technologies have significantly higher power leakage due to leakage currents. This leakage power has an exponential dependence on chip temperature [12,22–24]. All these factors result in an even higher increase in chip temperature, which, in turn, results in lower chip thermal reliability. The reliability of electronic systems can decrease by as much as 50% for every 10 °C increase in maximum chip temperature [12]. There are six major wear out mechanisms for chip reliability reduction: Electromigration, Stress Migration, Time Dependent Dielectric Breakdown, Negative Bias Temperature Instability, Hot Carrier Injection and Thermal Cycling. The failure rates for these various mechanisms have either exponential or power law dependence on chip temperature [23–27]. However, information on the empirical constants in expressions for these failure rates is usually proprietary. Among the several methods for prediction of electronic thermal reliability in the open source literature, the most widely known and used is the reliability prediction handbook MIL-HDBK-217 [28,29].

For any electronic component the instantaneous failure rate λ is defined as the number of components failing per unit time, which is typically a bathtub curve type function of time [23,28]. However, away from the early or the wear-out failure periods of the bathtub curve, during the intermediate useful life of a chip, its thermal reliability can be expressed with a constant failure rate as [25,28]:

$$R(t) = \exp(-\lambda t) \tag{1}$$

For microprocessors, the reliability is more commonly quantified using mean time to failure (MTTF), i.e. the expectation of time to failure, which for a constant λ becomes [28]:

$$\mathrm{MTTF} = \int_0^\infty R(t)dt = \int_0^\infty \exp(-\lambda t)dt = \frac{1}{\lambda}. \tag{2}$$

The overall predictions for failure rates are based on the roll-up, or summation, of all the individual component failure rates. For microprocessors [29,30],

$$\lambda = (C_1\pi_T + C_2\pi_E)\pi_Q\pi_L \tag{3}$$

where λ is the number of failures per million (10^6) hours, C_1 and C_2 are empirical constants, π_E is an environmental factor, π_T is a temperature factor, π_Q is a quality factor and π_L is a learning factor. The temperature factor, π_T, depends exponentially on the junction temperature (T_J) as

$$\pi_T = 0.1\exp\left(\frac{-E_a}{8.617\times10^{-5}}\left(\frac{1}{T_J+273}-\frac{1}{298}\right)\right) \tag{4}$$

where E_a is the effective activation energy in eV. The maximum chip temperature $T_{s,\max}$ is used as an estimate for T_j.

3. Experimental setup and measurements

Schematics of the flow loop and the test section designed to evaluate the heat sink performance are shown in Figs. 1(a) and (b). The coolant inlet temperature to the heat sink, $T_{f,in}$, is controlled using a heat exchanger which is connected to a separate flow loop where the temperature is regulated by a heater/chiller (Proline RP 855, Lauda, Germany). The resulting accuracy of $T_{f,in}$ is 0.1 °C. The coolant flow rate is measured using a Coriolis flow meter (Emerson, Switzerland) with an accuracy of 0.2% for the entire range (0.1–1.8 l/min) of operation. A differential pressure sensor (Honeywell, USA) and two thermocouples (Omega Engineering Inc., USA) have been used to measure the pressure drop, and inlet and outlet temperatures. The manufacturer-specified precision of the differential pressure sensor is 0.001 bar. The two thermocouples have been cross-calibrated in a temperature bath to make relative measurements with an accuracy of 0.1 °C. This precise calibration is needed because an error of 0.1 °C already corresponds to a 7 W heat flux error at a water flow rate of 1 l/min, which is significant given the 130 W maximum thermal load associated with the chip. A 7 μm pore filter (Swagelok, Solon, USA) has been used to keep the coolant free of large particles.

Fourteen Resistance Temperature Detectors (RTDs) integrated in the heating test chip (area: 2.31 cm^2) are used to determine the temperature field of the chip surface. Thermal grease (Dow corning TC-5026) is applied as thermal interface material (TIM) between the chip and the heat sink. Spring loaded screws are used to mount the chip/TIM/heat sink assembly onto a holder. The spring loading maintains a constant force of 98 ± 10 N on to the chip. The thermal grease improves heat spreading and helps make a good thermal connection between both parts. The thickness of the TIM layer is taken as the average of the values measured using

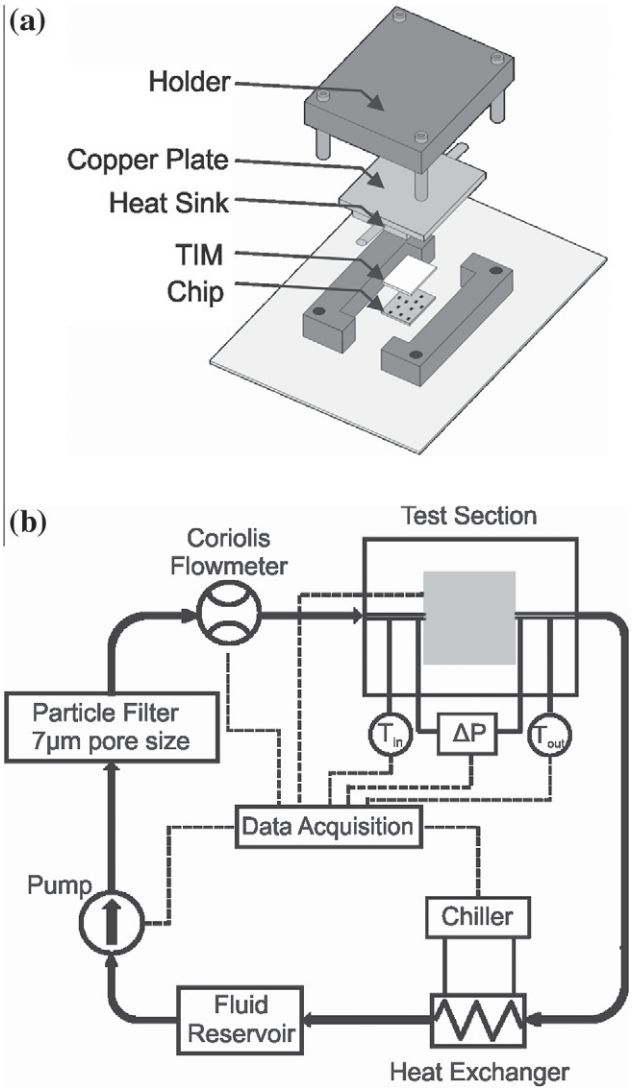

Fig. 1. Experimental setup: (a) test-section and (b) flow-loop.

four inductive length probes (P2001, Mahr, Goettingen, Germany) with an accuracy of ±1.5 μm. The probes, located at the four edges, are a fixed part of the holder.

4. Modeling of microchannel heat sink

The manifold microchannel heat sink is used in this study as a typical heat sink for electronic cooling. The heat sink material is copper and it is made by diffusion bonding the manifold and microchannel layers together (Wolverine, Inc.). A schematic of the manifold microchannel heat sink is shown in Fig. 2(a). The heat sink consists of one inlet manifold and two outlet manifolds. Fig. 2(a) depicts half of the heat sink with the flow path through the heat sink indicated by arrows. Coolant enters through the inlet pipe into the inlet manifold as a jet. The flow impinges on the microchannels through the slot nozzles in the base of the inlet manifold and divides equally into two streams. Each stream then flows through the microchannels absorbing heat coming from the chip underneath the TIM. Finally, the two streams of coolant enter the outlet manifold, merge and flow out of the heat sink via the outlet pipe.

4.1. Computational domain

As evident from above, the major part of the heat transfer from chip to water occurs in the microchannels. In order to capture the main heat transfer characteristics, and to reduce the computational cost, we model the flow only from microchannel inlet slot nozzle to microchannel outlet slot nozzle. The computational domain for the microchannel is shown in Fig. 2(b). The computational domain consists of one half of the channel from inlet to outlet nozzles.

Channel dimensions, as shown in Fig. 2(b), are listed in Table 1 below. TIM thickness, H_{TIM}, is small compared to rest of the channel and hence is not depicted in Fig. 2(b). These dimensions represent average channel dimensions obtained by measurement on a cross-section of the heat sink.

Following assumptions are made to decide the computational domain and boundary conditions:

(1) The impingement and exit flows, respectively, at inlet and outlet nozzles as well as the flow inside the channel are symmetric about the central axial plane of the channel. Thus, a symmetric boundary condition is imposed for flow at the planes shown in Fig. 2(c).
(2) Water from inlet manifold is uniformly distributed across all the channels.
(3) The heat sink loses some of the heat from the chip to the ambient and thus the entire heat from chip is not absorbed by water. It is essential to capture these losses in the microchannel model in order to closely predict the coolant temperature at heat sink outlet. It is assumed that the net measured loss from heat sink to surroundings can be equally divided among all the channels. This loss is imposed as outwards heat flux on the top and end walls of the channel as shown in Fig. 2(c). The measured total chip heat dissipation and the water temperatures at heat sink inlet and outlet are used to compute the heat loss per channel as

$$\dot{q}_{ch,loss} = \frac{\dot{Q}_{chip} - (\dot{m}\rho_f c_{p,f}(T_{f,out,meas} - T_{f,in}))}{N(A_{upperwall} + A_{endwall}) \times 2 \times 2} \tag{5}$$

where $A_{upperwall} + A_{endwall}$ is the total area of the channel upper and end walls (see Fig. 2(b)).

4.2. Governing equations, boundary conditions and solution methodology

The Reynolds number of the flow inside the channel, over all the operating conditions investigated, lies in the range of ~75–420. Thus the flow is laminar and governed by the following 3D mass, momentum and energy conservation equations [31].

Continuity

$$\nabla \cdot (\rho \mathbf{U}) = 0. \tag{6}$$

Momentum conservation

$$\nabla \cdot (\rho \mathbf{U} \otimes \mathbf{U}) = -\nabla P + \nabla \cdot \boldsymbol{\tau}, \tag{7}$$

where the stress tensor, $\boldsymbol{\tau}$, is related to the strain rate by

$$\boldsymbol{\tau} = \mu(\nabla \mathbf{U} + (\nabla \mathbf{U})^T - \frac{2}{3}\delta(\nabla \cdot \mathbf{U})). \tag{8}$$

Energy conservation

$$\nabla \cdot (\rho \mathbf{U} h) = \nabla \cdot (k_f \nabla T) + \boldsymbol{\tau} : \nabla \mathbf{U}. \tag{9}$$

For solid domain the 3D conduction equation is solved

$$\nabla \cdot (k_s \nabla T) = 0. \tag{10}$$

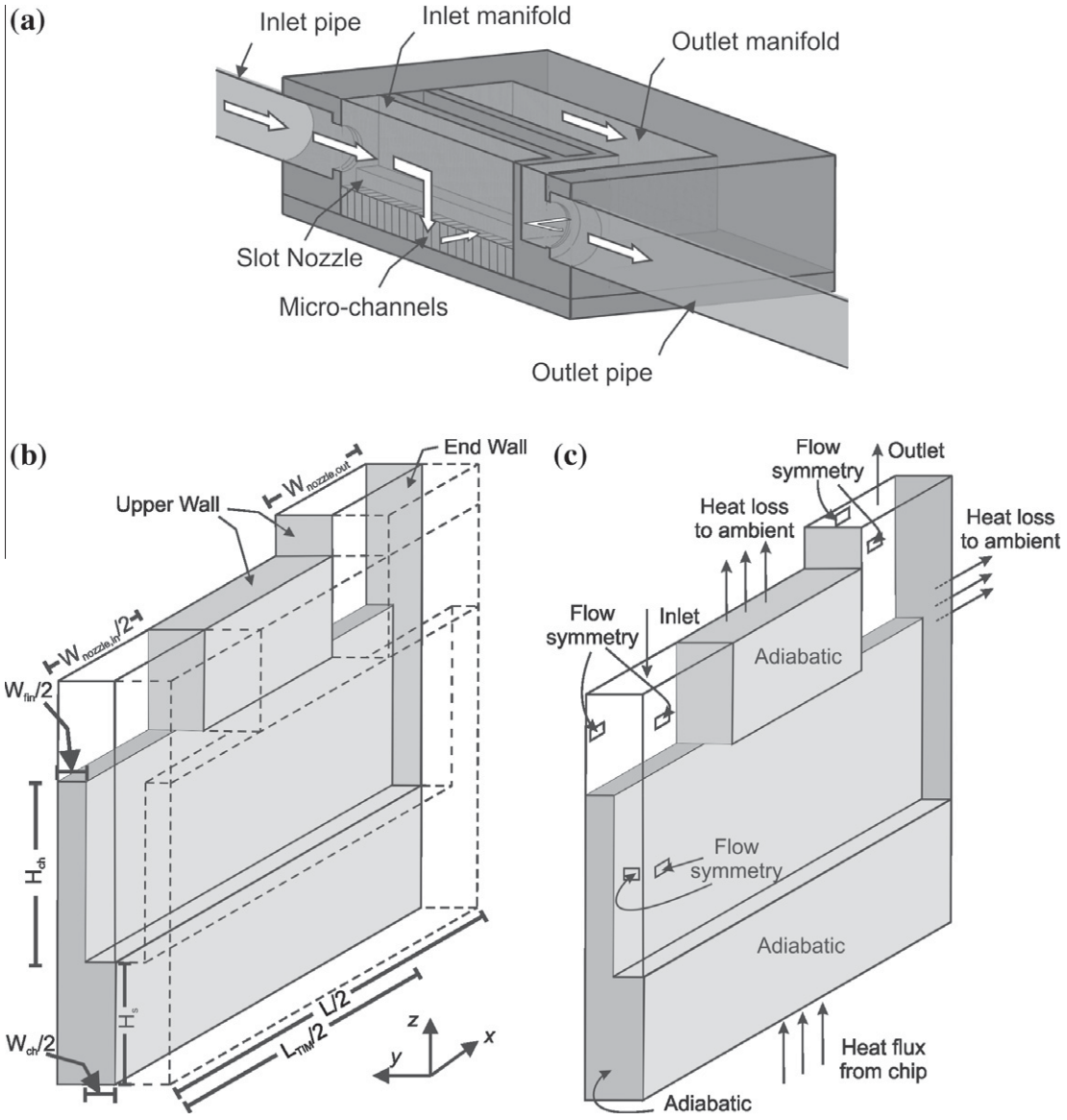

Fig. 2. (a) Schematic of the manifold microchannel heat sink used (arrows indicate direction of coolant flow), (b) computational domain and geometrical dimensions for the single microchannel and (c) boundary conditions for simulations.

Table 1
Microchannel dimensions.

Symbol	Description	Value
H_{ch}	Channel height	1473 μm
W_{ch}	Width of channel	159 μm
W_{fink}	Width of fin (i.e. microchannel side wall)	181 μm
L	Length of channel/fin	17,000 μm
$W_{nozzle,in}$	Width of inlet nozzle	2000 μm
$W_{nozzle,out}$	Width of outlet nozzle	2000 μm
H_s	Height of solid above TIM	1200 μm
H_{TIM}	TIM thickness	12 μm
L_{TIM}	Heated length of TIM	12,550 μm
N	Number of microchannels	62

The model takes into account the temperature dependence of intensive water properties such as density (ρ), dynamic viscosity (μ) and specific heat (c_p) [32]. Continuity of temperature and heat flux is imposed at the fluid-solid interface, as shown in Eqs. (11) and (12), where **n** is the direction normal to the interface.

Energy conservation at fluid–solid interface

$$-k_s((\nabla T)_{s,intf}\cdot\mathbf{n}) = -k_f((\nabla T)_{f,intf}\cdot\mathbf{n}), \tag{11}$$

$$T_s = T_f, \tag{12}$$

The boundary conditions are shown in Fig. 2(c). At the inlet, coolant mass flux and inlet temperature are imposed. At the outlet nozzle, an 'opening' type of boundary condition is imposed that takes care of both inflow and outflow of the fluid at the outlet boundary because it lies in recirculating flow [33]. Symmetric boundary condition for flow is imposed as already shown in Fig. 2(c). Uniform heat flux is imposed at the lower surface of TIM.

The conjugate heat transfer problem is solved using commercial solver Ansys CFX® version 12.1. The solver uses the finite volume approach to discretize the governing equations into mostly second-order accurate, coupled linear algebraic equations. The discretized hydrodynamic equations, Eqs. (6), (7), and (9), are solved in a coupled manner using the algebraic multi-grid method. The steady-state equations are solved using a pseudo-transient term to evolve the steady-state solution [31]. Convergence of the equations being solved is tracked by monitoring the normalized

equation residuals as well as global imbalances for conserved quantities of mass, momentum and energy [31,33]. We imposed 1×10^{-6} as the normalized residual target and 0.1% as the conservation target for our simulations.

4.3. Mesh and grid independence

A block-structured, hexagonal, non-uniform Cartesian mesh, with finer mesh near walls to adequately resolve boundary layer, was used to discretize the computational domain. In order to check grid independence and qualitatively estimate the discretization errors, the grid convergence index (GCI) methodology based on Richardson extrapolation [34] was used. GCI has been recommended as a uniform method for reporting of grid convergence [35]. It is defined as

$$GCI_{fine} = \frac{F_s}{r_{21}^p - 1}\left|\frac{f_2 - f_1}{f_1}\right|, \tag{13}$$

where F_s is a factor of safety and is set to 1.25. The solutions on the three grids are denoted by f_1, f_2 and f_3 and the mean grid spacing by h_1, h_2 and h_3, respectively, with h_1 being the finest and h_3 being the coarsest grid. The parameter r_{21} represents the grid refinement factor defined as the ratio of grid spacing h_2 to h_1. For f values, either a local solution variable or a solution functional can be used [36]. The resulting order of convergence, p, is obtained by the solution of a transcendental equation [35].The p value so computed is valid only if the grids are in asymptotic range i.e. the following condition is satisfied [36]:

$$\frac{GCI_{coarse}}{r_{21}^p GCI_{fine}} = 1. \tag{14}$$

We used three grids consisting of 1.12 million (14.91 μm, 17.27 μm), 4.1 million (9.55 μm, 11.29 μm) and 15.05 million (6.16 μm, 7.35 μm) cells. The numbers in parenthesis indicate mean grid spacing in fluid and solid sub-domains respectively. The results for three grids are shown in Tables 2, wherein $T_{s,max}$–$T_{f,in}$ is used as the solution functional (i.e. f).

The ratio $\frac{GCI_{coarse}}{r_{21}^p GCI_{fine}}$ is close to one indicating that three grids are in asymptotic range. A similar analysis was performed by choosing the pressure drop as the functional (not shown for brevity) and that also resulted in this ratio being close to one. The GCI_{fine} and the GCI_{coarse} were small for both the solution functionals. Additionally, the relative change in solution functional values was smaller between mesh 2 and mesh 1 as compared to the corresponding change between mesh 3 and mesh 2. Therefore, mesh 2 with a total of 4.1 million cells is used for all further simulations.

5. Exergy based optimization

This section describes the formulation and solution methodology of the optimization problem. In essence this optimization problem deals not with the design of a heat sink as covered in the literature cited in Section 1 [13–16,18,19], but instead with defining the operating conditions of this heat sink so as to maximize the overall exergetic efficiency (i.e. the second law efficiency) of the cooling system as well as the thermal reliability of the electronic system being cooled. The design variables and objective functions for this optimization problem are described in the following section.

5.1. Design variables and objectives

The maximum chip temperature during operation decides its thermal reliability and the fluid outlet temperature provides a limit on the exergy extracted from the cooling system. For a steady computing load on the chip – which amounts to constant rate of heat dissipation – the maximum chip and the fluid outlet temperatures are functions of the fluid flow rate, $\dot{m}$, and the fluid inlet temperature, $T_{f,in}$. Therefore, $\dot{m}$ and $T_{f,in}$ are chosen as the design variables of the optimization problem. The two design objectives of maximizing the second law efficiency and the thermal reliability of the electronic chip are formulated next.

5.1.1. Exergetic efficiency

The second law efficiency of the cooling system is defined as [37]

$$\eta_{II} = \frac{Ex_{out}}{Ex_{in} + \dot{W}_{pump} + \dot{W}_{elect}} = \frac{Ex_{out}}{Ex_{in,tot}} \tag{15}$$

where the flow exergy Ex_j at jth location, with j indicating either inlet or outlet, is defined as

$$Ex_j = \dot{m}\left(h_j - h_0 - T_0(s_j - s_0) + \frac{1}{2}|\mathbf{U}|^2\right). \tag{16}$$

Ambient conditions of $T_0 = 25$ °C and $P_0 = 1$ atm are used to evaluate flow exergy in Eq. (16). In essence, the control volume for exergy analysis includes both the heat sink and the electronic chip and it is the exergetic efficiency of this combined system that is aimed to be optimized.

5.1.2. Normalized failure rate

It is important that we use a normalized value of the failure rate or MTTF so that the objective functions are in the same range of magnitude. The failure rate or MTTF can be normalized with the maximum values attained over the entire possible range of operation of the combined system. Hence, the normalized values can be expressed as:

$$\mathrm{MTTF}_{\mathrm{nm}}(T) = \frac{\mathrm{MTTF}(T)}{\mathrm{MTTF}_{\max}} = \mathrm{MTTF}(T)\lambda_{\min} \tag{17}$$

and

$$\lambda_{nm}(T) = \frac{\lambda(T)}{\lambda_{\max}}, \tag{18}$$

where the maximum and minimum values of instantaneous failure rate (i.e. $\lambda_{\max}$ *and* $\lambda_{\min}$ respectively) occur at maximum and minimum chip temperatures and the subscript *nm* indicates normalized value. The value of λ is obtained using Eqs. (3) and (4). The values of empirical constants are selected from [29] as $C_1 = 0.56$, $C_2 = 3.64 \times 10^{-4}(224)^{1.08}$, $E_a = 0.6$ eV and $\pi_E = 0.5$. As already mentioned, these values are only representative of a typical electronic chip as actual values are usually proprietary information.

Table 2
Discretization error and grid independence test using $T_{s,max}$-$T_{f,in}$ as solution functional.

Mesh	Number of cells (million)	r	$f = T_{s,max} - T_{f,in}$ (K)	p	GCI_{fine}	GCI_{coarse}	$\frac{GCI_{coarse}}{r_{21}^p GCI_{fine}}$
1	15.05	–	4.5340	1.7856	1.5591×10^{-3}	3.3836×10^{-3}	1.0015
2	4.1	1.5420	4.5274				
3	1.12	1.5420	4.5131				

5.2. Optimization approaches

This optimization problem can be solved by either combining the two objectives into a single function or by using the concept of Pareto optimality to find a trade-off between the two objectives.

5.2.1. Single objective optimization approach (net efficiency)

The second law efficiency from Eq. (15) and the normalized MTTF from Eq. (17) can be combined into a single parameter as

$$\eta_{net} = \frac{\text{Exergy}_{\text{actual,out}}}{\text{Exergy}_{\text{maximum,in}}} = \frac{\text{MTTF}Ex_{out}}{\text{MTTF}_{\max}Ex_{in,tot}} = \text{MTTF}_{\text{nm}}\eta_{II} \tag{19}$$

where η_{net}, the net efficiency, can be interpreted as the ratio of actual exergy extracted from the combined system to the maximum possible exergy that could ideally be absorbed by the system if it were to run for the maximum time before chip failure. The resulting single objective optimization problem is as below:

$$\text{Maximize} \quad \eta_{net} \tag{20}$$

subject to the constraints

$$\begin{aligned} \dot{m}_{\min} \leqslant \dot{m} \leqslant \dot{m}_{\max} \\ T_{f,in,\min} \leqslant T_{f,in} \leqslant T_{f,in,\max} \end{aligned} \tag{21}$$

where $\dot{m}_{\min}$, $T_{f,in,\min}$ and $\dot{m}_{\max}, T_{f,in,\max}$ are the lower and upper limits of the design variables.

5.2.2. Multi-objective optimization approach

We can also approach the optimization as a multi-objective problem with two essentially disparate objectives. For mathematical convenience, we define our multi-objective optimization as a minimization problem. The first objective function (F_1) is defined as the total exergy destruction expressed as a fraction of the input exergy

$$F_1 = 1 - \eta_{II} \tag{22}$$

Minimizing the total exergy destruction is equivalent to the concept of total entropy generation ($\dot{S}_{gen,tot}$) minimization [38] as $1 - \eta_{II} = \frac{T_0 \dot{S}_{gen,tot}}{\dot{E}x_{in,tot}}$. The second objective function (F_2) is chosen to be same as the normalized failure rate from Eq. (18) i.e.

$$F_2 = \lambda_{nm} \tag{23}$$

Thus, the multi-objective optimization problem is defined as:

$$\text{Minimize} \quad [F_1, F_2] \tag{24}$$

subject to the constraints as defined in Eq. (21)

5.2.2.1. Pareto optimality. The Pareto methodology is commonly used for solving multi-criteria optimization problems, where the best solution is often dependent upon a designer's preferences leading to what is often termed the best compromise solution. Typically, the aim is to identify feasible solutions that form what is termed as the Pareto optimal set or Pareto front. A feasible solution to a multi-criteria optimization problem is said to be Pareto optimal if there exists no other solution that will yield improvement in one criterion without worsening at least one other criterion [39]. Thus any solution on the Pareto front is 'non-dominated.' The solutions not lying on the Pareto front are dominated by the solutions lying on it. For a bi-objective minimization problem, the Pareto optimal set forms the south-western boundary of the criteria space.

Various methods have been reported in literature for approximation of the Pareto front [39]. Among these, the weighting method is the oldest and most commonly used method. Under this method, an overall objective function is defined as a weighted sum of the individual objective functions. Thus, the overall objective function to be minimized is given by

$$F = w_1 \cdot F_1 + w_2 \cdot F_2 \tag{25}$$

where w_1 and w_2 are the weights such that

$$w_1 + w_2 = 1 \tag{26}$$

Then, a single objective optimization for different combinations of the weights yields various solutions in the criteria space, from which the Pareto front can be identified. The disadvantage of using the weighting method is that it is able to describe the Pareto front only if the Pareto set is strictly convex [39]. Other methods to circumvent this issue have been reported in literature. However, as shown in Section 6, the Pareto set for the optimization problem under consideration here is indeed convex and thus we will use this method for the approximation of the Pareto front.

5.2.2.2. Multi-criteria Decision Analysis (MCDA). Finally, the best feasible solution, from the point of view of the designer, can be selected from amongst the multiple alternatives comprising the Pareto optimal set. This problem belongs to Multi-criteria Decision Analysis (MCDA) [40]. There are various methods, with their own advantages and disadvantages reported in literature [41,42]. Among these, TOPSIS (Technique for Order Preference by Similarity to Ideal Solutions) and MAUA (Multi-attribute Utility analysis) method are flexible and thus can be used for dissimilar criteria. These methods can rank the various available alternatives. MAUA also accounts for the worth of a particular criterion to the decision maker and thus decision is not based on values of various criteria alone. This method has been applied successfully to a variety of decision making problems [21,41]. Hence, we have selected these two methods for our optimization problem.

In the TOPSIS method, first an ideal solution is defined as the one having the best values of all the criteria. Next, for all the available alternative solutions, the criterion values are suitably normalized. Then the best or the preferred solution is the one that has minimum deviation from the ideal solution [42]. In the MAUA approach, the utility of design is defined for each criterion according to the worth of the criterion to the decision maker. It can be a non-linear function of the absolute value of the criterion. A utility function U_i for ith criterion varies from 0 to 1 as the value of the criterion varies from its worst to the best level. These utility functions can then be combined as

$$U = \sum_i K_i U_i, \tag{27}$$

where K_i is the scaling parameter for utility U_i and reflects the acceptable trade-off between attributes. K_i can be defined as the overall utility of the design when the ith attribute is at its best level and all other attributes are their respective worst levels. The individual utility functions U_i and the scaling parameters K_i can be derived by using the certainty equivalent method [41]. For method illustration, we assume some salient forms of these functions in Section 6.3.2.

6. Results and discussion

6.1. Model validation

Experimental measurements made for $\dot{m}$ values between 0.3 to 1 l/min in steps of 0.1 l/min and at 4 different water inlet temperatures, $T_{f,in}$, between 30 °C and 60 °C were used to validate the numerical simulations. The heat dissipation from the chip, $\dot{Q}_{chip}$, was kept constant at 100 W. Fig. 3 shows the validation of the model in terms of predictions for the water temperature at the heat sink outlet, $T_{f,out}$ As evident from Fig. 3, the single microchannel model

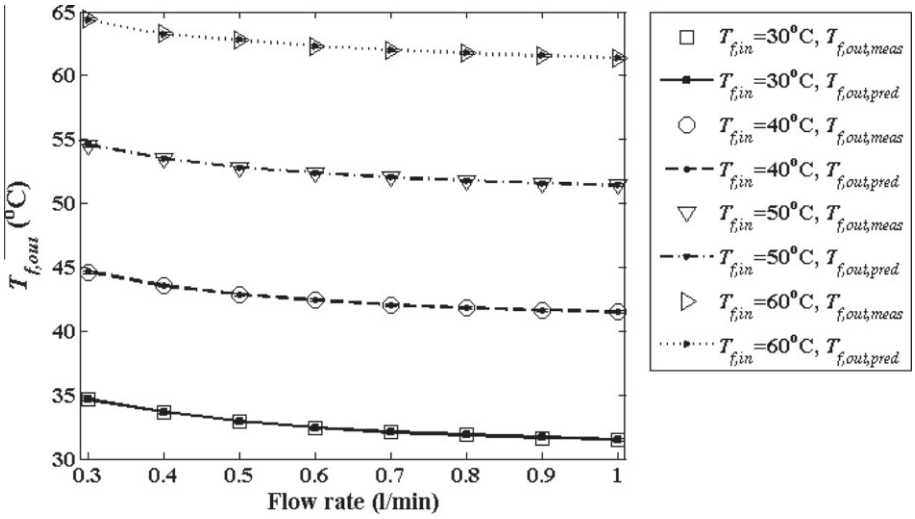

Fig. 3. Model validation against experiments.

is able to capture well the heat absorbed by water as it flows through the microchannels of the heat sink. However, the chip level maximum temperature is not predicted as closely and the predictions deviate from experimental measurements by 6–7 °C. A possible explanation for this deviation is the unavoidable error introduced by the assumption of uniform mass distribution of the coolant across all the channels due to the lack of better information. This is because the fluid enters the inlet manifold as a jet which induces non-uniform distribution of coolant among the channels [11]. Another possible contribution to this error can come from the assumption of uniform distribution of heat dissipation from the heating test chip. A future numerical analysis of flow in the full heat sink will aim at capturing this behavior.

With respect to the optimization problem, $T_{s,\max}$ is used to compute the normalized failure rate using Eq. (3), Eq. (4) and Eq. (18), but it does not appear in the exergetic efficiency calculation (c.f. Eq. (15)). The deviation in $T_{s,\max}$ predictions, however, causes only about 5% variation in normalized failure rate estimation using Eq. (18).

6.2. Thermal performance of the heat sink

The most important performance measure of a heat sink is its thermal resistance defined as:

$$R_{th} = \frac{A_{chip}(T_{s,\max} - T_{f,in})}{\dot{Q}_{chip}} \tag{28}$$

where A_{chip} is the chip area of 2.11 cm^2. The variation of the predicted thermal resistance with flow rate for four different $T_{f,in}$ values is shown in Fig. 4(a). Thermal resistance sharply decreases with increasing flow rate due to higher heat transfer coefficient at higher flow rates.

The behavior of the heat transfer coefficient can be analyzed in terms of the Nusselt number (Nu). The numerical results are processed to extract the local Nu variation along the channel length, defined as

$$Nu(x) = \frac{h(x)D_h}{k_f(x)} \tag{29}$$

where the local heat transfer coefficient $h(x)$ at any axial location x can be expressed as

$$h(x) = \frac{\dot{q}_{w,avg}(x)}{T_{w,avg}(x) - T_{f,bulk}(x)} \tag{30}$$

where $\dot{q}_{w,avg}(x)$ denotes the average wall heat flux and $T_{w,avg}(x)$ the average wall temperature at any axial location x. These are calculated as

$$\dot{q}_{w,avg}(x) = \frac{1}{l_{intf}(x)}\left(\int_{l_{intf}(x)} \dot{q}_w(x,y,z)dl\right) \tag{31}$$

$$T_{w,avg}(x) = \frac{1}{l_{intf}(x)}\left(\int_{l_{intf}} (x)T_w(x,y,z)dl\right) \tag{32}$$

with l_{intf} (i.e. the length of the solid-liquid interface at any axial location x) spanned during integration in the following manner:

$$l_{intf}(x) = \begin{cases} \frac{W_{ch}}{2}|_{intf}, z = H_s + H_{ch}|_{intf}, H_s < z < H_s + H_{ch} + \frac{W_{fin}}{2}|_{intf}, z = H_s + H_{ch} \\ \qquad \text{if } \begin{cases} (0 \leqslant x \leqslant \frac{W_{nozzle,in}}{2}) \\ (\frac{L}{2} - W_{nozzle,out} \leqslant x \leqslant \frac{L}{2}) \end{cases} \\ \frac{W_{ch}}{2}|_{intf}, z = H_s + H_{ch}|_{intf}, H_s < z < H_s + H_{ch} + \frac{W_{ch}}{2}|_{intf}, z = H_s + H_{ch} \\ \qquad \text{if } \left(\frac{W_{nozzle,in}}{2} < x < \frac{L}{2} - W_{nozzle,out}\right) \end{cases} \tag{33}$$

The fluid bulk temperature at any axial location x, $T_{f,bulk}(x)$, is calculated on a plane through the fluid domain, normal to the channel axial direction as

$$T_{f,bulk}(x) = \frac{\int_{A(x)} \rho_f c_{p,f} T_f(x,y,z)|\mathbf{U}\cdot\mathbf{n}|dA(x)}{\int_{A(x)} \rho_f c_{p,f}|\mathbf{U}\cdot\mathbf{n}|dA(x)} \tag{34}$$

Here $A(x)$ is the area of the plane under consideration at location x and $\mathbf{n}$ is the normal to the plane (which is the unit vector in the channel axial direction for all the planes). In order to calculate these quantities, 300 equally spaced axial locations are considered. Fig. 4(b) shows the variation of the Nusselt number along channel length for three different (low, intermediate and high) coolant flow rates and one inlet temperature. The behavior of Nu for other flow rates and fluid inlet temperatures is similar and is not shown for brevity.

As the flow rate increases, the heat transfer coefficient values also increase over almost the entire axial length span of the channel from inlet to outlet nozzle. Normally, the heat transfer coefficient for fully developed laminar flow is independent of the flow Reynolds number. However, in case of flow inside a microchannel of a manifold microchannel heat sink, the flow enters as a slot jet, impinges on the channel floor and then reattaches to the channel upper wall after traveling a significant fraction of the channel length. Hence, the flow is developing over most of the channel axial

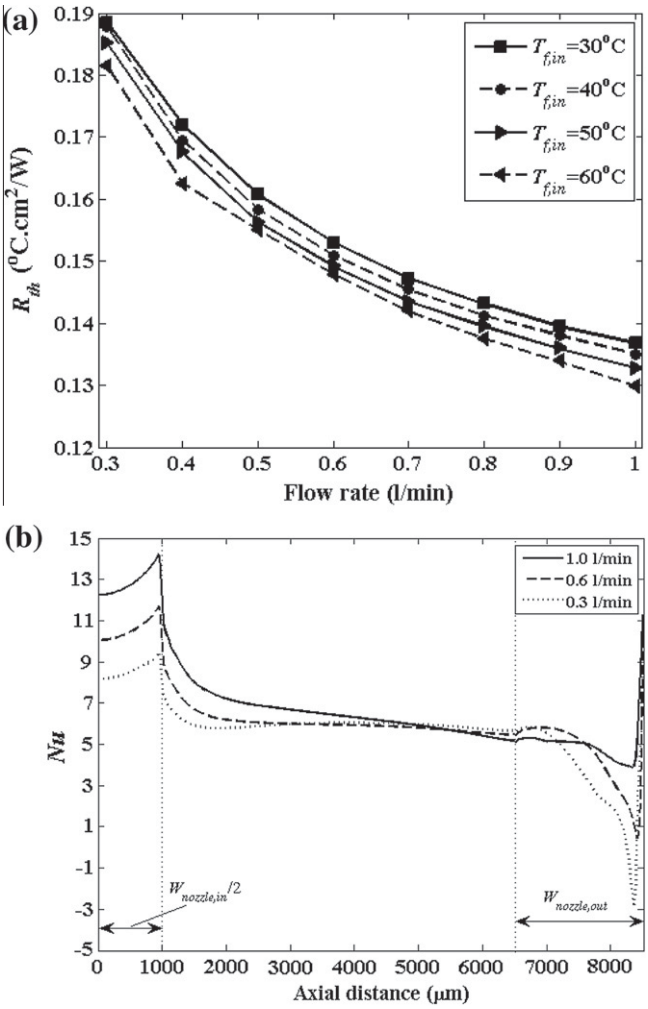

Fig. 4. (a) Thermal resistance of the heat sink at various operating conditions and (b) variation of Nu along channel length (for $T_{f,in}$ = 60 °C).

length and increasing the flow rate (and thus flow Reynolds number) leads to an increase in the heat transfer coefficient. This explains the decreasing thermal resistance with increasing flow rates. The flow pattern inside a microchannel is evident from the velocity vectors shown in Fig. 5(a).

For every flow rate value, Nu first increases steadily, starting from the symmetry plane in inlet slot nozzle (i.e. $x = 0$ in Fig. 4(b)), till $x = 1000$ μm. This is the point where the inlet nozzle region ends. In this region, Nu increases due to the thinning of the thermal boundary layer due to flow impingement [13]. For $x > 1000$ μm, the thermal boundary layer grows with increasing x and the heat transfer coefficient is reduced. Nu curves for different flow rates merge in the second half of the rectangular channel length as the flow approaches the fully developed laminar flow condition for a short time during its travel through the microchannel. Beyond this point the curves again split as the fluid moves into the outlet nozzle region. In the outlet nozzle region, Nu turns negative for the lower flow rates. At lower flow rates, the fluid temperature next to wall becomes slightly higher than the wall temperature in the outlet nozzle region thus locally reversing the direction of heat flux and sign of the numerator in Eq. (30). However, the bulk mean temperature of the fluid, $T_{f,bulk}$ remains lower than the average wall temperature $T_{w,avg}$. As a result, the heat transfer coefficient in Eq. (30) and Nu in Eq. (29) become negative. Temperature contours in the fluid and the solid are shown in Fig. 5(b). As the channel end wall is approached, the heat transfer coefficient increases sharply in a thin region next to the wall. This sharp jump in heat transfer coefficient and Nu is caused by the local increase in the heat flux from the wall due to fluid recirculation over the outlet nozzle corner.

Since for any given fluid inlet temperature $T_{f,in}$, the heat transfer coefficient increases with increase in flow rate, the temperature differential, $T_{w,avg}(x) - T_{f,bulk}(x)$ required for same amount of heat transfer from solid to fluid reduces. Thus, exergy destruction due to heat transfer over a finite temperature differential is also reduced [37]. On the other hand, the exergy loss due to fluid pressure drop increases at higher flow rates. However, in the case of liquid cooling, the contribution of the pressure drop term to the exergy destruction (in the form of pumping power, $\dot{w}_{pump}$, see Eq. (15)) is less than 0.25% and therefore negligible as compared to other terms for the range of flow rates considered. Another component that is accounted for in the exergy efficiency but has negligible contribution to the overall analysis is the fluid kinetic energy $\frac{1}{2}\dot{m}|\mathbf{u}|^2$ (see Eq. (16)). Its contribution to flow exergy at microchannel inlet/outlet is less than 0.04%. Hence, as the flow rate increases, the exergetic efficiency increases at any fluid inlet temperature. This trend is shown in Fig. 6, which clearly shows that exergetic efficiency also increases with increase in fluid inlet temperature at any given flow rate. This is due to the increase in exergy content of the fluid at both inlet and outlet to the heat sink with increase in $T_{f,in}$ and a resulting relatively larger change in Ex_{out} than $Ex_{in,tot}$ (see Eq. (15)).

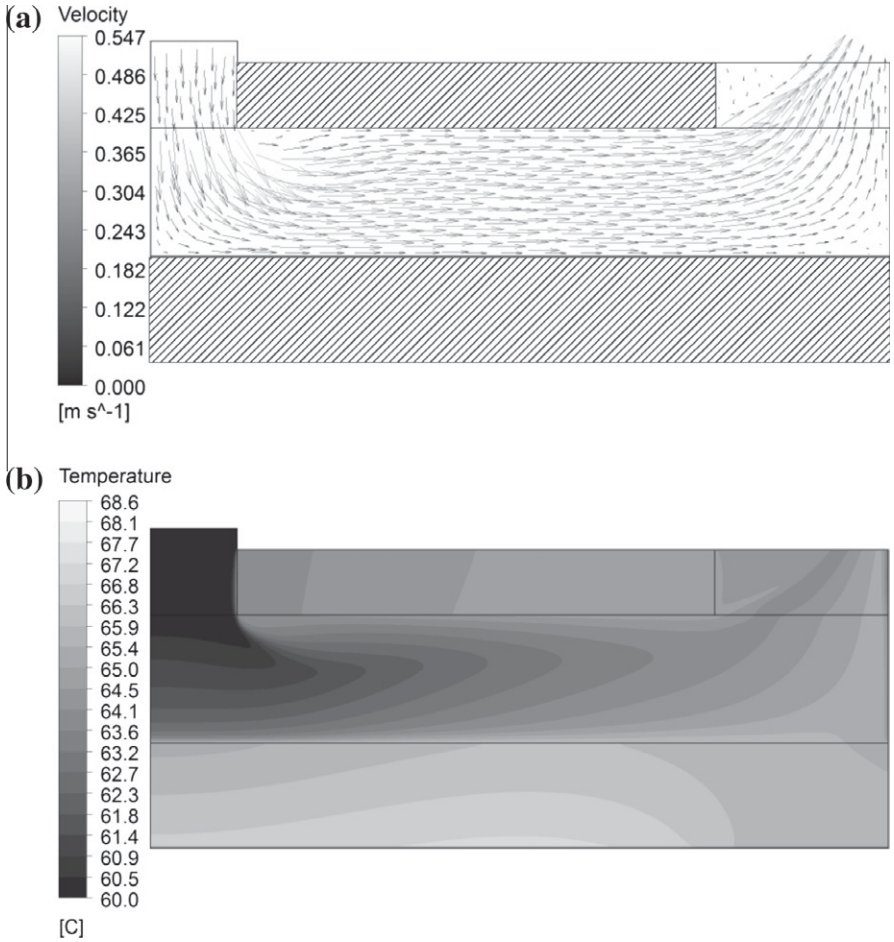

Fig. 5. (a) Velocity vectors in microchannel at coolant flow rate of 0.3 l/min (hatched region indicates solid) and (b) temperature contours in microchannel (at coolant flow rate of 0.3 l/min and $T_{f,in}$ = 60 °C).

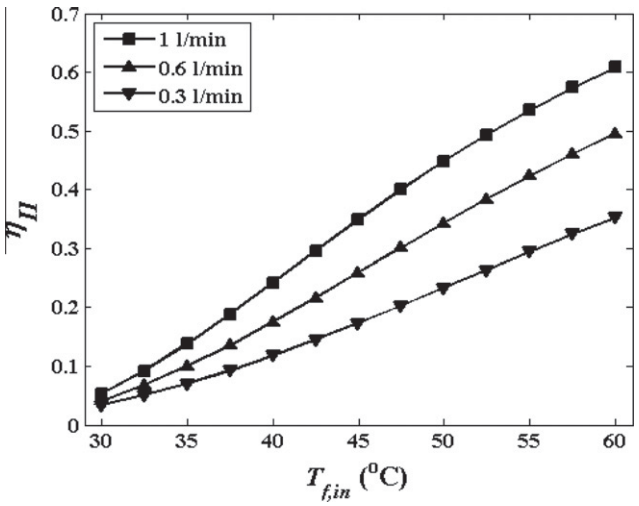

Fig. 6. Variation of second law efficiency (computed using Eq. (19)) with change in operating conditions.

6.3. Optimization of the operating conditions

The optimal operating values for heat sink design variables are determined in this section. In order to increase the number of operating conditions populating the design variable space, we first simulate the heat sink performance at intermediate fluid inlet temperatures, $T_{f,in}$ in addition to the ones at which measurements were performed. In order to estimate the heat loss boundary condition (see Eq. (5)) at these intermediate temperatures, we linearly interpolate the measured heat loss to ambient at the four temperatures at which the experiments were performed. In this manner, the heat sink operation was analyzed at $T_{f,in}$ values in the range of 30–60 °C with a resolution of 2.5 °C (see Fig. 6).

6.3.1. Net efficiency approach

The net efficiency, η_{net}, leads to a single objective maximization problem as defined by Eq. (20) and constraints Eq. (21). This parameter has a maximum as the fluid inlet temperature is varied at given flow rate (Fig. 7(a) for a flow rate of 1 l/min). As the fluid inlet temperature increases, the second law efficiency, η_{II}, improves. However, the reliability and $MTTF_{nm}$ worsen (see Eqs. (2) and (17)) due to increase in the maximum temperature of chip and thus instantaneous failure rate (see Eqs. (3) and (4)). For flow rate of 1 l/min, the maximum η_{net} is located at $T_{f,in}$ = 45 °C. Similarly the maximum point can be located by spanning over all the operating conditions, Fig. 7(b).

The operating conditions corresponding to maximum net efficiency do not change below 0.8 l/min in Fig. 7(b). However, if more intermediate operating conditions between 45 °C and 47.5 °C are simulated, then the optimum operating condition line corresponding to the locus of maximum net efficiency will slope gradually. This becomes more evident if the locus of maximum net efficiency is plotted as a function of $T_{s,max}$. The resulting figure is similar to Fig. 7(b) and hence not shown for brevity. However, the solution

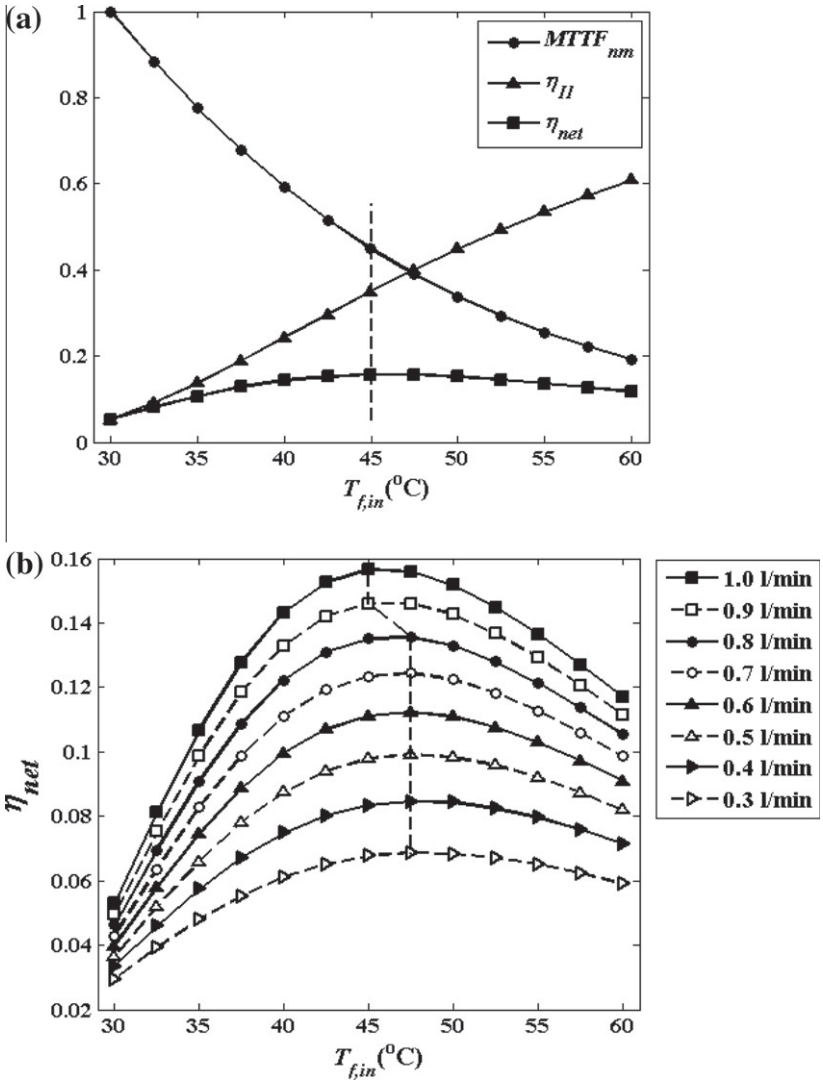

Fig. 7. Optimization using net efficiency. (a) Illustration of maximum in net efficiency for flow rate of 1 l/min and (b) net efficiency curves and maxima for various flow rates, as function of water inlet temperature $T_{f,in}$.

following this approach is unique as the maximum net efficiency occurs at the highest flow rate. Thus, optimum operating conditions are a flow rate of 1 l/min and a fluid inlet temperature of 45 °C. As discussed before, this approach masks other possible solutions and fails to accommodate specific preferences of the designer in terms of which of the two criteria is considered more or less important for operation. This is improved by the multi-objective optimization approach.

6.3.2. Multi-objective optimization approach

In order to approximate the Pareto front, for each flow rate, different combinations of weights w_1 and w_2 are chosen. For every such combination, F (see Eq.(25)) is calculated for all fluid inlet temperatures $T_{f,in}$ The value $T_{f,in}$ for which F is minimum is selected and this yields one point in the criteria space for that flow rate. In other words, for ith flow rate and jth combination of weights, a point in criteria space can be obtained using

$$F_{i,j} = \min_{k}(w_{1,j}F_{1,(i,k)} + w_{2,j}F_{2,(i,k)}) \tag{35}$$

where k spans over all the fluid inlet temperatures for the ith flow rate. A total of 41 combinations of weights were required to uncover all the unique points in the criteria space for each flow rate. These points are plotted in the criteria space, from which the Pareto front is easily recognized as the south-west boundary of the data as shown in Fig. 8(a).

As evident from the figure, the Pareto front is formed at the highest flow rate. This is natural since the exergy destruction is minimal at the highest flow rate. The Pareto front is convex and therefore the method of weighted combination of objective functions works well for this problem. A total of 12 points appear on the Pareto front for the 41 combinations of the weights w_1 and w_2. This occurs because multiple combinations of weights yield the same $F_{i,j}$ in the criteria space, as becomes clear from Fig. 8(b), which shows the combined objective function F as a function of the fluid inlet temperature for 1 l/min and different combination of weights. Note that curves corresponding to only some of the weight combinations have been plotted in Fig. 8(b) for the sake of clarity. The minima plotted in Fig. 8(b) correspond to the points on the Pareto front from right to left in Fig. 8(a) and are listed in Table 3. Therefore, using the Pareto optimality, we achieve multiple non-dominated solutions on the Pareto front. Next, we employ the MCDA methodologies of TOPSIS and MAUA, as described in Section 5.2.2.2, to choose the best condition among these feasible solutions.

According to the methodology of TOPSIS, we first define the ideal or utopian solution. Typically, this represents a preferred

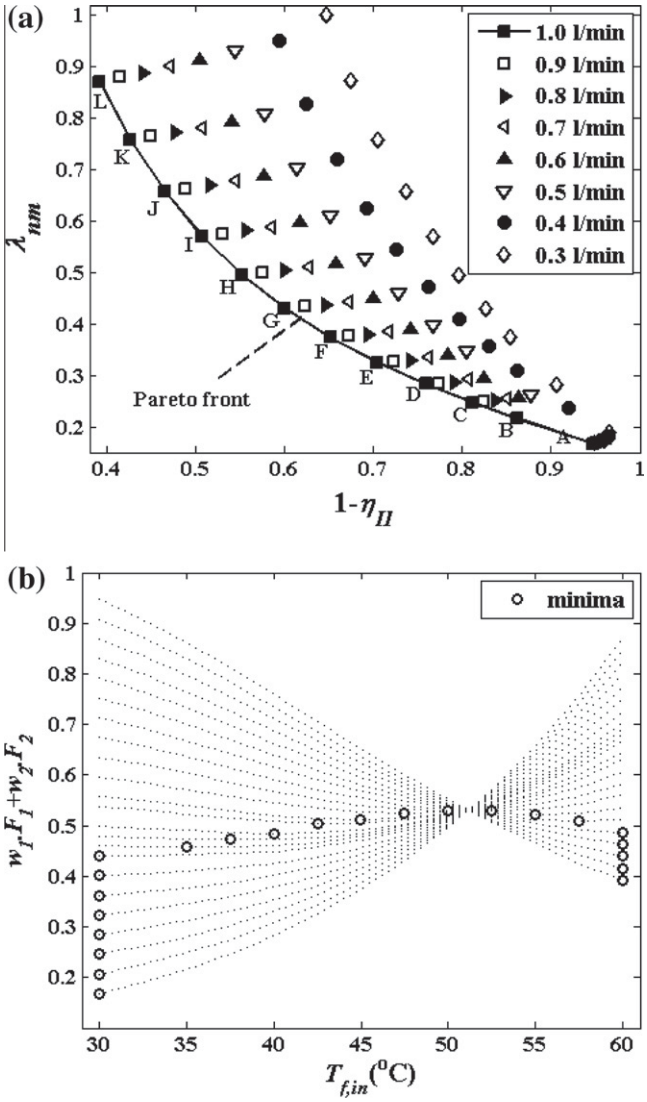

Fig. 8. (a) Pareto front: south-west boundary of criteria space consisting of the two criteria of normalized failure rate λ_{nm} and exergy destruction $(1-\eta_{II})$ and (b) variation in combined objective function F with weight combinations for a flow rate of 1 l/min.

ideal target of a designer. Therefore, to illustrate the concept, we define it here as the solution corresponding to minimum exergy destruction and minimum normalized thermal failure rate from among the points plotted in the criteria space shown in Fig. 8(a). This utopian solution is shown in Fig. 9. Then, the best solution is the point with minimum deviation from the ideal solution as below:

$$S_{best} = \min_k((\lambda_{nm,k}-\lambda_u)^2 + (\eta_{II,k}-\eta_{II,u})^2)_{k=1 \text{ to } N_p} \quad (36)$$

where S_{best} is the Euclidean distance of the best solution point on the Pareto front from the utopian point, N_p is the total number of points on the Pareto front and subscript u indicates criteria values corresponding to the utopian solution. Using TOPSIS, point F is chosen as the best solution with flow rate of 1 l/min and fluid inlet temperature of 45 °C (refer Table 3).

In order to use MAUA, the utility functions for both the attributes of thermal reliability and second law efficiency have to be available. In order to illustrate this methodology, we assume two hypothetical non-linear utility functions U_1 and U_2 for exergy destruction and normalized failure rate, respectively, as:

$$U_1 = -2.42(1-\eta_{II})^2 + 1.54(1-\eta_{II}) + 0.76 \quad (37)$$

$$U_2 = 1.15\lambda_{nm}^2 - 2.55\lambda_{nm} + 1.39 \quad (38)$$

Thereafter, depending on the choice of the scaling parameters, the individual utility functions can be combined using Eq. (27) to analyze the overall utility of all the design alternatives available from the Pareto front. The overall utility is plotted in Fig. 9 for two combinations of the scaling factors. The best solution among the available alternatives is the one with maximum overall utility to the designer i.e.:

$$U_{best} = \max_k(K_1U_{1,k} + K_2U_{2,k})_{k=1 \text{ to } N_p} \quad (39)$$

The best designs obtained with two combinations of scaling factors are points D and G in Fig. 9. These design choices are flow rate, $T_{f,in}$ of 1 l/min and 40 °C and 1 l/min and 47.5 °C, respectively (c.f. Table 3). The first design choice reflects higher preference towards maximization of electronic reliability than exergetic efficiency (as $K_1 < K_2$) while the opposite is true for the second design choice. The second design is more suitable for energy reuse as the fluid temperature at the exit is higher (nearly 49 °C). Modern electronic chips can withstand maximum chip temperatures in the range of 85–90 °C and can have lower instantaneous failure rates than considered here. An important change in the trade-off is possible when electronics have built in fault tolerance or re-configurable "spare parts". In such a case the MTTF is lengthened to a level when all the spare components are used up. This allows an optimization of the lifetime exergy recovery in the single parameter case and an increase in the exergy utility function in the multi-objective optimization approach. Hence, the designer can further push the trade-off in favor of exergetic efficiency (higher K_1) by simultaneously keeping an eye on reduction in chip reliability at higher temperatures. The methodology presented here provides a systematic way to achieve such trade-offs.

7. Conclusions

The thermal performance and optimal operating conditions of a hot water cooled manifold microchannel heat sink for electronic chip cooling has been analyzed. A 3D conjugate single-channel heat transfer model is developed to evaluate the heat sink performance and validated against experimental measurements. The heat sink is used as an example to illustrate that a trade-off exists

Table 3
Non-dominated solutions on Pareto front.

Point	Flow rate	$T_{f,in}$ (°C)	λ_{nm}	$1-\eta_{II}$	Point	Flow rate	$T_{f,in}$ (°C)	λ_{nm}	$1-\eta_{II}$
A	1 l/min	30	0.95	0.17	G	1 l/min	47.5	0.60	0.43
B		35	0.86	0.22	H		50	0.55	0.49
C		37.5	0.81	0.25	I		52.5	0.51	0.57
D		40	0.76	0.28	J		55	0.47	0.66
E		42.5	0.70	0.32	K		57.5	0.43	0.76
F		45	0.65	0.37	L		60	0.39	0.87

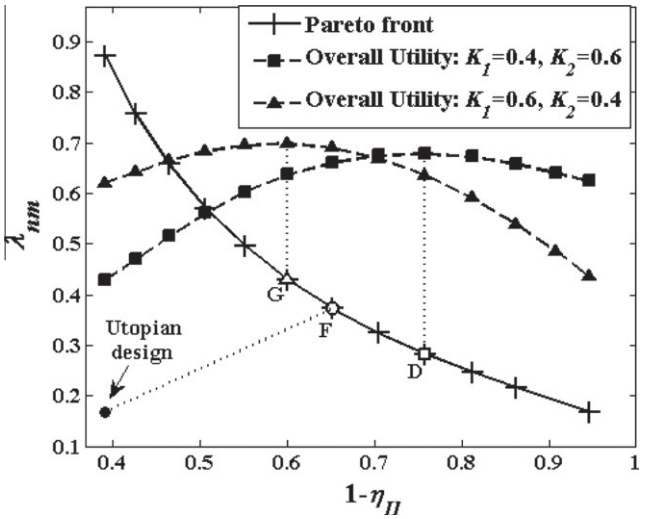

Fig. 9. Choice of design on Pareto front using TOPSIS and MCDA methods.

between two conflicting objectives of performance maximization; chip thermal reliability exergetic efficiency of the overall system (consisting of both the heat sink and the chip being cooled).

We show that the optimal operating conditions for chip cooling can be obtained via two different approaches: (a) a single objective maximization problem by defining a net efficiency of the overall system and (b) a multi-objective optimization approach using Pareto optimality to achieve multiple alternative trade-offs. To illustrate the fundamental framework put forth in this paper, the thermal reliability of the chip is estimated using a representative failure rate function from open source literature. This failure rate function is a conservative estimate given the tremendous progress in state-of-the-art microprocessors for which the failure rates are typically proprietary information. For the chip under consideration, an optimum coolant inlet temperature ($T_{f,in}$) in the range 40–47.5 °C is obtained at an optimum flow rate of 1 l/min, depending on the optimization technique employed. The methodology illustrated herein, provides a systematic approach to maximize the potential of reuse of heat recovered from the electronic chip and simultaneously ensure high thermal reliability for the chip being cooled.

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