EXPERIMENT NO-06

TITLE OF THE EXPERIMENT: Flip-Flop

AIM: Design, test and investigation of S-R Flip-Flop, D Flip-Flop and J-K Flip-Flop.

APPARATUS/COMPONENTS REQUIRED:

Sl. no.	Name of the equipment/component	Specification	Quantity
1	Trainer board	Digital	1 no
2	2 input NAND gate	IC 7400	1 no
3	3 input NAND gate	IC 7410	2 no
4	NOT gate	IC 7404	1 no
5	J-K Flip-Flop	IC 7476	1 no
6	Connecting wires	Hook up	As required

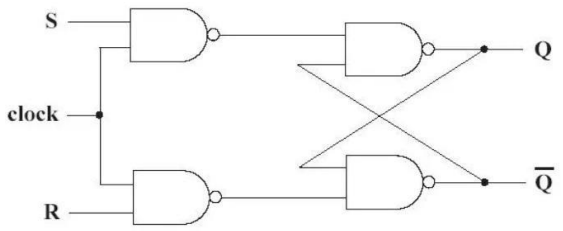
THEORY: Flip-Flops are the basic building blocks of most sequential circuits in which output at any instant not only depends upon the present input but also depends upon the past value of this inputs. A Flip-Flop is known formally as a bi-stable multi vibrator.

S-R Flip-Flop: The Set-Reset (SR) Flip-Flop refers to a Flip-Flop that obeys the truth table shown in this figure below. It has two inputs, namely, a Set input or S, and a Reset input, or R. It also has two outputs, the main output Q and its complement of Q.

Truth table: S-R Flip-Flop

Clk	S	R	Output (Q_n)
↑	0	0	Previous value(last value)->Q_{n-1}
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	1	Indeterminate

Logic diagram: S-R Flip-Flop

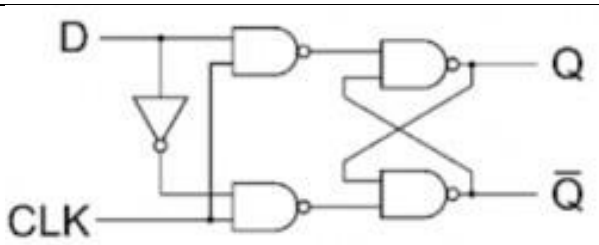


The D Flip-Flop: The D-type Flip-Flop is just a clocked Flip-Flop with a single digital input D. Every time a D-type Flip-Flop is clocked, its output follows whatever the state of D is.

Truth table: D Flip-Flop

Clk	D (input)	Q_n (output)
↑	0	0
↑	1	1

Logic diagram: D Flip-Flop

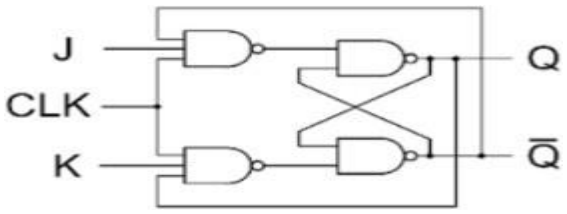


The J-K Flip-Flop: J-K Flip-Flop is very versatile and also the most widely used. The functioning of the J-K Flip-Flop is identical to that of the S-R Flip-Flop, except that it has no invalid state like that of S-R Flip-Flop

Truth table: J-K Flip-Flop

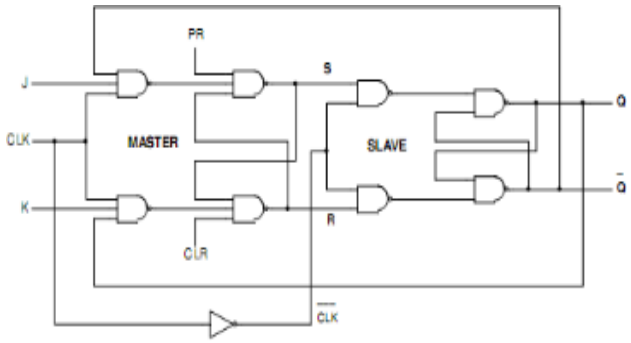
Clk	J (Input)	K (Input)	Output (Q_n)
↑	0	0	NC(No Change)=(Past value) -> Q_{n-1}
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	1	Toggle (Complement of previous output) -> Q_{n-1}'

Logical diagram: J-K Flip-Flop

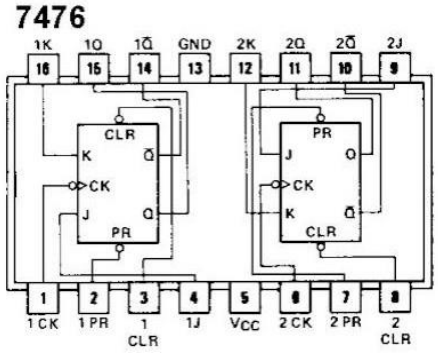


Master-Slave Flip-Flop: The Master-Slave Flip-Flop is used to avoid the problem of logic race in clocked Flip-Flops. Slave follows Master. Whatever the output of Master, same output results in Slave. So truth table as like as J-K Flip-Flop. Two inputs (PR)', (CLR)' are low input systems. Only one can be applied at a time (either (PR)' or (CLR)'). To set the Flip-Flop (PR)' is used and to clear (reset) the Flip-Flop (CLR)' is used.

Logic diagram: Master-Slave Flip-Flop

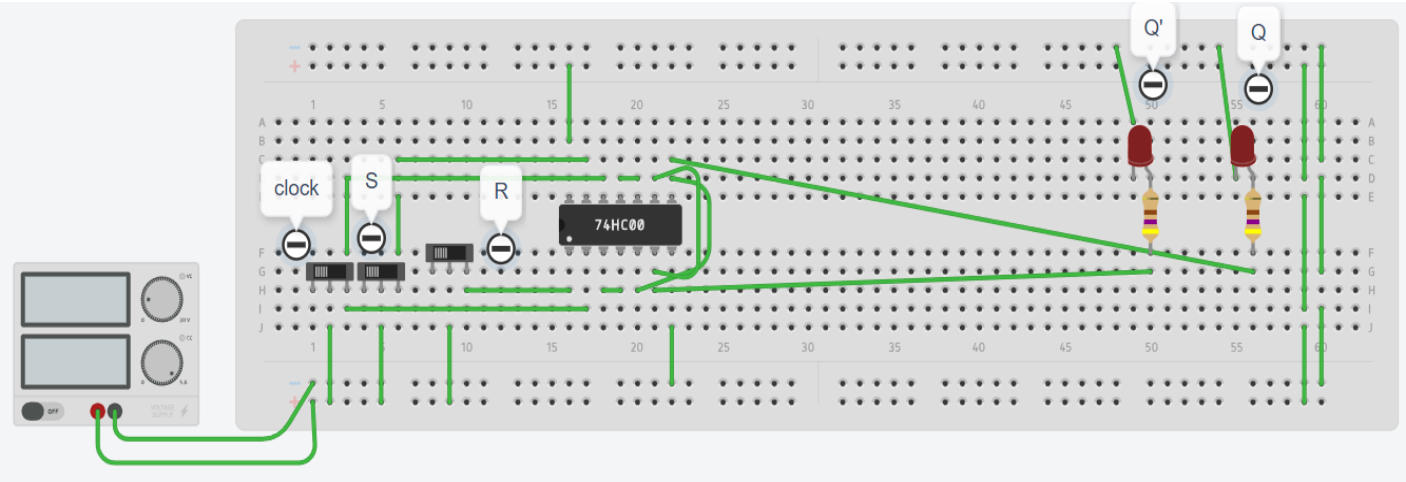


Pin Out diagram: IC 7476

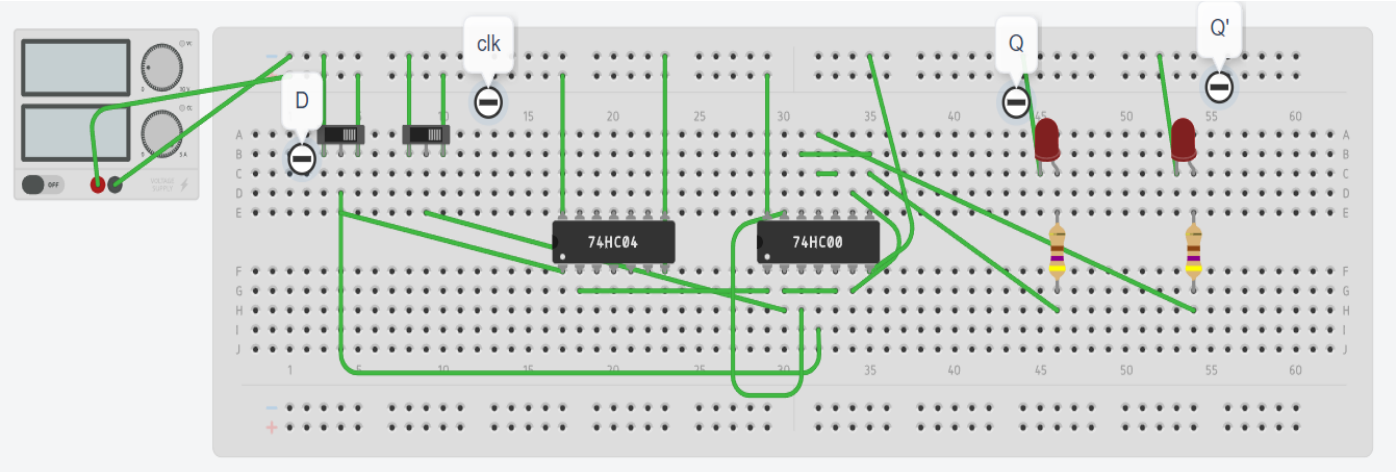


CIRCUIT DIAGRAM:

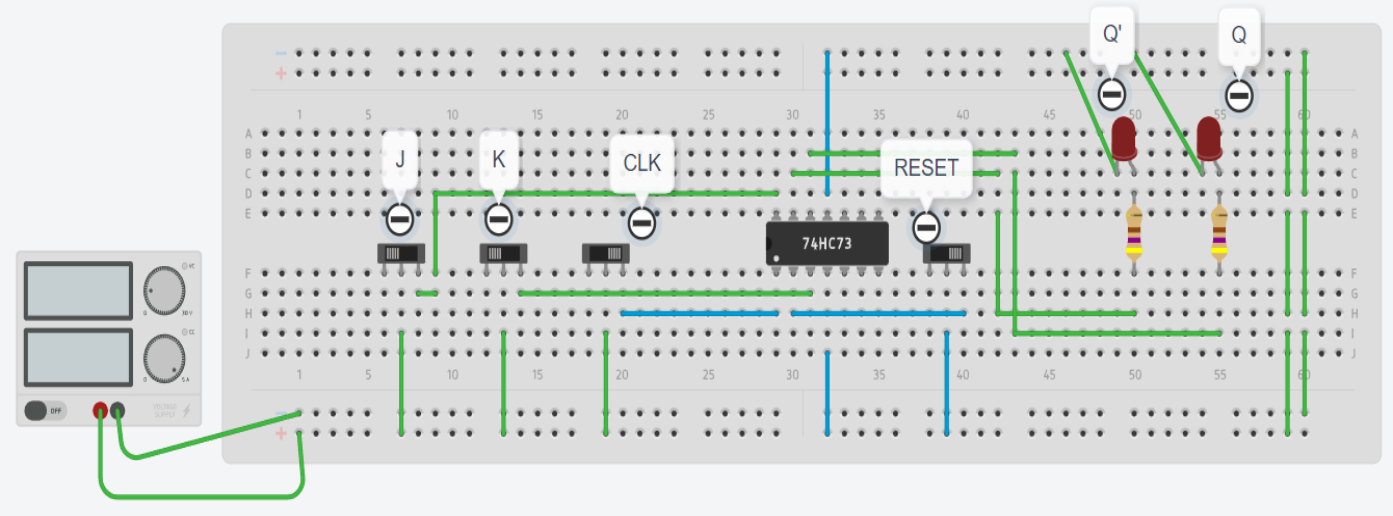
S-R Flip-Flop:



D Flip-Flop:



J-K Flip-Flop:



OBSERVATION:

Observation table: S-R Flip-Flop					
Clock Pulse	Input		Output		
	S	R	Q	Q'	Comment
↑	0	0	Previous value	Previous value	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Indeterminate	Indeterminate	Forbidden

Observation table: D Flip-Flop				
Clock Pulse	Input (D)	Output		
		Q	Q'	Comment
↑	0	0	1	Reset Q>>0
↑	1	1	0	Set Q>>1

Observation table: J-K Flip-Flop					
Clock Pulse	Input		Output		
	J	K	Q	Q'	Comment
↑	0	0	Previous Value	Previous Value	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Compliment of previous value	Compliment of previous value	Toggle

PROCEDURE:

1. Design the logic circuit.
2. Switch off the trainer board before assembling the circuit and doing the connection.
3. Assemble the circuit on the breadboard as per the circuit diagram.
4. Connect the positive supply and ground correctly to the circuit.
5. Provide the logic inputs required to verify the truth table.
6. Check whether all connections are correct before switch on the trainer board.
7. Switch on the trainer board.
8. Observe the output and verify the truth table according to the observation table.

CONCLUSION:

From this experiment we learnt Design, test and investigation of S-R Flip-Flop, D Flip-Flop and J-K Flip-Flop.

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