2 marks

1) . Identify the size of the decoder required to generate addresses for a 1Kb memory chip which has 8-bit word size.

1kb=1024=2^10

8bit =2^3

Answer=2^10/2^3=128

2) 2. Define Programmable Logic Device and enumerate its types

2. Programmable Logic Devices:

The circuits in programmable logic devices can be programmable as per requirement.

- PLD is an integrated circuit with internal logic gates that are connected through electronic fuses.
- The gates in a PLD are divided in to an AND array & an OR array to provide an AND-OR sum of product implementation.

- The main advantage of PLD approach is that PLD can be easily configured by the individual user for specific application.

There are 3 types of PLDs based on which of the arrays are programmable.
1. Programmable Read – only Memory (PROM)
2. Programmable Array Logic (PAL)
3. Programmable Logic Array (PLA)

3. What is the constraint in encoder and mention its remedial measure.

Limitation of Encoder:
One of the main drawbacks of conventional (standard) encoder is, if the value of more than one input bits becomes 1 then encoder output will be in undetermined state. To overcome this problem, it has to "Prioritise" the level of each input and if more than one input bits are 1, then the output would only correspond to the input with the highest designated priority. Then this type of digital encoder is commonly known as **priority Encoder**.

4. Convert the following from Gray code to binary code
   0010   ii) 0011   iii)1110   iv) 1100
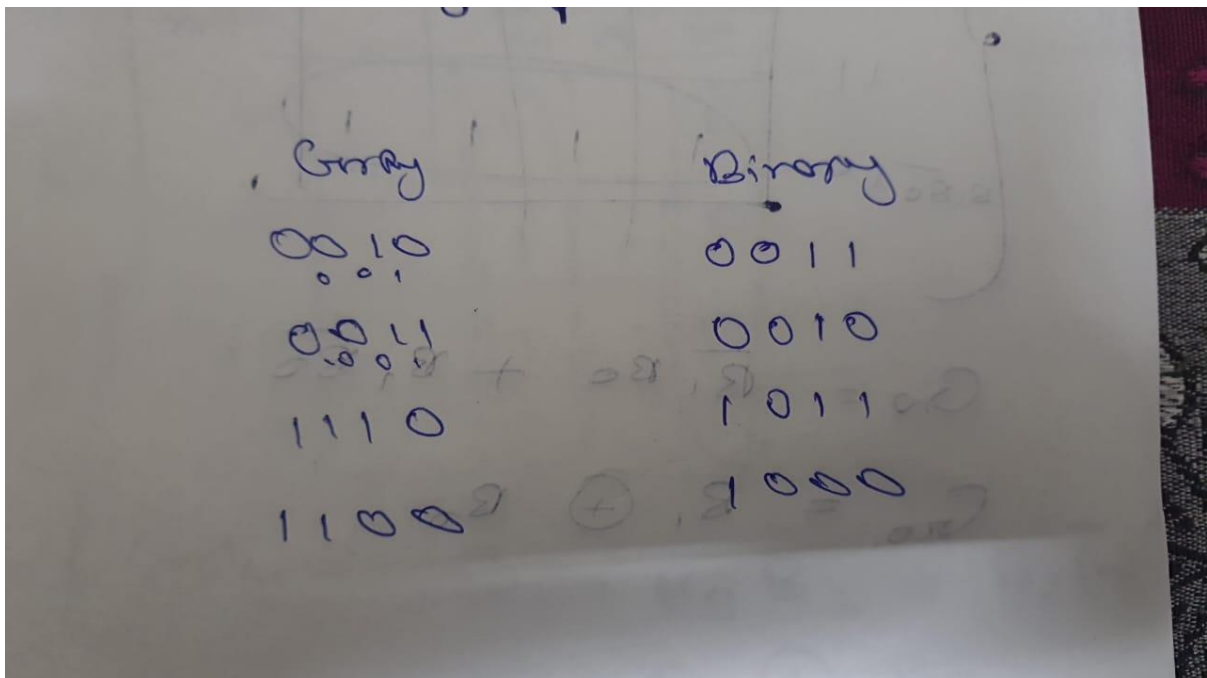
5. What is meant by sequential logic circuit? Give an example.

Sequential circuits refer to the combinational logic circuits that consist of input variables (X) and logic gates (or Computational circuits) along with the output variable (Z). For example, flip-flops, counter, register, clocks, etc.

7. Why multiplexer is referred as data selector?

circuit that selects binary information from one of many input lines and transmits it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Multiplexer is also called as a data selector. It is abbreviated as MUX. The block

8. If a memory unit is represented by 2 n x m, in this what is "n" and "m"?

In the context of a memory unit represented by $2^{(n \times m)}$, the variables "n" and "m" typically refer to the dimensions of the memory array.

* "n" usually represents the number of rows in the memory array.
* "m" typically represents the number of columns in the memory array.

So, $2^{(n \times m)}$ denotes a memory unit with $2^{(n \times m)}$ storage locations, where each location can store a binary value (0 or 1). The total number of storage locations is determined by the product of the number of rows (n) and the number of columns (m) in the memory array.

9. Mention the PLD which has programmable AND array and fixed OR array

Inputs → Programmable AND Array → Fixed OR Array → Outputs

b) Programmable Array Logic (PAL)
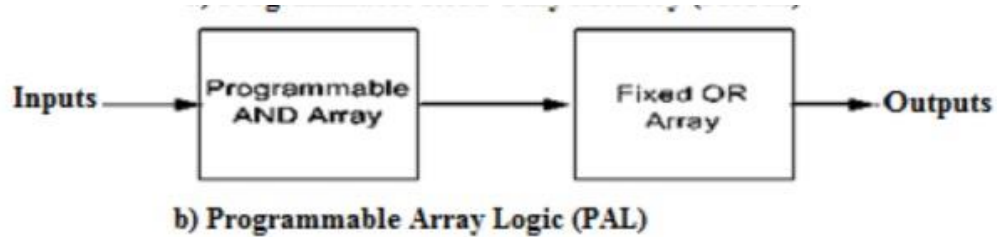
10. Compare volatile and non-volatile memory

S.No	Volatile Memory	Non Volatile Memory
1	Volatile memory is the type of memory where data is lost when power is turned off	Non Volatile Memory is a type of memory where the data is not lost when a computer is switched off.
2	Data temporarily stored in volatile memory	Data permanently stored in non volatile memory
3	It is faster than non-volatile memory.	It is slower than volatile memory.
4	It has less storage capacity	It has more storage capacity than volatile memory
5	Data can be easily transferred	Data can not be easily transferred
6	It is more costly per unit size.	It is less costly per unit size.
7	CPU has direct access to data.	CPU has no direct access to data.
8	Process can read and write	Process can only read.
9	It has a high impact on the system's performance.	It has a high impact on a system's storage capacity.
10	Data and programs that are currently fetch by CPU are stored in Volatile memory	Any kind of data and programs are stored in Non Volatile memory
11	Example: RAM and Cache Memory	Example: ROM and HDD

Difference between Volatile memory and Non Volatile...

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11 What is the minimum and maximum number of outputs if a demultiplexer has Four select lines?

A demultiplexer (often abbreviated as demux) with "n" select lines has 2^n output lines. Each output line corresponds to a unique combination of the select line inputs. The minimum and maximum number of outputs for a demultiplexer with four select lines can be determined as follows:

- Minimum number of outputs: When all select lines are set to their minimum value (usually 0 in a binary system), the demultiplexer will route the input signal to one of the 2^0 = 1 output lines. So, the minimum number of outputs is 1.
- Maximum number of outputs: When all select lines are set to their maximum value (usually 1 in a binary system), the demultiplexer will route the input signal to one of the 2^4 = 16 output lines. So, the maximum number of outputs is 16.

Therefore, a demultiplexer with four select lines can have a minimum of 1 output and a maximum of 16 outputs.
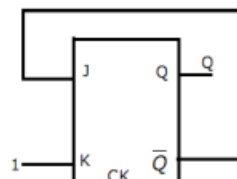
Min=1

Max=16

12 Specify the combinational circuit that can be used as data selector.

Answer :Multiplexer

13 Solve the output Q of the JK flip-flop after applying 2clock pulses. Assume the initial output is Q=0.

The truth table for a JK flip-flop is as follows:

J	K	Q(n)	Q(n+1)
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1

Assuming you apply two clock pulses, the state transitions would be:

1. First clock pulse: Q = 0 → Q = 0 (no change)
2. Second clock pulse: Q = 0 → Q = 1 (toggle)

14 Calculate the even parity bit for the following binary sequence 01001011100

You

Calculate the even parity bit for the following binary sequence 01001011100

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Even parity means that the total number of '1' bits in the binary sequence, including the parity bit, should be an even number. If the number of '1' bits is already even, then the parity bit is set to '0'; if it's odd, the parity bit is set to '1' to make the total count even.

Let's calculate the even parity bit for the given binary sequence 01001011100:

1. Count the number of '1' bits in the sequence: 0+1+0+0+1+0+1+1+1+1+0+0 = 5
2. Since the count is 5 (odd), we need to set the parity bit to make it even.
3. Set the parity bit to '1' (since 5 + 1 = 6, which is even).

Therefore, the even parity bit for the binary sequence 01001011100 is '1'.

15 What is encoder?

12. ENCODER

An encoder is a combinational circuit it encodes a 2^n input data lines into an n output data lines. Encoders are used to reduce the number of bits needed to represent some given data either in data storage or in data transmission. The block diagram shows an encoder that has 2^n input lines and n output lines.

2^n input lines — **ENCODER** — n output line
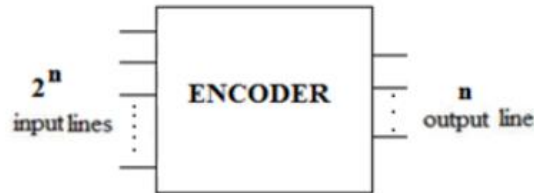
16 State the truth table of 1-bit magnitude comparator

14.1. MAGNITUDE COMPARATOR (1-BIT)

The truth table of 1-bit magnitude comparator is shown as

INPUTS		OUTPUTS		
A	B	G $A > B$	E $A = B$	L $A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

The output functions are obtained from the truth table is as follows,

$G = A.B'$

$E = A'.B' + A.B$

$L = A'.B$

17 What is meant by parity bit and mention its purpose in parity generator.

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit added with a binary message to check whether the parity is odd or even. The message with the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if checked that the parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator. The circuit that checks the parity in the receiver is called a parity checker.

18 Illustrate the state diagram for a 2-bit up counter
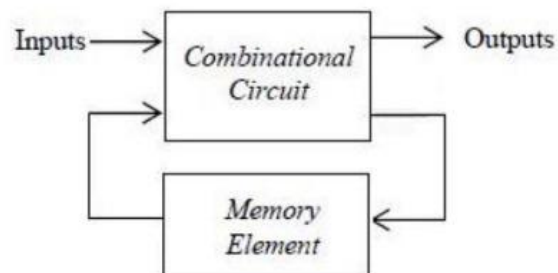
Logic circuit for 2-bit synchronous up counter:
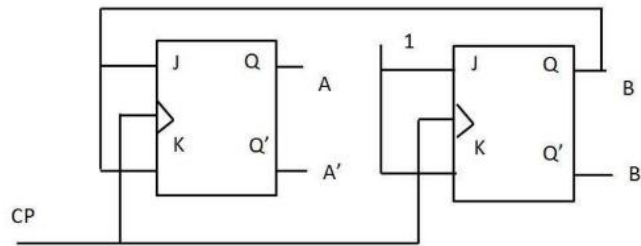
19) What is a sequential circuit? Draw its general block diagram

4. SEQUENTIAL CIRCUITS

The output of the sequential circuit depends on the present inputs and the past outputs of the circuit (i.e. past behaviour of the circuit). Example: **Counter.**

Block diagram of the sequential circuit:

20) State the truth table of 2:4 decoder.

Truth table of 2:4 line decoder:

INPUT		OUTPUT			
X	Y	D$_3$	D$_2$	D$_1$	D$_0$
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0