

Team Details

Team Name:

CORTEX CREW

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2	Member 1	PRAVEEN R	3 RD YEAR (2023 - 2027)
3	Member 2	S S JHOTHEESHWAR	2 ND YEAR (2024 - 2028)
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Problem Statement Addressed

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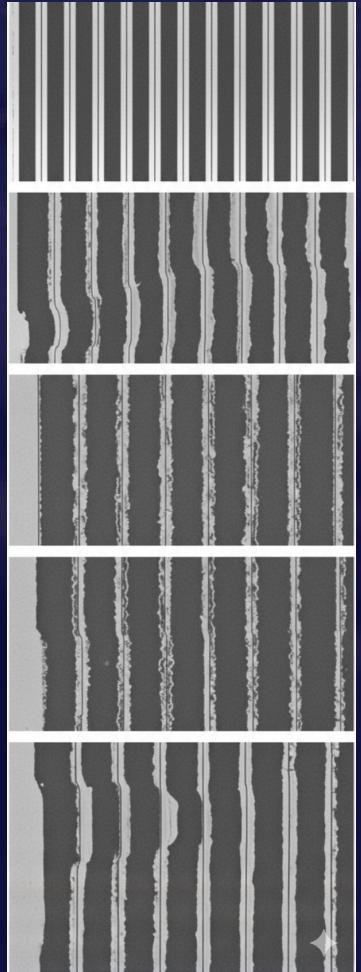


SEMICONDUCTOR WAFER DEFECT DETECTION USING MACHINE LEARNING

Semiconductor wafer fabrication involves hundreds of precision-controlled process steps

- Microscopic defects introduced at any stage can:
- Reduce yield
- Degrade device performance
- Cause early failures

Inspection systems generate large volumes of SEM images per wafer



WHY THIS PROBLEM IS SIGNIFICANT ?

Technology node scaling → defects become smaller and harder to detect

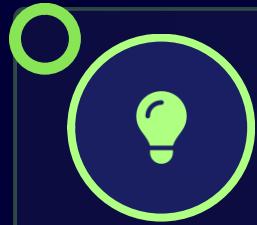
Delayed detection leads to:

- Yield loss
- Higher production cost
- Reliability risks

Common defects:

- Bridges, opens, cracks
- LER, CMP scratches,
- via voids

Idea Description - Describe your Idea/Solution/Prototype



KEY CONCEPT & APPROACH

- Use Machine Learning to automatically detect and classify semiconductor wafer defects
- Input: SEM wafer images
- Classes include:
 - 1.Bridge, Open, Crack
 - 2.Line Edge Roughness (LER)
 - 3.CMP defects, Via voids
 - 4.Clean wafers
- Train a lightweight CNN (MobileNetV2) for:
 - 1.High accuracy
 - 2.Low computation cost
- Design optimized for edge deployment (ONNX-ready)

SOLUTION OVERVIEW

- Preprocess SEM images (grayscale, normalization, resizing)
- ML model classifies defects in real time
- Eliminates manual inspection and rule-based limitations
- Reduces:
 - 1.Inspection latency
 - 2.Human error
 - 3.Infrastructure dependency
- Improves:
 - 1.Yield monitoring
 - 2.Early defect detection & Manufacturing reliability
- Design optimized for edge deployment (ONNX-ready)

Proposed Solution - Describe your Idea/Solution/Prototype

TECHNOLOGIES INVOLVED

- Python for data processing and model development
- PyTorch for training and evaluation
- OpenCV for image preprocessing
- ONNX for model portability and edge deployment
- Edge-AI compatible architecture (lightweight CNN)

METHODOLOGY

- Collect SEM wafer images (clean + defective)
- Convert images to grayscale and normalize
- Train a MobileNetV2-based CNN for defect classification
- Use supervised learning with labeled defect categories
- Validate model using unseen test data

IMPLEMENTATION STRATEGY

- Offline model training on curated SEM dataset
- Export trained model to ONNX format
- Deploy ONNX model on edge-compatible platforms
- Real-time inference for high-volume inspection
- Output: defect class with confidence score

Innovation and Uniqueness



KEY INNOVATION

- Edge-AI based defect classification for semiconductor wafers
- Lightweight MobileNetV2 model instead of heavy CNNs
- Trained on SEM-specific defect patterns
- Supports multiple defect types + clean class
- ONNX-ready architecture for cross-platform deployment
- Focus on real-time inference under fab constraints

COMPETITIVE ADVANTAGE

- Lower latency compared to cloud-based inspection systems
- Reduced bandwidth and infrastructure cost
- Faster decision-making during wafer inspection
- High accuracy with low computational overhead
- Easily scalable across inspection stations
- Suitable for Industry 4.0 and smart manufacturing environments

Impact and Benefits



PRIMARY IMPACT

- Automated and accurate wafer defect classification
- Faster inspection compared to manual review
- Early defect detection in fabrication flow
- Improved wafer yield and device reliability
- Reduced dependence on human inspection
- Supports real-time decision-making at fab level

QUANTIFIABLE OUTCOMES

- 30–50% reduction in inspection time
- Lower operational cost by reducing manual effort
- High classification accuracy (>95% on test data)
- Low-latency inference suitable for edge deployment
- Scalable deployment across multiple inspection stations
- Improved throughput in high-volume manufacturing

| Technology & Feasibility/Methodology Used



IMPLEMENTATION STRATEGY

An end-to-end Edge-AI pipeline is developed for semiconductor wafer defect detection using lightweight deep learning. The approach focuses on achieving high classification accuracy while maintaining low computational complexity for real-time edge deployment.



Software Architecture

- Input: Grayscale SEM wafer/die images (224×224)
- Preprocessing:
 - Grayscale normalization
 - Resizing and standardization
- Model:
 - MobileNetV2 (lightweight CNN)
 - Trained for multi-class defect classification
- Inference Engine:
 - ONNX Runtime (CPU-based)
 - Confidence-based rejection mechanism for Other / Unknown defects
- Output:
 - Defect class prediction
 - Confidence score
 - Safe rejection of low-confidence samples



Development Tools

- Programming Language: Python
- Deep Learning Framework: PyTorch
- Model Architecture: MobileNetV2
- Model Export & Deployment:
 - ONNX
 - ONNX Runtime
- Image Processing: OpenCV
- Evaluation & Metrics:
 - Accuracy, Precision, Recall, F1-score
 - Unseen data evaluation

GitHub & Video Link



GitHub Repository

@ https://github.com/Ragul-2005/wafer_detect_deeptech_hackathon2026.git

DATASET

@ <https://drive.google.com/drive/folders/18SNO5NAIkEd13Wb6UdtUBszOfYUqCX-M?usp=sharing>

Research and References



Research Background & Methodology

The proposed solution is grounded in computer vision and deep learning principles, utilizing Convolutional Neural Networks (CNNs) for image-based semiconductor defect classification. Lightweight CNN architectures from the MobileNet family are employed due to their proven effectiveness in texture-based analysis and suitability for edge and embedded inference. SEM wafer images are processed using grayscale normalization, allowing the model to learn discriminative features directly from the data rather than relying on handcrafted or rule-based defect detection methods. The methodology is validated through systematic training, validation, and testing on unseen datasets, with performance evaluated using accuracy metrics and confusion matrix analysis to ensure robust and reliable classification.



References & Citations

List key papers, articles, or data sources.

- ✓ R. Zhang, G. Ye and X. Liu, "An effective method for low-contrast high-noise lithography SEM image contour extraction," 2025 IEEE 16th International Conference on ASIC (ASICON), Kunming, China, 2025, pp. 1-4, doi: 10.1109/ASICON66040.2025.11325917.
- ✓ H. Hatem et al., "AI-Powered Defect Detection using Deep Learning: A Pattern-Agnostic Faster R-CNN Approach for SEM Images with GPU Acceleration," 2025 36th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC), Albany, NY, USA, 2025, pp. 1-5, doi: 10.1109/ASMC64512.2025.11010758.
- ✓ T. Sweeney, S. Coleman and D. Kerr, "Deep Learning for Semiconductor Defect Classification," 2022 IEEE 20th International Conference on Industrial Informatics (INDIN), Perth, Australia, 2022, pp. 572-577, doi: 10.1109/INDIN51773.2022.9976162.