Faculty Of Engineering and Technology

Electrical and Computer Engineering Department

CIRCUITS AND ELECTRONICS LABORATORY

ENEE 2103

Experiment #: 6

Diode Characteristic and Applications

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1. DIODE CHARACTERISTICS

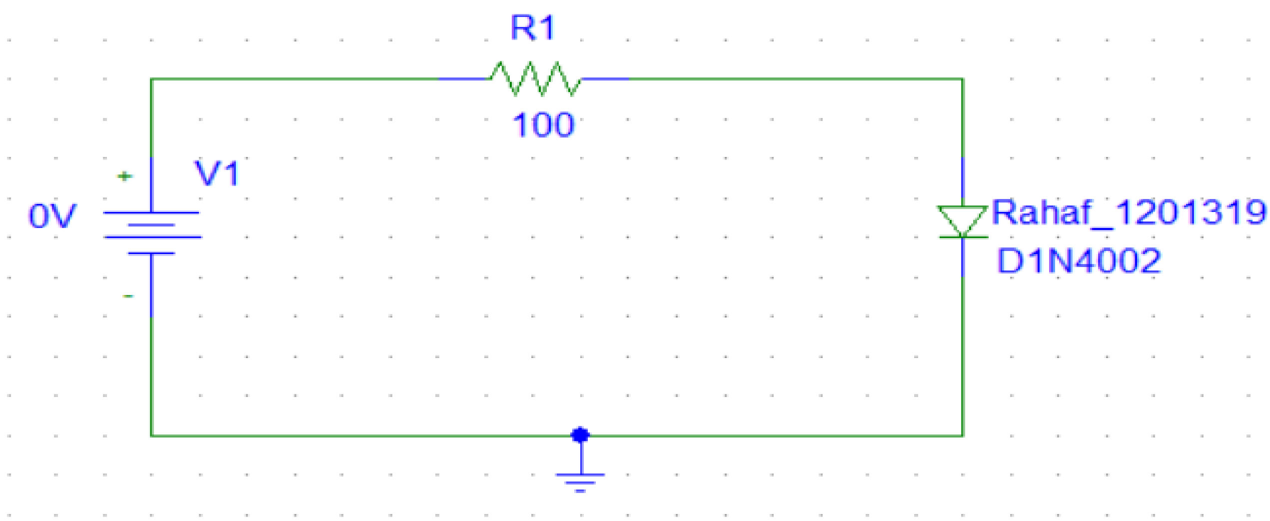


Figure 1.1: RD series circuit implementation

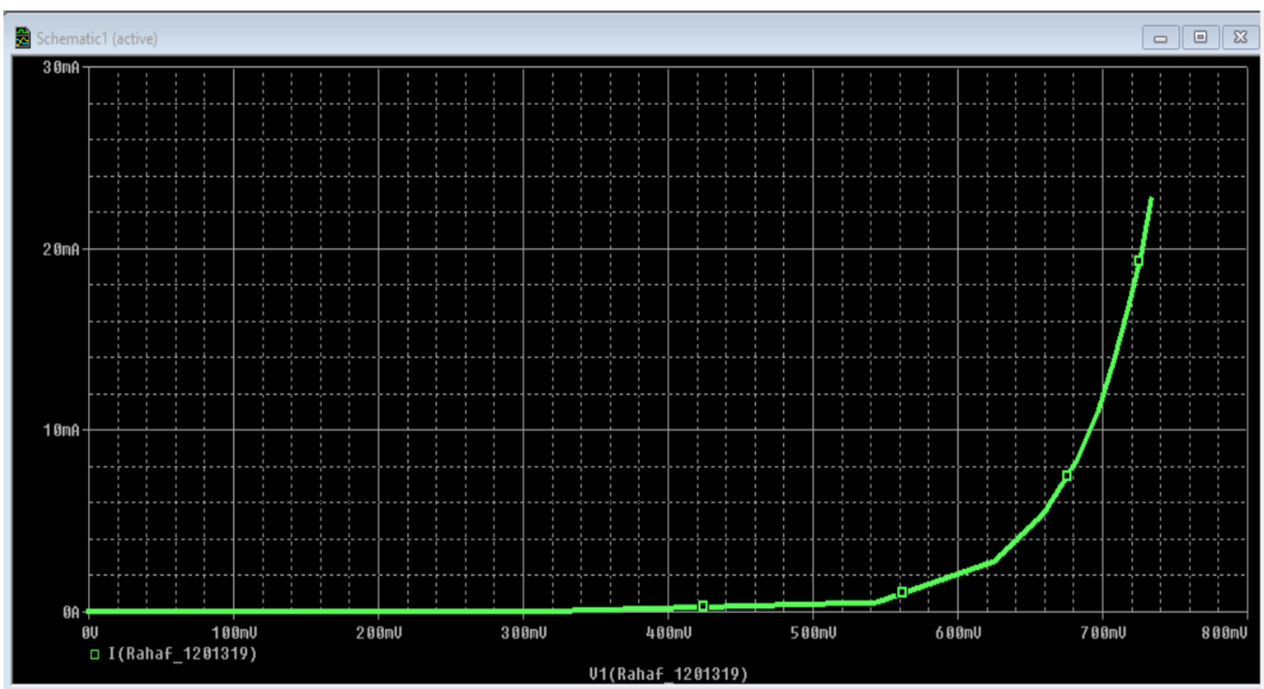


Figure 1.2: RD series circuit simulation result

VS	VR	VD	ID
0	0	0	0
0.2	0	0.2	0
0.4	0	0.4	0
0.6	0.009	0.591	0.00009
0.8	0.137	0.663	0.001
1	0.315	0.685	0.003
1.5	0.791	0.709	0.008
2	1.278	0.722	0.013
2.5	1.769	0.731	0.018
3	2.262	0.738	0.023

Table 1: Diode characteristics table

In this case VR = VS-VD

ID = VR * R

Using KVL:

->when VS = 0.2 :   -0.2+0+VD=0->VD =0.2v

ID = VR/R=0/100=0

->when VS = 0.4 :   -0.4+0+VD=0->VD =0.4v

ID = VR/R=0/100=0

->when VS = 0.6 :   -0.6+0.009+VD=0->VD =0.591v

ID = VR/R=0.009/100=0.00009A

->when VS = 0.8 :   -0.8+0.137+VD=0->VD =0.663v

ID = VR/R=0.137/100=0.001A

->when VS = 1 :   -1+0.315+VD=0->VD =0.685v

ID = VR/R=0.315/100=0.0032A

->when VS = 1.5 :   -1.5+0.791+VD=0->VD =0.709v

ID = VR/R=0.791/100=0.008A

->when VS = 2 :   -2+1.278+VD=0->VD =0.722v

ID = VR/R=1.278/100=0.013A

->when VS = 2.5 :   -2.5+1.769+VD=0->VD =0.731v

ID = VR/R=1.769/100=0.018A

->when VS = 3 :   -3+2.262+VD=0->VD =0.738v

ID = VR/R=2.262/100=0.023A

Reverse the diode:

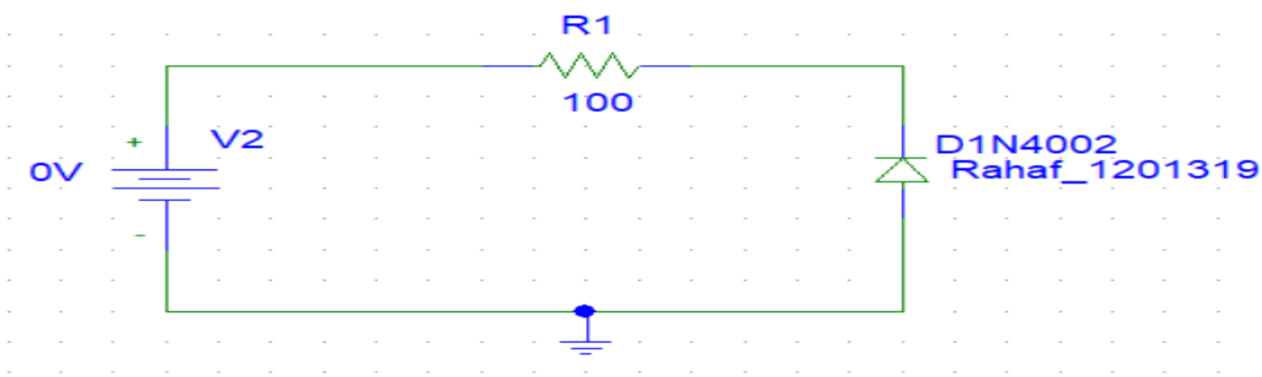


Figure 1.3: RD series circuit implementation– When reverse the diode

The diode will behave as an open circuit after being reversed since the voltage across the anode is greater than the voltage across the cathode. So, VD =VS and ID=0 VR=0

VS	VR	VD	ID
0	0	0	0
0.2	0	0.2	0
0.4	0	0.4	0
0.6	0	0.6	0
0.8	0	0.8	0
1	0	1	0
1.5	0	1.5	0
2	0	2	0
2.5	0	2.5	0
3	0	3	0

Table 2: Reverse diode characteristic table

2.RECTIFICATION

2.1. Half-wave rectification

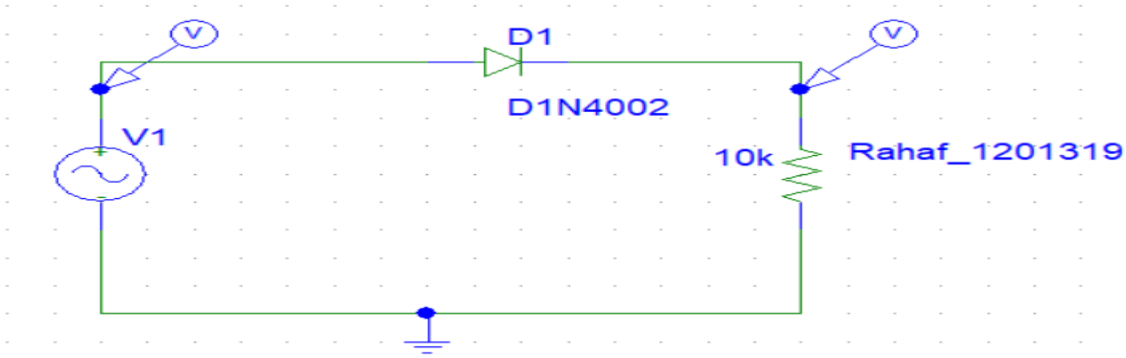


Fig 2.1.1: Half-Wave Rectification circuit implementation

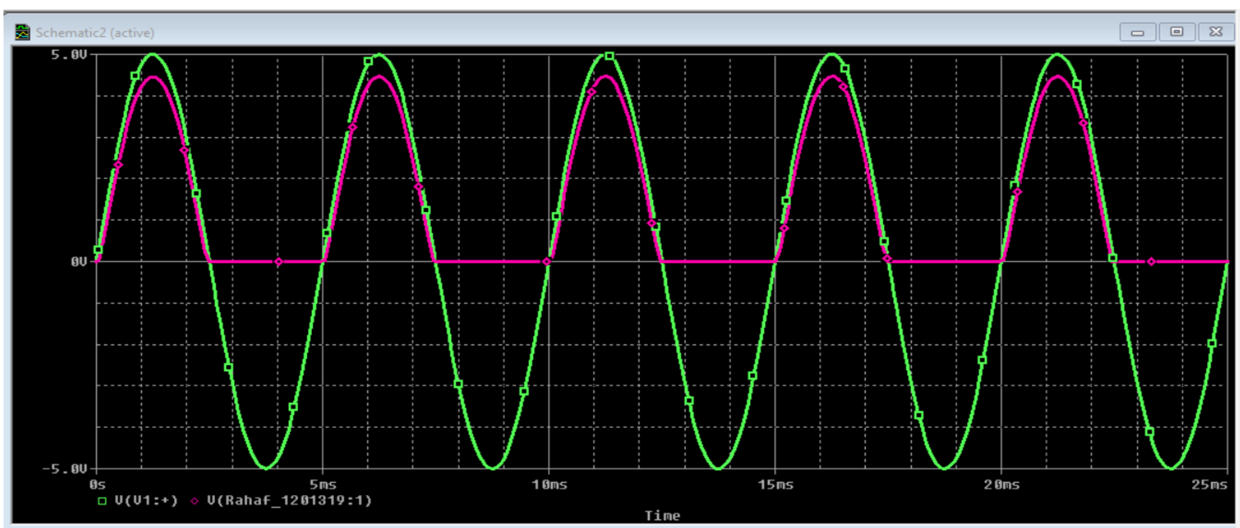


Fig 2.1.2 : Half-Wave Rectification circuit implementation

➢ Period T and dc value

-> T = 1 / f = 1/200 = 5 ms

-> peak value V peak (experimentally) = 4.4683v

->dc value = V peak/ π = 1.42305v

When reverse the diode:

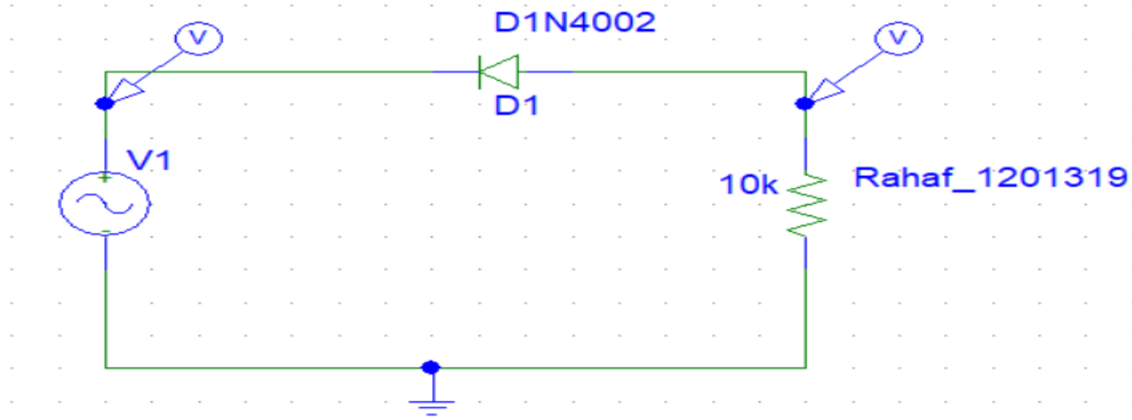


Fig 2.1.3 :Half-Wave Rectification circuit implementation - When Reverse the diode

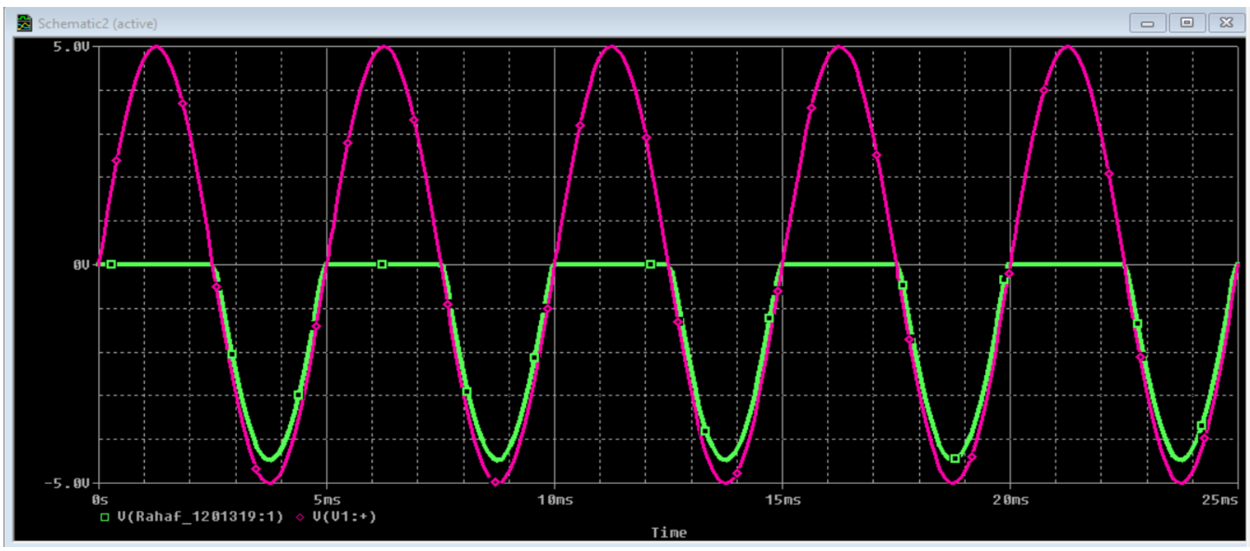


Fig 2.1.4 : Half-Wave Rectification circuit implementation - When Reverse the diode-wave form

➢ Period T and dc value

-> T = 1 / f = 1/200 = 5 ms

-> peak value V peak (experimentally) = - 4 .4516v

-> dc value = V peak/ π = - 1.4177v

->When Adding C = 2.2 μF :

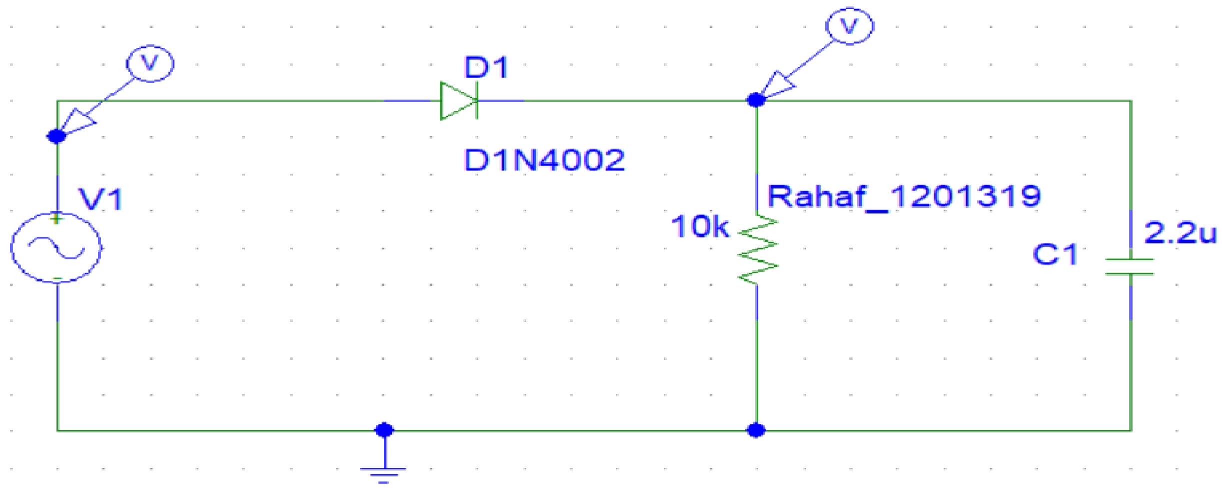


Fig 2.1.5 : Half-Wave Rectification circuit implementation after adding 2.2 μF capacitor

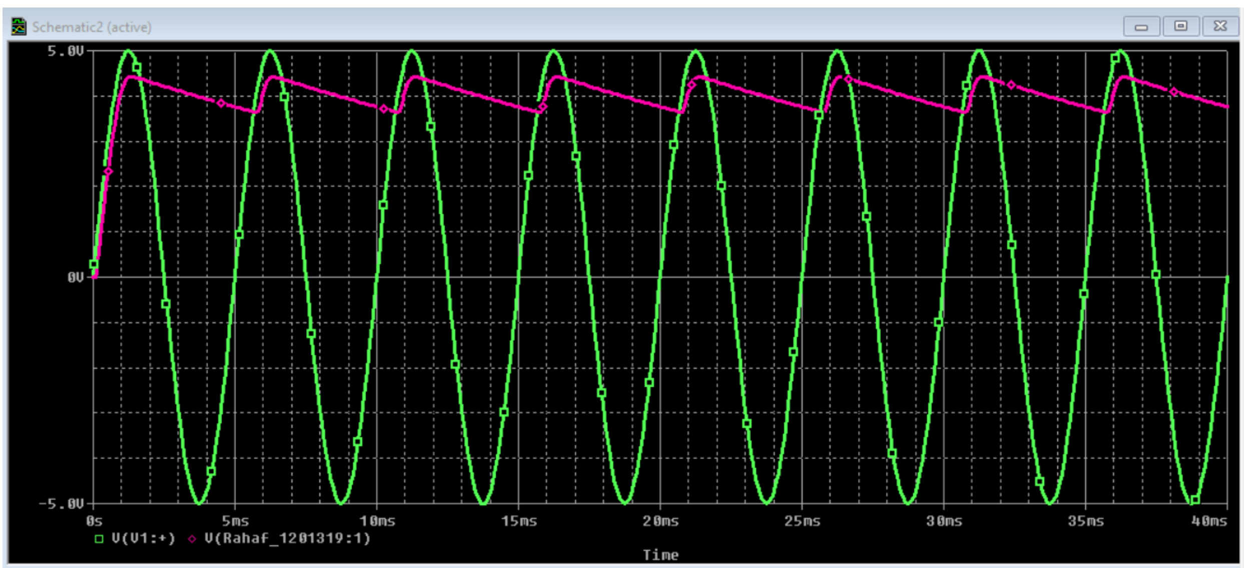


Fig 2.1.6 : Half-Wave Rectification circuit after adding 2.2 μF capacitor -wave form

▪ dc value:

-> peak value V peak (experimentally) = 4.4273 v

-> VLR-pp = 4.4273 – 3.6310 = 0.7963v

-> dc value = V avg = V peak − 0.5 VL-pp = 4.4273 − 0.5 ∗ 0.7962 = 4.02915 v

Ripple factor:

r% (experimentally) = ((VLR−PP)/2√3)/V avg) ∗ 100% = 5.7052%

r% (theoretically) =(1/√3[2f0RC−1]) * 100%

= (1/((3^0.5)((2*200*10*100*2.2*10^-6)-1))*100%=7.4019

->Using C = 47 µF :

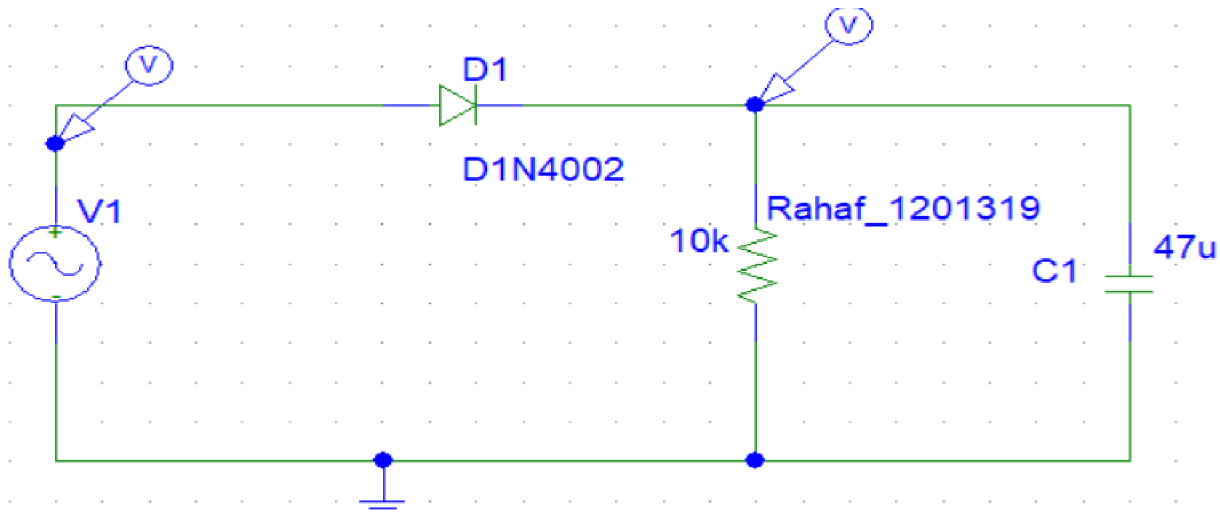


Fig 2.1.7:: Half-Wave Rectification circuit after adding 47 µF capacitor

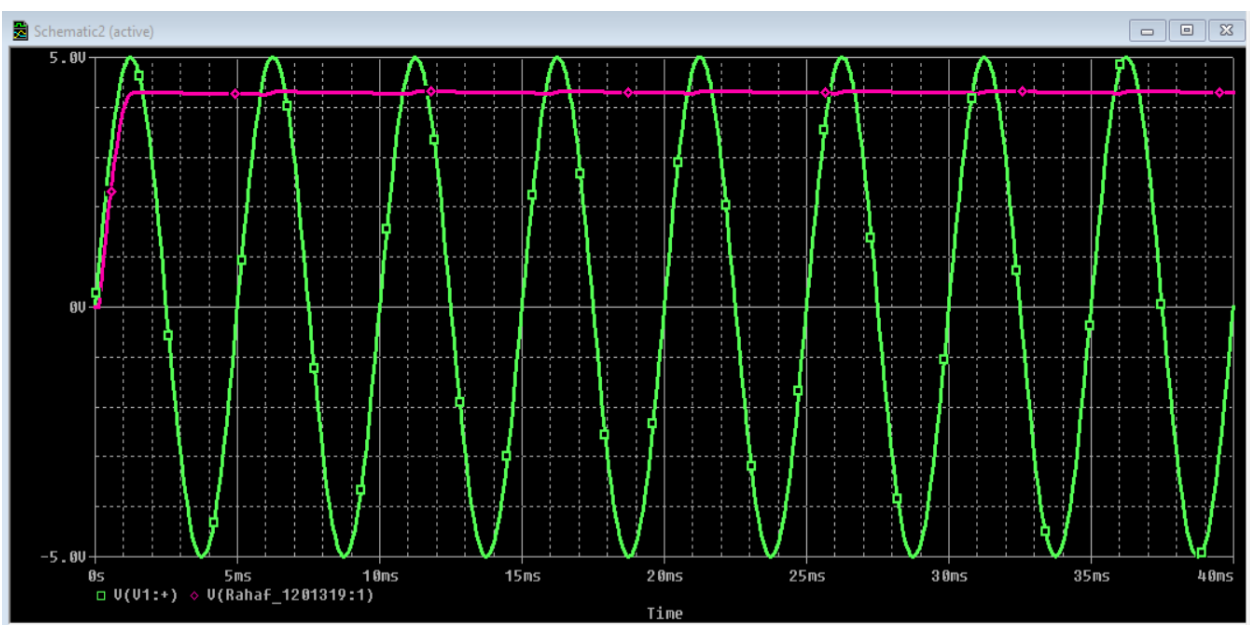


Fig 2.1.8:: Half-Wave Rectification circuit after adding 47 µF capacitor-wave form

dc value:

-> peak value V peak (experimentally) = 4.3234 v

-> VLR-pp = 4.3234 – 4.2810= 0.0424v

-> dc value = V avg = V peak − 0.5 VL,p−p = 4.3234 − 0.5 ∗ 0.0424 = 4.3022 v

Ripple factor:

r% (experimentally) =(((VLR−PP)/2√3)/Vavg) ∗ 100% = 0.2845 %

r% (theoretically) =(1/√3[2f0RC−1]) * 100%

=1/ (√3[2 ∗ 200 ∗ 10 ∗ 1000 ∗ 47 ∗ 10^−6]) *100% = 0.3087%

->We note that when the capacitor value is increased, the ripple factor decreases and the value of the mean voltage increases.

2.2. Full-wave rectification

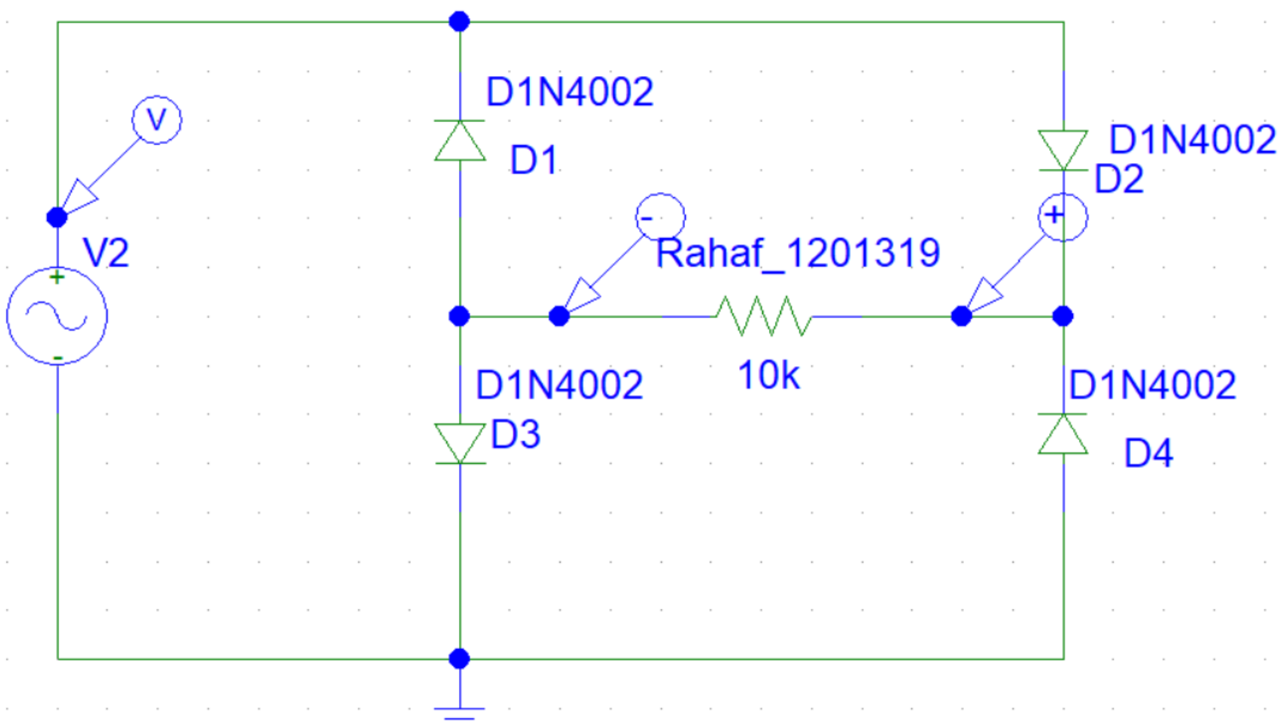


Figure 2.2.1: Full-Wave Rectification

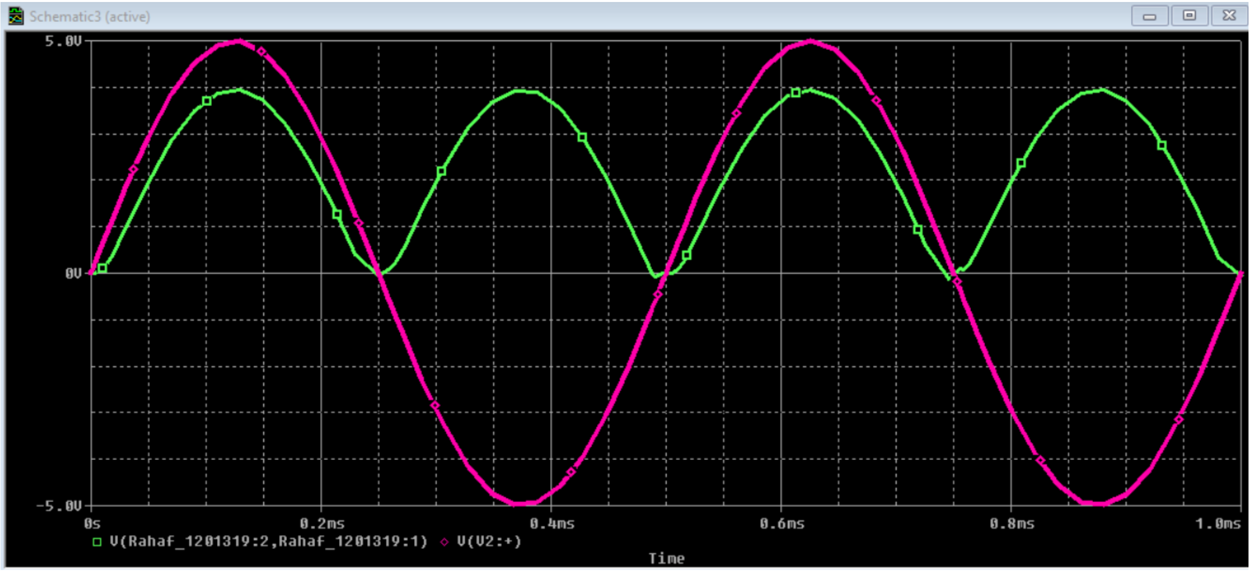


Figure 2.2.2: Full-Wave Rectification wave form

➢ Period T and dc value

-> T = 1 / f = 1/2000 = 0.5 ms

-> peak value V peak(experimentally) = 3.9355v

->dc value = V peak/ π = 1.2533v

When Adding C = 2.2 μF:

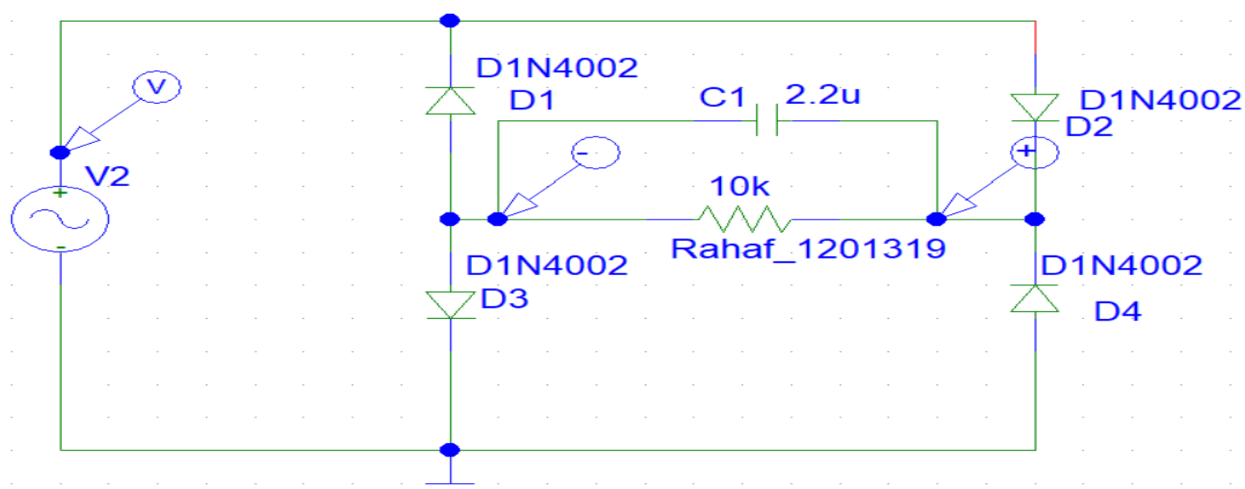


Figure 2.2.3: Full-Wave Rectification when adding the capacitor of 2.2 μF voltage response

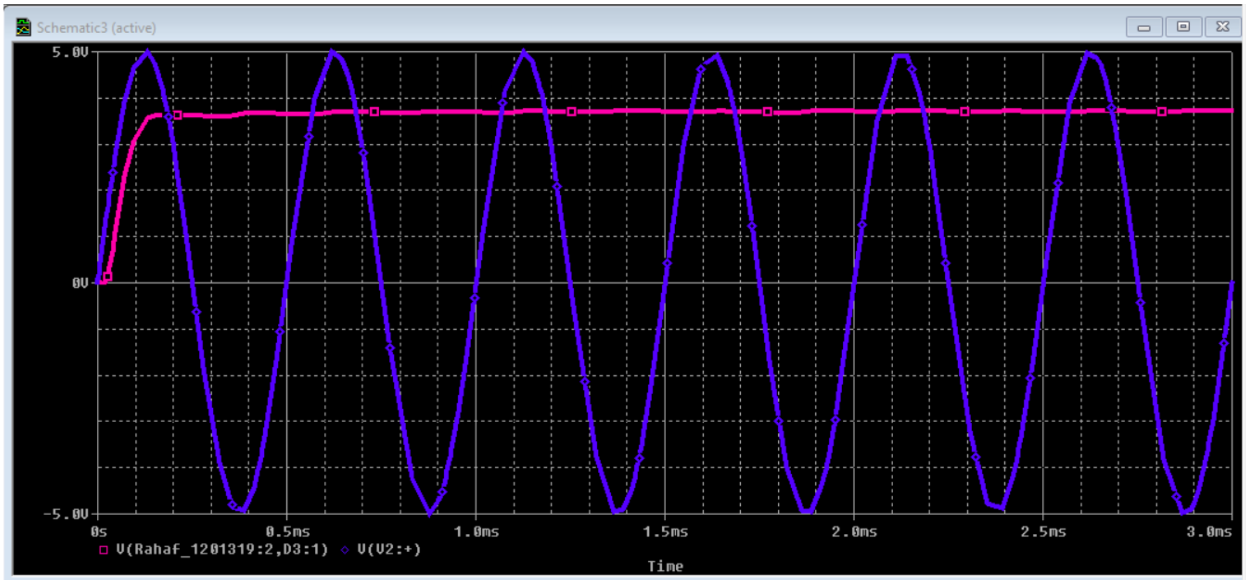


Figure 2.2.4: Full-Wave Rectification when adding the capacitor of 2.2 µF wave form

dc value:

-> peak value V peak (experimentally) = 3.7431v

-> VLR-pp = 3.7431–3.7114= 0.0317v

-> dc value = V avg = V peak − 0.5 VL,p−p =3.7431− 0.5 ∗ 0.0317 = 3.7272v

ripple factor:

r% (experimentally) =(((VLR−PP)/2√3)/V avg) ∗ 100% = 0.2455 %

r% (theoretically) =(1/√3[4f0RC−1]) * 100%

= (1/√3[4∗ 2000 ∗ 10 ∗ 1000 ∗ 2.2 ∗ 10−6]) *100% =0.3299%

3. OTHER APPLICATIONS

3.1. Clipping

When dc=0v

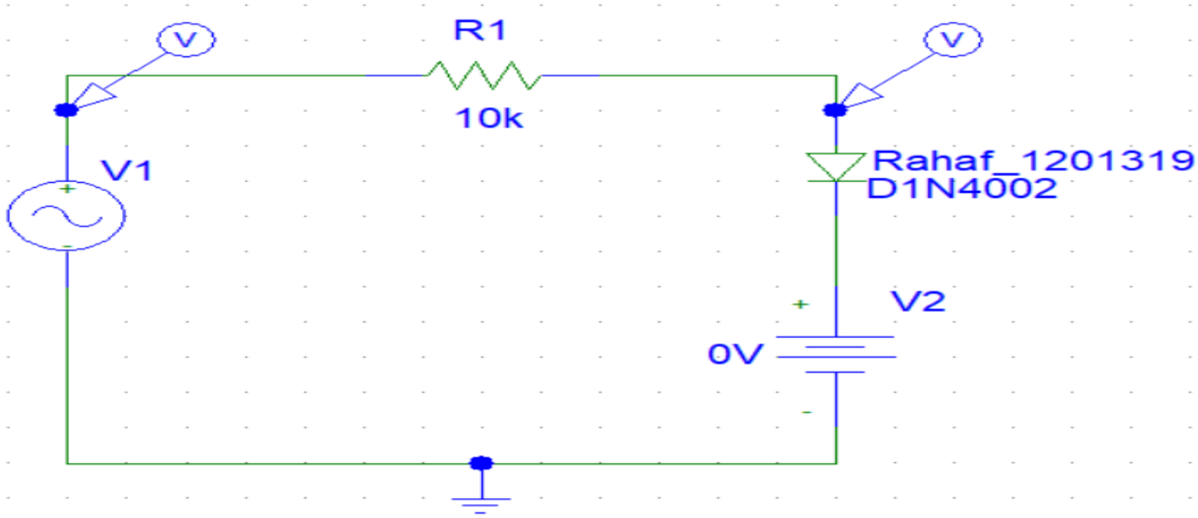


Figure 3.1.1: Clipping circuit implementation when dc =0v

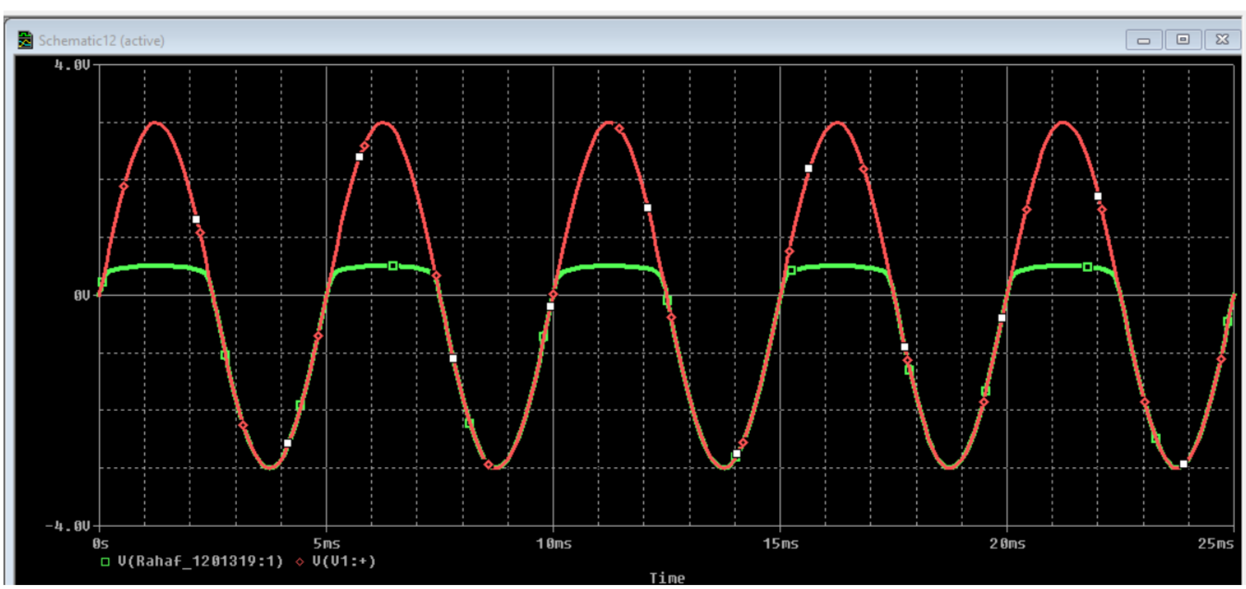
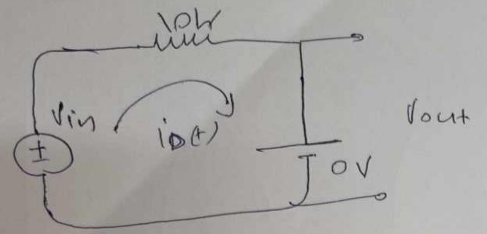


Figure 3.1.2: Clipping circuit implementation-wave form when dc = 0v

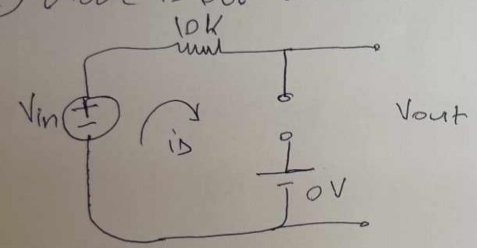
when dc = 0V

① assume diode is on

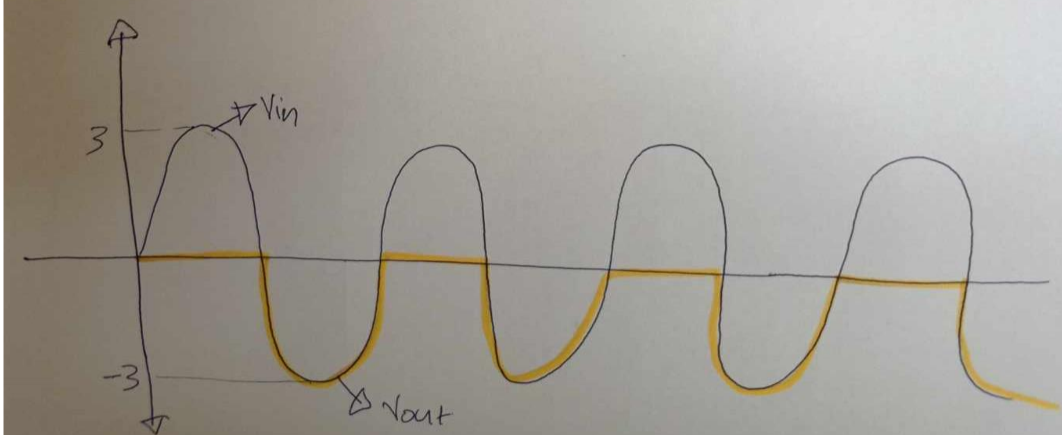


$i_D(t) = \frac{V_{in}}{10k} > 0 \rightarrow V_{in} > 0 \rightarrow V_{out} = 0V$

② diode is off when $V_{in} < 0$



$V_{out} = V_{in}$



When dc=1.5

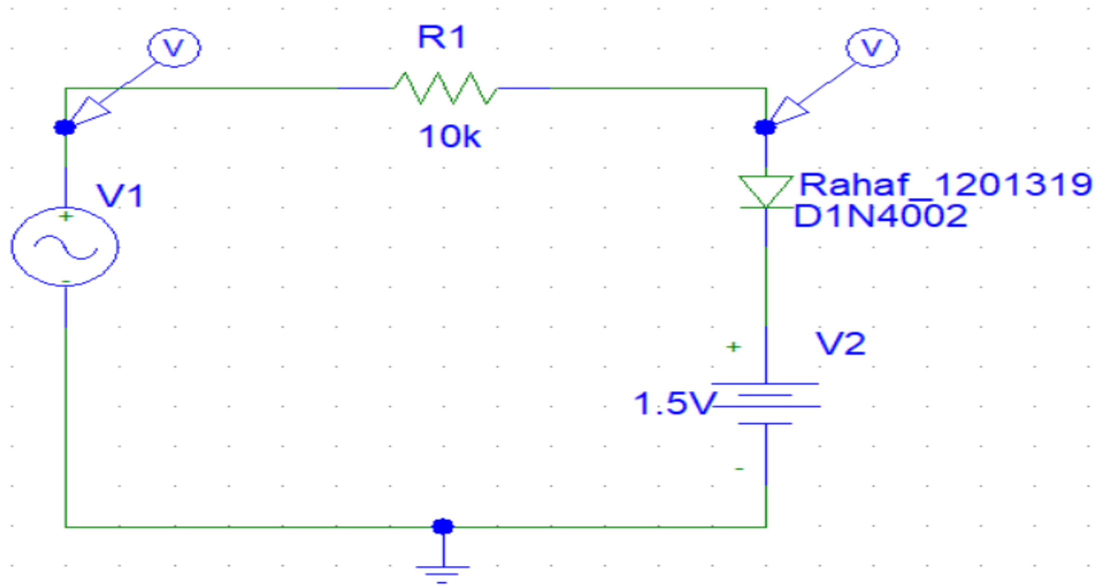


Figure 3.1.3: Clipping circuit implementation when dc =1.5v

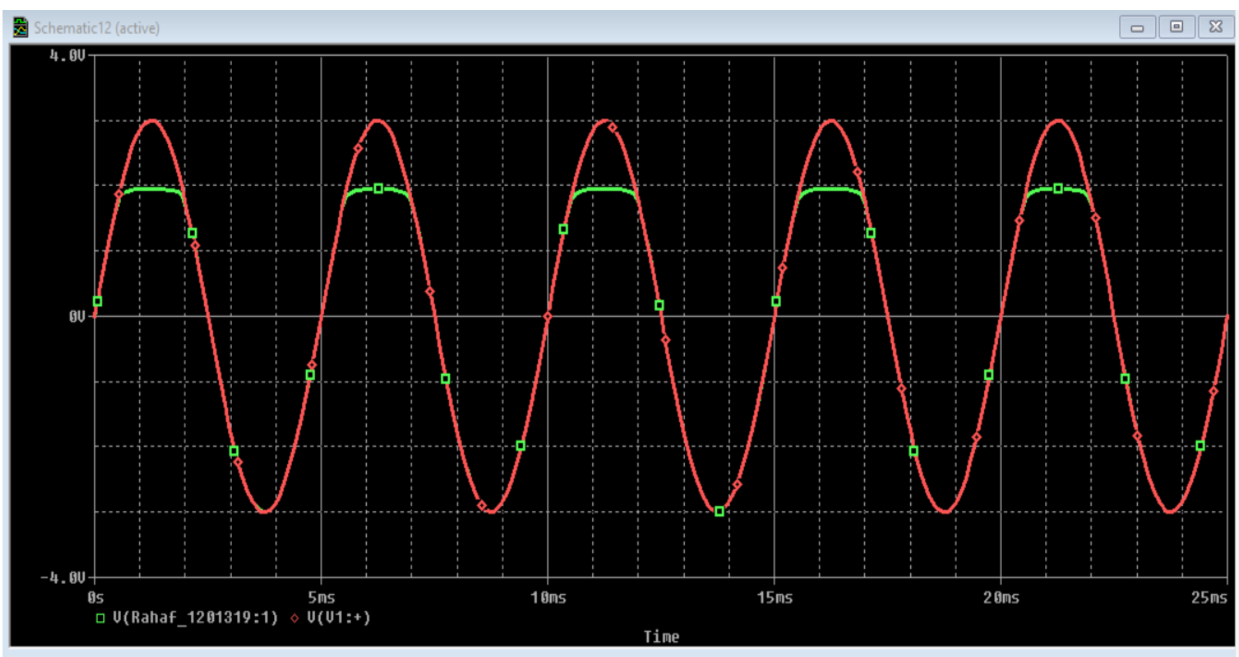
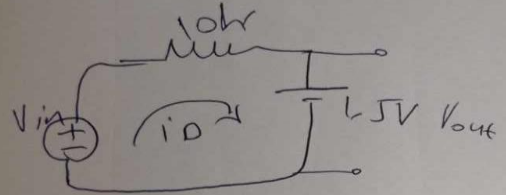


Figure 3.1.4: Clipping circuit implementation -wave form when dc = 1.5v

when $dc = 1,5V$

① assume diode is on

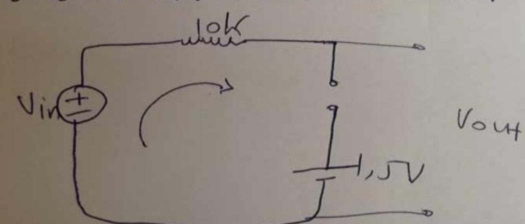


$-V_{in} + i_D\,10k + 1,5V = 0$

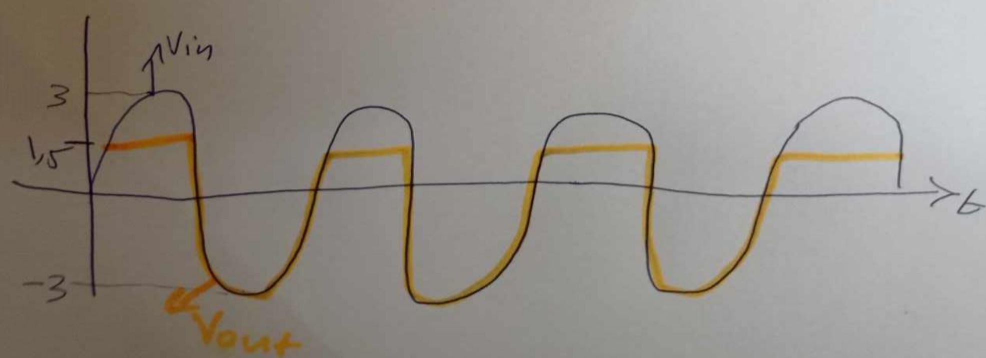
$i_D = \dfrac{V_{in} - 1,5}{10k} > 0 \Rightarrow V_{in} > 1,5V$

$V_{out} = 1,5$

② diode is off when $V_{in} < 1,5V$



$V_{out} = V_{in}$



When dc=4v

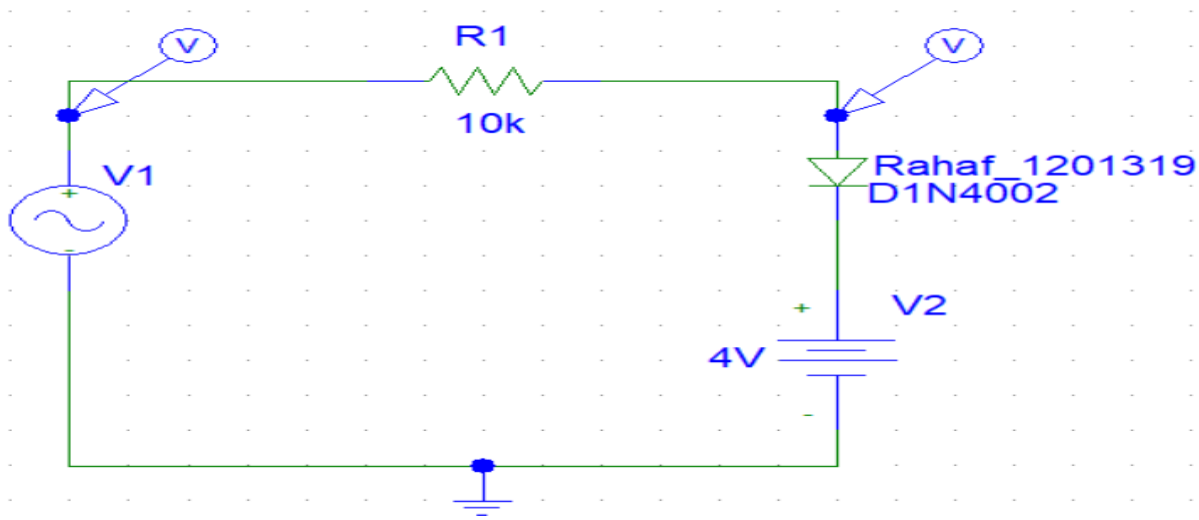


Figure 3.1.5: Clipping circuit implementation when dc =4v

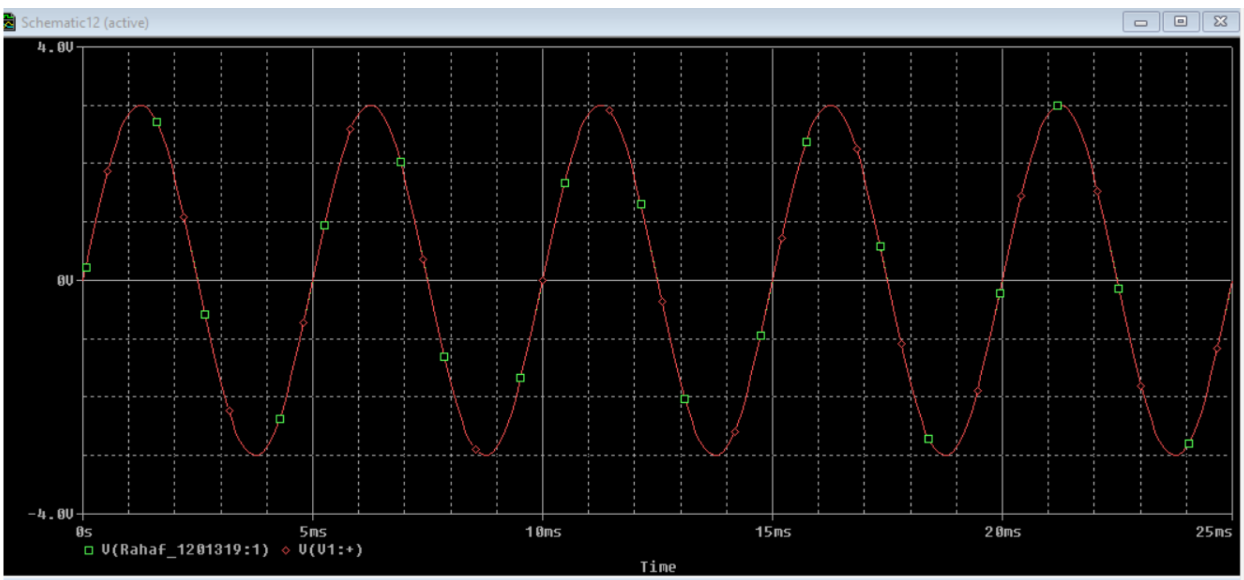
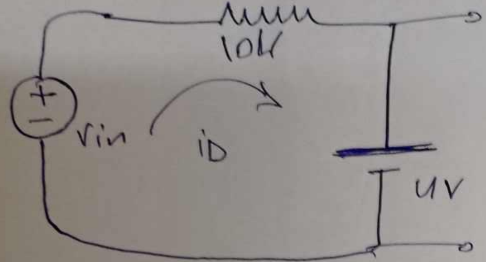


Figure 3.1.6: Clipping circuit implementation -wave form when dc =4v

When dc = 4V

① assume diode is on



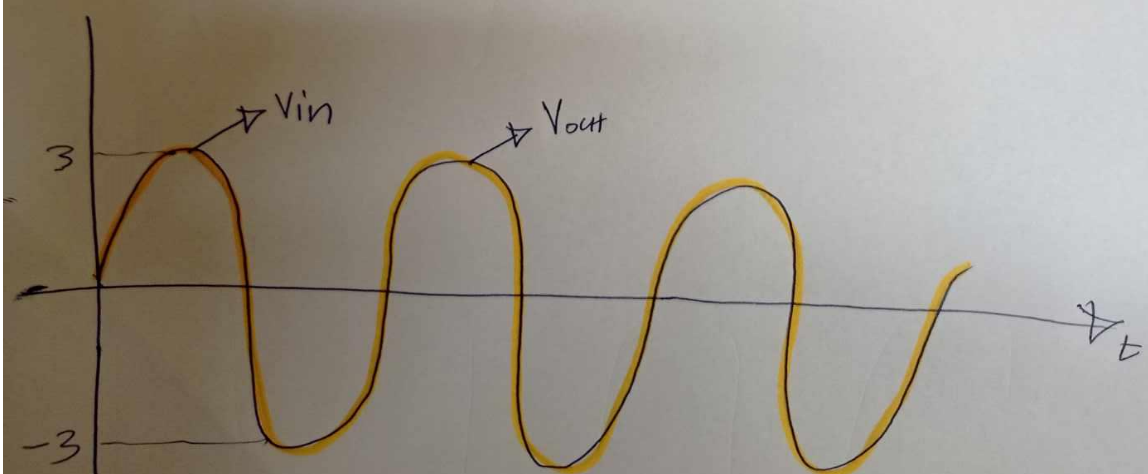
$-V_{in} + i_D\, 10k + 4V = 0$

$i_D = \frac{V_{in} - 4}{10k} > 0 \qquad V_{in} > 4$

$V_{out} = 4$ volt

② diode is off when $V_{in} < 4$

$V_{out} = V_{in}$



3.2. Clamping

When dc =0v

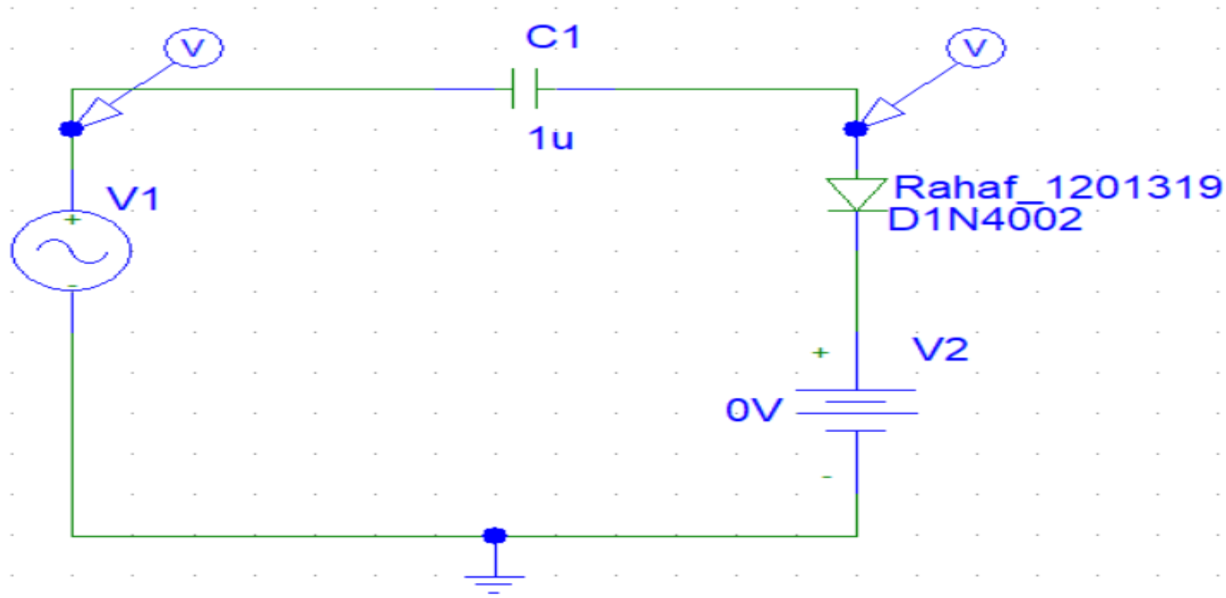


Figure 3.2.1: Clamping circuit implementation when dc=0v

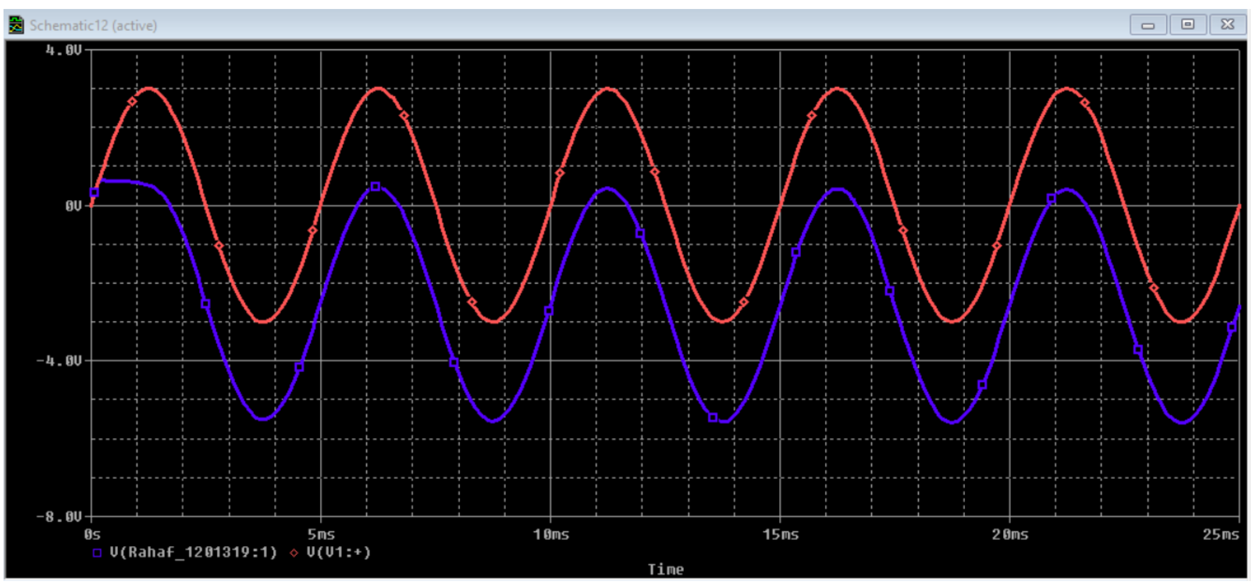


Figure 3.2.2: Clamping circuit implementation- wave form when dc = 0v

When dc =1.5v

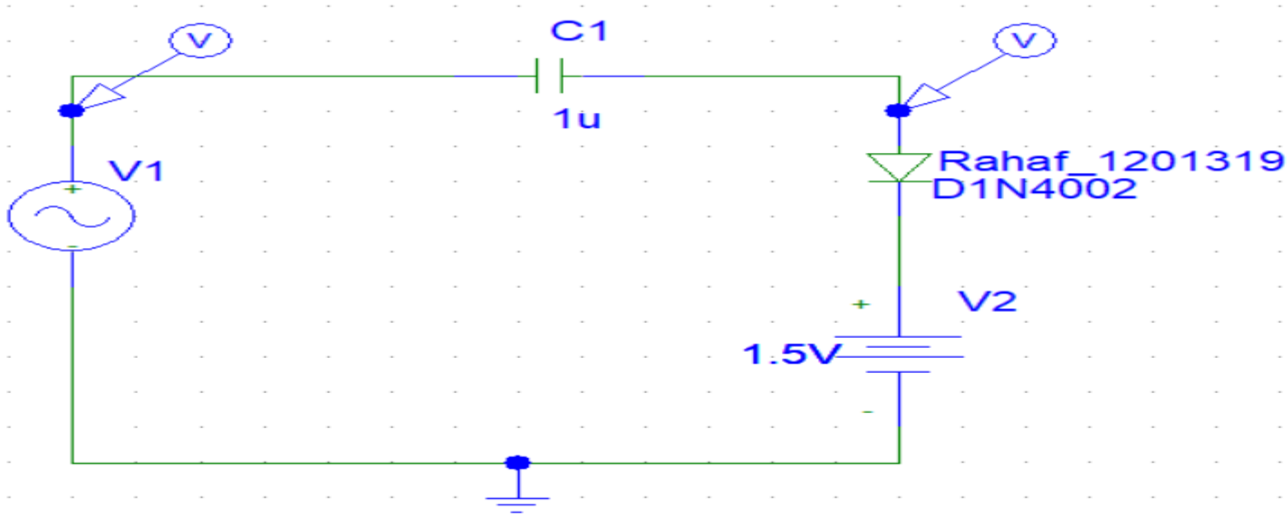


Figure 3.2.3: Clamping circuit implementation when dc=1.5v

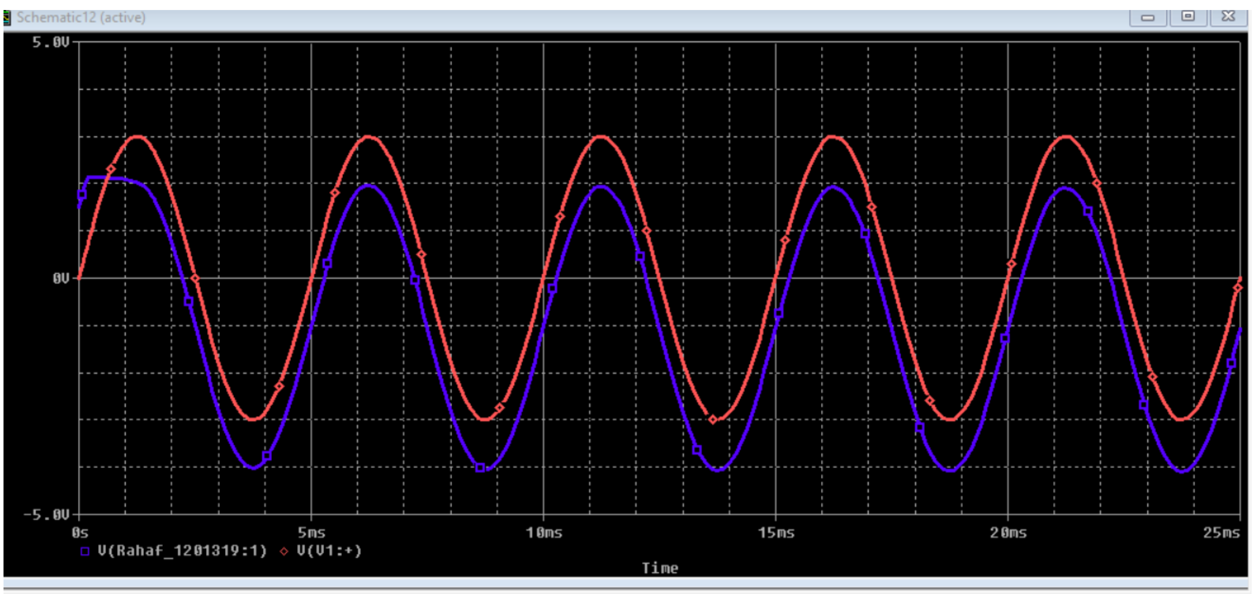
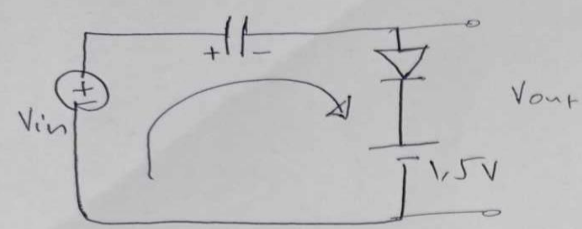
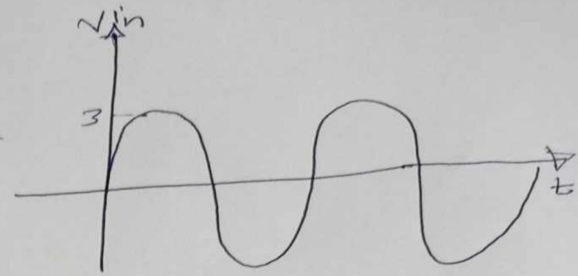


Figure 3.2.4: Clamping circuit implementation- wave form when dc = 1.5v

when $dc = 1,5$ Volt





① when $V_i = 3V$

$-V_{in} + V_c + 1,5 = 0$

$-3 + V_c + 1,5 = 0$

$V_c - 1,5 = 0$

$\boxed{V_c = 1,5\ V}$

$\boxed{V_{out} = 1,5 \text{ Volt}}$

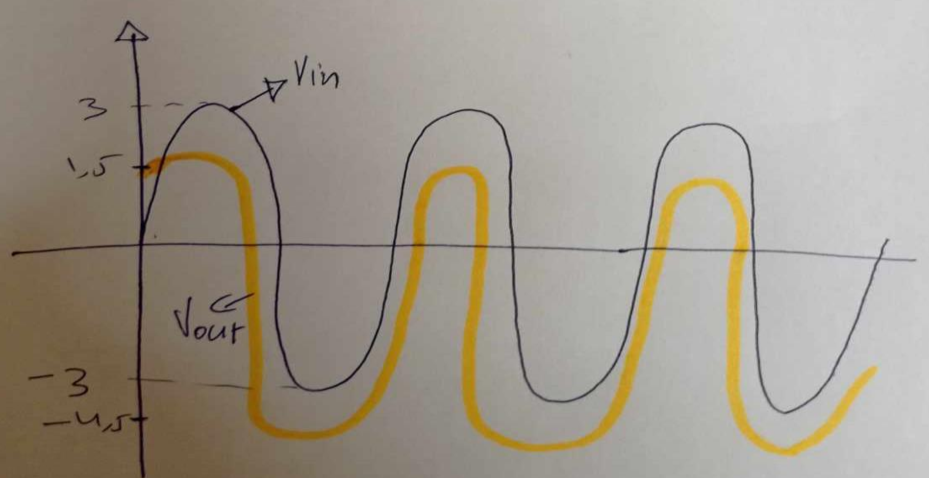
② for $V_i = -3$

$3 + 1,5 + V_D + 1,5 = 0$

$V_D = -6$

$V_D < 0$ diod is off

$\boxed{V_{out} = V_{in} - 1,5 = -4,5}$



When dc =4v

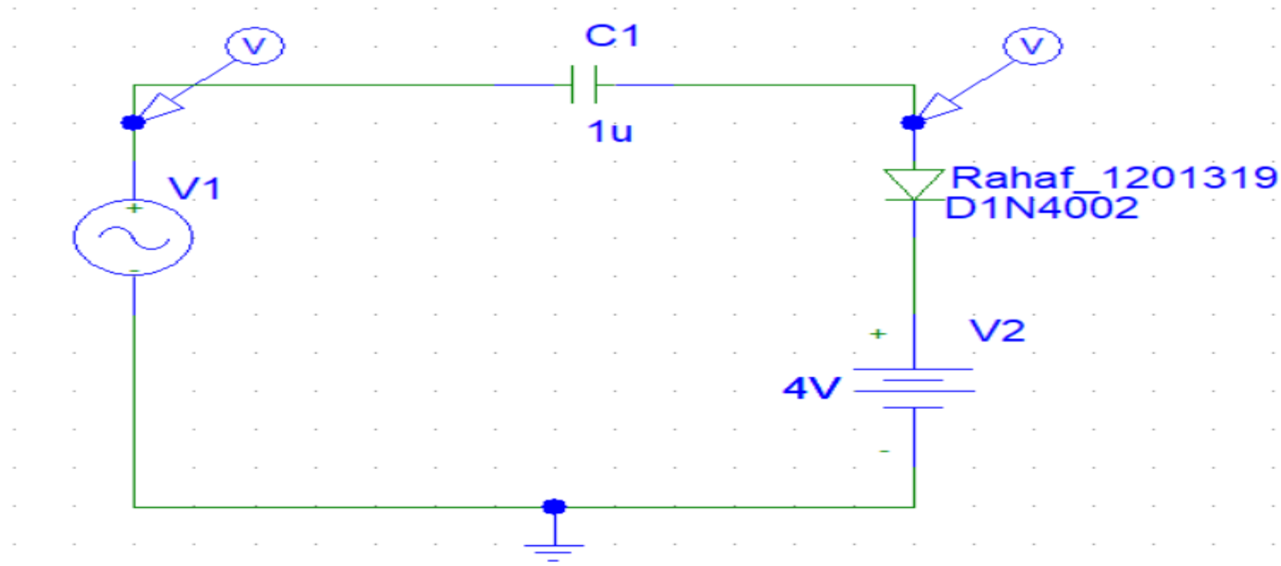


Figure 3.2.5: Clamping circuit implementation when dc=4v

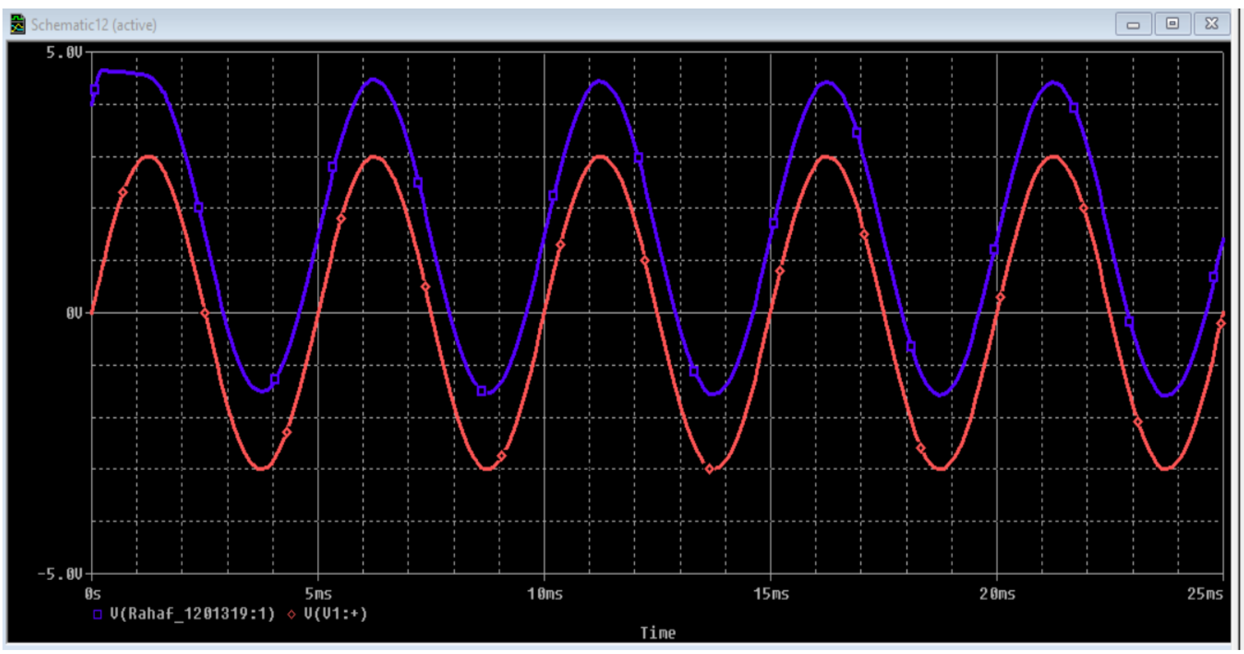
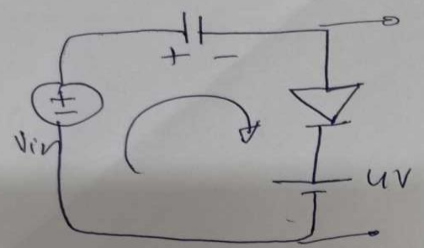
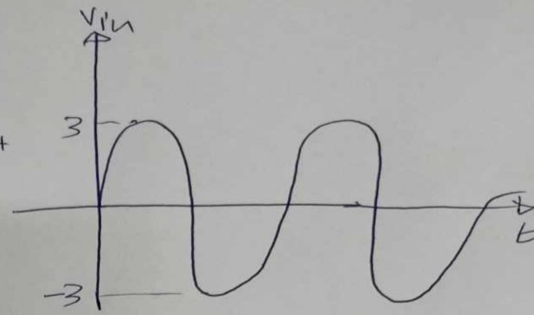


Figure 3.2.6: Clamping circuit implementation- wave form when dc = 4v

when dc = 4 volt



Vout



① when $V_{in} = 3V$

$-3 + V_c + 4 = 0$

$V_c = -1$

$V_{out} = 4$ volt

② when $V_i = -3$

$3 + -1 + V_D + 4 = 0$

$V_D = -6$

$V_D < 0$ diode is off

$V_{out} = V_{in} - V_c = -3 - 1 = -2$ Vo