Faculty Of Engineering and Technology

Electrical and Computer Engineering Department

CIRCUITS AND ELECTRONICS LABORATORY

ENEE 2103

Experiment #: 8

The Field-Effect Transistor

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1.Abstract

The aim of this experiment is to understand the difference between the bipolar and the field effect transistor, and to estimate the characteristics of N-channel JFET when using as a common source and common drain. There are many tools used in this experiment and these tools are JFET transistors, dc power supplies, potentiometer, sine wave generator, digital multimeter, resistors, capacitors, oscilloscope, and digital multi meter (DMM).

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2.Theory

2.1. Field-Effect transistors (FET)

The Junction Field Effect transistor (JFET) is the earliest type of FET, In this type of transistor the current flows through an active channel between sources to drain terminals, and the voltage applied between gate and source controls the flow of electric current between the source and drain of the JFET. If we want to apply a reverse bias voltage to the gate terminal, the electric current is switched off completely.[1]

There are two types of JFET transistors, these types are N-channel and P-channel transistor.

If we want to use N-channel JFET, we must apply a positive voltage +VDD to the drain terminal of the transistor and we will not apply voltage to the gate terminal of the transistor. This way will allow the current to flow through the drain-source channel. If the gate voltage VG equal 0V, the drain current will be at its largest value for safe operation, and the JFET will be in the active region. In conclusion, after using positive voltage VDD and zero voltage applied to the base, the N-channel JFET has the largest current.[2]

if we look to Figure 2.2.1 we notice that the JFET is biased through a DC supply, which will control the VGS of the JFET. If we want to control the applied voltage across the Drain and Source terminal we must varying the VGS. From there, we can plot the I-V characteristics curve of a JFET.

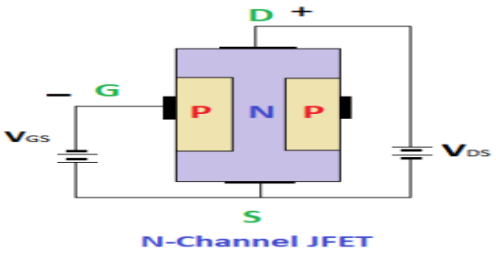


Figure 2.2.1: N-channel JFET

The output characteristics of JFET are drawn between drain current (ID) and drain-source voltage (VDS) at a constant gate-source voltage (VGS), as shown in Figure 2.2.2 below.

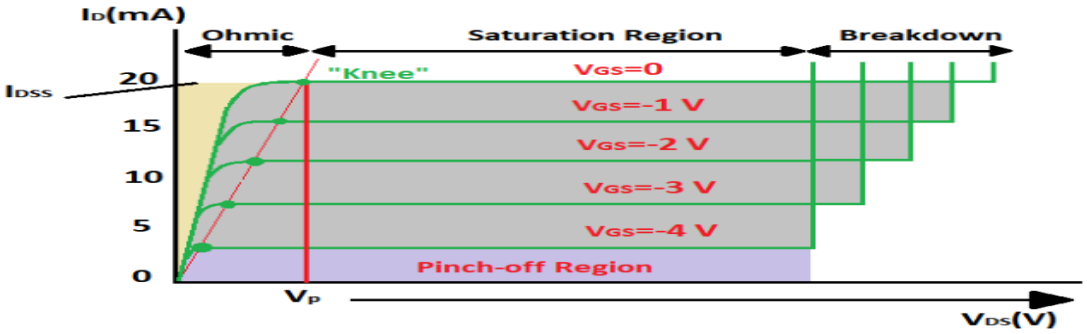


Figure 2.2.2: curve of ID and VDS

-Cut-off Region : This is the region where the JFET is off, that means there is no drain current and ID flows from drain to source.

-Ohmic Region : In this region, JFET begins to show some resistance to the drain current, ID that is starting to flow from drain to source. The current flowing through the JFET is linearly proportional to the applied voltage.

-Saturation Region :In this region, the drain-source voltage reaches a value such that the current flowing through the device is constant with the drain-source voltage and varies only with the gate-source voltage, the device is said to be in the saturation region.

-Breakdown Region :In this region, the drain to source voltage VDS exceeds the maximum threshold value, that causes the depletion region to break down, the JFET loses its ability to resist current, and the drain current increases indefinitely.[3]

2.2. JFET Amplifier

The JFET Amplifier is an electronic circuit in which the transistor is one of the main components. Among types of transistors, JFET is the second one. If JFET is present in an amplifier circuit, it is said to be a JFET amplifier.

The JFET can be operated mainly in three regions. Those are the Cut-off, Ohmic and Saturation regions. We must operate the JFET in the Ohmic or linear regions for amplification.

We can classify the JFET amplifiers in multiple ways. There is three types of JFET amplifiers since we have three configurations of JFET.

- Common Gate (CG) Amplifier
- Common Source (CS) Amplifier
- Common Drain (CD) Amplifier

1)Common Gate JFET Amplifier

In this type, the Gate terminal of JFET is common to both input and output. And we will consider the Source and Drain terminals of the JFET amplifier as the input and output terminals.

The Common Gate (CG) amplifier is like the Common Base (CB) amplifier. In this JFET amplifier, the AC (sinusoidal) voltage waveform applied at the Source terminal will be produced at the Drain terminal. There won't be any phase difference between the input and output waveforms.

This JFET amplifier's input and output resistances are low and high, respectively. We can use a CG amplifier as a voltage amplifier since it has a high voltage gain. The current gain of this amplifier is approximately equal to one.

2) Common Source (CS) Amplifier

In this type, the Source terminal of JFET is common to both input and output. And we will consider the Gate and Drain terminals of the JFET as the input and output terminals.

The Common Source JFET amplifier is like the Common Emitter (CE) amplifier. In this JFET Amplifier, the AC (sinusoidal) voltage waveform applied at the Gate terminal will be amplified and produced at the Drain terminal.

Both the input and output resistances of this JFET amplifier have a medium value. Even this amplifier's voltage and current gain are of medium value. We can use a CS amplifier as a power amplifier, just like a CE amplifier, since it has high power gain.

3) Common Drain (CD) Amplifier

In this type, the Drain terminal of the JFET amplifier is common to both input and output. And we will consider the Gate and Source terminals of the JFET as the input and output terminals.

The Common Drain JFET amplifier is like the Common Collector (CC) amplifier. In this JFET amplifier, the AC (sinusoidal) voltage waveform applied at the Gate terminal will be produced at the Source terminal with unity voltage gain. There won’t be any phase difference between the input and output waveforms.

This JFET amplifier's input and output resistances are high and low, respectively. The voltage gain of this amplifier is approximately equal to one.[4]

3.Procedure & Discussion

3.1.CHARACTERESTIC OF AN N-CHANNEL JFET

In this part the circuit was connected as shown in Figure 3.1.1, the current limit was set on bench power supply to its minimum value, and the voltage was set to zero, then the power supply was switched , the value of VDS was set to the first value in table 3.1 and the value of ID was read for each value of VGS, then this step was repeated for all the values of VDS in the Table 3.1.1, and the corresponding ID values was recorded in this table.

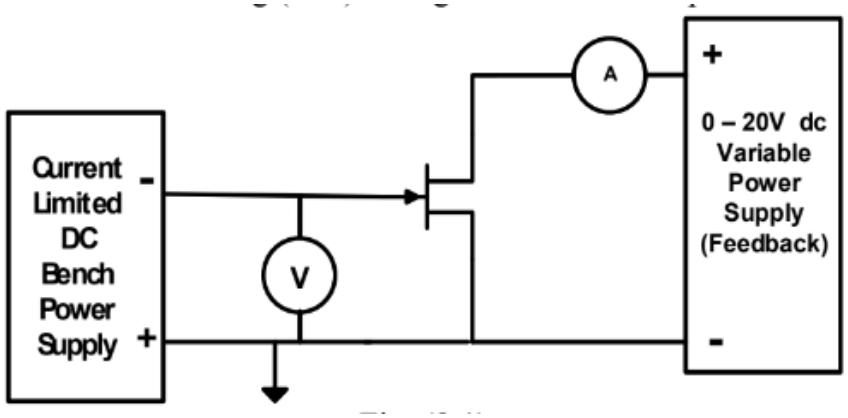


Figure 3.1.1: N-channel JFET circuit

VGS(V)		ID(mA) for VDS=(V)						
desired	actual	0	0.5	1	2	5	10	15
0	0	47.88Ua	1.15mA	3.29mA	4.85mA	7.01mA	7.18mA	7.114mA
-0.5	0.5	0.106mA	1.52mA	2.72mA	4.25mA	5.51mA	5.65mA	5.65mA
-1	1.1	97uA	1.12mA	2.28mA	3.17mA	4.01mA	4.11mA	4.12mA
-1.5	1.5	89uA	0.937mA	1.81mA	2.568mA	3.06mA	3.15mA	3.17mA
-2	2	746uA	0.75mA	1.34mA	1.86mA	2.16mA	2.2mA	2.24mA
-2.5	2.6	66uA	0.569mA	0.874mA	1.055mA	1.16mA	1.201mA	1.22mA

Table 1: values of ID for VDS

After that the VDS was set to 10v and VGS to -1.0v to measure IG .

The result is-> IG =0.05mA (it is too small).

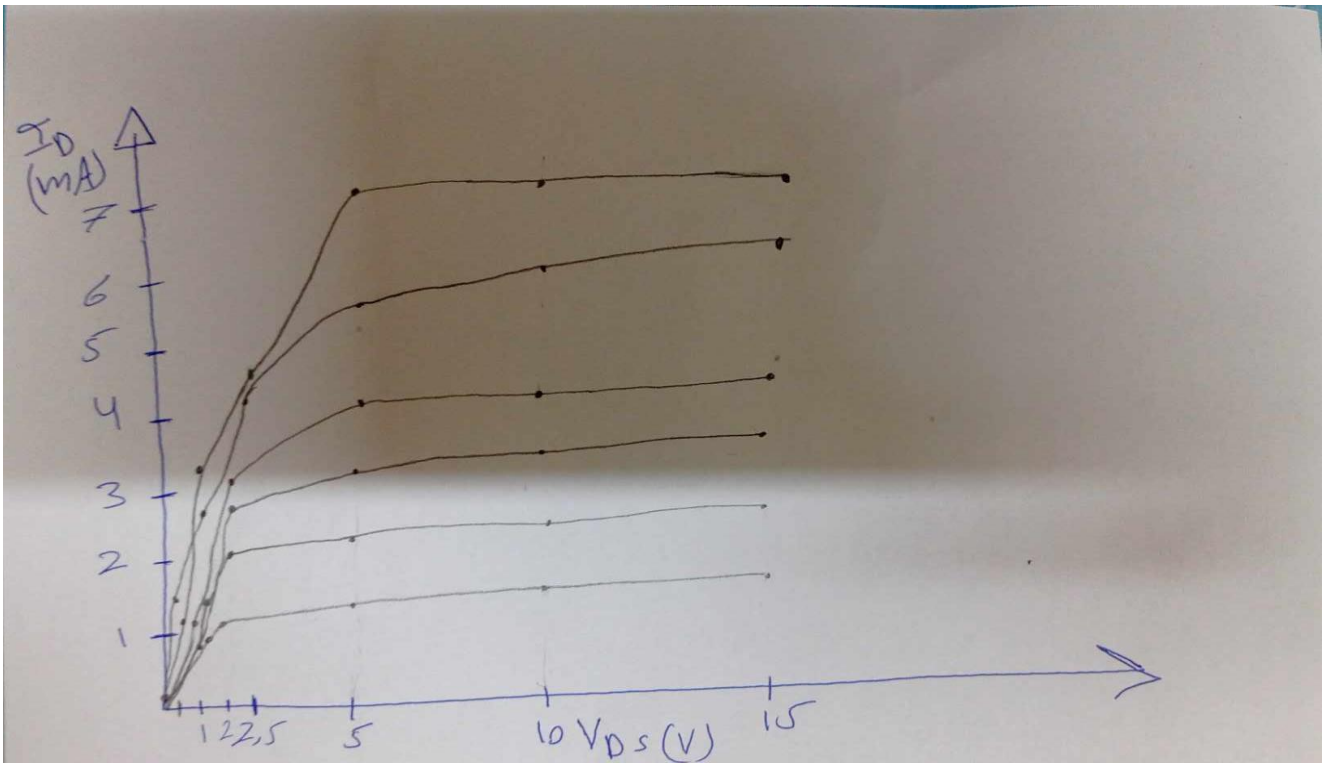


Figure 3.1.2: curve of ID and VDS for each value of VGS

The Figure 3.1.2 was showed that after the VDS reaches 5 volts the drain current ID start to be un affected by any change. And the relation between the drain current and VGS is approximately linear that's mean any decrease in VGS will decrease the current. The gate current in the N-channel JFET is very small because the gate-source junction is never forward biased, this is because channel remains open without any current flow through the gate.

To find the trans-conductance(gm) this equation was used ->

gm=(change in ID)/(change in VGS)

gm = (5.65-4.11)/(-0.5+1)=3.1m

Quantity	Value
IG	0.05mA
gm	3.1m

Table 2: measured values of part1

3.2.A JFET AMPLIFIER

In this part the circuit was connected as shown in Figure 3.2.1, the sine wave generator was set to a frequency of 1KH, and first the output amplitude was tuned to zero, so there was no signal input to the circuit, then the generator was applied an input of 2 volts peak-to-peak, the potentiometer was set to give a value of +10 V for VDS, then the output was observed on the oscilloscope as shown in Figure 3.2.2.

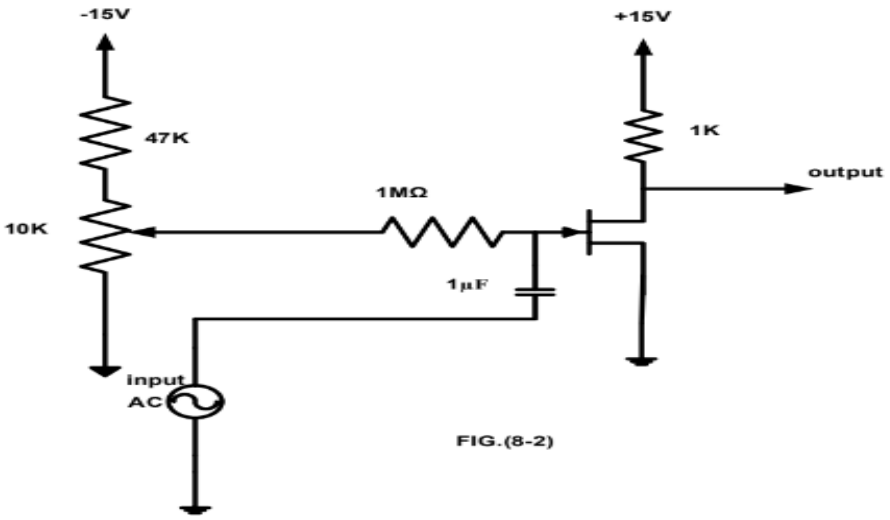


Figure 3.2.1: JFET Amplifier circuit

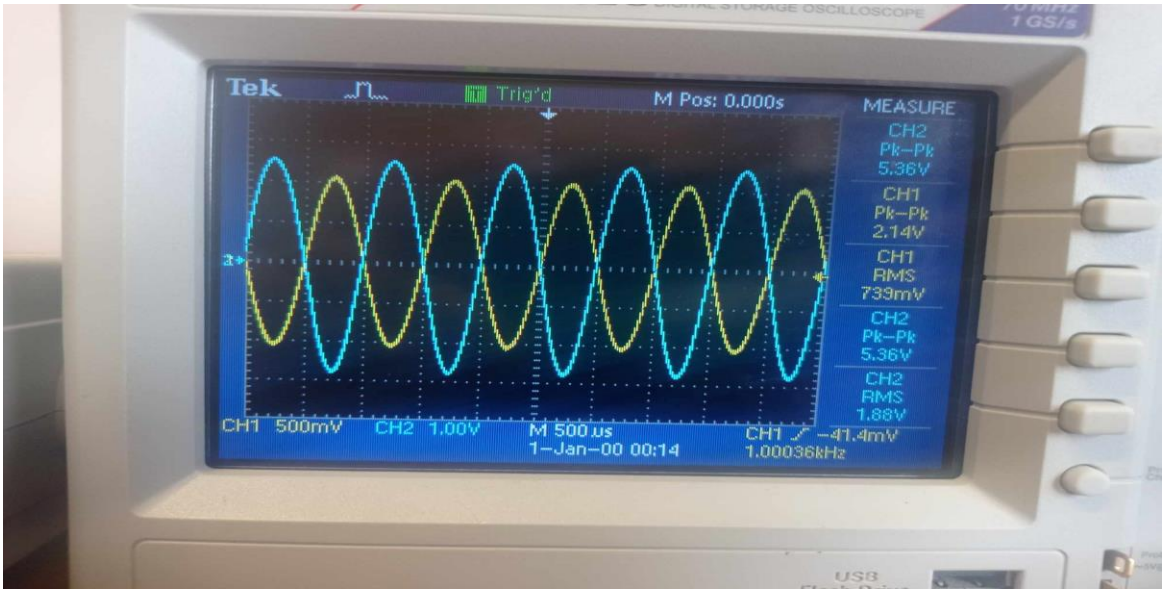


Figure 3.2.2: Vo and Vin

From Figure 3.2.2 -> peak-to-peak output voltage = 5.36v

Peak-to-peak input voltage = 2.14v

Voltage gain= Vo/Vin=5.36/2.14 =2.5

After that, the ac input current and voltage were measured using DMM, and the result is:

Vin = 0.72v

Iin = 25.8uA

So , Zin= Vin/Iin=0.72v/25.8uA=28 kohm

Quantity	Value
Vo	5.36v
Vin	2.14v
Voltage gain	2.5
Iin	25.8uA
Zin	28Kohm

Table 3: measured values of part 2

3.3.COMMON DRAIN AMPLIFIER

In this part, the circuit was connected as shown in Figure 3.3.1, the sine wave generator was set to a frequency if 1KH, and the output amplitude was turned to zero, so there was no signal input to the circuit.

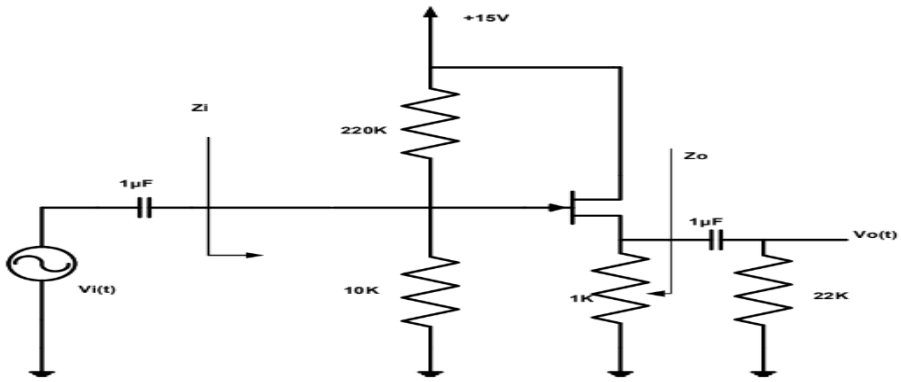


Figure 3.3.1: common drain amplifier

Then the DC voltages of VG and VS was measured. the result ->

VG=0.65v

VS= 2.53v

Then the generator was applied an input of 0.4 volts peak-to-peak, and the output was observed on the oscilloscope as shown in Figure 3.3.2.

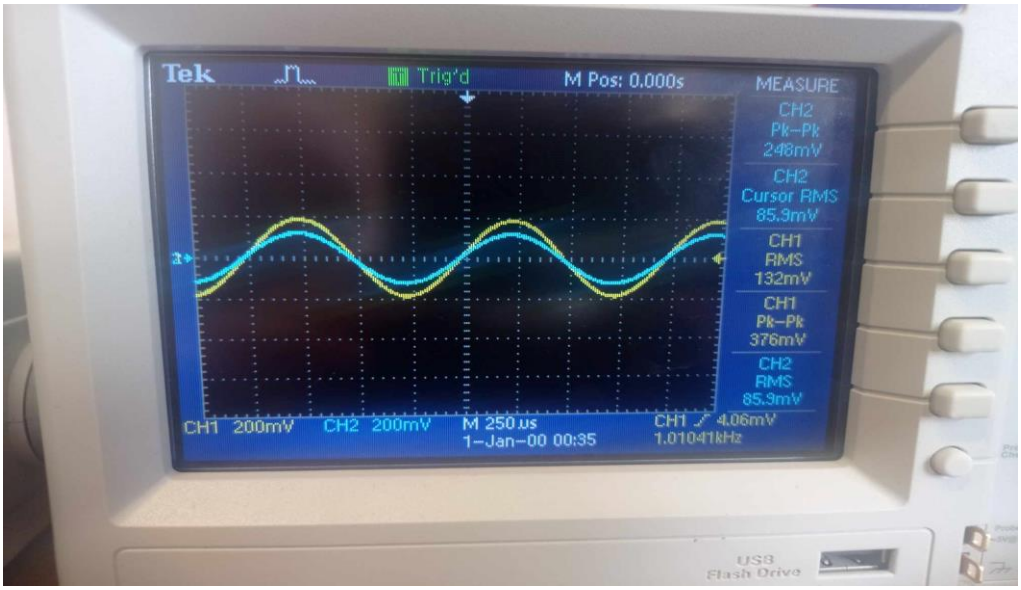


Figure 3.3.2: Vo and Vin

From Figure 3.3.2, the result is:

Vo=248mV

Vin = 376mV

Voltage gain=Vo/Vin=0.248/0.376=0.66

There is no phase shift between the input and the output voltage

Zin=Vin/Iin=130mV/26.3uA= 4.9 kohm

Zo=Vo/Iin=85mV/3.8uA= 22.4 kohm

to find voltage gain theoretical Vout = Rs(gm * Vgs) and Vgs=Vg-Vs=Vin-Vout

and Vout = Rs gm(Vin-Vout) , so Av=Vo/Vin=(Rs*gm)/(1+Rs*gm)

and gm = -2*(IDSS(1-Vgs/Vp)=3.5mV

substituting the values of the source resistance and the transconductance gives

Av=Vo/Vin=0.77, the obtained value was 0.66 which is close to the value of theoretical calculations.

Quantity	Value
VG	0.65v
VS	2.53v
Vo	248mv
Vin	376mv
Zin	4.9Kohm
Zo	22.4Kohm
Voltage gain (Av)	0.66
Voltage gain (Av) (theoretical)	0.77

Table 4: measured values of part3

4.Conclusion

In conclusion, after we finished this experiment we became able to estimate the characteristics of N-channel JFET when using as a common source and drain source with analysis of DC and AC small signal circuits, and we understand the difference between the bipolar and the field effect transistor, by using oscilloscope, DMM, JFET transistor, resistors, and capacitors.

5.References

[1] https://www.electronics-tutorials.ws/transistor/tran_5.html (accessed date 8/23/2023)

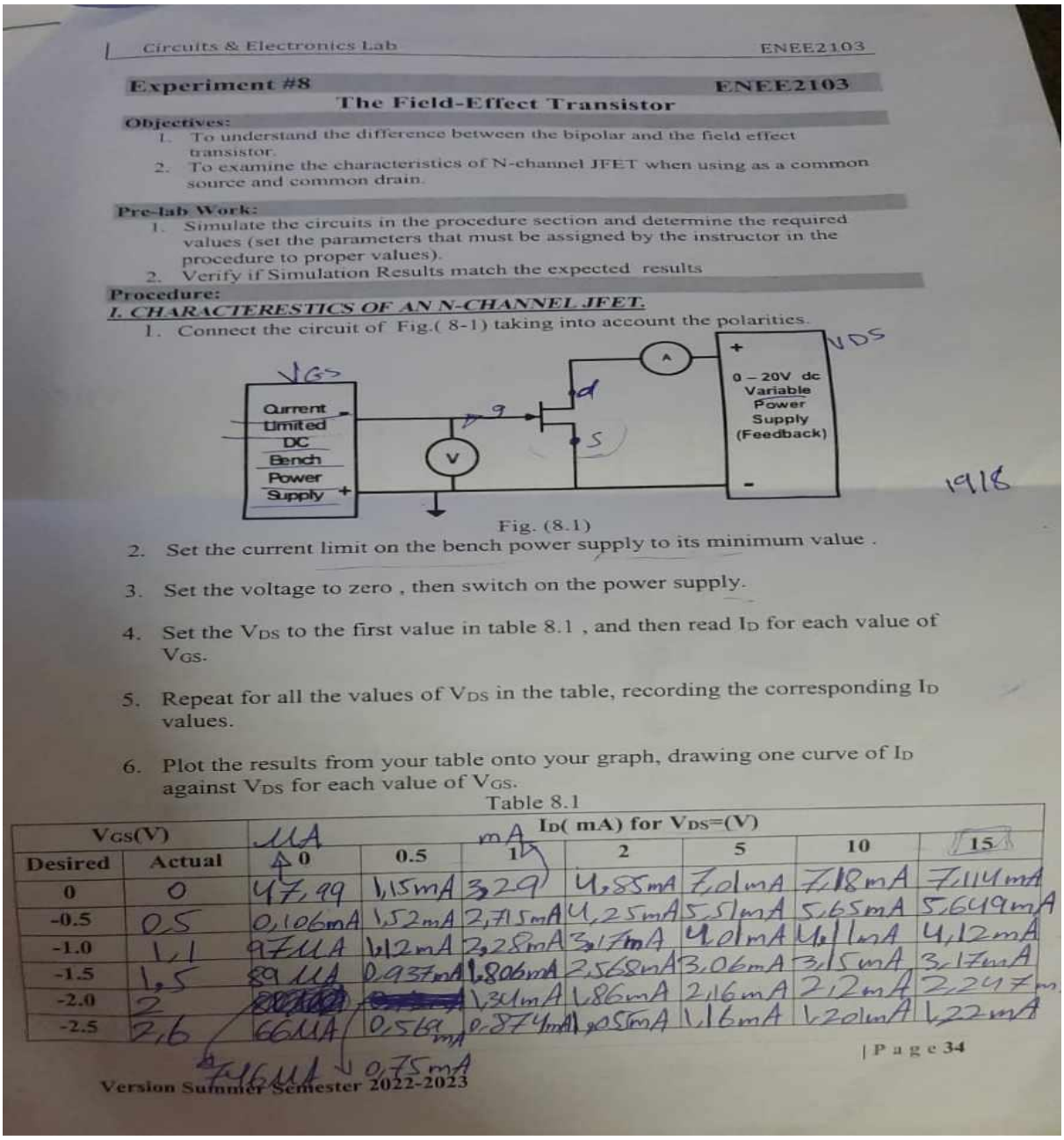
[2] https://www.learningaboutelectronics.com/Articles/N-channel-JFET

(accessed date 8/23/2023)

[3] https://staff-old.najah.edu/sites/default/files/Chapter%209.pdf (accessed date 8/23/2023)

[4] https://byjusexamprep.com/jfet-amplifier-i (accessed date 8/23/2023)

6.Appendices



Circuits & Electronics Lab ENEE2103

Experiment #8 **ENEE2103**

The Field-Effect Transistor

Objectives:

1. To understand the difference between the bipolar and the field effect transistor.
2. To examine the characteristics of N-channel JFET when using as a common source and common drain.

Pre-lab Work:

1. Simulate the circuits in the procedure section and determine the required values (set the parameters that must be assigned by the instructor in the procedure to proper values).
2. Verify if Simulation Results match the expected results

Procedure:

I. CHARACTERESTICS OF AN N-CHANNEL JFET.

1. Connect the circuit of Fig.(8-1) taking into account the polarities.

Fig. (8.1)

2. Set the current limit on the bench power supply to its minimum value .
3. Set the voltage to zero , then switch on the power supply.
4. Set the V_{DS} to the first value in table 8.1 , and then read I_D for each value of V_{GS}.
5. Repeat for all the values of V_{DS} in the table, recording the corresponding I_D values.
6. Plot the results from your table onto your graph, drawing one curve of I_D against V_{DS} for each value of V_{GS}.

Table 8.1

V_{GS}(V)		I_D(mA) for V_{DS}=(V)						
Desired	Actual	0	0.5	1	2	5	10	15
0	0	47,99	1,15mA	3,29	4,85mA	7,01mA	7,18mA	7,114mA
-0.5	0,5	0,106mA	1,52mA	2,715mA	4,25mA	5,51mA	5,65mA	5,649mA
-1.0	1,1	97uA	1,12mA	2,28mA	3,17mA	4,01mA	4,11mA	4,12mA
-1.5	1,5	89uA	0,937mA	1,806mA	2,568mA	3,06mA	3,15mA	3,17mA
-2.0	2	[illegible]	[illegible]	1,34mA	1,86mA	2,16mA	2,12mA	2,247mA
-2.5	2,6	66uA	0,569mA	0,874mA	1,055mA	1,16mA	1,20mA	1,22mA

716uA 0,75mA

7. Now go back to your circuit and set V_{DS} to 10 V and V_{GS} to -1.0 V ,then try to measure I_G.

Note: When preparing the prelab in Pspice use dc and parametric sweep to get the curves measured in Table 8.1

Questions:

- From your graph above which values of V_{DS} is I_D almost unaffected by V_{DS} when V_{GS}=0?
- For a given value of V_{DS} , (say 10 V),do equal changes of V_{GS} cause equal changes of I_D?
- Can you measure I_G or is it too small?
- From your graph, estimate the change in I_D for 0.5 change in V_{GS} when V_{DS} =10 V , and V_{GS} -1.0 V ,then find the trans conductance of the transistor(g_m).

Note: trans-conductance g_m =(change in I_D)/(change in V_{GS}).

II. A JFET AMPLIFIER.

1. Connect the circuit as shown in Fig. (8-2).

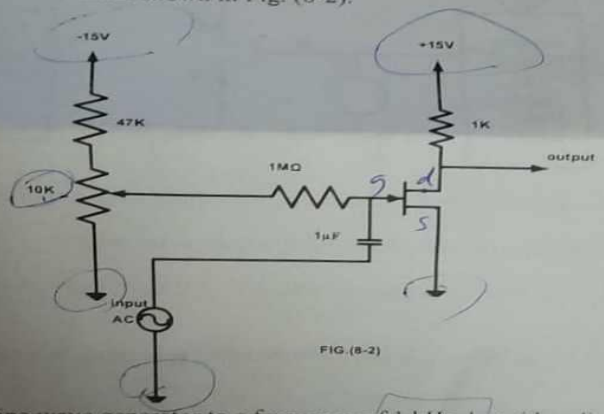


FIG.(8-2)

2. Set the sine wave generator to a frequency of 1 kHz ,but either disconnect its output ,or turn its output amplitude to zero, so there is no signal input to the circuit.
3. Set the potentiometer to give a value of +10 V for V_{DS}.
4. Now apply an input of 2volts peak-to-peak from the generator and observe the output on the oscilloscope.
5. Measure the peak-to-peak output voltage and calculate the voltage gain.

6. Measure the ac input current and voltage using DMM and calculate the input impedance Zin seen by the source. $V_{in} = 0.72V$ $I_{in} =$ 25.8 μA

III. COMMON DRAIN AMPLIFIER

1. Connect the circuit as shown in fig. (8-3).

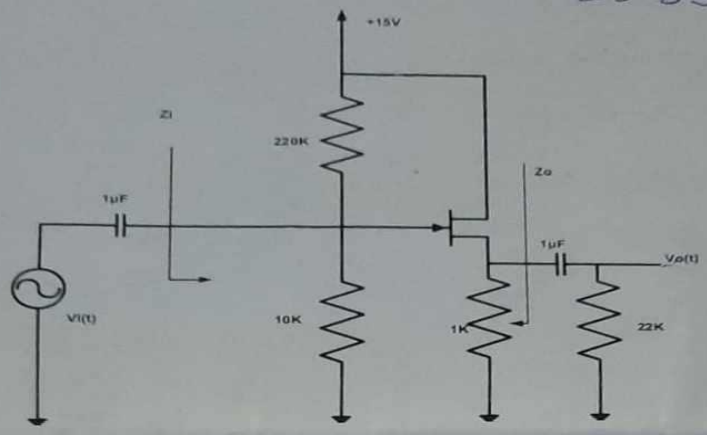


Fig.(8-3)

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2. Set the sine wave generator to a frequency of 1 kHz ,but either disconnect its output ,or turn its output amplitude to zero, so there is no signal input to the circuit.
3. Measure the DC voltages of V_G, and V_S. $V_G = 0.65$ V $V_S = 2.53$ V
4. Now apply an input of 0.4 volts peak-to-peak from the generator and observe the output on the oscilloscope. zero
5. Calculate the voltage gain and the phase shift between the input and output voltage. $V_o = 248$ mV, $V_{in} = 400$
6. Measure the values of Z_{in} and Z_{out} using the appropriate voltages and currents at the places shown in the previous figure. $V_{in} = 130$ mV $I_{in} = 26.3$ μA $V_{out} = 85$ mV $I_{out} = 3.8$ μA

Question:

- Compare the voltage gain of step 5 with the theoretical gain value.