Design Verification Project
“SPI – Track”

Group members:

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Introduction:

This report outlines the verification master plan for the SPI – Track project, focusing on validating the Serial Peripheral Interface (SPI) and Wishbone (WB) bus protocols. The project is structured into four phases: developing SPI and WB UVCs, testing the SPI Peripheral, system integration, and incorporating a Scoreboard UVC. Each phase defines specific tasks, verification strategies, and deadlines to ensure a systematic and efficient verification process.

Phase1: building the SPI and WB UVCs

Overview:

This phase focuses on developing the key UVCs required for the project:

1. Create the SPI UVC (Rahaf & Shahed).
2. Create the Wishbone UVC (Yasir).
3. Validate the standalone functionality of SPI and Wishbone before DUT integration.

Sequence item:

1. **SPI**

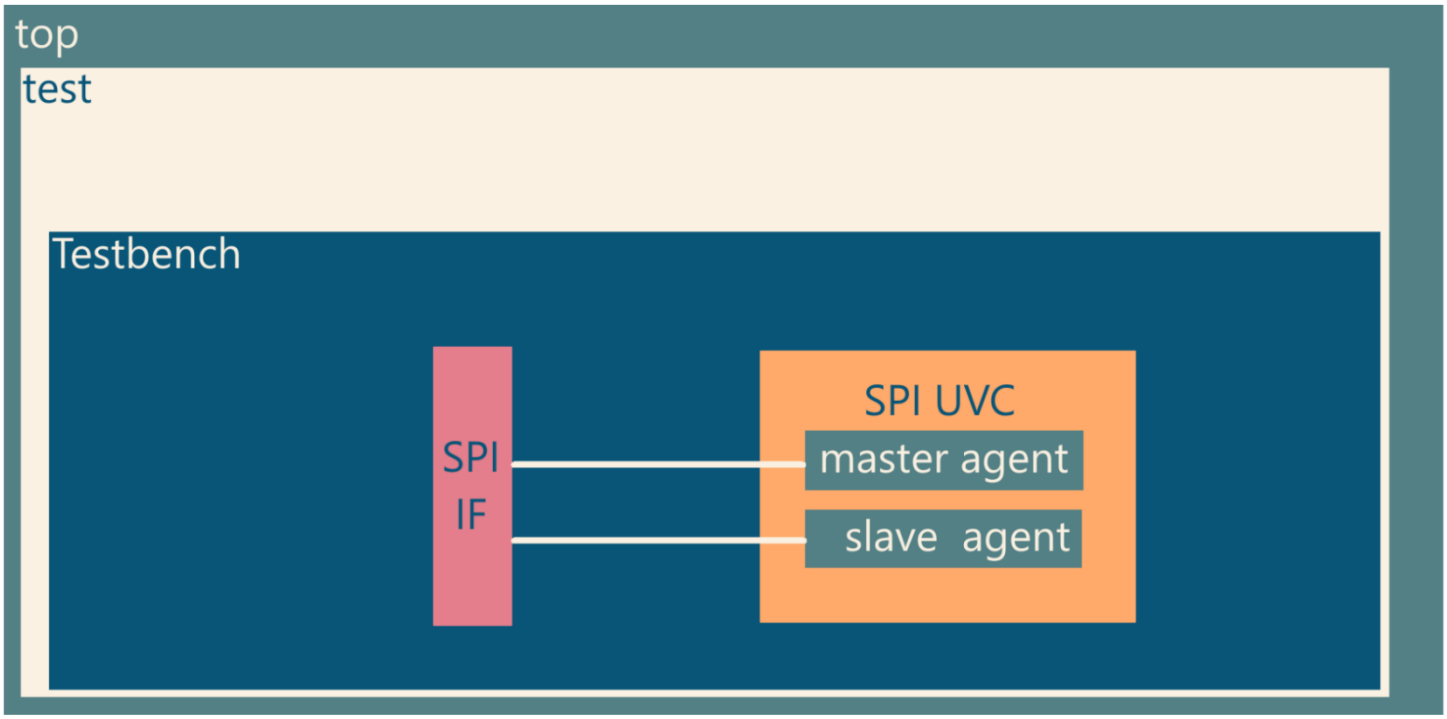
```
rand logic [7:0] din ;
rand logic [7:0] dout;
```

2. **WB**

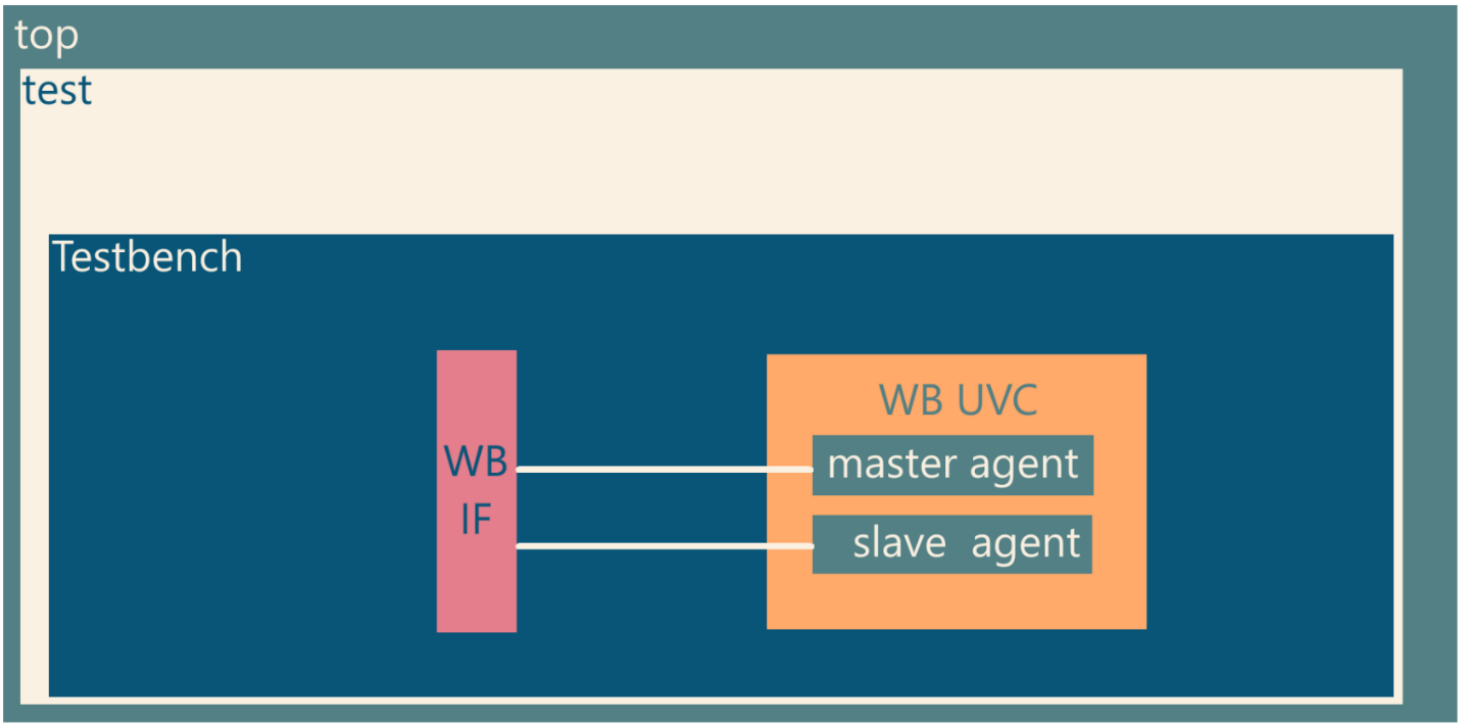
```
typedef enum bit  [1:0] { wb_read, wb_write , wb_ideal } op_type_enum;
rand op_type_enum op_type;
rand logic [31:0] addr;
rand logic [7:0] din ;
rand logic [7:0] dout;
```

Microarchitecture:

1. Serial Peripheral Interface (SPI) UVC**:**



2. Wishbone interconnect UVC**:**



verification Plan:

1. SPI UVC

No.	Test Case	Test Description	Test Type
1	**Basic Write Transaction**	SPI Master sends a single byte to Slave.	Directed
2	**Burst Write**	Master sends multiple bytes in sequence.	Directed
3	**Loop back Test**	MOSI connected to MISO to check data transfer.	Directed

2. WB UVC

No.	Test Case	Test Description	Test Type
1	**Write Transaction**	Generate data in master then ensure correct receive in slave side	Directed
2	**Read Transaction**	Generate data in slave then ensure correct receive in master side	Directed
3	**address = Data Transaction**	Send data to all SPI peripheral addresses (from master to sleave) and ensure correct receiving in slave	Directed
4	**Write Transaction to invalid address**	Send data to invalid addresses (from master to slave) and ensure error response	Directed

Deadline:
END of Monday, 19-March.

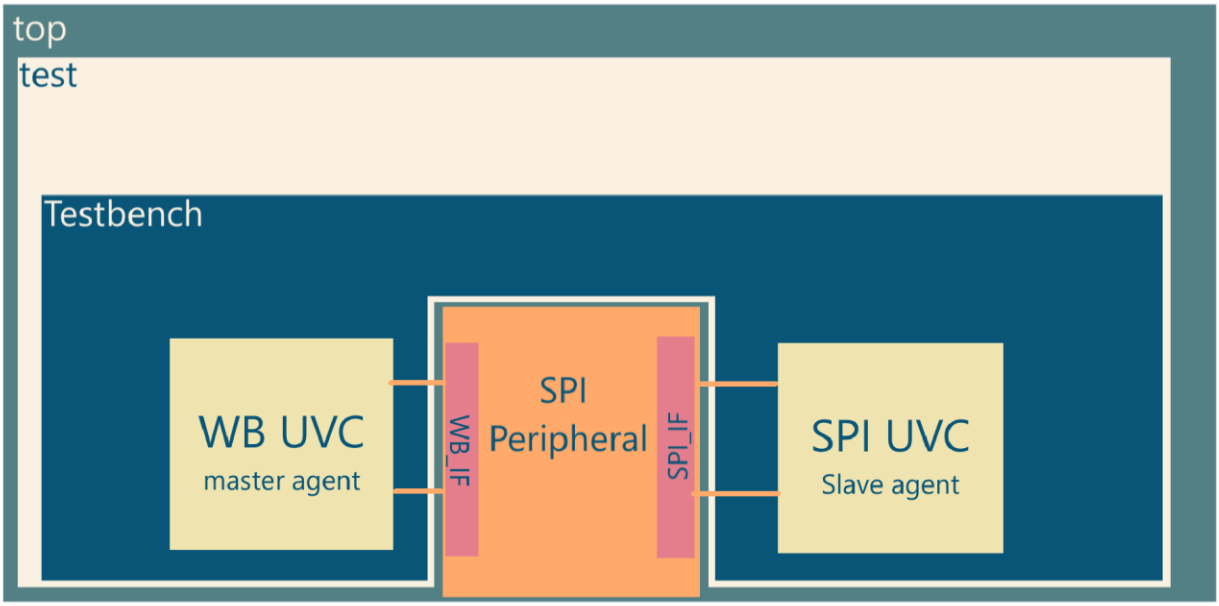
Phase2: Testing SPI Peripheral

Overview:

Before full system integration, this phase ensures the SPI Peripheral operates correctly by:

1. Connect the SPI slave UVC and Wishbone master UVC to the DUT SPI(Peripheral).
2. applying the transaction through WB master and verify the result in SPI slave by applying the tests in verification plans .

Microarchitecture:



Verification Plan:

TBC.

Deadline:
End of Tuesday, 18-March.

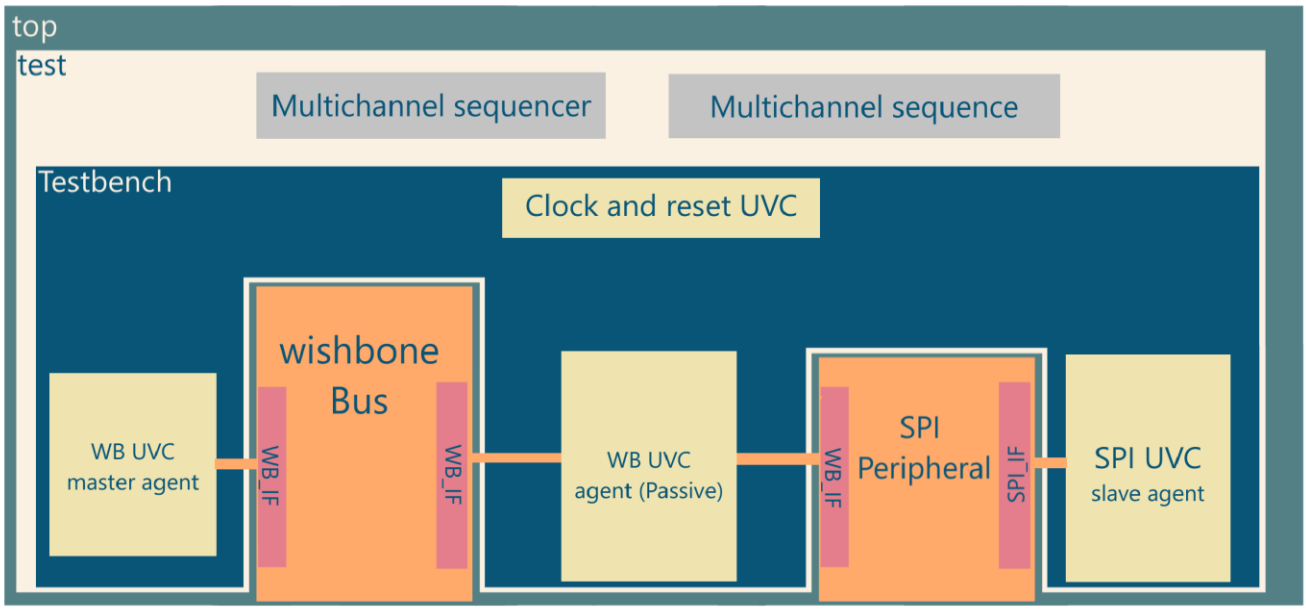
Phase 3: system integration (without Scoreboard).

Overview:

This phase consists of these primary tasks:

1. Integrating SPI Peripheral and WB interconnect bus into single testbench.
2. create a clock and rest UVC which will generate the clock and reset signal to the system.
3. creating a multichannel sequencer and a multichannel sequence and integrate them into the system.
4. Verify the system functionality.

Microarchitecture:



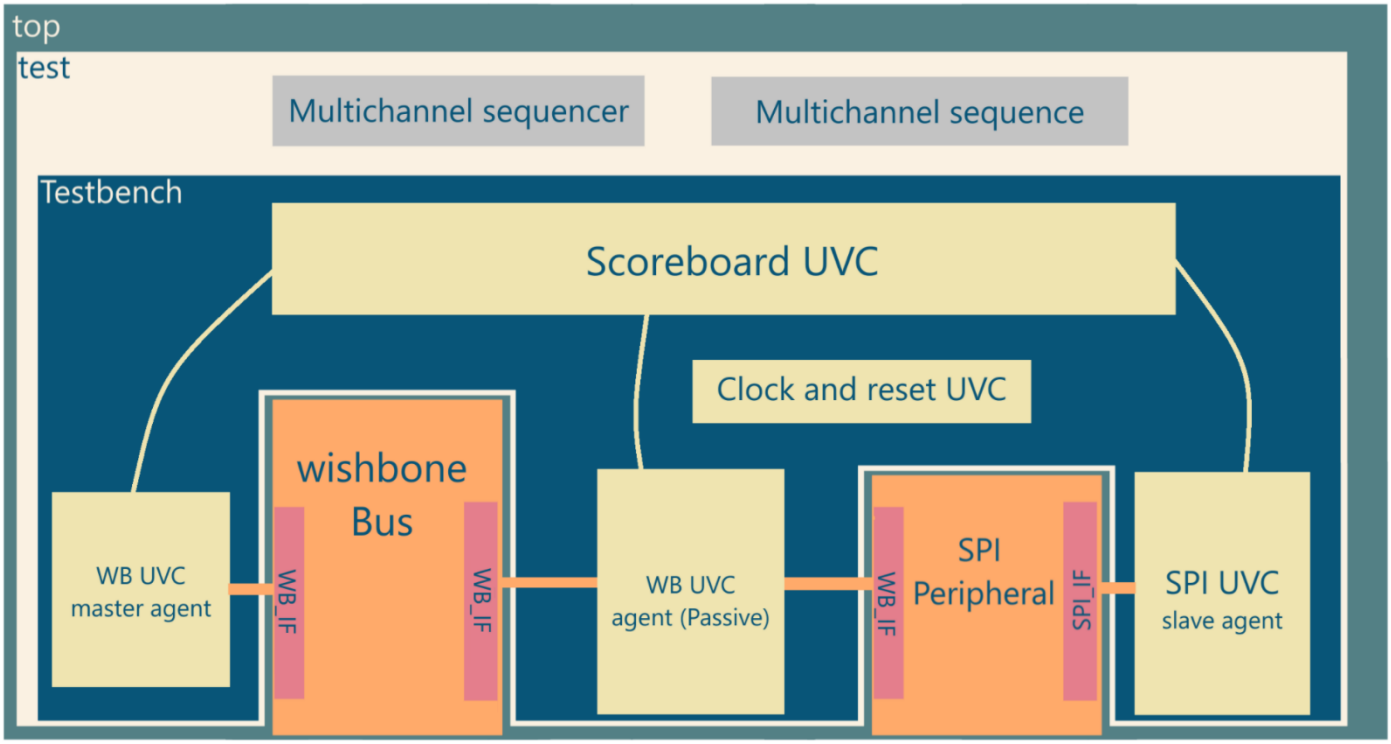
Verification Plan:
TBC.

Deadline:
END of Wednesday, 19-March.

Phase 4: adding Scoreboard UVC

Overview:
The focus of this phase is to incorporate the Scoreboard UVC and verify the complete system through final testing.

Microarchitecture:



Verification Plan:
TBC.

Deadline:
END of Thursday, 20-March.