Rahman Qureshi (Ray)

rahman.a.qureshi@gmail.com • http://rahmanqureshi.github.io

EDUCATION

University of Toronto, *BASc in Engineering Science – Computer Engineering* June 2019 (Expected)

- Relevant Courses: Machine Learning, Operating Systems, Algorithms, Control, Probability & Statistics

TECHNICAL SKILLS

- Fluent in C++, C, Java, Python, and Verilog (System)
- Relevant Technologies: Linux, Git, SciPy Stack, ROS, Gazebo, FreeRTOS, ARM Cortex M4, CMake, SQL, GCP
- Experience with circuit/pcb design and analysis tools including LTSpice, Altium

PROFESSIONAL EXPERIENCE

Software Engineering Intern May 2018 (Expected) – August 2018 (Expected)
Google Waterloo, ON, Canada

- Expected to develop compiler tools and libraries for GPU applications

Embedded Software Engineering Intern May 2017 – February 2018
Rapyuta Robotics Chuo-ku, Tokyo, Japan

- Developed embedded software for the ARM Cortex M4 microprocessor—specifically the STM32F4 MCU
- Wrote an application to receive simulated sensor data from gazebo over UART and publish over CAN
- Rewrote driver implementation for the MPU9250 IMU using STM's newer Hardware Abstraction Library (HAL)
- Developed drivers for an I2C Serial EEPROM chip (24AA64), and a logging library to store records in EEPROM. Used these to log important information that would be missed during a critical failure
- Developed Python infrastructure to support automated Hardware-In-The-Loop (HWIL) testing
- Developed a ROS package to run on embedded Linux to diagnose faulty hardware (e.g. sensors, radio modules)
- Learned about drone dynamics and control on the side through company resources

Software Engineering Intern January 2017 – April 2017
Google San Francisco, CA, USA

- Used Java and internal tools to integrate the AppEngine front-end into a sandbox environment
- Used AngularJS2, Flask, and BigTable to write a web-tool which identified Borg Job flag changes (side project)

Device Modelling and Design Verification Engineer May 2016 – December 2016
Intel San Jose, CA, USA

- Worked on modelling and verification of the transceiver (XCVR) of Intel's new 14nm FPGA, Stratix 10—mainly focusing on models for the Fractional Phase-Locked Loop (FPLL) and Transmit Data Path

Research Intern May 2015 – August 2015
Ultrasonic Non-Destructive Evaluation Laboratory Toronto, ON, Canada

- Developed a method to detect weak adhesion using ultrasound and machine learning, resulting in a trained SVM that could predict bond strength with >95% accuracy (k-fold cross-validation, k=10) on one type of pipe
- Used low-pass filtering and windowing to extract peak locations of echo responses, and fit a decaying exponential function to estimate the decay constant

Backend Web Developer May 2014 – August 2014
University of Toronto Information and Technology Services Toronto, ON, Canada

- Worked on the backend of a new website that is similar to Google API console as part of an initiative by the University to enable students to access University data

EXTRACURRICULARS AND PERSONAL PROJECTS

University of Toronto Aerospace Team May 2015 – May 2016

- Worked on the power subsystem of a 3U CubeSat as part of the Canadian Satellite Design Challenge

Programming Competition Director May 2015 – January 2016

- Designed a programming competition package for the University of Toronto Engineering Competitions
- Created app using City of Toronto Open Data map data (http://toronto-route-planner.herokuapp.com/)

8x8x8 LED Cube May 2016 – July 2016

- Designed, built, and programmed an 8x8x8 LED cube from scratch including base PCB and analog circuitry