ECE 303 Lab #3

A Design and Test of a Differential Amplifier with Variable Differential Gain and High CMRR

Lab section: (D6) Bench: #15 Date: 7th June, 2017

Abstract

The purpose of this lab is to design and build a differential amplifier as well as a current source to bias it. The differential amplifier and the current source are intended to eventually be used to create an op-amp. The differential amplifier and the current source were designed and tested modularly so that it would be easy to troubleshoot them. The differential amplifier provided a gain of 109 V/V at 100 kHz and a CMRR of 87 dB. The 4Q amplifier had DM amplification of 40.9 dB for frequencies less than 100 kHz and has a 3-dB drop-off point of 1.0 MHz. Two different current sources were designed; one with 2 transistors (2Q) and the other with 4 transistors (4Q). It was found that the 4Q current source was more stable; thus the differential amplifier was coupled with the 4Q current source for the final design.

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Our signatures certify that we are submitting our own, original work only, and do so in accordance with the University Code of Student Behaviour and APEGGA's Code of Ethics.

1. Objectives

The project's objectives were to design, build and test a high-CMRR differential amplifier with variable differential gain. A secondary objective of the lab was to experimentally compare various implementation of the differential amplifier for stability of the output. We were restricted to use a ±15V power supply and a biasing current of 10-15 mA to operate the differential amplifier. We decided to build a simple long-tail resistor differential amplifier and 2Q and 4Q current mirrors; We expected the amplifier with 4Q-current source to create the most stable output. The output of this differential amplifier circuit will later be used as the input to a simple operational amplifier. This stage will be coupled differentially to the operational amplifier. See Figure 1, for block diagram of a differential amplifier.

2. Design

We designed, built, and tested the differential amplifier modularly, as documented below.

2.1 Classical Long-Tail Differential Amplifier

A classical Long-Tail BJT Differential Amplifier, see Figure 2, was considered such that it operated with DC bias current of 14.3 mA and power supply of ±15 V. To select suitable resistors, we performed the following DC analysis:

1. Assumed zero input at the bases of the BJTs: $V_{IN}^{+} = V_{IN}^{-} = 0\ volts$.
2. Therefore, the emitter voltages would be $V_{Emitters} = V_B - V_{BE} = 0 - 0.7 = -0.7\ volts$.
3. Hence, long tail resistor of the following value needed: $R_{EE} = \frac{V_{Emitters} - V_{EE}}{I_{EE}} = \frac{-0.7\ V - -15\ V}{14.3\ mA} = 1\ k\Omega$. We expect a power dissipation of $P = IV = 14.3\ mA * 14.3\ V = 204\ mW$ which is an acceptable value for this temporary configuration.
4. For the BJTs to stay in forward bias mode, $V_{Collector} \geq V_{Emitter} + 0.3\ V = -0.4\ V$. Thus, collector resistor maybe in the following range: $0 < R_C \leq \frac{V_{CC} - V_C}{\frac{I_{BIAS}}{2}} = \frac{15 - -0.4}{\frac{14.3}{2}} = 2.15\ k\Omega$. We selected collector resistors of 1.2 kΩ. We expect a power dissipation of $P = I_{R_C} V_{R_C} = \frac{14.3\ mA}{2} * (15 - \frac{14.3}{2} 1200) = 4.59\ mW$ across this resistor.

In summary, we selected a bias current of 14.3 mA using R_C = 1.2 kΩ and R_{EE} = 1 kΩ. Additionally, we expect single ended differential amplification of this design to be $A_d^{SE} = \frac{R_C\ I_{Bias}}{4V_T} = 172\frac{V}{V}$. We

expect that this value to be a function of input frequency and it would also be prone to power supply limits and other unaccounted for variables.

2.2 Simple 2Q Current Source

A simple 2Q current source, see Figure 3, capable of delivering 14.3 mA was designed. The current source was connected to the ground at one end, and to -15 V at the other. The resistor that was used had a resistance of $R_{REFF} = \frac{\Delta V_{REFF}}{I_{REFF}} \approx \frac{0-V_C}{I_{BIAS}} = \frac{0-(V_{EE}+V_{BE})}{I_{BIAS}} = \frac{14.3\,V}{14.3\,mA} = 1.0\,k\Omega$. We expect the beta of the transistors to be 500 at when collector emitter voltage is about 10 V (from data sheets). Additionally, the output resistance of this configuration is expected to be $\frac{V_A}{I_{BIAS}} = \frac{V_A}{14.3\,mA}$. The early voltage of the BJT is provided to be between 23 to 990 volts in the datasheets.

2.3 High Stability 4Q Current Source

A high stability 4Q current source, see Figure 4, capable of delivering 14.3 mA was designed using ±15V power supply and 2.0 kΩ resistor. The required resistance that was used was calculated as follows:

$$R_{REFF} = \frac{\Delta V_{REFF}}{I_{REFF}} = \frac{V_{CC}-V_{EE}-2V_{BE}}{I_{BIAS}} \approx \frac{15--15+2*0.7}{14.3} = 2.0\,k\Omega.$$

The output resistance of this configuration is expected to be $\beta\frac{V_A}{2\,I_{BIAS}} = \frac{250\,V_A}{14.3\,mA}$. The early voltage of the BJT is provided to be between 23 to 990 volts in the datasheets.

2.4 Differential Amplifier with 4Q Current Source

Finally, the 4Q current source, which is expected to be the more stable current source, would replace the long-tail resistor used in design 2.1. The circuit diagram of this design is shown in figure 5. We still expect a 14.3 mA bias current. This design requires a total of 28.6 mA of current and ±15 V power supply.

3. Test results

For the long-tail differential amplifier, we measured the bias voltages at each nodes, frequency response of common and differential modes, and linearity measurements of common and differential modes. For the 2Q and 4Q current mirrors, we tested the stability of the circuit as a function of load resistance. Finally, for the differential amplifier with 4Q current source, we tested its frequency response and linearity under differential and common mode input. Additionally, we measured the DC biasing point of this design.

3.1 Long-Tail Differential Amplifier

To measure the DC bias point, we grounded the base of the BJTs and measured the collectors and emitters voltages. See figure 2. We found the two collector voltages to be $V_{OUT}^{+} = V_{OUT}^{-} = 6.45\ V$ and the emitter voltage to be $V_{EMITTERS} = -0.675\ V$. This implies the current through the long-tale resistor to be $I_{R_{EE}} = \frac{V_{EMITTERS} - V_{EE}}{R_{EE}} = \frac{-0.675 - -15}{1000} = 14.3\ mA$, as expected.

The frequency response of the voltage gain under differential mode was measured by grounding the input V_{in}^{-} and feeding to V_{in}^{+} a variable frequency sinusoid of 50 mV peak-to-peak. The peak-to-peak output voltage was then measured at the V_{out}^{+} node. From this value, the differential voltage gain was calculated $-\ Gain\ in\ dB = 20 \log\left(\frac{V_{out}}{V_{in}}\right) -$ and the differential mode 3-dB bandwidth found to be 900 kHz. See Table 1(a) and Graph 1 for summary of results.

To observe DM voltage gain linearity, we fixed the input frequency to 100 kHz and varied the peak-to-peak amplitude of the input from 50 mV to 170 mV. We observed that saturation begins to form at 150 mV_{pp} input. See Graph 2 for summary of results.

Similarly, for common mode frequency response, the same 50 mV_{pp} sinusoid was fed to inverting and noninverting inputs of the differential amplifier and $V_{out}^{+}$was measured at various input frequencies. See Table 1(b) and Graph 3 for summary of results. We found the common mode 3-dB bandwidth of this design to be 1.2 MHz.

Finally, similar to DM linearity measurement, to observe the CM voltage gain linearity, we fixed input frequency to 100 kHz and varied the peak-to-peak input voltage. We observed saturation at about 350 mV_{pp} input. See Graph 4 for summary of results. See Appendix A for gathered raw data.

3.2 Current Mirrors, 2Q and 4Q

To test the stability of the current sources, we connected the output current to a variable resistor and varied the load resistance from 100 Ω to 2.0 kΩ. We noticed that the output current of the 2Q current mirror changes linearly from 33 mA to 14.3 mA as the load resistance changes from 300 Ω to 1.0 kΩ. See Graph 6. On the contrary, 4Q current mirror output a stable 14.8±0.5 mA current for load resistance in the range 200 Ω to 1.0 kΩ. See Graph 7. Thus, we conclude that the 4Q current mirror is more stable than 2Q current mirror. See Appendix B for gathered raw data.

3.3 Differential Amplifier with 4Q Current Mirror

With the long-tail resistor replaced with 4Q current source, we performed all the measurements in 3.1 again. We found the DC bias point of the circuit to be non-symmetrical, which was unexpected, and while $V_{IN}^{+} = V_{IN}^{-} = 0\ V$, we measured the following DC parameters, (See figure 5):

$$V_{OUT}^{+} = 4.91\,V$$

$$V_{OUT}^{-} = 4.01\,V$$

$$V_{Emitters} = -666\,mV$$

$$V_{BASE\ Q3-Q4} = -13.9\,V$$

$$V_{BASE\ Q5-Q6} = -14.6\,V$$

The single ended gain in differential mode was obtained when input voltage was 50 mV_{pp} and the 3-dB drop-off frequency was found to be 1.0 MHz. The SE DM gain was found to be 40.9 dB for frequencies less than 100 kHz, see Graph 7. The SE CM gain was obtained when the input voltage was fixed at 3.80 V_{pp}; this mode resulted in gain of -46±1 dB in the range 850 to 1000 kHz, see Graph 8. See Appendix C for gathered raw data.

4. Simulation results

Prior to assembling and testing of the designs, LT Spice was used to obtain better estimates of the behavior of the circuit. The LT Spice simulations were performed using the same set up as described in the testing section above.

The DC operating point of the Long-Tail Differential Amplifier was found as follows: the collector voltages were found to be at 6.46V while the voltage at the emitter was found to be -0.707V. The DC current of the differential amplifier was 14.3 mA. See Appendix D for further nodal voltage analysis of this configuration. AC and transient behavior of the circuit was observed visually to confirm that it behaves similar to experimental measurements. Additionally, we visually observed the CM and DM simulations, but due to extensive amount of analysis and lake of time we were unable to provide findings with this report.

Similarly, models of 2Q and 4Q current mirrors were drawn in LT Spice. Operating points of the models were found using 1.0 kΩ test load. See appendix E and F for DC nodal voltages. For the 2Q current mirror, an output current of 14.1 mA was simulated while the 4Q current mirror suggested 14.27 mA. Transient and frequency responses of the simulation was visually observed.

Finally, differential amplifier with 4Q current source was simulated and operating point was found. See appendix G for the DC nodal voltages.

5. Discussion

We were able to design a differential amplifier that is highly stable; it has a DM gain of 78 V/V at 100 kHz and -46.4 dB CM gain.

The theoretical, simulation, and experimental data agree with each other reasonably well. For example, the DC bias point at the emitter of the long tail differential amplifier was computed to be -0.7 V (see section 2.1) and it was measured to be -0.675 V (see section 3.1). The simulated voltage at this node was -7.07 V (see section 4). For the simulation stage, the main source of error was the absence of the exact model of the BJT transistor that we were using. We used BJT models for 2N2222 by NPX for our simulations while MPQ2222 by Central was used during the implementation. To reduce the experimental sources of error, we aimed to follow the matching principal and used transistors in the same pack to create the differential amplifier and another set for the current source. Unfortunately, as it was discovered later during testing of the 4Q differential amplifier, as it is evidence by the nonsymmetrical bias voltages (see section 3.3), our amplifier is not totally symmetric. We are fairly certain that this id due to discrepancies in the actual resistance of R_{C1} and R_{C2}. We believe that using 1% resistors instead of 5% resistors would enhance the performance of our design. Additionally, during testing phase, we discovered that the is a notable amount of coupling between adjacent wires used to build the circuit. We believe use of wires with better shielding and a more shielded breadboard would decrease the amount of coupling and thus the noise we observed.

6. Conclusion

We built and tested 2Q and 4Q current mirrors and found that 4Q current mirror has a high current stability over a wide range of test loads (200-1000 ohms), while 2Q current source has almost a linear output current that varies depending on the resistance of the load. Additionally, we discovered that a differential amplifier has coupled with a 4Q current source has a higher CMRR than that of classical long-tail resistor differential amplifier. Our purposed 4Q amplifier has a voltage gain of 109 V/V at 100 kHz and a CMRR of 87 dB. The DM amplification of this design is 40.9 dB for frequencies less than 100 kHz and has a 3-dB drop-off point of 1.0 MHz.

Appendix

Appendix A: Raw data collected for the long-tail differential amplifier for CM and DM

Differential Mode Frequency Response Raw Data

Frequency	DM Peak to Peak Output Voltage
f (kHz)	$V_{out\ pp}$ (V)
0.05	6.40
0.5	6.50
200	6.40
250	6.25
350	6.00
450	5.73
550	5.60
650	5.35
750	5.05
850	4.78
900	4.50
950	4.36
960	4.35
1000	4.25
1100	4.00
1200	3.70
1300	3.55
1400	3.35

Differential Mode Linearity Raw Data

Input Voltages (V)	Output Voltage (Pk to Pk) (V)
0.05	6.5
0.10	11.4
0.11	12.2
0.12	13.0
0.13	13.6
0.14	14.2
0.15	14.4
0.16	14.5
0.17	14.7

Common Mode Frequency Response Raw Data

Frequency (Hz)	Peak to Peak Voltage (V)
100	0.125
1000	0.125
100000	0.125
500000	0.113
1000000	0.096
1100000	0.094
1200000	0.089
1300000	0.086
1400000	0.083
1500000	0.08
1600000	0.077
1700000	0.075
1800000	0.072
1900000	0.07
2000000	0.069
10000000	0.028

Common Mode Linearity Raw Data

Input Voltages (V)	Output Voltage (Pk to Pk) (V)
0.05	0.031
0.10	0.061
0.20	0.115
0.25	0.143
0.30	0.168
0.31	0.173
0.32	0.175
0.33	0.180
0.34	0.185
0.35	0.185

Appendix B: Raw data collected to analyze 2Q and 4Q current mirror stability

2Q Current Mirror Raw Data

Resistance	Output Voltage
R_{test} (Ω)	V_o (V)
100	-6.8
150	-7.1
200	-8.5
300	-10.0
400	-11.6
500	-12.8
600	-13.8
700	-14.8
800	-14.8
900	-14.8
1000	-14.8
4000000	-15.0

4Q Current Mirror Raw Data

Resistance	Output Voltage
R_{test} (Ω)	V_o (V)
100	-1.30
200	-2.89
300	-4.45
400	-5.99
500	-7.51
600	-9.06
700	-10.62
800	-12.15
900	-13.97
950	-14.18
1000	-14.26
1500	-14.23
2000	-14.24

Appendix C: Raw data collected to analyze Differential Amplifier with 4Q current mirror.

Differential Mode Frequency Response Raw Data

Frequency f (kHz)	DM Peak to Peak Output Voltage $V_{out\ pp}$ (V)
0.20	5.45
0.50	5.53
1.00	5.53
3.00	5.53
5.00	5.47
10.00	5.47
15.00	5.47
50.00	5.53
75.00	5.49
100.00	5.39
500.00	4.92
600.00	4.72
750.00	4.46
850.00	4.22
900.00	4.10
1000.00	*3.90*
1100.00	3.66
1200.00	3.42
1300.00	3.26
1400.00	3.06
1500.00	2.89

Differential Mode Linearity Raw Data

Input Voltages (V)	Output Voltage (Pk to Pk) (V)
0.050	5.5
0.060	6.8
0.065	7.2
0.075	8.0
0.085	8.9
0.090	9.4
0.098	10.1
0.100	10.3

Common Mode Frequency Response Raw Data

Frequency	CM Peak to Peak Output Voltage
f (kHz)	$V_{out\ pp}$ (V)
0.750	0.0260
1.50	0.0233
5.00	0.0200
7.50	0.0196
8.50	0.0185
9.00	0.0181
9.50	0.0180
10.00	0.0179
15.00	0.0171
50.00	0.0162
100.00	0.0182
200.00	0.0240
300.00	0.0328
500.00	0.0513

Appendix D: DC operating point of long-tail differential amplifier.

```
       --- Operating Point ---
V(supply_15v):  15             voltage
V(Vout+):       6.46493        voltage
V(Vout-):       6.46493        voltage
V(Vemitters):   -0.706583      voltage
V(Supply_-15):  -15            voltage
V(Vin+):        0              voltage
V(Vin-):        0              voltage
Ic(Q2):         0.00711256     device_current
Ib(Q2):         3.41477e-005   device_current
Ie(Q2):         -0.00714671    device_current
Ic(Q1):         0.00711256     device_current
Ib(Q1):         3.41477e-005   device_current
Ie(Q1):         -0.00714671    device_current
I(R_ee):        0.0142934      device_current
I(R_c1):        0.00711256     device_current
I(R_c2):        0.00711256     device_current
I(Vin-):        -3.41477e-005  device_current
I(Vin+):        -3.41477e-005  device_current
I(V2):          0.0142934      device_current
I(V1):          -0.0142251     device_current
```

Appendix F: DC operating point of 2Q current mirror.

```
       --- Operating Point ---
V(base):        -14.2716       voltage
```

```
V(v_ee_-15v):   -15            voltage
V(i_output):    -14.1406       voltage
Ic(Q2):         0.0141406      device_current
Ib(Q2):         7.39356e-005   device_current
Ie(Q2):         -0.0142145     device_current
Ic(Q1):         0.0141237      device_current
Ib(Q1):         7.39449e-005   device_current
Ie(Q1):         -0.0141977     device_current
I(R_reff):      0.0142716      device_current
I(R_test):      -0.0141406     device_current
I(V1):          -0.0284122     device_current
```

Appendix E: DC operating point of 4Q current mirror.

```
       --- Operating Point ---

V(base_q1_q2): -13.5428       voltage
V(q1_q3):      -14.2711       voltage
V(q2_collector):-13.557       voltage
V(base_q3_q4): -14.2715       voltage
V(v_ee_-15v):   -15           voltage
V(v_cc_15v):    15            voltage
Ic(Q3):         0.0141966     device_current
Ib(Q3):         7.43436e-005  device_current
Ie(Q3):         -0.014271     device_current
Ic(Q4):         0.0141966     device_current
Ib(Q4):         7.43436e-005  device_current
Ie(Q4):         -0.0142709    device_current
Ic(Q2):         0.0142705     device_current
Ib(Q2):         7.47596e-005  device_current
Ie(Q2):         -0.0143453    device_current
Ic(Q1):         0.0141227     device_current
Ib(Q1):         7.39391e-005  device_current
Ie(Q1):         -0.0141966    device_current
I(R_reff):      0.0142714     device_current
I(R_test):      -0.0142705    device_current
I(V_cc_15v):    -0.0142714    device_current
I(V_ee_-15v):   -0.0285419    device_current
```

Appendix F: DC operating point of differential amplifier with 4Q current mirror.

```
       --- Operating Point ---
V(supply_15v): 15             voltage
V(vout+):      6.46683        voltage
V(vout-):      6.46683        voltage
V(vin+):       0              voltage
V(vemitters):  -0.706576      voltage
V(vin-):       0              voltage
V(base_q3_q4): -13.5461       voltage
V(q3_q5):      -14.2745       voltage
V(base_q5_q6): -14.2714       voltage
V(v_ee_-15v):   -15           voltage
Ic(Q5):         0.014207      device_current
Ib(Q5):         7.44042e-005  device_current
Ie(Q5):         -0.0142814    device_current
Ic(Q6):         0.0142074     device_current
```

```
Ib(Q6):          7.4404e-005    device_current
Ie(Q6):          -0.0142818     device_current
Ic(Q4):          0.0142902      device_current
Ib(Q4):          6.59963e-005   device_current
Ie(Q4):          -0.0143562     device_current
Ic(Q3):          0.014133       device_current
Ib(Q3):          7.39969e-005   device_current
Ie(Q3):          -0.014207      device_current
Ic(Q2):          0.00711098     device_current
Ib(Q2):          3.41393e-005   device_current
Ie(Q2):          -0.00714512    device_current
Ic(Q1):          0.00711098     device_current
Ib(Q1):          3.41393e-005   device_current
Ie(Q1):          -0.00714512    device_current
I(R_reff):       0.014273       device_current
I(R_c1):         0.00711098     device_current
I(R_c2):         0.00711098     device_current
I(V_ee_1):       -0.0285633     device_current
I(Vin-):         -3.41393e-005  device_current
I(Vin+):         -3.41393e-005  device_current
I(V1):           -0.028495      device_current
```

Tables and Figures

Figure 1: Block diagram of a differential amplifier is shown below. For our design, we require V_{CC} = 15 V and $-V_{EE}$ = -15 V. We aimed for bias current of I_{BIAS3} = 10 to 15 mA.

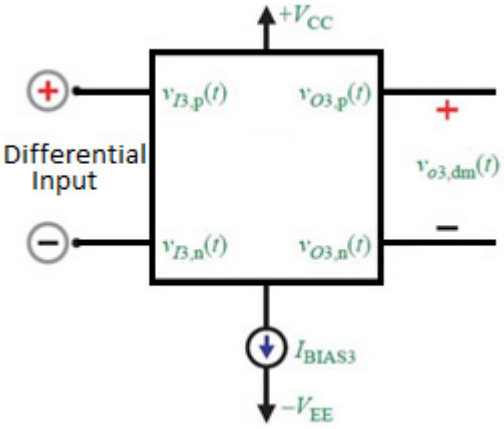


Figure 2: The designed BJT long-tail resistor differential amplifier is shown below. The simulated DC bias current of the amplifier is I_{R_EE} = 14.3 mA with collector voltages of V_C = 6.46 volts.

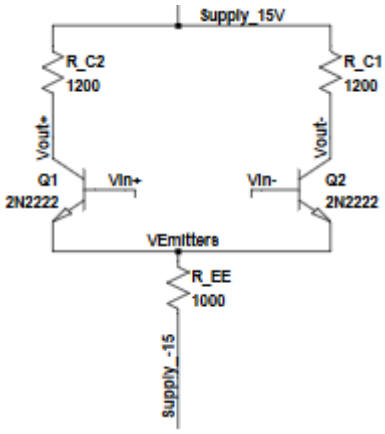


Figure 3: The designed BJT 2Q Current Source is shown below. As seen below, the current source is connected to the ground and -15 V supply and employs a 1.0 kΩ resistor. The output current is expected to be on the order of 14.3 mA.

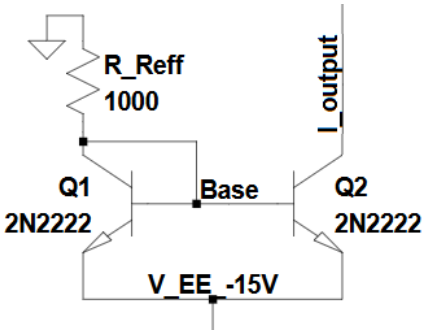


Figure 4: The designed 4Q Current Source is shown below. As seen below, the current source is connected to the ground and ±15 V supply and employs a 2.0 kΩ resistor. The output current is expected to be on the order of 14.3 mA.

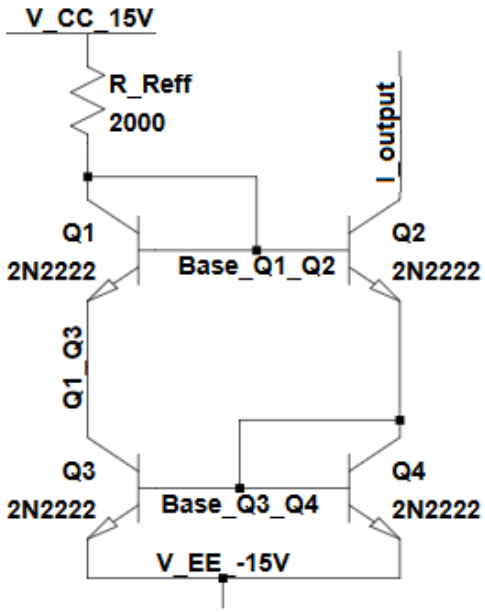
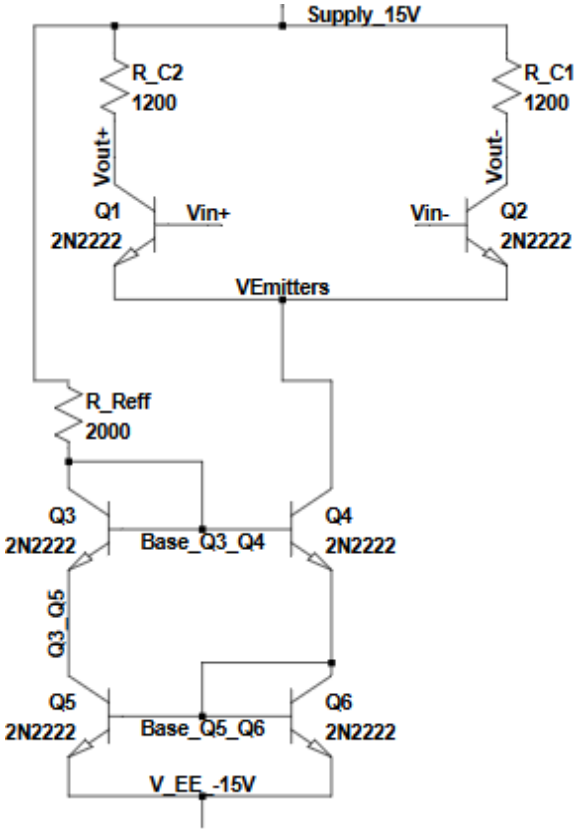


Figure 5: The designed Differential Amplifier with 4Q current source shown below. The amplifier requires 28.6 mA of current and ±15 V power supplies.



Tables 1(a) & 1(b): Differential Mode & Common Mode Gain Measurements for Differential Amplifier with Long Tail Resistor (R_{LT}):

Table 1(a): Diff. Amp. (w/ R_{LT}) DM Gain Measurement

Frequency (kHz)	Gain (dB)
0.050	42.14
0.500	42.28
200	42.14
250	41.94
350	41.58
450	41.18
550	40.98
650	40.59
750	40.09
850	39.61
900	*39.08*
950	38.81
960	38.79
1000	38.59
1100	38.06
1200	37.38
1300	37.03
1400000	36.52

Table 1(b): Diff. Amp. (w/ R_{LT}) CM Gain Measurement

Frequency (kHz)	Gain (dB)
0.100	-4.08
1.00	-4.08
100	-4.08
500	-4.96
1000	-6.38
1100	-6.56
1200	*-7.03*
1300	-7.33
1400	-7.64
1500	-7.96
1600	-8.29
1700	-8.52
1800	-8.87
1900	-9.12
2000	-9.24

Tables 2(a) & 2(b): Resulting Output Currents I_O over Varying Test Resistances for 2Q & 4Q Current Source Configurations:

Table 2(a): 2Q Output Current I_O over Varying Test Resistance R_{Test}

R_{Test} (Ω)	I_O (mA)
100	-68.30
150	-47.40
200	-42.55
300	-33.33
400	-29.00
500	-25.60
600	-23.00
700	-21.14
800	-18.50
900	-16.44
1000	-14.80

Table 2(b): 4Q Output Current I_O over Varying Test Resistance R_{Test}

R_{Test} (Ω)	I_O (mA)
100	-13.00
200	-14.45
300	-14.83
400	-14.98
500	-15.02
600	-15.10
700	-15.17
800	-15.19
900	-15.52
950	-14.93
1000	-14.26
1500	-9.49
2000	-7.12

Tables 3(a) & 3(b): Differential Mode & Common Mode Gain Measurements for Differential Amplifier with 4Q Current Source:

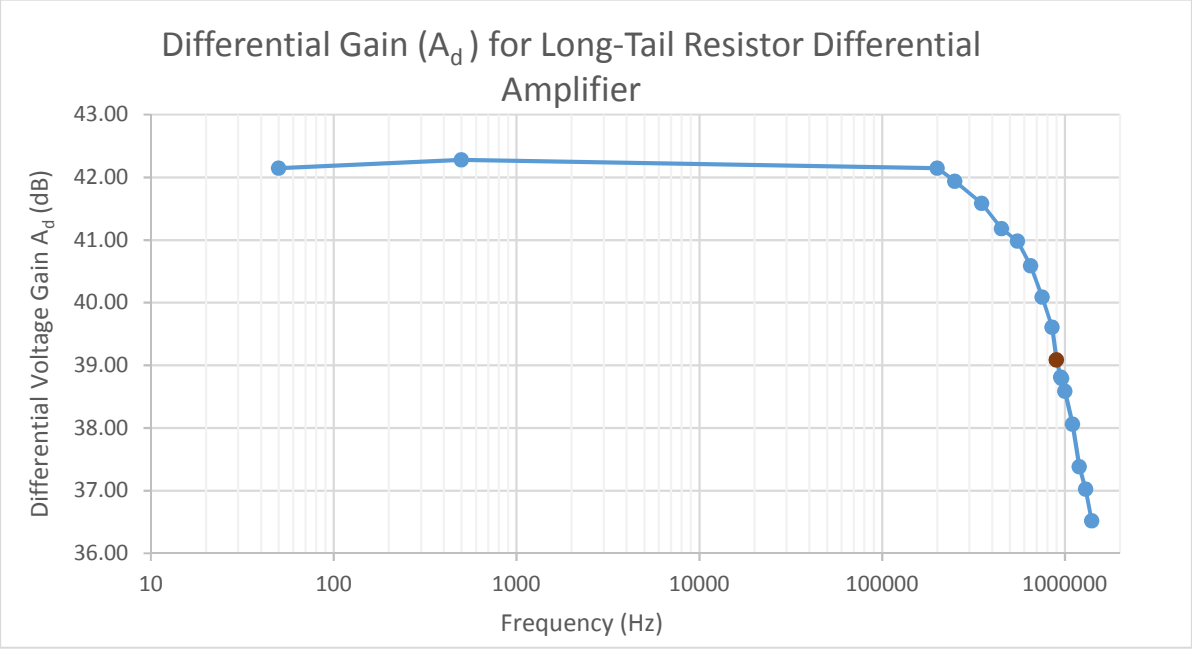
Table 3(a): Diff Amp (w/ 4Q) DM Gain

Frequency (Hz)	Gain (dB)
200	40.75
500	40.88
1000	40.88
3000	40.88
5000	40.78
10000	40.78
15000	40.78
50000	40.88
75000	40.81
100000	40.65
500000	39.86
600000	39.50
750000	39.01
850000	38.53
900000	38.28
1000000	*37.84*
1100000	37.29
1200000	36.70
1300000	36.28
1400000	35.74
1500000	35.24

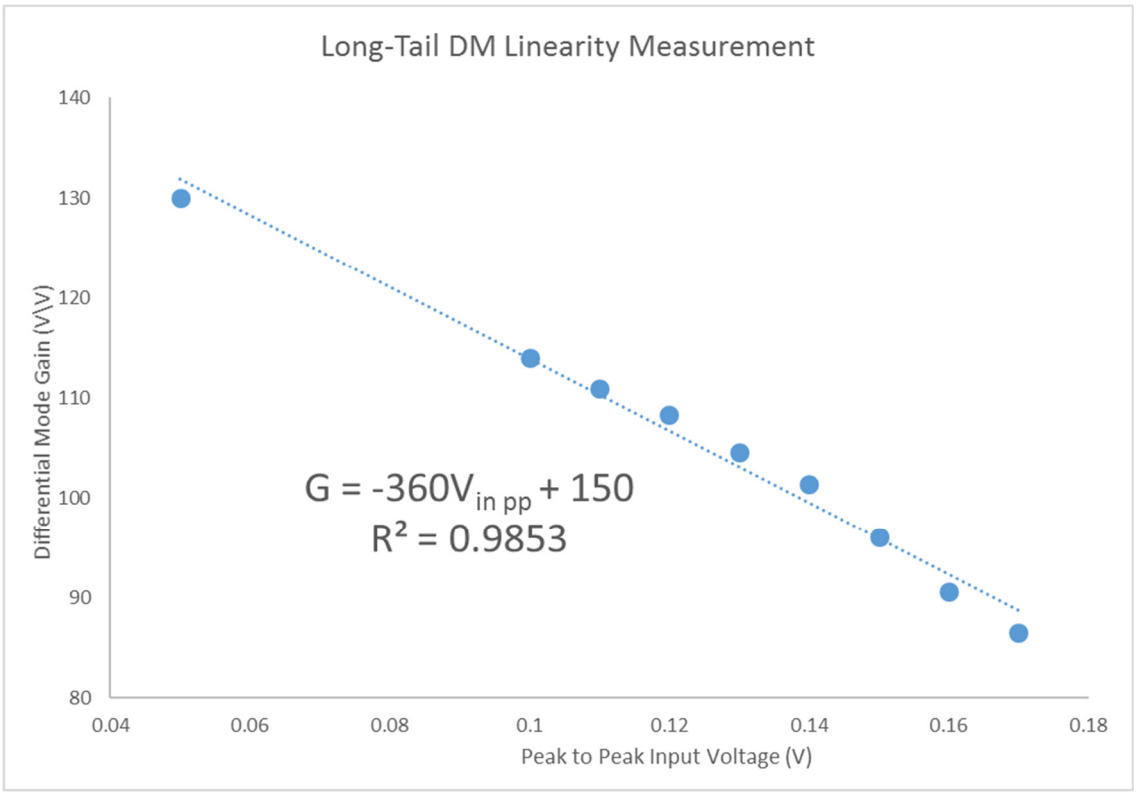
Table 3(b): Diff Amp (w/ 4Q) CM Gain

Frequency (Hz)	Gain (dB)
750	-43.30
1500	-44.25
5000	-45.58
7500	-45.75
8500	*-46.25*
9000	-46.44
9500	-46.49
10000	-46.54
15000	-46.94
50000	-47.41
100000	*-46.39*
200000	-43.99
300000	-41.28
500000	-37.39

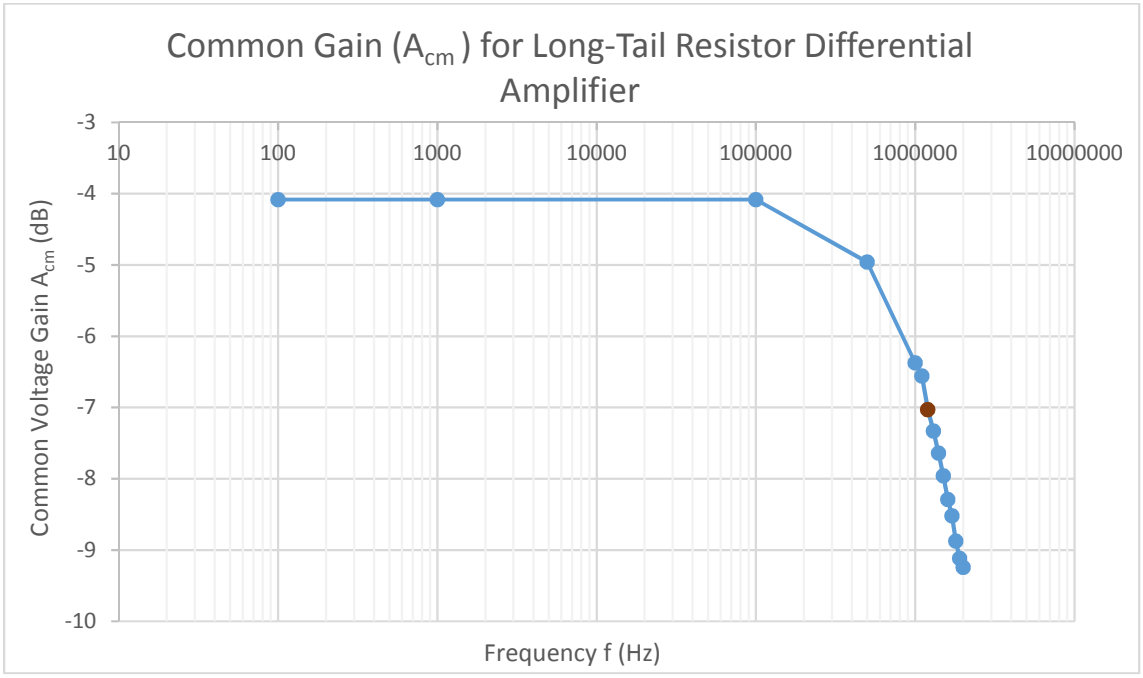
Graph 1: Resultant differential mode gain as a function of frequency for Long-Tail Resistor amplifier. The brown marker indicates the 3-dB drop-off point.



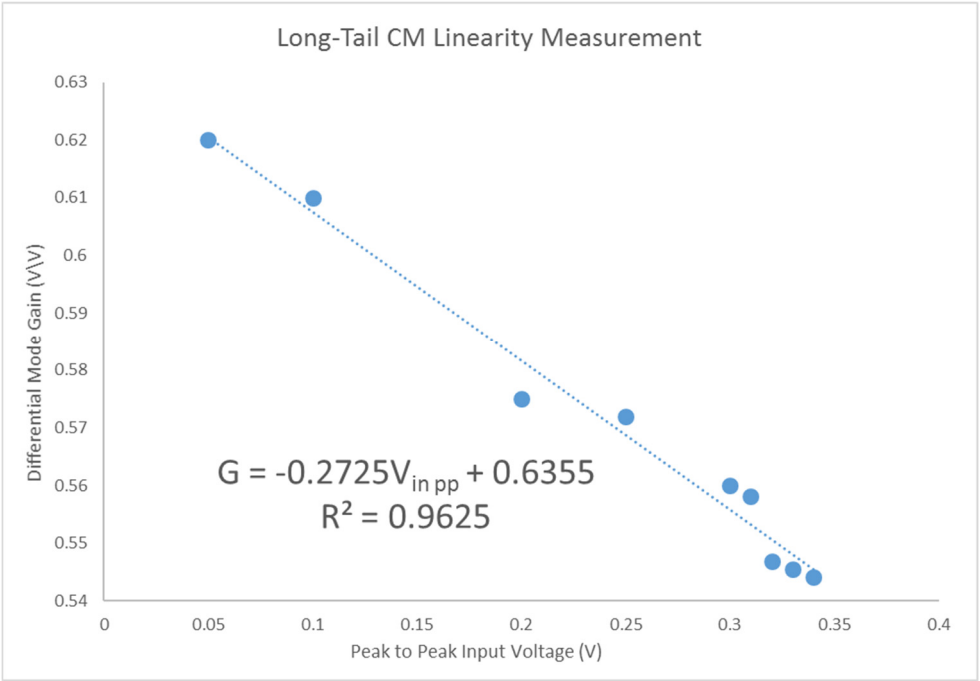
Graph 2: DM linearity measurement of differential amplifier with long tail resistor. The voltage gain linearly decreases from 130 V/V for 50 mV_{pp} input to 86 V/V for 170 mV_{pp} input.



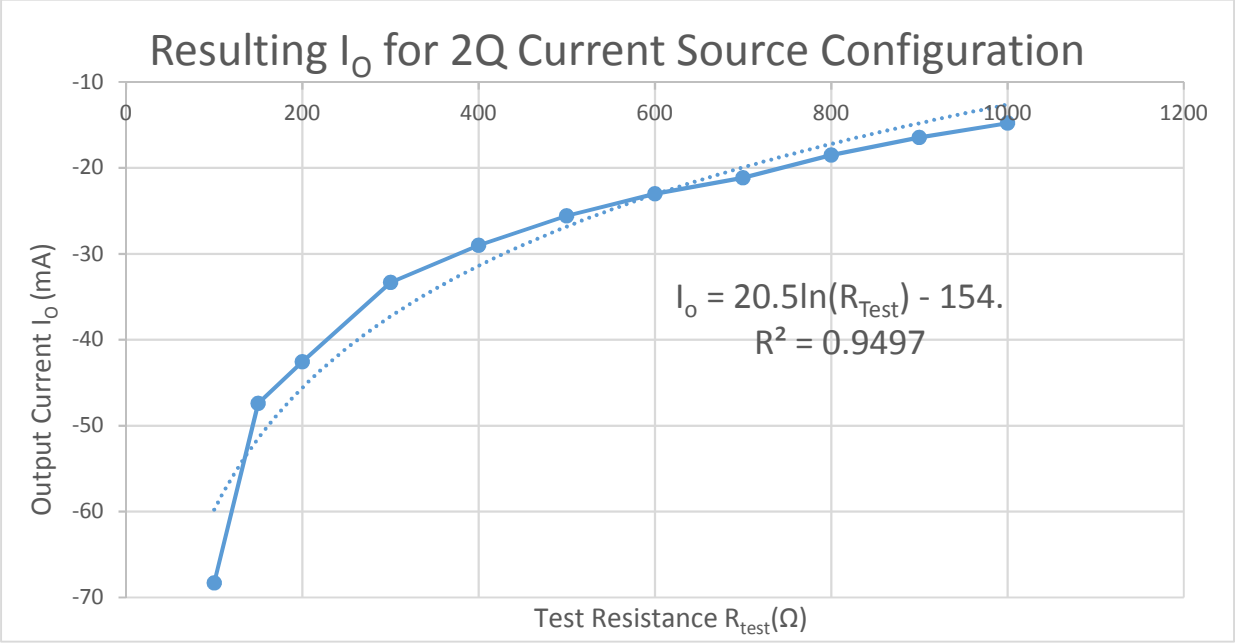
Graph 3: Resultant common mode gain as a function of frequency (w/ Long Tail Resistor). The brown marker indicates the 3-dB drop-off point



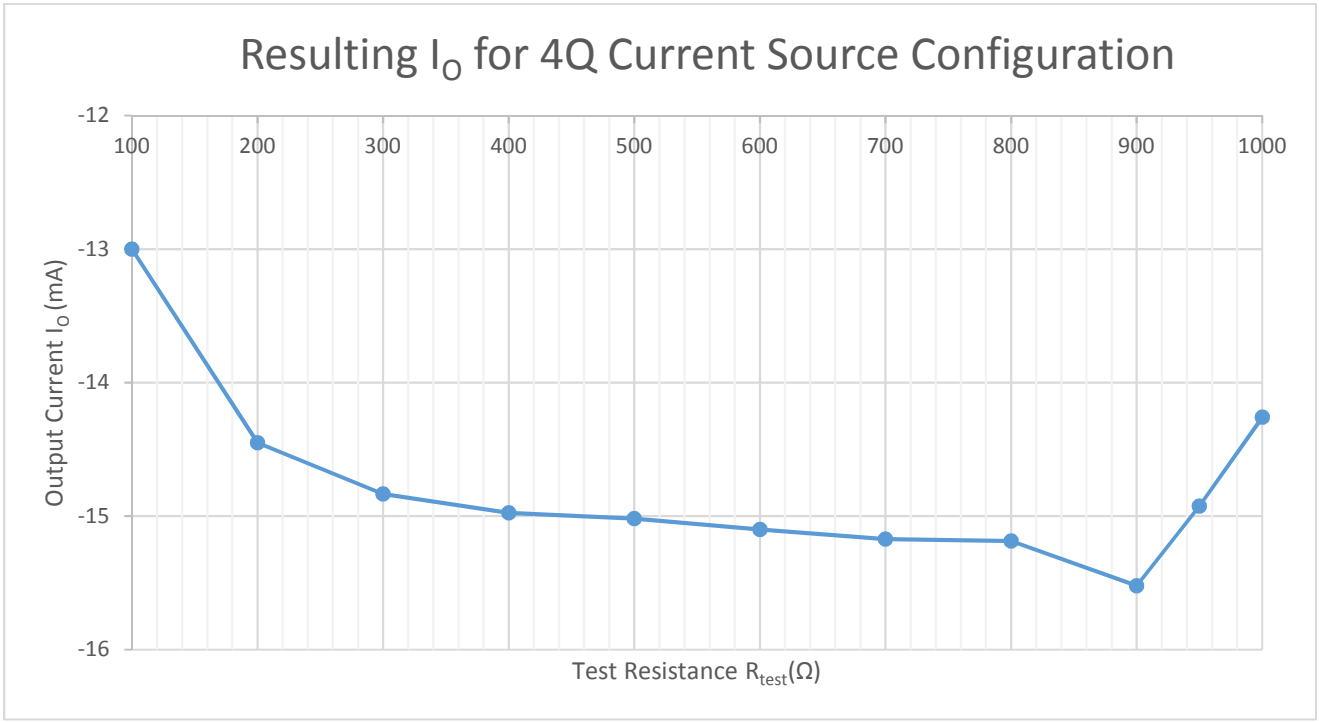
Graph 4: CM linearity measurement of differential amplifier with long tail resistor. The voltage gain linearly decreases from 130 V/V for 50 mV_{pp} input to 86 V/V for 170 mV_{pp} input.



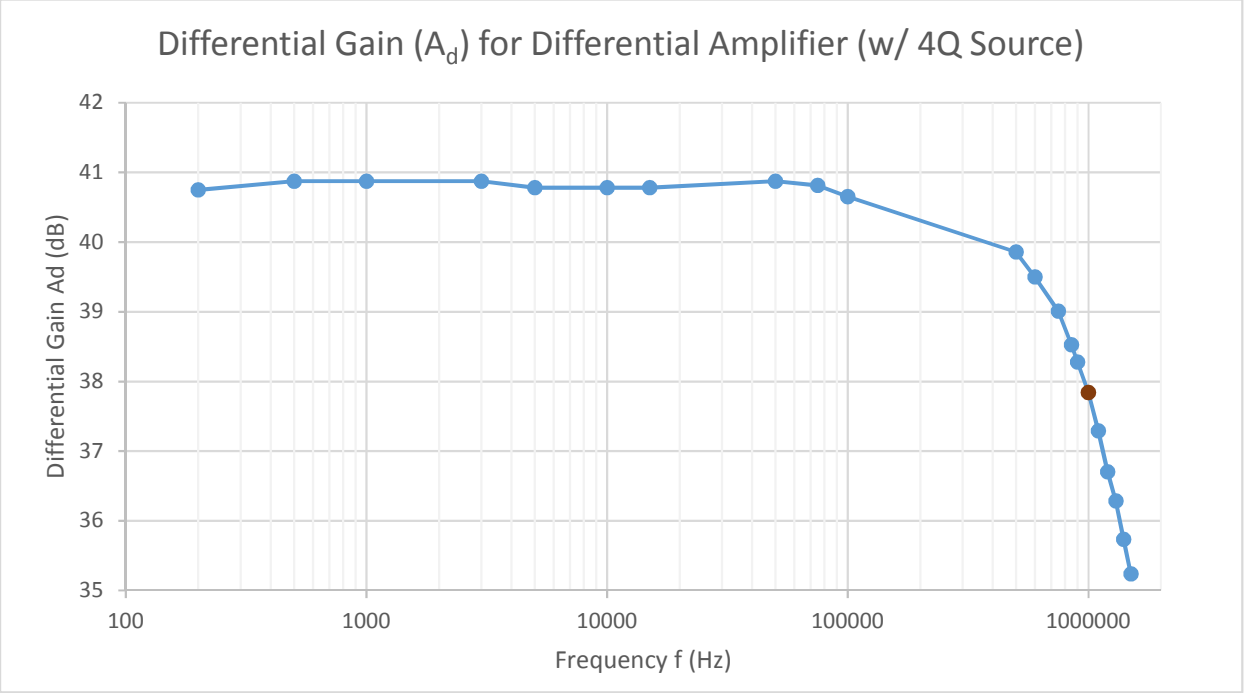
Graph 5: Load resistance response of 2Q current source is shown below. Note that the current varies considerably the load is varied.



Graph 6: Load resistance response of 4Q current source is shown below. Note that the current is virtually 14.3 mA in the range 200 to 900 ohms.



Graph 7: Resultant DM gain as a function of frequency (w/ 4Q amplifier configuration). The brown marker indicates the 3-dB drop-off point, located at 1.0 MHz.



Graph 8: Resultant CM gain as a function of frequency (w/ 4Q amplifier configuration). The brown markers indicate the 3-dB frequencies points; located at 0.85 MHz and 1.0 MHz.