Design of an 16-bit Signed Input Radix-4 Booth's Multiplier Using Carry Save Array Multiplier and Pipelining with D-Flip Flop

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I. Abstract

In this project, we implement an 16-bit Signed input, radix-4, Booth multiplier. Generally, for a multiplier the two important parameters are speed and its area. Radix-4 Booth multiplication needs to reduced number of partial products and Carry save array multiplier is used along with D flip flop for pipelined in order to speed up the process further and also reduces the area when compared to the conventional multipliers. The layouts of individual blocks such as the Inverter, Nand2, Nand3, Xor2, Aoi, Booth encoder, Booth selector, Full-Adder, Half-Adder, D flip flop as well as the final multiplier circuit are illustrated in this report. This work presents the complete architecture of the multiplier circuit and layout of all the individual block with extraction also discusses its performance in terms of post- parasitic delay, area and power consumption.

Keywords—Booth's algorithm, column addition, carry propagate adder

II. Introduction

In modern chip design, multipliers are crucial building blocks for various computing units. Optimizing their power consumption and speed is therefore paramount. The simplest type of multiplier is the array multiplier [1]. However, these are known for being power-hungry and slow, which is why D flip-flops are used to pipeline them and reduce the number of partial product arrays.

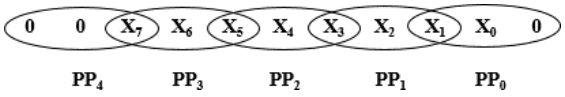

Fig. 1. Grouping of multiplier bits

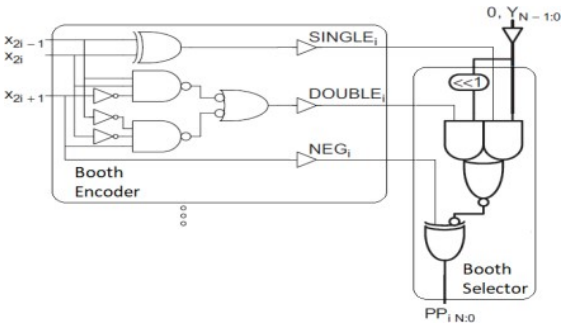

Fig. 2. Radix-4 Booth encoder and selector (Partial Product)

For signed number multiplication, particularly in two's complement notation, the Booth algorithm shines [4, 5]. Its strength lies in its speed, making it one of the fastest multiplication algorithms [6, 7]. Moreover, radix-n Booth multipliers further optimize by generating fewer partial products, leading to even faster computations.

In this work, radix-4 Booth's algorithm is used to generate the partial products, which are added using ripple carry adder array architecture. The rest of the project is organized as follows.Section II represent the introduction, section III presents the

architecture of the 16-bit signed input radix-4 Booth encoded Ripple Carry multiplier. The strategy of measuring the performance of the multiplier circuit is discussed in Section IV. section V presents the performance of the circuit in terms of static and dynamic power consumption, area, delay and maximum possible frequency. section VI Finally concludes this work.

Constant	Value
L_{MIN}	45nm
$Wmin_{PMOS}$	390 nm
$Wmin_{NMOS}$	260 nm
VDD_{NOM}	1.0V

III. ARCHITECTURE

In the radix-4 Booth encoded multiplier design,Fig. 1(a) shows the grouping of the 8-bit multiplier X and Fig. 1(b) presents the logic diagram of the Booth encoder and selector. An signed radix-4 Booth encoded multiplier requires eight partial products.

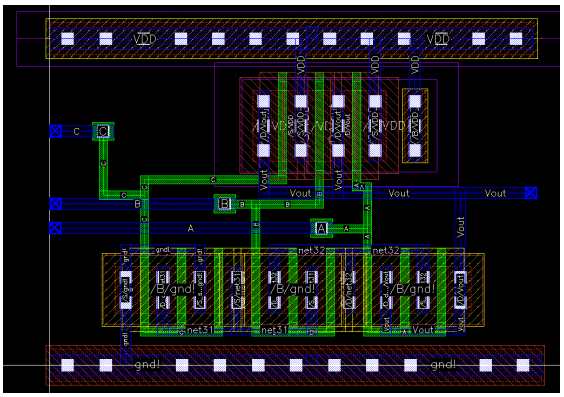

Fig. 3. Nand3 Layout

IV. TESTING:STRATEGY,CORNER

To determine the performance parameters of the multiplier circuit, input shaping and use of load and load-on-load devices should be done as shown . For a specific PVT corner, the maximum propagation delay can be obtained if the MSB of output changes with the change of the LSB of multiplier. An example of such input pattern is Y=11111111 and

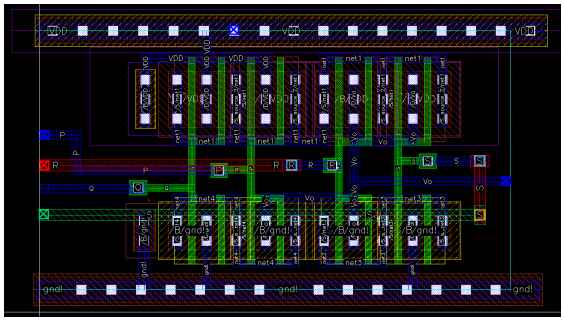

Fig. 4. AOI Layout

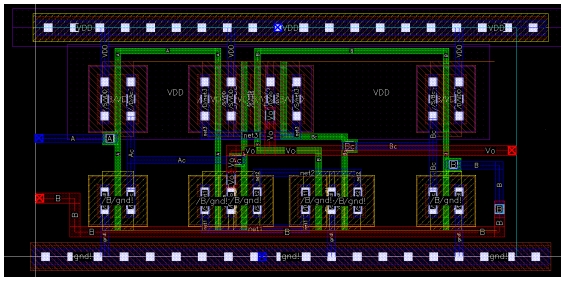

Fig. 5. Xor2 Layout

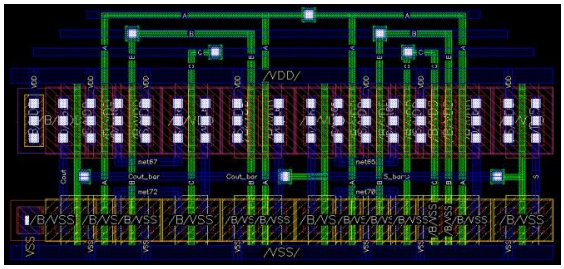

Fig. 6. Extracted Layout Full Adder

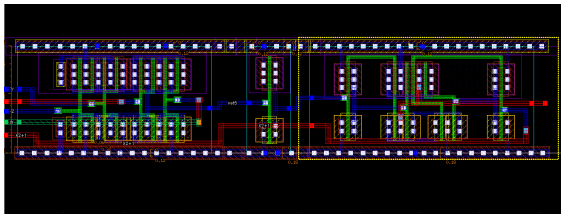

Fig. 7. Booth Selector Layout

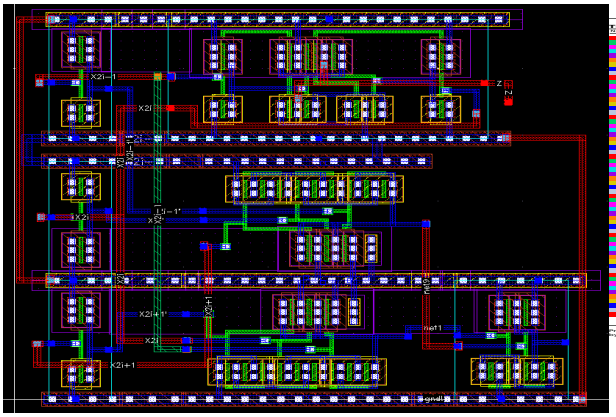

Fig. 8. Booth Encoder Layout

Block	Area (u)	Corner	Delay (ps)
Booth encoder	9.7	TT, 27°C	77
		SS, 125°C	132
		FF, -40°C	58.5
Booth selector	5.994	TT, 27°C	118
		SS, 125°C	178.5
		FF, -40°C	65.4
Full-adder	8.232	TT, 27°C	125
		SS, 125°C	234
		FF, -40°C	69
Half-adder	5.953	TT, 27°C	79
		SS, 125°C	88
		FF, -40°C	47
Multiplier	1370.7	TT, 27°C	1251
		SS, 125°C	2046
		FF, -40°C	831

X=1000000b, where 'b' switches between 0 and 1. Worst case delay is obtained in SS corner at 125°C and best case delay is obtained in FF corner at -40°C.

V. Power Calculation

A. Power

While a preliminary analysis using Vdd x Iavg suggests the 16x16 multiplier consumes 486 microWatts, this number is incomplete without accounting for the crucial impact of final-stage routing. To obtain a definitive power estimate, we must finalize the routing and conduct a thorough evaluation.

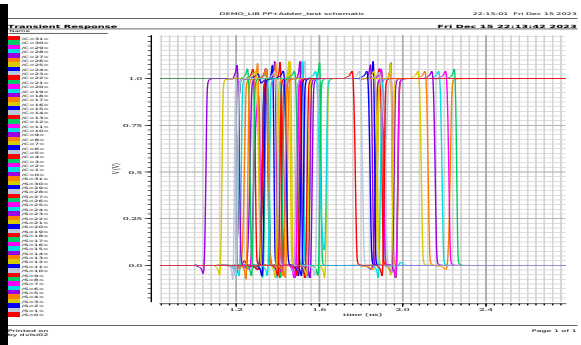

Fig. 9. Delay of Stage 1

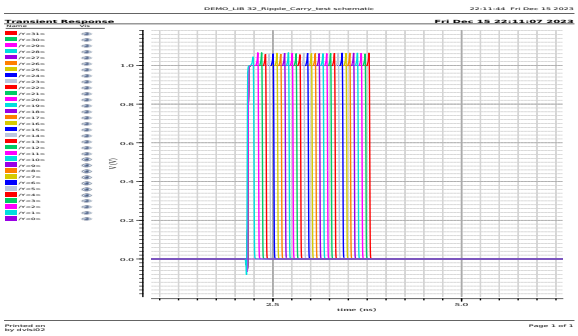

Fig. 10. Delay of Stage 2

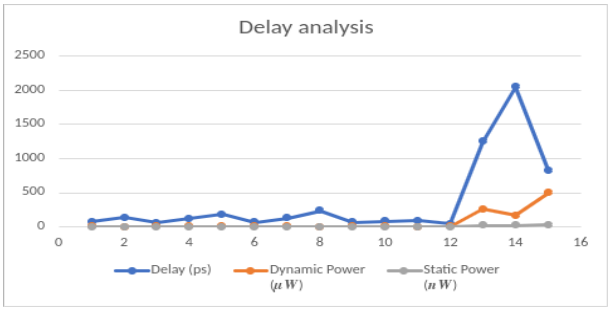

Fig. 11. Total Delay analysis on corner

B. Area

1.Multipath Pin Utilization: Traditional single-pin connections were replaced with strategically

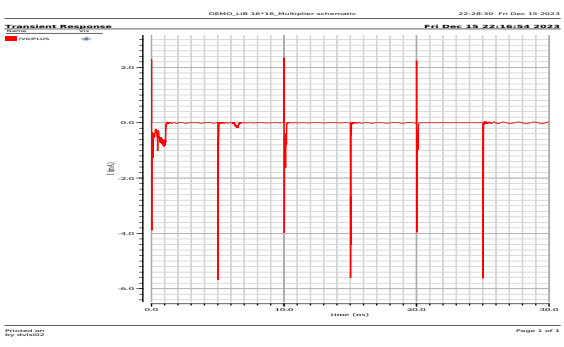

Fig. 12. Extracted (con-fig. file test bench Current supply from voltage source

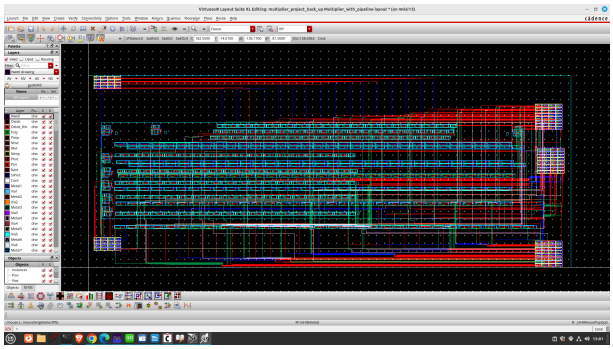

Fig. 13. Complete Layout with auto routing

distributed multipath pins, increasing routing resources and reducing congestion.

2. Flipping Standard Cells for Shared Power Rails: Standard cell placement was optimized by flipping cells to align VDD and ground rails with neighboring cells, enabling shared power rails and reducing area.

3. Multi-Metal Routing with Controlled Wire Crossing: Signal routing was optimized by utilizing up to metal 4 layers, providing additional routing channels and allowing for efficient path planning with controlled wire crossings.

C. Frequency analysis

Delay of stage 1 (including Partial product generator and Carry save array) is about 1.59 n seconds. Delay of stage 2 (including ripple carry adder) isabout 1.69 n seconds. So Tclock should be greater than maximum of (Delay of stage 1, Delay of stage2). Hence maximum frequency comes outto be 368.827 MHz.

VI. SUMMARY AND CONCLUSION

In this report, an 8-bit unsigned input multiplier is designed using radix-4 Booth's algorithm and Wallace tree architecture. The circuit can correctly compute the product of two numbers ranging from 0×0 and 255×255. This work also measures the area, delay and power of the circuit in the typical, worst and best PVT corners.

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