VLSI Questions

Lecture-1

1. What is Moore's Law? Why and how was it modified in 1975?
2. What is the impact of Moore's law on the development of VLSI?
3. Explain the brief history of IC industry.
4. Explain the different steps in VLSI realization process.
5. What are the problems of VLSI design on today?

Lecture-2

6. How do you define LSI and VLSI?
7. What is yield? How cost is related to yield in chip designing?
8. What are the design issues?
9. What do you mean by design synthesis?
10. What is verification? What is testing?
11. Explain VLSI design Cycle.
12. Explain the different steps in Physical Design.

Lecture-3

13. What is semiconductor?
14. Explain the Energy Band theory of crystal.
15. In the light of energy band theory, explain semiconductor, metal, insulator.
16. Why Si, Ge are semiconductors?
17. What are holes? Explain how holes can be carrier of electricity.
18. What is doping in semiconductor? What are its effects?
19. Explain donor and acceptor impurity in semiconductors?
20. What is semiconductor diode? What is depletion region? Explain the operation of semiconductor diode with both forward and reverse biased.
21. Explain Bipolar junction transistor. Explain its three modes of operation. How does it act as an amplifier? How does it act as a switch?
22. Compare the operations of semiconductor diode and transistor.

Lecture-4

23. What are the problems of bipolar junction transistor? Compare bipolar junction transistor versus junction field effect transistor.
24. Classify Field effect transistors.
25. Sketch the basic structure of an n-channel field effect transistor.
26. Explain the characteristics of JFET. How does it behave for small VDS and large VDS? How and when it turns from ohomic region to saturation region?

27. Define pinch-off voltage. Sketch the depletion region before and after pinch-off.
28. Explain JFET as amplifier and switch.
29. Explain MOSFET. What are the advantages of MOSFET over JFET?
30. Explain MOSFET with both enhancement and depletion mode.
31. Compare the transfer characteristics in JFET, depletion type MOSFET, enhancement type MOSFET.
32. Explain how the different operating points of JFET, depletion type MOSFET, enhancement type MOSFET change the uses of them.

Lecture-5

33. Explain the functioning of nMOS inverter considering the load as a) resistor b) enhancement type transistor c) depletion type transistor.
34. What is the problem of the nMOS inverter with pull up as an enhancement type? How is it improved with depletion type pull up?
35. Why is transistor being used in place of the resistor in designing a NOT gate?
36. What are the drawbacks of MOSFETs?
37. What are the advantages of CMOS over MOSFET? What are the disadvantages of CMOS design?
38. How does CMOS work as an inverter?
39. How do you compare FET, enhancement type NMOS, depletion type NMOS with respect to operating point?
40. Explain the output and transfer characteristics enhancement type NMOS, depletion type NMOS, enhancement type PMOS and depletion type PMOS?
41. How is CMOS working as a switch?
42. Compare the speed-power performance of different technologies in semiconductor design.

Lecture-6

43. What are pass transistors? What are their uses?
44. In the inverter circuit, what is meant by Zpu and Zpd. What is the significance of finding the ration Z_{pu}/Z_{pd}.
45. Prove that the ratio of impedances of the pull-up to pull-down transistors of a nMOS inverter is 4 : 1.
46. What will be the value of Z_{pu}/Z_{pd} of a MOS inverter having the following parameters? V_{th} = Threshold voltage of MOS transistor = $0.34V_{DD}$, where V_{DD} is the inverter's supply voltage and V_{inv} = Logic threshold voltage of the inverter = $0.525\ V_{DD}$.
47. An n MOS inverter is driven by another nMOS inverter having pull-up to pull-down ratio of 4.50:1, through 3 pass transistors each having threshold voltage of 0.265 VDD. Find the desired ratio of the pull-up to pull-down impedance of the driven inverter.
48. Deduce the pull-up to pull-down impedance ratio of an nMOS inverter being driven by another nMOS inverter through four pass transistors.

49. An nMOS inverter is driven by another nMOS inverter having pull-up to pull-down ratio of 4·75 : 1, through three pass transistors each having threshold voltage of 0·275 VDD . Find the desired ratio of the pullup to pull-down impedance of the driven inverter.
50. For a CMOS inverter, explain the transfer characteristics and the variation of current with respect to input voltage V_{in}.
51. Deduce the pull-up to pull-down impedance ratio of an ideal CMOS inverter with respect to the variation in $\frac{L}{W}n$ / $\frac{L}{W}p$.

Lecture-7

52. On what parameters, the threshold voltage of a MOS transistor dependent? Evaluate these parameters.
53. What are the main forms of MOSFET capacitances?
54. Derive the different capacitances of MOSFET.
55. Explain the existence of different resistances in MOSFET fabrication.
56. Derive transconductance of MOSFET and bipolar transistor. Compare the current and transconductance in CMOS and Bipolar Technology.
57. Compare CMOS versus bipolar technology.
58. Explain the structure of BiCMOS. What is its advantage?
59. What is the latchup problem in CMOS? Explain the variation of latchup current with respect to voltage.
60. What are the remedies for latchup. How can it be avoided in BiCMOS?
61. Explain the BiCMOS inverter circuit.

Lecture-8

62. Implement the Boolean function f = ab + ad + cd with the help of nMOS.
63. Implement the Boolean function f = ab + ad + ad with the help of pMOS.
64. Implement the Boolean function f = ab + ad + cd with the help of
a)CMOS NAND b)CMOS NOR.
65. What is single complex cell design in CMOS? What are its advantages and disadvantages of it?
66. Implement the Boolean function f= ab+ ad +cd using single complex cell designs in four different ways (consider that for any input, its complement is also available).
67. Implement the Boolean function $\bar{f}$= ad+ $\bar{b}$d +c$\bar{d}$ using single complex cell designs in four different ways (consider that for any input, its complement is also available).
68. Implement the Boolean function $\bar{f}$= ad+ $\bar{b}$d +c$\bar{d}$ using NMOS.
69. Implement the Boolean function $\bar{f}$= ad+ $\bar{b}$d +c$\bar{d}$ using PMOS
70. Implement the Boolean function
(i) f = (w+$\bar{x}$ +$\bar{z}$) ($\overline{w}$+y+x) [using n MOS transistors]
(ii) g = $\overline{A}C\overline{D}$ + A$\overline{B}$C [using CMOS transistors]

71. Implement the Boolean function
(i) f = W $\overline{X}$Z + $\overline{W}$ $\overline{Y}$ [using n MOS transistors]

(ii) g = (A + $\overline{B}$ + D) ($\overline{A}$ + BD) [using CMOS transistors]

Lecture-9

72. What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation?
73. Draw the layout of NAND and NOR using CMOS designs.
74. How to reach mask diagram from stick diagram.
75. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
    i)f = A$\overline{B}$ + $\overline{A}\overline{C}$ [using nMOS transistors]
    ii)g = (w +x + z). ($\overline{w}$ + xz) [using CMOS transistors]
76. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
    (i) f = W $\overline{X}$Z + $\overline{WY}$ [using n MOS transistors]
    (ii) g = (A + $\overline{B}$ + D) ($\overline{A}$ + BD) [using CMOS transistors]
77. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
    (i) f = A$\overline{B}$ + $\overline{A}$C +$\overline{C}$D [using nMOS transistors]
    (ii) g = (w + $\overline{x}$) ($\overline{y}$ + z) [using CMOS transistors]
78. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
    (i) f = (w+$\overline{x}$ +$\overline{z}$) ($\overline{w}$+y+x) [using nMOS transistors]
    (ii) g = $\overline{A}$C$\overline{D}$ + A$\overline{B}$C [using CMOS transistors]
79. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
    (i) f = A$\overline{B}$C + $\overline{A}$B$\overline{C}$ [using nMOS transistors]
    (ii) g = ($\overline{w}$+x+z) (w+$\overline{x}$+$\overline{z}$) [using CMOS transistors]
80. Draw the stick diagram of a shift register cell using a transmission gate followed by a CMOS inverter.
81. Convert the stick diagram obtained in previous question to symbolic form and show an example of optimization in it.

Lecture-10

82. Compare Silicon versus Germanium in the use of chip designing.
83. How the silicon wafer is prepared from sand? Explain the steps.
84. What is photoresist? Explain its uses in fabrication process.
85. Define lithography.
86. Explain the basic processing steps in fabrication.
87. Describe etching process.
88. What is the role of silicon dioxide in fabrication?
89. Explain the different steps in nMOS fabrication.
90. What is polysilicon? What is its use in fabrication process?

91. Explain the chemical vapour deposition technique.
92. Explain the different fabrication steps in CMOS.
93. Compare the p-well and n-well process in CMOS fabrication.

Lecture-11

94. Discuss the problems of manufacturing in sizing of the different elements in fabrication.
95. What is design rule? What is the advantage of generalized design rule?
96. What do you mean by λ–based IC design rules?
97. What are the rules of design rules.
98. Explain nMOS design rules.
99. Explain CMOS design rules.
100. Explain the design rules for different contact cuts.
101. Explain the design rules for via and cut.

Lecture-12

102. What is partitioning? Why do we need it?
103. What are the different levels of partitioning?
104. Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight $\frac{1}{2}$, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.
105. In refer to Question 3, prove that optimal balanced partitioning of G cannot be done if each edge of H interconnects at most four vertices (i.e., give a counter example).
106. Explain Kernighan-Lin algorithm for partitioning a graph. Find its time complexity.
107. Consider a path graph v_1, v_2,....., v_n. That is, v_1 is connected to v_{i+1}, for $1 \leq i \leq n-1$. Apply the Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all odd values of a be in one set , and v_b, for all even values of b, be in the other set.
108. Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all internal vertices, be in one set and v_b, for all leaves, be in the other set.
109. Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of V_1= {1,2,3,.....,n}, and V_2={n+1,n+2,n+3,.....,2n}.
110. What are the drawbacks of Kernighan-Lin algorithm?

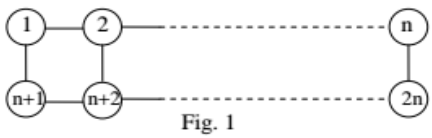

Fig. 1

111. The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning.

	a	b	c	d
a	0	1	2	3
b	1	0	1	4
c	2	1	0	3
d	3	4	3	0

Fig.2

Lecture-13

112. What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?
113. What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?
114. Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.
115. Apply Fiduccia-Mattheyses Algorithm for the problem in question 7.
116. Apply Fiduccia-Mattheyses Algorithm for the problem in question 8.
117. Apply Fiduccia-Mattheyses Algorithm for the problem in question 10.
118. "There is a trade off associated for partitioning with replication." Is it true or false? Justify.
119. Discuss how Partitioning is affecting overall delay.
120. What do you understand by performance driven partitioning?
121. Discuss the approach of clustering in case of partitioning.

Lecture-14

122. Define Floorplanning.Define sliceable and non-sliceable floorplan with examples. What are the advantages of sliceable floorplan?
123. State with an example how a sliceable floorplan can be represented by a binary tree.
124. When an adjacency graph cannot admit a rectangular dual?
125. Obtain the hierarchical floorplan tree for the floorplan given in Fig.5.
126. Illustrate the steps of rectangular dualization on an inherently non-sliceable graph of n vertices.
127. Obtain a rectangular dual of the following adjacency graph.

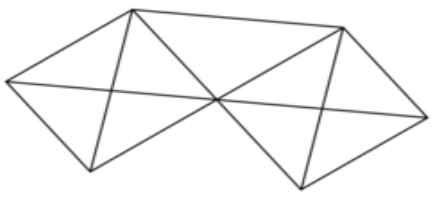

Fig. 3

128. Obtain the rectangular dual of the following adjacency graph below of Fig. 4.
129. Are the Floorplans obtained in 17 and 18 sliceable?

130. Prove that there is a one-to-one correspondence between a sliceable floorplan and a normalized Polish expression.
131. Give the adjacency graph for the following floorplan of Fig.5.

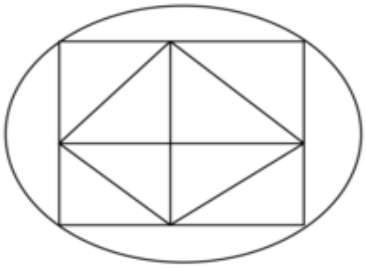

Fig. 4

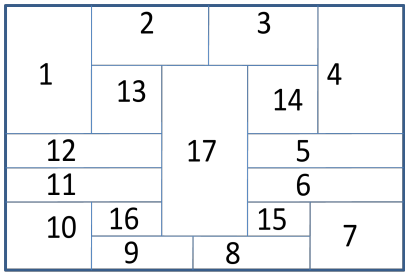

Fig.5

132. Explain Bottom-up and Top-down approach in Floorplan.
133. What is extended dual.
134. Prove that if a rectangular dual graph does not contain any PTG, it can always have a corresponding sliceable floorplan.
135. Show with the example that the number of possible sliceable floorplan increases exponentially with the number of modules.
136. What are the different types of internal nodes for a hierarchical floorplan.
137. Explain Hierarchical floorplan with some Greedy procedure for a sliceable floorplan.
138. State the steps in the Hierarchical floorplan with Bottom up Greedy procedure for the following adjacency graph, where edges have some weights.
139. Explain how the procedure in question 36 may lead to wastage of space. What is the solution for it?
140. How do you estimate the cost of floorplan.
141. Consider the following adjacency graph where the edge weights are providing the distance between two vertices. Estimate the routing cost in different sliceable florplans for it.

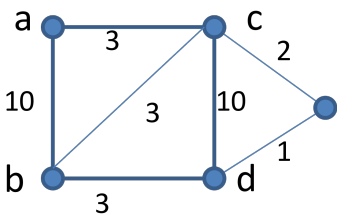

Fig.6

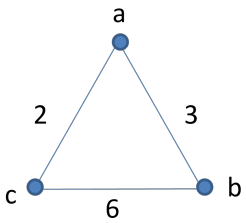

Fig.7

Lecture-15

142. What is simulated annealing? How simulated annealing approach can be applied in Floorplan.
143. State the three different operations in simulated annealing approach in Floorplanning. How they will be applied in a given floorplan.
144. Given a Polish expression corresponding to a given slicing floorplan. Show that the expression 12+3+4+.....+n+ can be reached, and vice versa, using three operations in simulated

annealing approach of floorplan. (+ and * represent horizontal and vertical bisection respectively.)

145. State Floorplan sizing problem.
146. Considering hierarchical nature of floorplan, discuss how to deal with the sizing problem.
147. In a hierarchical florrplan sizing problem, there are given two subfloorplans corresponding to two subtrees of a node v, one with t and other with s nonredundant implementations, prove that v has at most s+t-1 nonredundant realizations.
148. Given a fllorplan with fixed cell environment, what are the significance of horizontal dependency graph and vertical dependency graph.
149. Draw the horizontal and vertical dependency graph of the floorplan given in Fig. 5.
150. Considering no restriction on the organization of the modules, formulate the floorplan sizing problem as an Integer Linear Programming (ILP).
151. What are the advantages of integer linear programming technique in case in floorplanning.

Lecture 16

152. State the consequences of placement in VLSI Design.
153. State the importance of Placement problem.
154. Give a brief discussion on the objective functions and routing estimation in placement.
155. Formulate the placement problem.
156. Discuss the cost components in Placement.
157. State the various approaches for placement problem- Top-down, iterative, constructive?
158. Explain the Force directed Placement algorithm.
159. Compare the constructive and iterative algorithm in Placement problem.
160. State two different approaches in Force directed algorithm.
161. What are pros and cons of Force directed algorithm?

Lecture 17

162. Explain congestion problem in time of placement.
163. State partitioning approach in placement with goal and objectives.
164. Explain the different procedures for Breuer's Algorithm.
165. What are pros and cons of Breuer's algorithm?
166. Explain simulated annealing algorithm in case of placement problem.
167. What are the pros and cons of simulated annealing technique in placement.
168. Explain the quadratic placement approach.
169. What is analytical placement? What is the advantage of doing this type of placement?
170. State the pros and cons of quadratic placement approach.
171. State the clustering approach in case of placement.

Lecture-18

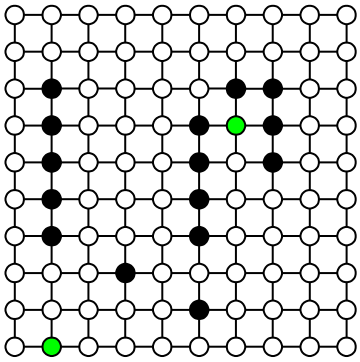

Fig. 8

172. Define Routing problem.
173. What are different routing regions?
174. Define Channel, terminal, switchbox with respect to routing.
175. Define channel capapcity.
176. What are the objectives of Routing?
177. What are constraints of routing?
178. Explain Global Routing and Detailed Routing.
179. Explain the different graph models used in Global Routing.
180. Fig. 8 shows a grid graph with several blocked vertices. It also shows terminals (marked by green) of a two-terminal net. Use Lee's algorithm to find the path for this net the number of nodes explored in (a).
181. Use Soukup's algorithm in the case of the example of question 110.
182. What is the running time of Lee's maze router when there is only one two-terminal net in an n $\times$ n grid and the rectilinear distance between the two terminals is d? For what configuration of obstacles is the running time independent of n and depends only on d?
183. Give an example or counter example as the case may be for the following statement: Soukup's maze router always produces the shortest path.

Lecture-19

184. Explain Detailed routing.
185. What is via?
186. Explain grid-based and gridless model in case of detailed routing.
187. What are reserved and unreserved layers in case of detailed routing?
188. What is dogleg?
189. Explain Horizontal and Vertical Constraint Graphs.
190. Give an instance of channel routing problem in which there are cyclic constraints.
191. Draw the constraint graphs and compute the lower bound on number of tracks for the following channel

TOP = {7 2 7 0 0 1 4 6 0 7 4 0}
BOT = {2 5 6 5 6 2 1 0 3 0 3 4}

192. Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 4 5

193. What are the drawbacks of Left edge algorithms?

194. Route the following channel

TOP = {7 2 7 0 0 1 4 6 0 7 4 0}

BOT = {2 5 6 5 6 2 1 0 3 0 3 4}

Lecture 20

195. Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 4 5

196. Use Dogleg router to route the Channel discussed in question 91.

197. What is the advantage of YK router. Show with an example. Use YK algorithm to route the Channel discussed in question 91.

198. What are the drawbacks of Left Edge Algorithm? How are they tackled in dogleg router.

199. What are the different routing sequences in case of dogleg router? Define range. How the routing is dependent on the sequence and range in dogleg router.

200. How the zones are defined in YK router? Show with an example.

201. Explain Greedy Channel Router.

202. Compare the different detailed routing methods- LEA, Dogleg, YK, Greedy with their merits and demerits.

203. Route the following channel

TOP = {7 2 7 0 0 1 4 6 0 7 4 0}

BOT = {2 5 6 5 6 2 1 0 3 0 3 4}

204. Using any suitable algorithm. Mention its name and salient features.

205. How can you do the Switchbox Routing?