FIRST CLASS TEST-VLSI DESIGN-BCSE 4th YEAR-2018 FULL MARKS:30

1. What is Moore's Law? How is it modified in 1975?
2. What are the different steps in physical design.
3. What is semiconductor?
4. How do you compare FET, enhancement type NMOS, depletion type NMOS with respect to operating point?
5. Why is transistor being used in place of the resistor in designing a NOT gate?
6. What is the use of photoresist in fabrication.
7. What are NMOS design rules.
8. Implement the Boolean function $f = ab + cd + bd$ using single complex cell designs in four different ways (consider that for any input, its complement is also available).
9. Draw the coloured stick diagram for implementing the following Boolean functions :

   $f = A\ \bar{B}C + \bar{A}B\ \bar{C}$ [using n MOS transistors]
10. Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of $V_1 = \{1,2,3,\ldots\ldots,n\}$, and $V_2 = \{n+1,n+2,n+3,\ldots\ldots,2n\}$. See Fig.1.
11. What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?

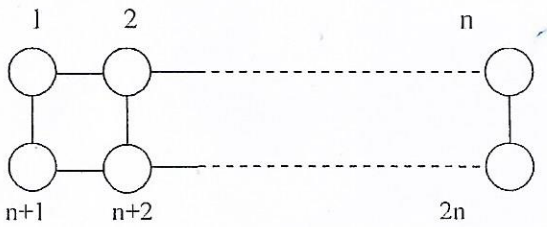

Fig.1

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2+2+2+3+2+2+2+5+2+6+2