BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2016

(3rd Year, 1st Semester)

VLSI DESIGN

Time : Three hours Full Marks : 100

Answer any ***five*** questions

1. a) How do you define LSI and VLSI? What is Moore's law?
   b) Explain VLSI design Cycle.
   c) Compare CMOS versus bipolar technology
   d) Deduce the pull-up to pull-down impedance ratio of an ideal CMOS inverter..

3+5+4+8

2. a) Explain the functioning of nMOS inverter considering the load as depletion type transistor.
   b) On what parameters, the threshold voltage of a MOS transistor dependent? Evaluate these parameters.
   c) What will be the value of Z_{pu}/Z_{pd} of a MOS inverter having the following parameters? V_{th} = Threshold voltage of MOS transistor = 0.34 V_{DD}, where VDD is the inverter's supply voltage and V_{inv} = Logic threshold voltage of the inverter = 0.525 V_{DD}.

4+10+6

3. a) Implement the following Boolean function with the help of (i) nMOS (ii) pMOS (iii) CMOS NAND gates (iv) CMOS single complex cell design.

   Y=ab+bd+cd

   b) Draw the coloured stick and mask diagrams for implementing the Boolean function mentioned in question 3 (a) using (i) NMOS (ii) CMOS.

10+10

4. a) What are the different levels of partitioning?
   b) Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of V_1= {1,2,3,……,n}, and V_2={n+1,n+2,n+3,…..,2n}.

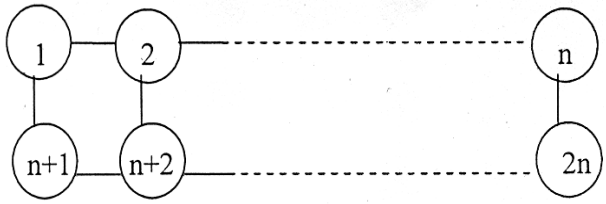

Fig. 1

   c) What are the drawbacks of Kernighan-Lin algorithm?
   d) State the similarities between Fiduccia-Mattheyses algorithm and K-L algorithm.

4+10+3+3

5. a) State with an example how a sliceable floorplan can be represented by a binary tree.
   b) Obtain a rectangular dual of the following adjacency graph (Fig.2).
   c)How do you estimate the cost of floorplan. Consider the adjacency graph of Fig.3 where the edge weights are providing the distance between two vertices. Estimate the routing cost in different sliceable florplans for it.
   d) State the advantages of integer linear programming technique in case in floorplanning.

3+7+7+3

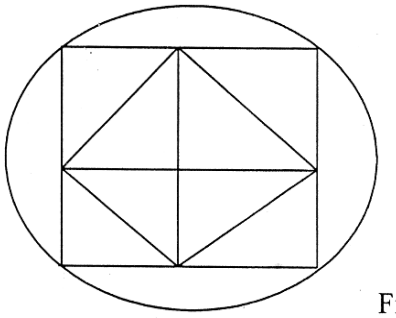

Fig.2

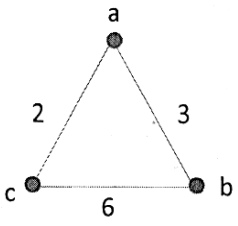

Fig. 3

6. a) State the consequences and importance of placement in VLSI Design
   b) Explain the Force directed Placement algorithm with its prospects and consequences.
   c) Explain the different procedures for Breuer's Algorithm.

4+8+8

7. a) Explain Global Routing and Detailed Routing.
   b) Fig. 4 shows a grid graph with several blocked vertices. It also shows terminals s and t as source and target of a two-terminal net. Use Lee's algorithm to find the path for this net.
   c) Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty position. TOP = 3 4 0 1 2 4 3 5 2 1 0
   BOT = 1 0 3 0 4 0 5 2 1 4 5

4+8+8

Fig. 4