Design Rules

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- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducable

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Design Rules - The Reality

- Manufacturing processes have inherent limitations in accuracy and repeatability
- Design rules specify geometry of masks that provide reasonable yield
- Design rules are determined by experience

Problems - Manufacturing

- Photoresist shrinking / tearing
- Variations in material deposition
- Variations in temperature
- Variations in oxide thickness
- Impurities
- Variations across the wafer

Problems - Manufacturing

- Variations in threshold voltage
  - oxide thickness
  - ion implantation
  - poly variations
- Diffusion - changes in doping (variation in R, C)
- Poly, metal variations in height and width -> variation in R, C
- Shorts and opens
- Via may not be cut all the way through
- Undersize via has too much resistance
- Oversize via may short

Meta Design Rules

- Basic reasons for design rules
- Rules that generate design rules
- Under worst case misalignment and maximum edge movement of any feature, no serious performance degradation should occur

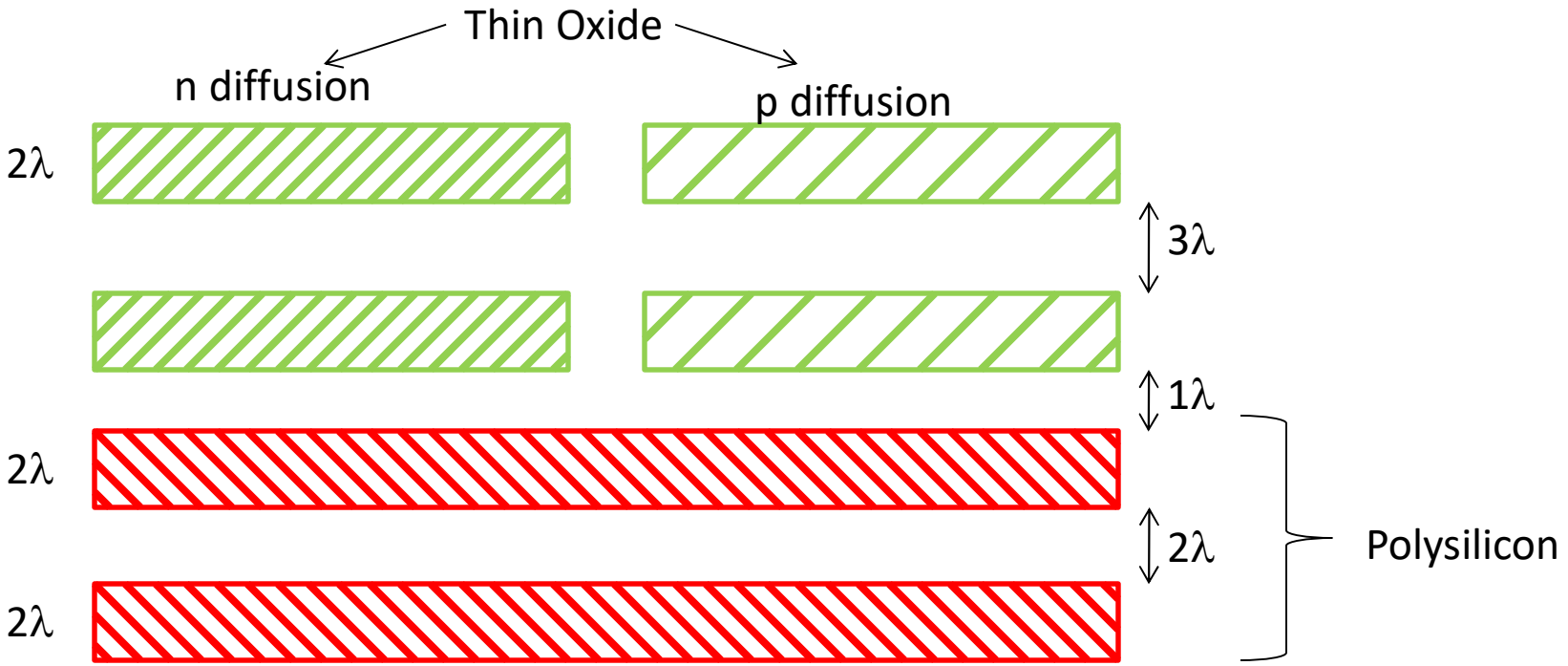
Advantages of Generalised Design Rules

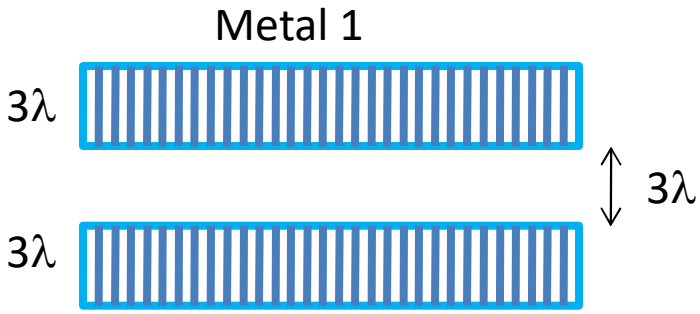
- Ease of learning because they are scalable, portable, durable
- Longevity of designs that are simple, abstract and minimal clutter
- Increase designer efficiency
- Automatic translation to final layout

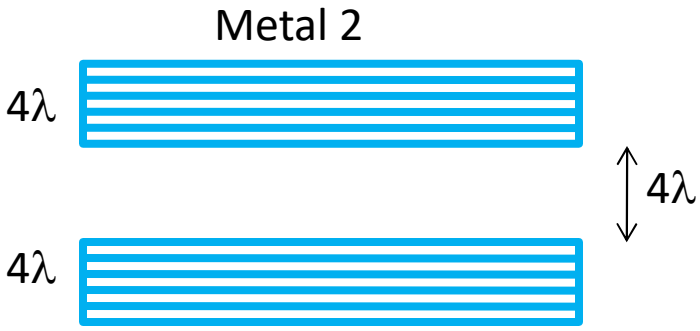
Lambda Based Design Rules

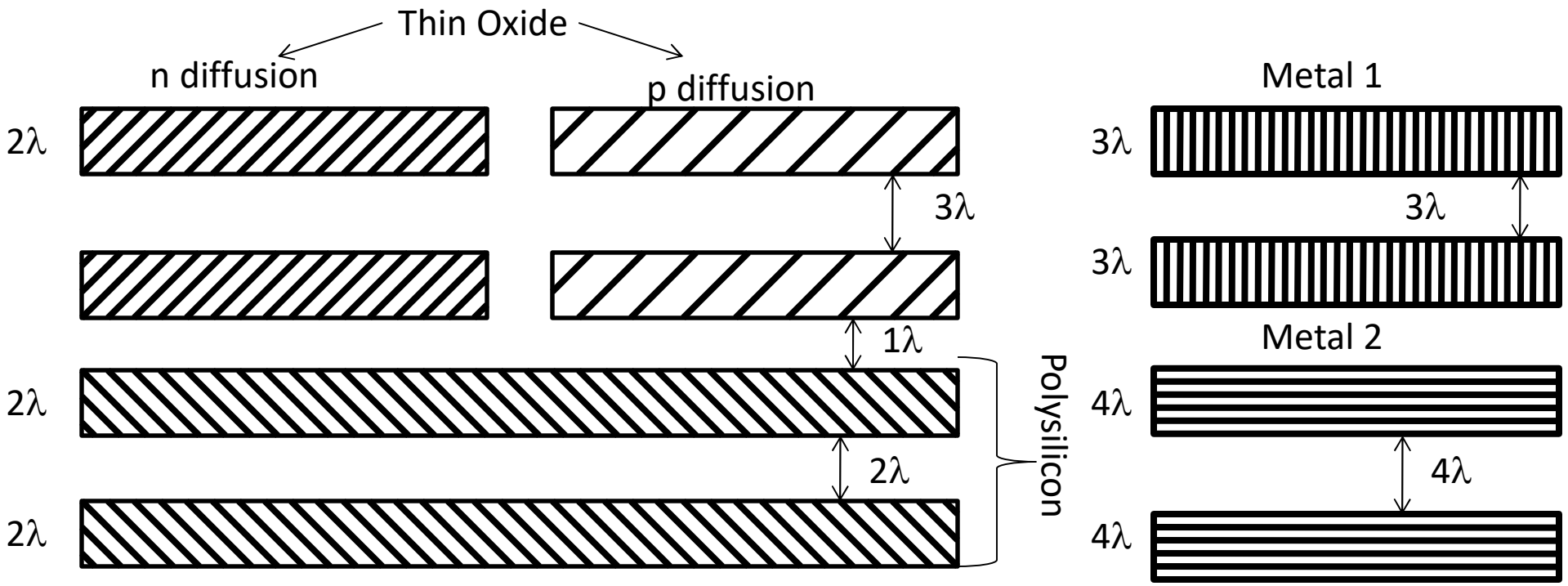
- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

DESIGN RULES





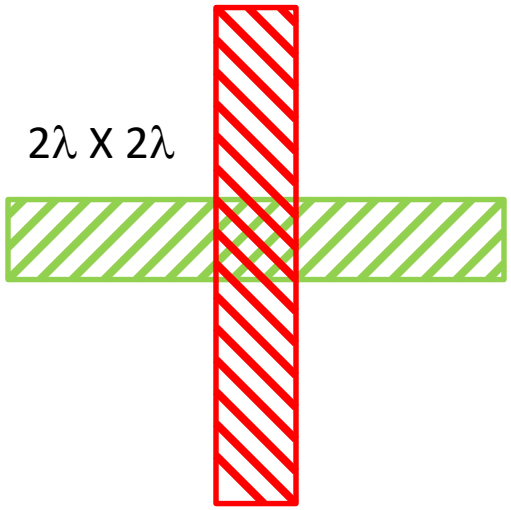




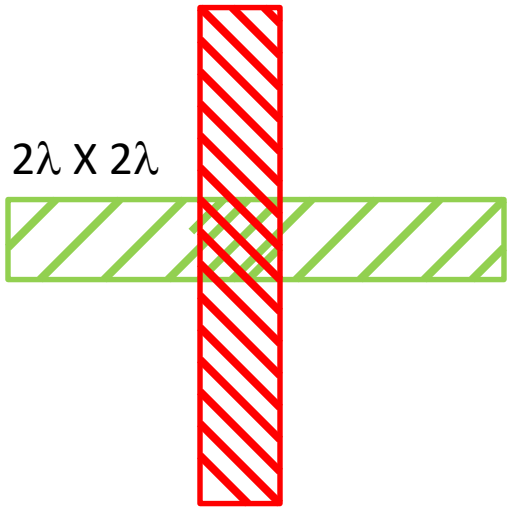
Basic nMOS design Rules

Different widths	Value
Diffusion Region width	2λ
Polysilicon region width	2λ
Diffusion-Diffusion spacing	3λ
Poly-Poly spacing	2λ
Polysilicon gate extension	2λ
Contact extension	λ
Metal width	3λ

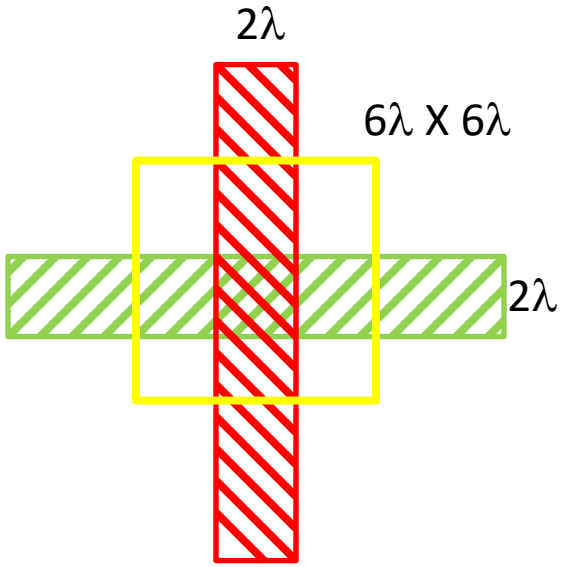
DESIGN RULES



nMOS enhancement

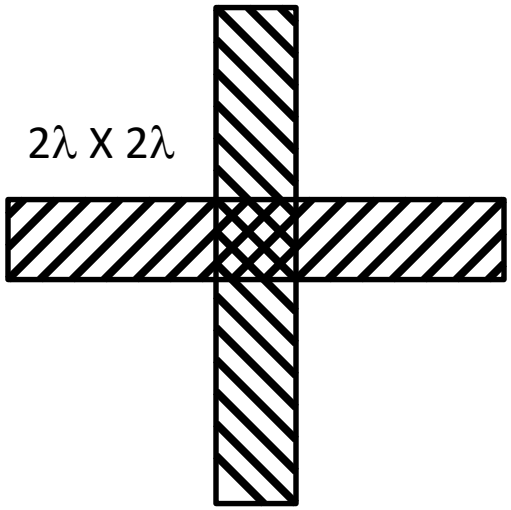


pMOS enhancement

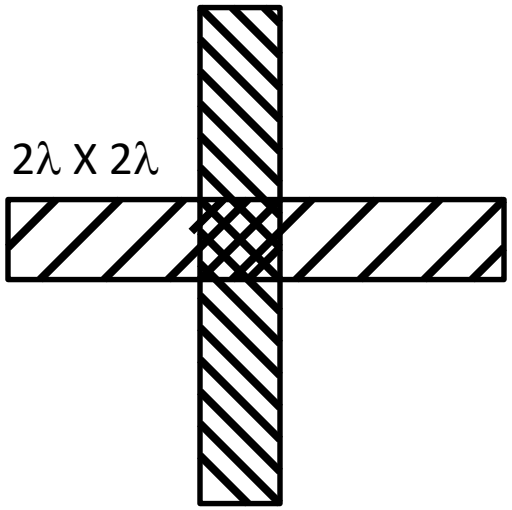


nMOS depletion

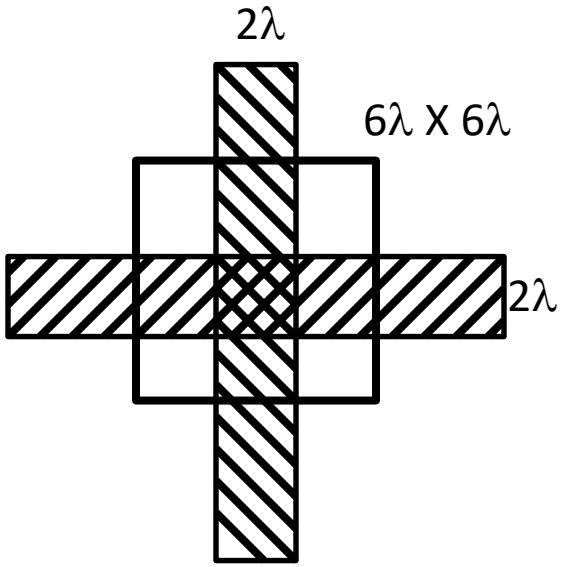
DESIGN RULES



nMOS enhancement



pMOS enhancement



nMOS depletion

DESIGN RULES

Size Rules

The minimum feature size of a device or interconnect is determined by the line patterning capability of lithographic equipment

Design rule must specify the minimum feature sizes on different layers to ensure a valid design of a circuit

Separation Rules

Different features on the same layer or in different layers must have some separations from each other

Most IC processes have a spacing rule for each layer and several rules for interlayer spacing

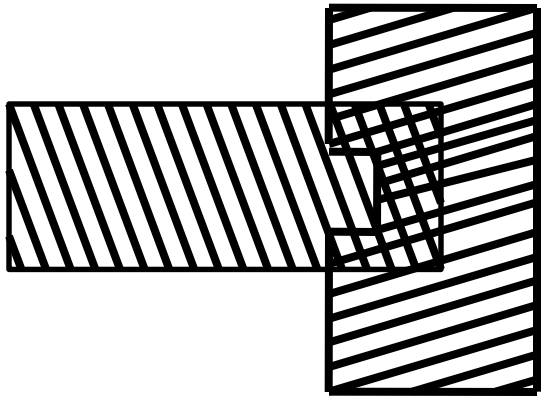
DESIGN RULES

Overlap rules

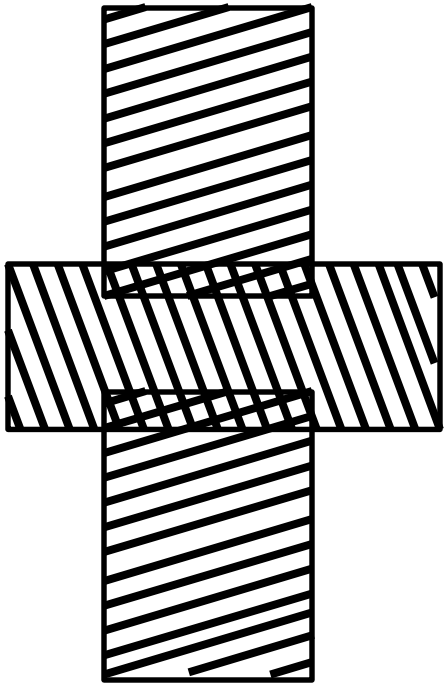
Design rules must protect against fatal errors

Example of Fatal errors

- A short circuited channel caused by mismigration of poly or diffusion
- The formation of an enhancement mode FET in parallel with depletion device
- Misregistration of ion-implant area and source/drain diffusion



Incorrectly formed

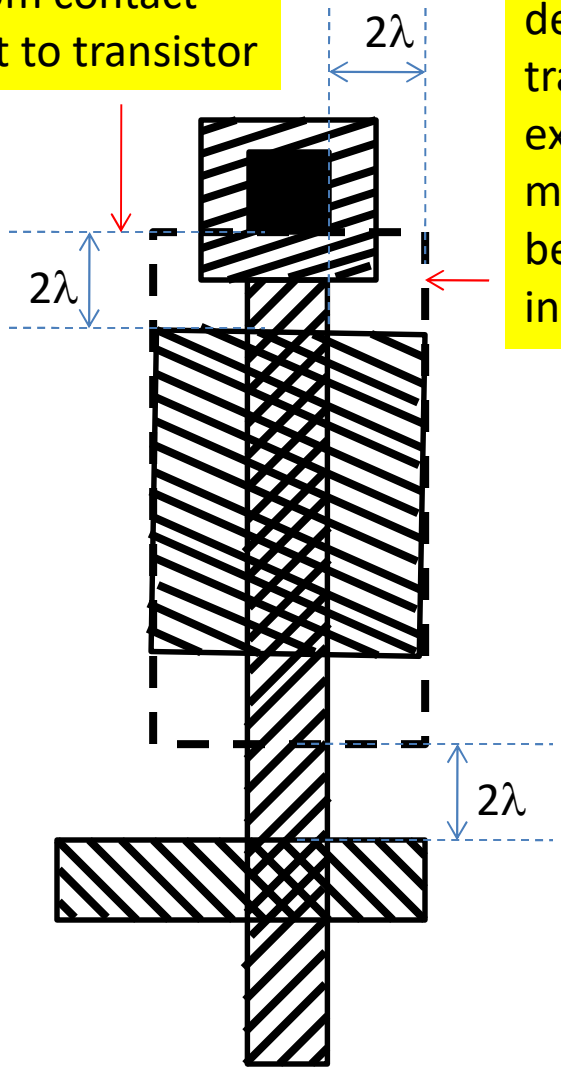


Correctly formed

DESIGN RULES

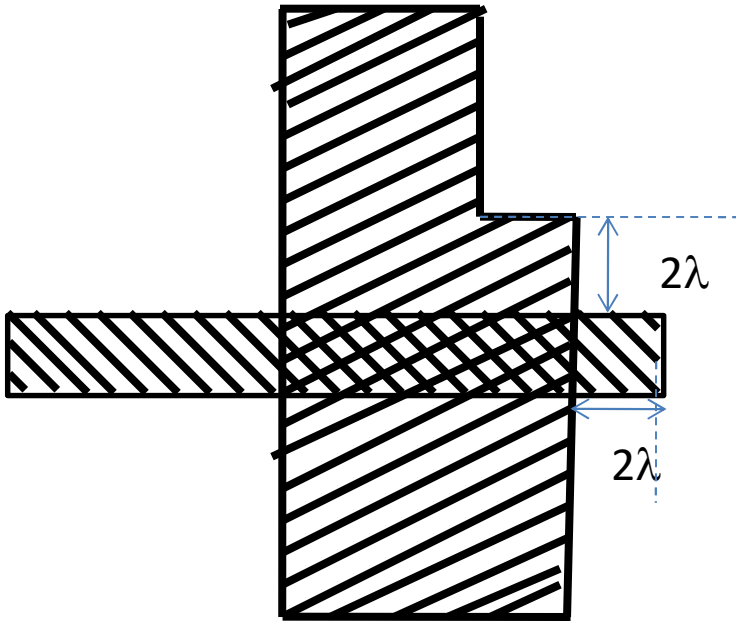
Separation from contact cut to transistor

Implant for an nMOS depletion mode transistor to extend 2λ minimum beyond channel in all directions



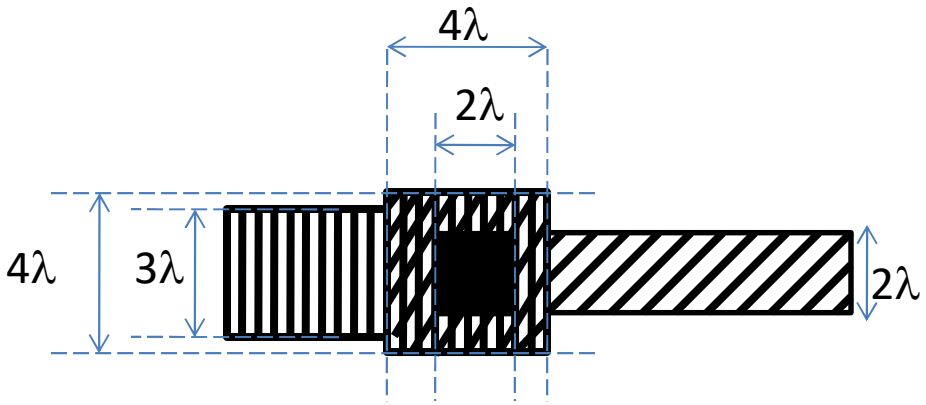
Separation from implant to another transistor

Diffusion is not to decrease in width < 2λ from polysilicon

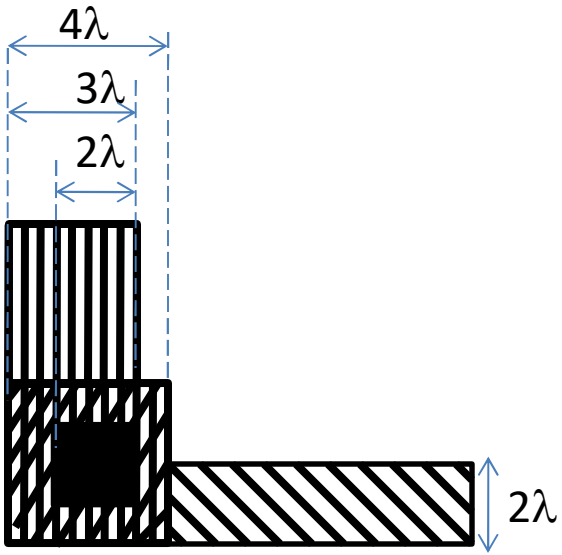


Polysilicon to extend minimum 2λ beyond diffusion biundaries

Overlap rules for contact cuts: nMOS and CMOS

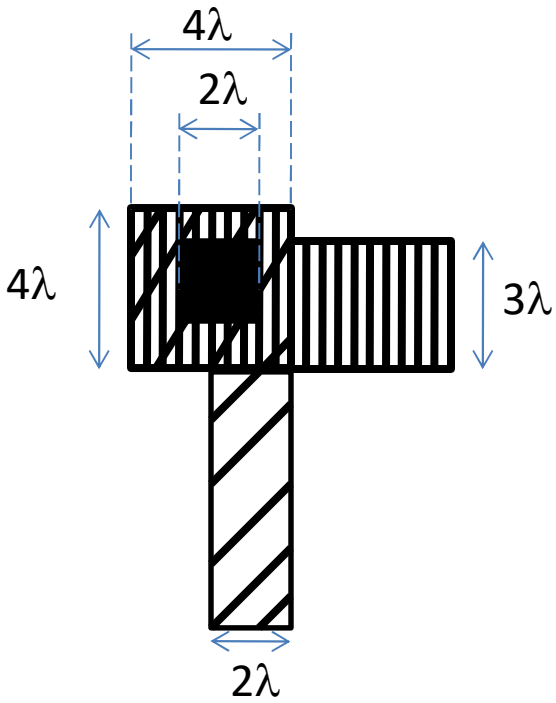


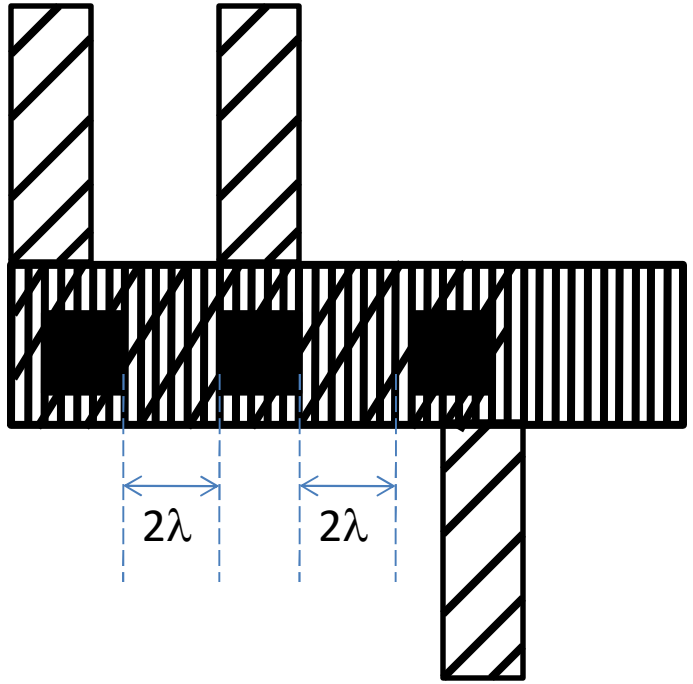
Metal to Polysilicon



Metal to Diffusion

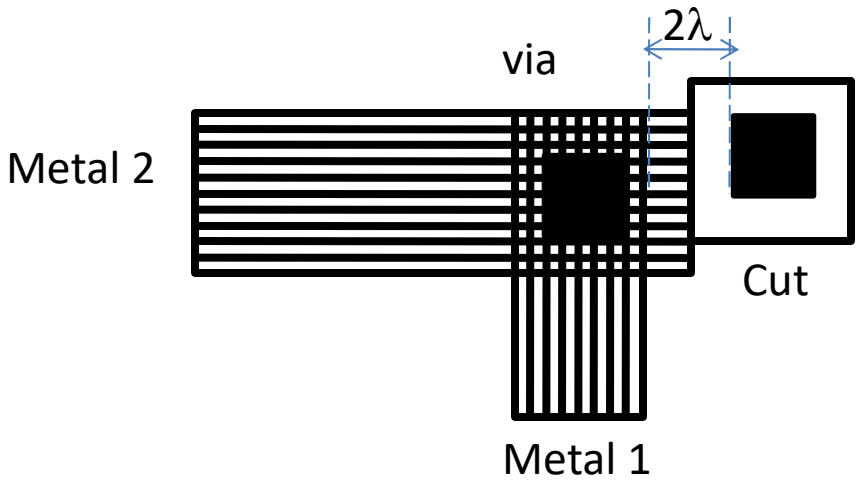
Overlap rules for contact cuts : nMOS and CMOS





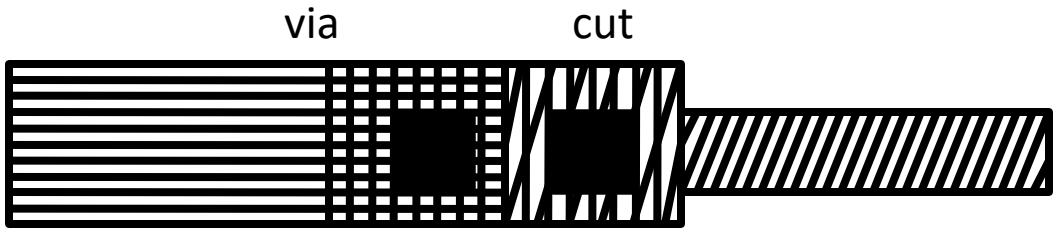
Multiple Contact cuts

Overlap rules for contact cuts and via : nMOS and CMOS



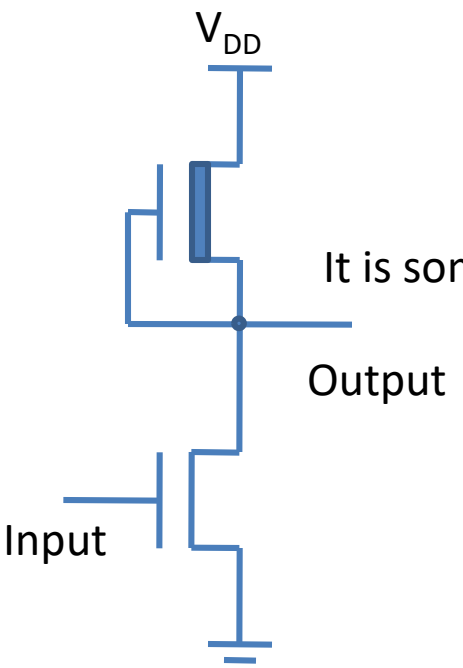
Via:

- Contact from metal2 to metal 1
- Contact through other layer



Metal 2 to diffusion

Design rules: NMOS



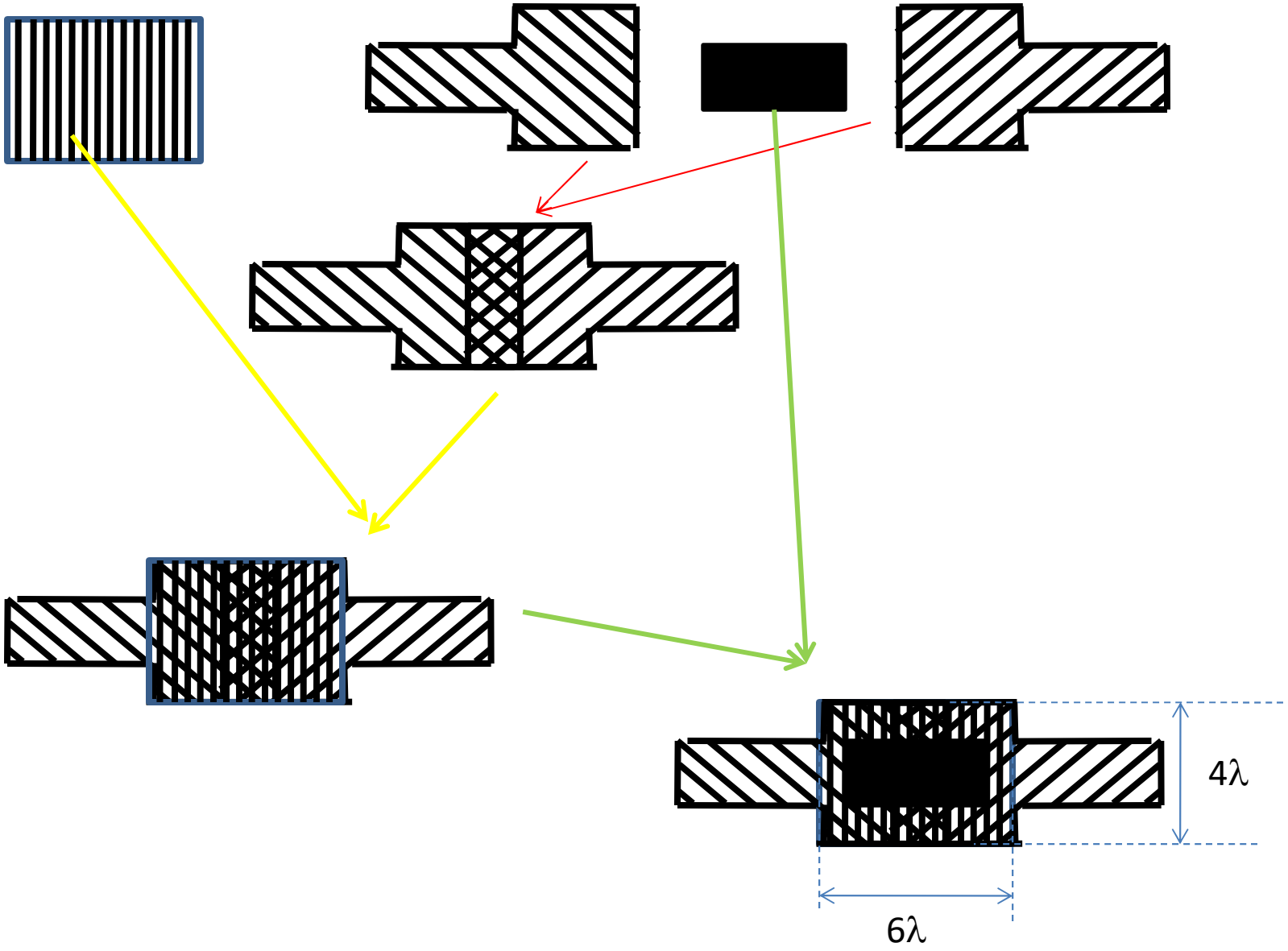
It is sometimes advantageous to connect polysilicon to diffusion

Two basic contacts are there for these contacts

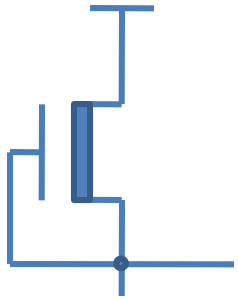
(1) Butting contact

(2) Buried Contact

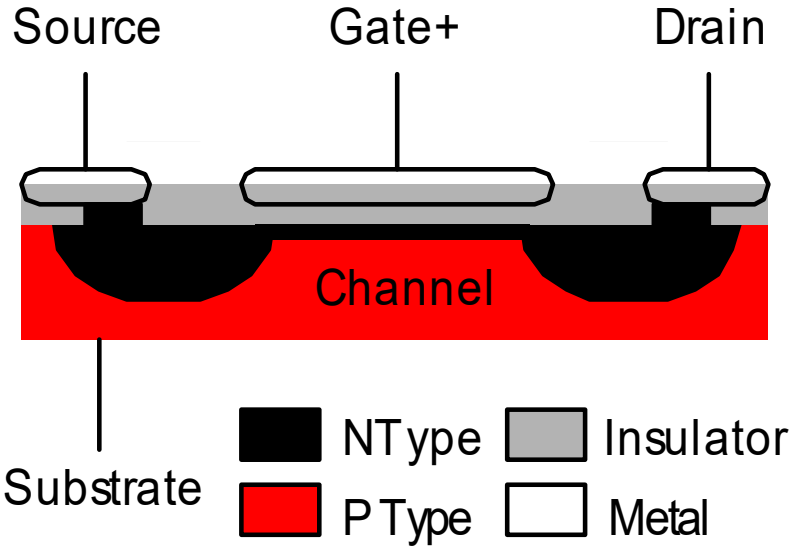
Butting Contact: nMOS



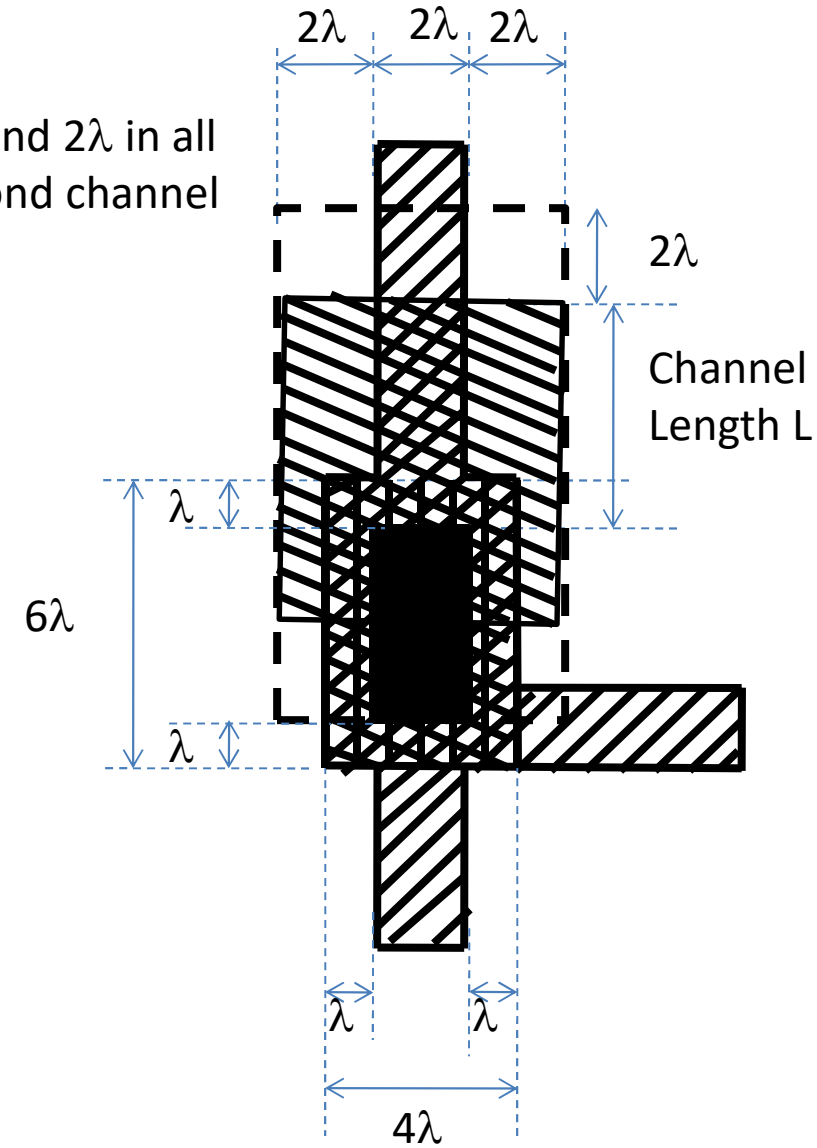
Butting Contact: nMOS



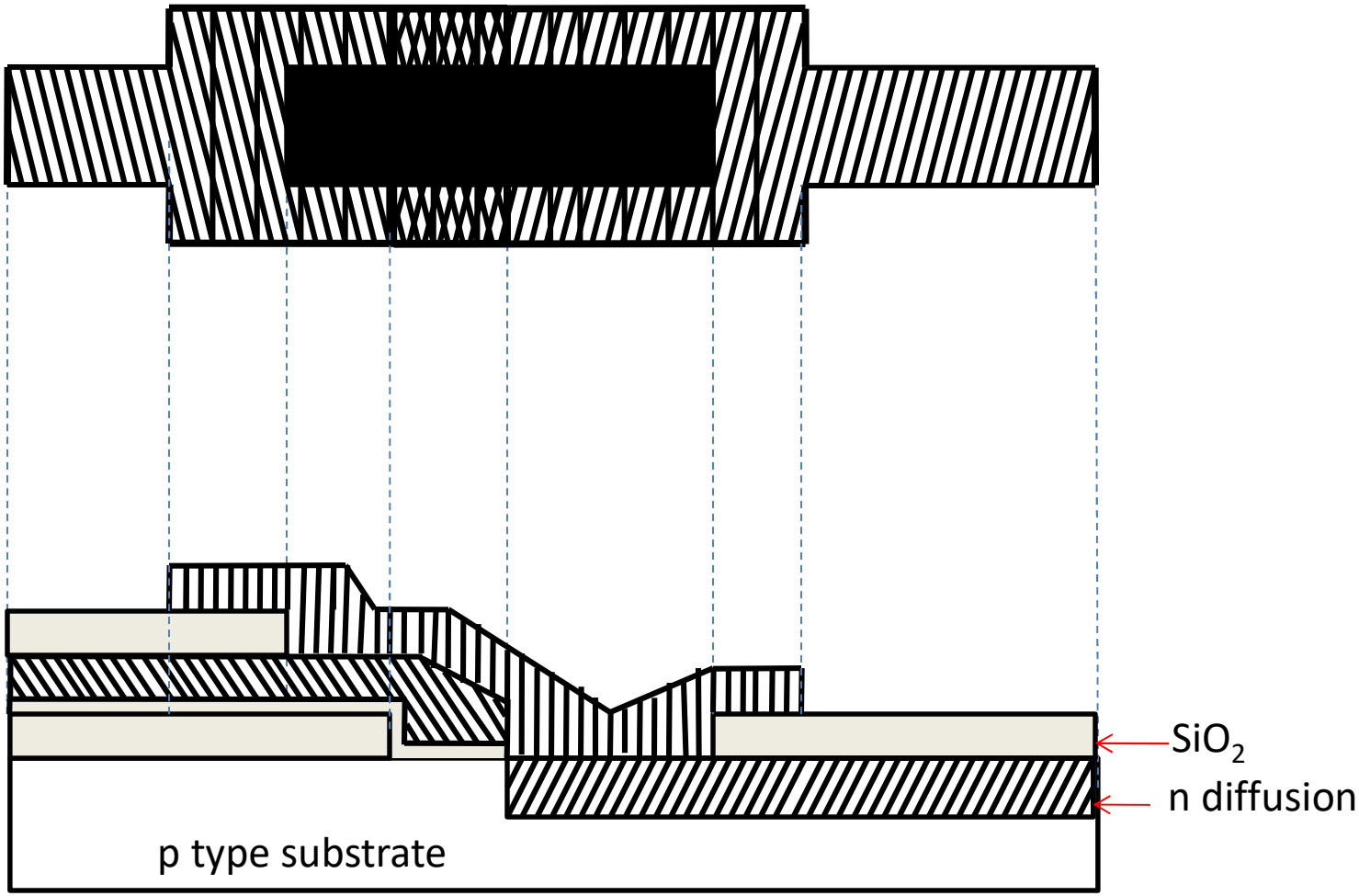
Pull up transistor in nMOS



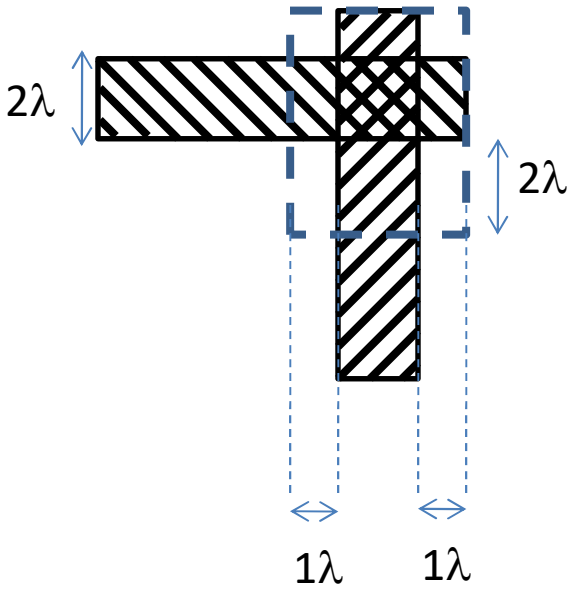
Implant to extend 2λ in all directions beyond channel

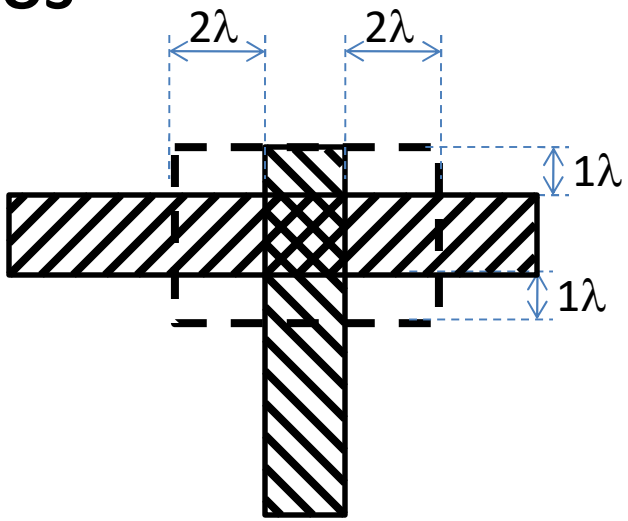


Butting Contact



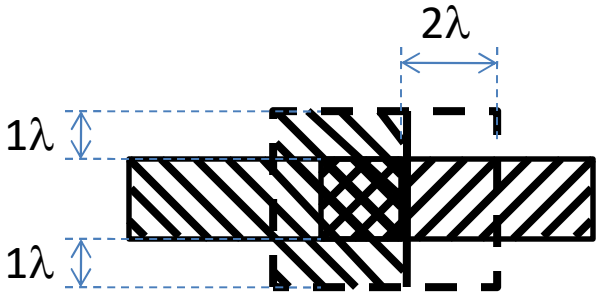
Buried Contact: nMOS

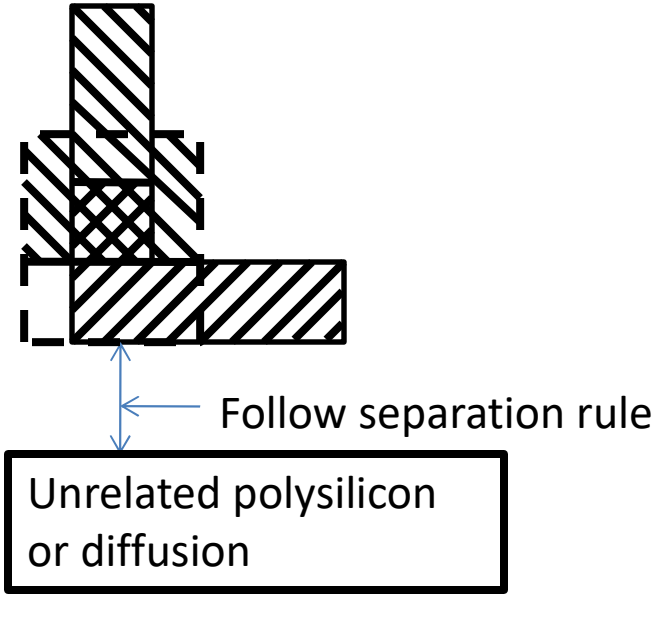




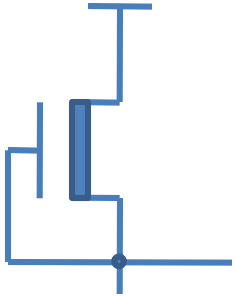
Layers are joined over a 2λ X 2λ area with the buried contact cut extending by 1λ to all directions around the contact area

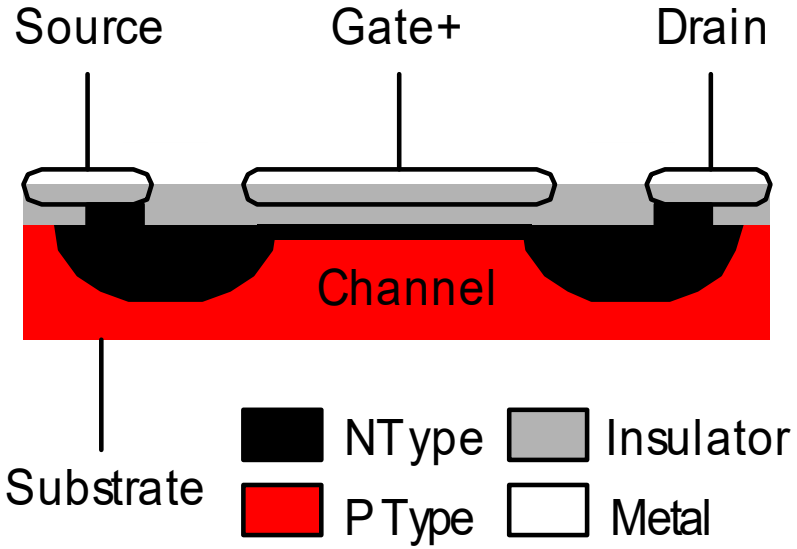
(But the contact cut extension is 2λ in diffusion paths leaving the contact area)



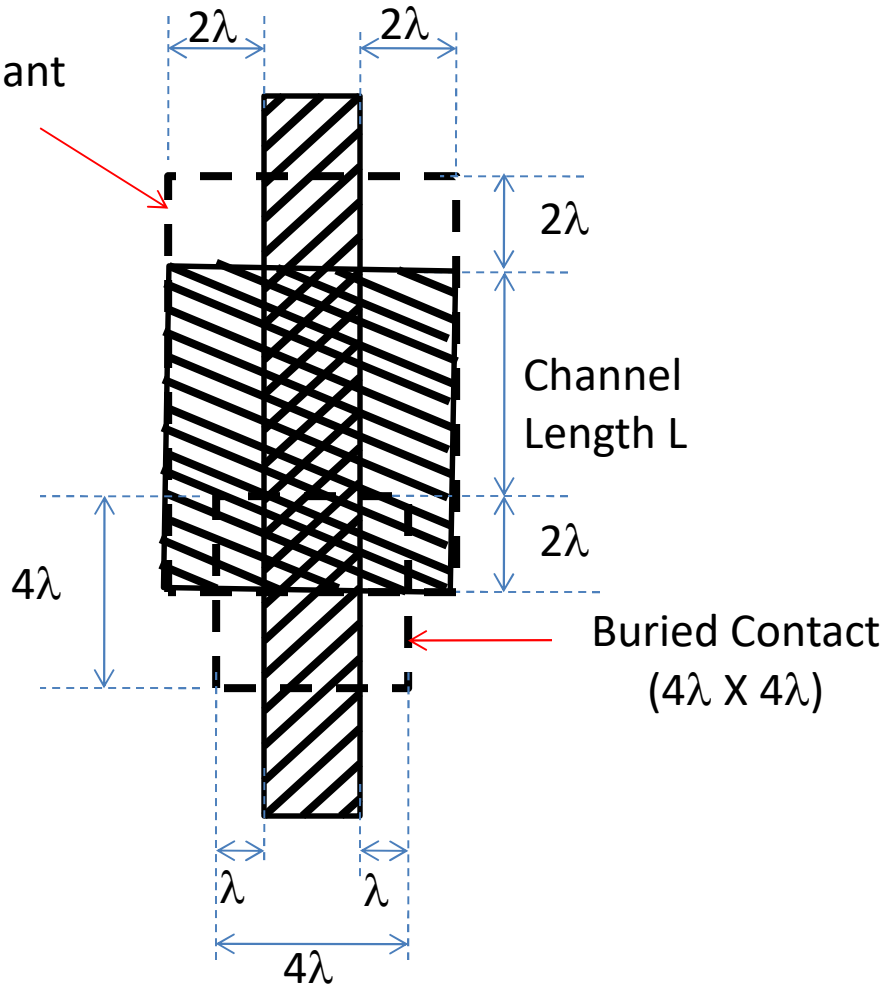


Buried Contact (nMOS pull up)

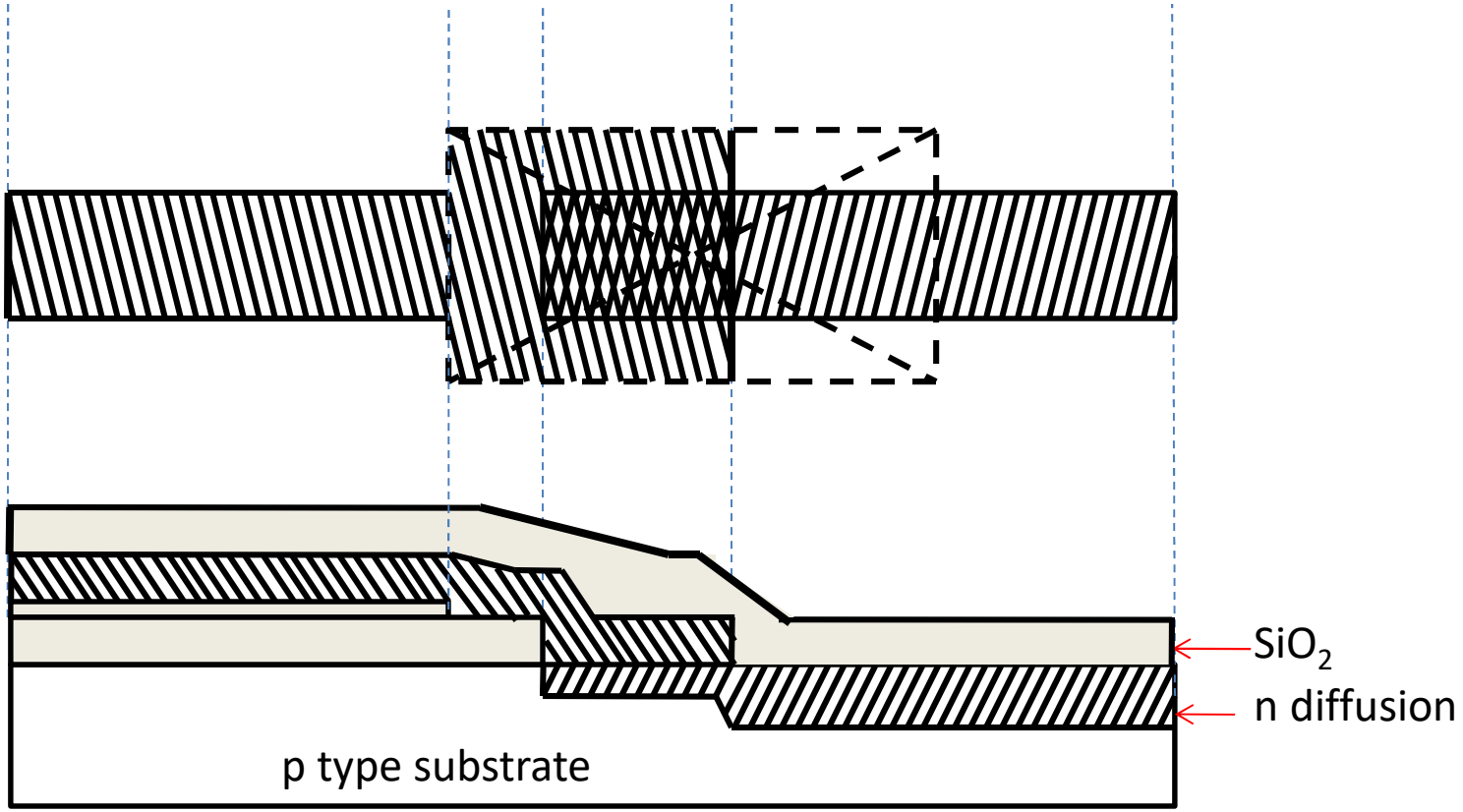




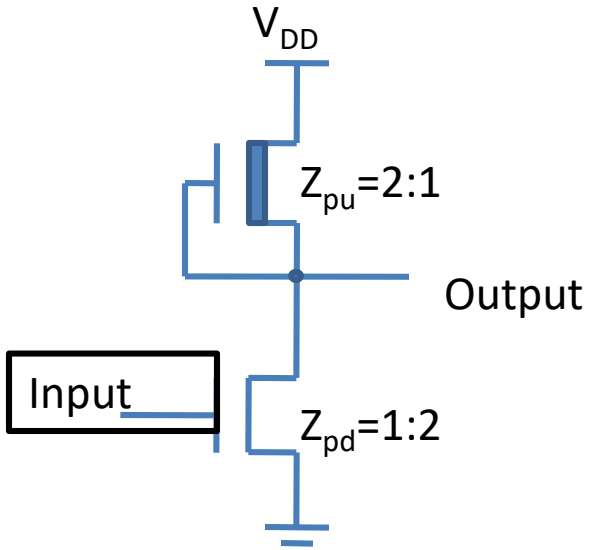
Implant to extend 2λ in all directions beyond channel

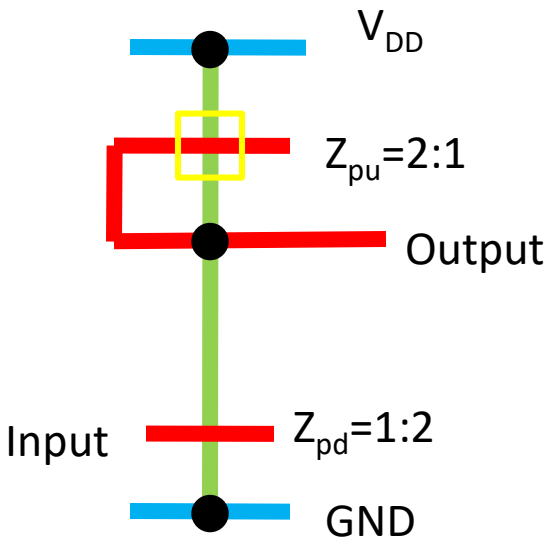


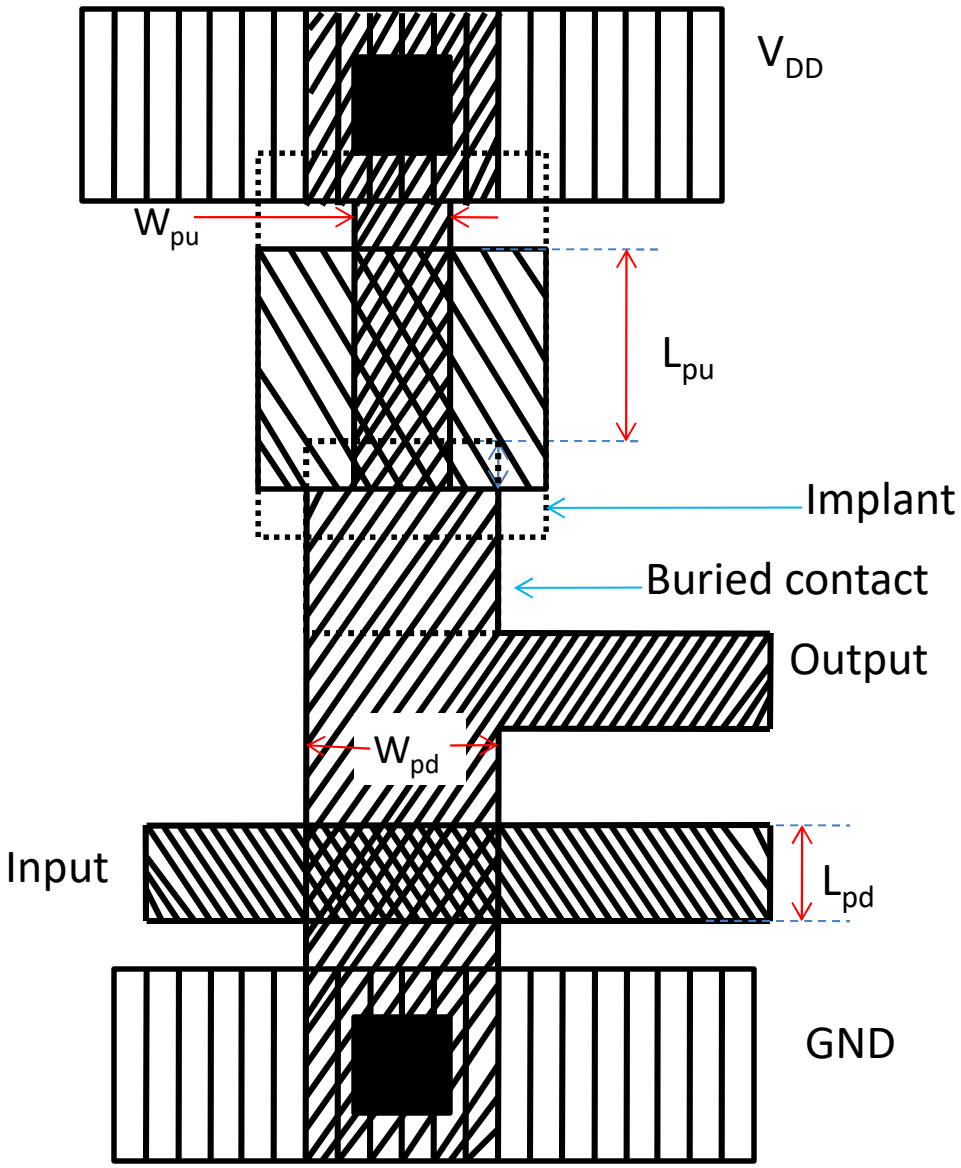
Buried Contact: Cross Section



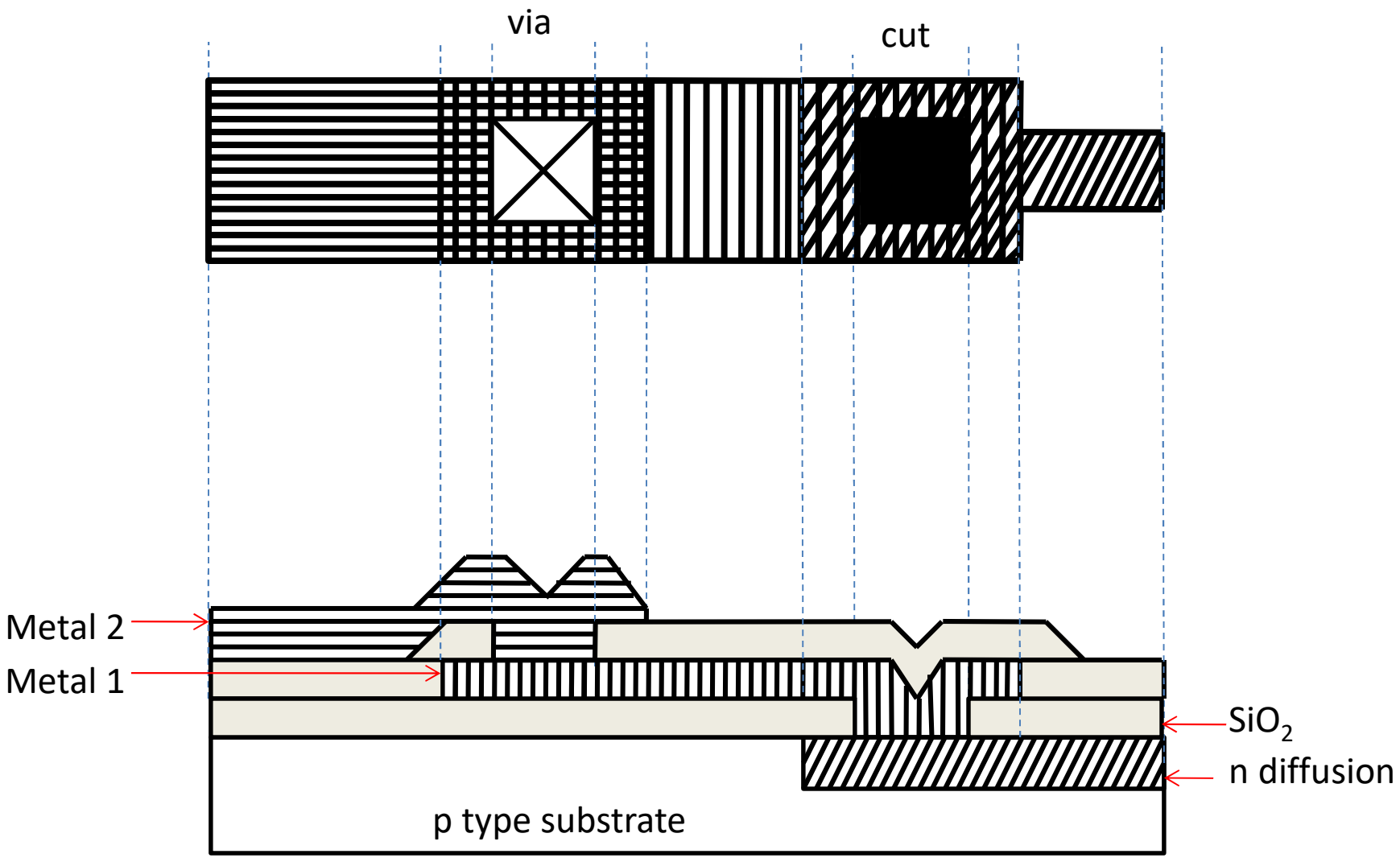
NMOS Inverter: Circuit-stick diagram-mask



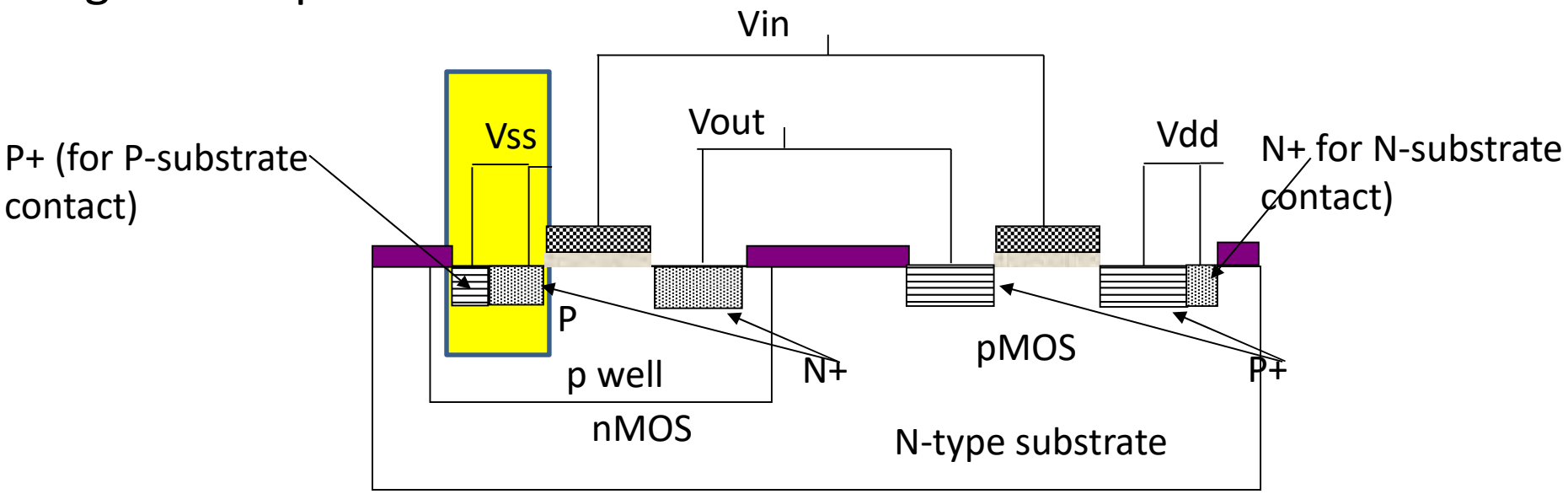


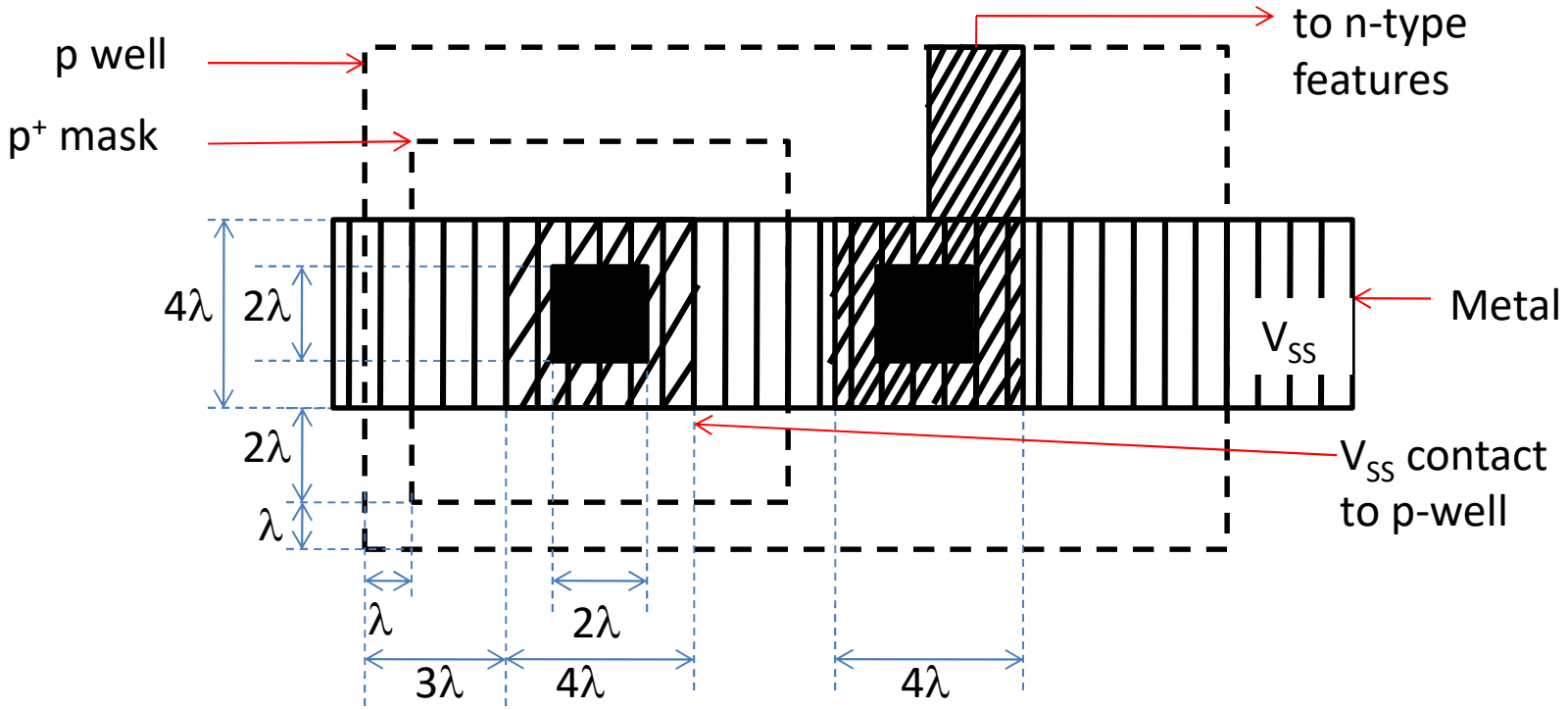


Metal2-via-Metal1-cut-ndiffusion connection

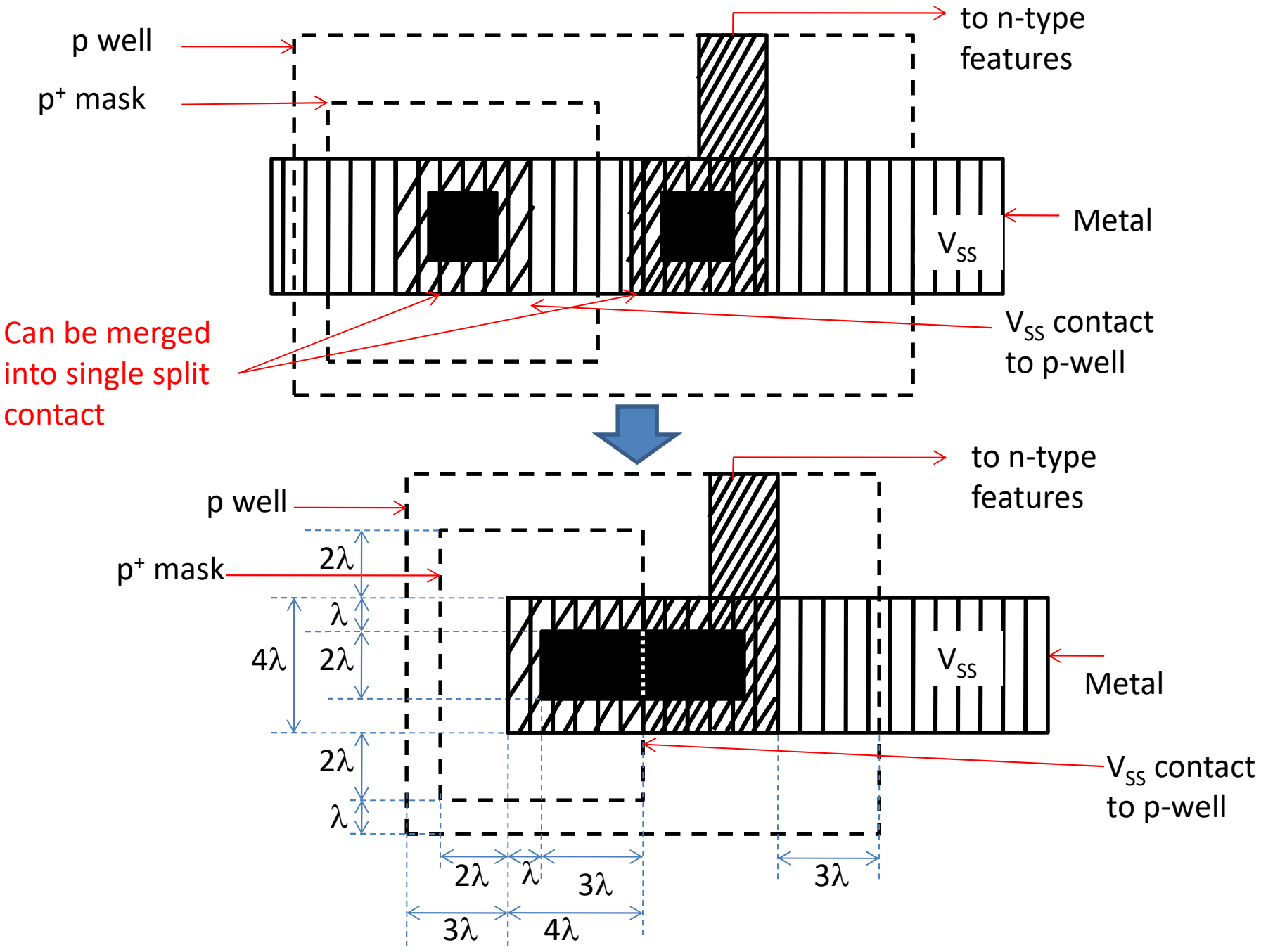


Design Rules: p-well CMOS

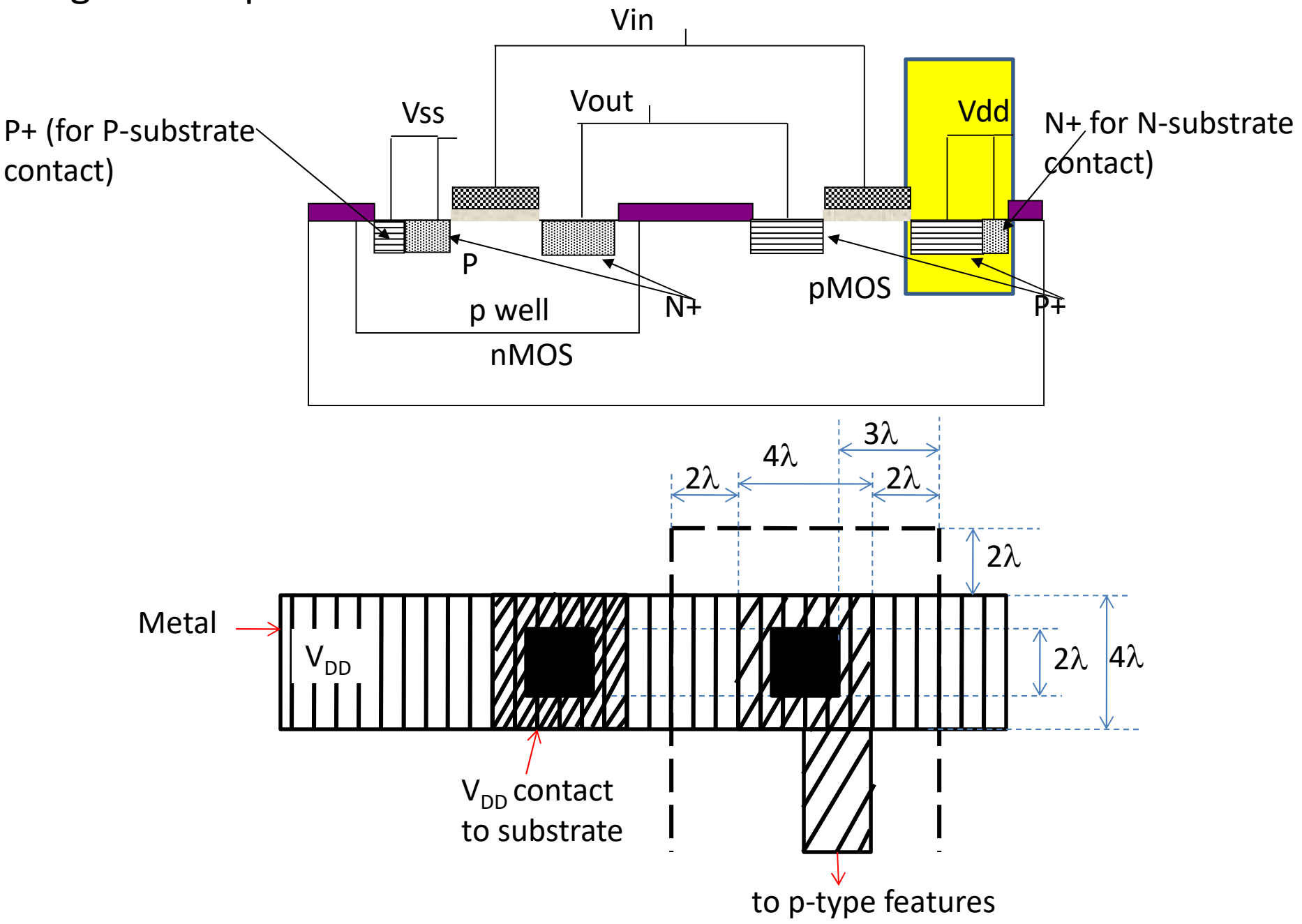




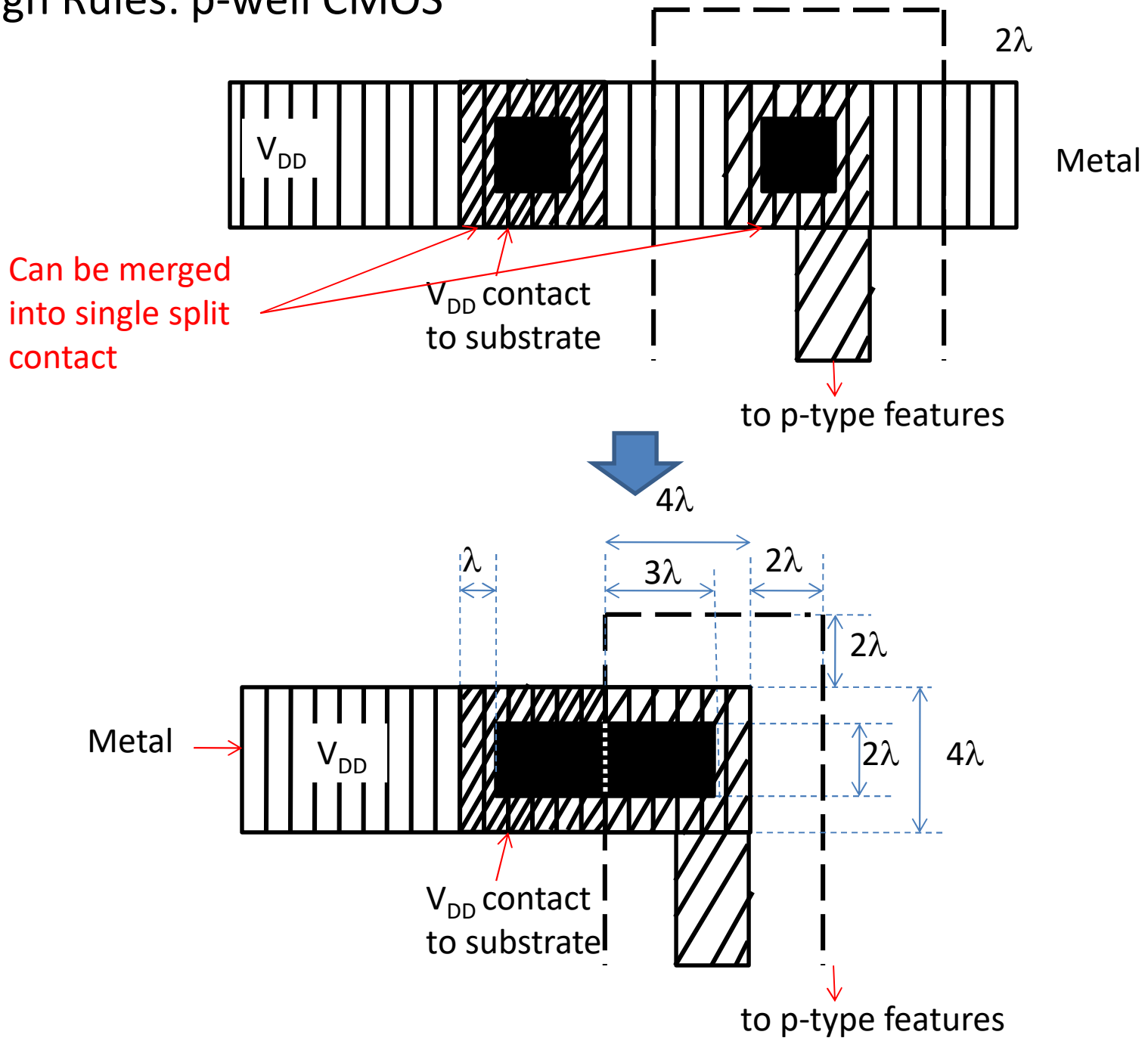
Design Rules: p-well CMOS



Design Rules: p-well CMOS

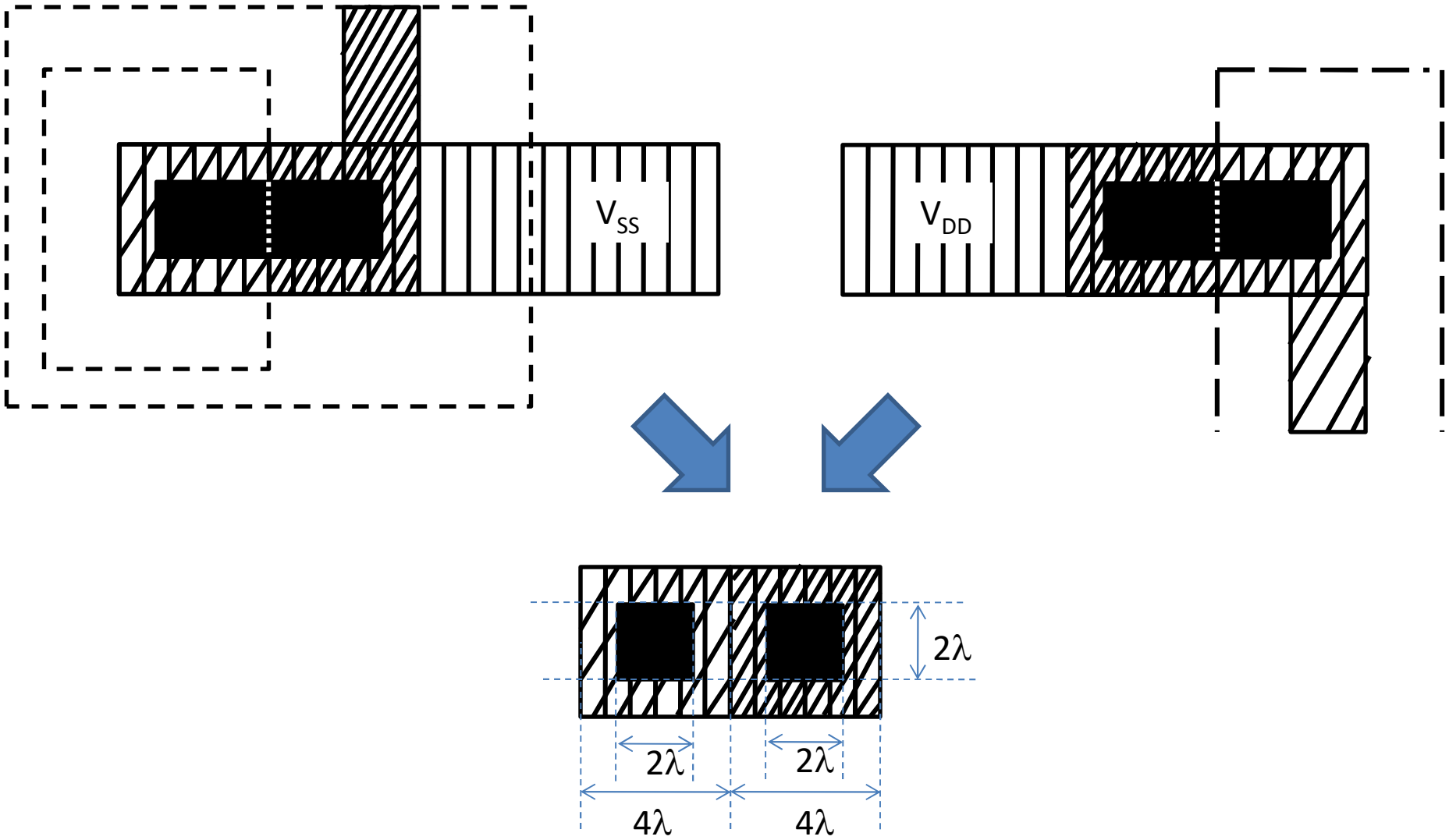


Design Rules: p-well CMOS

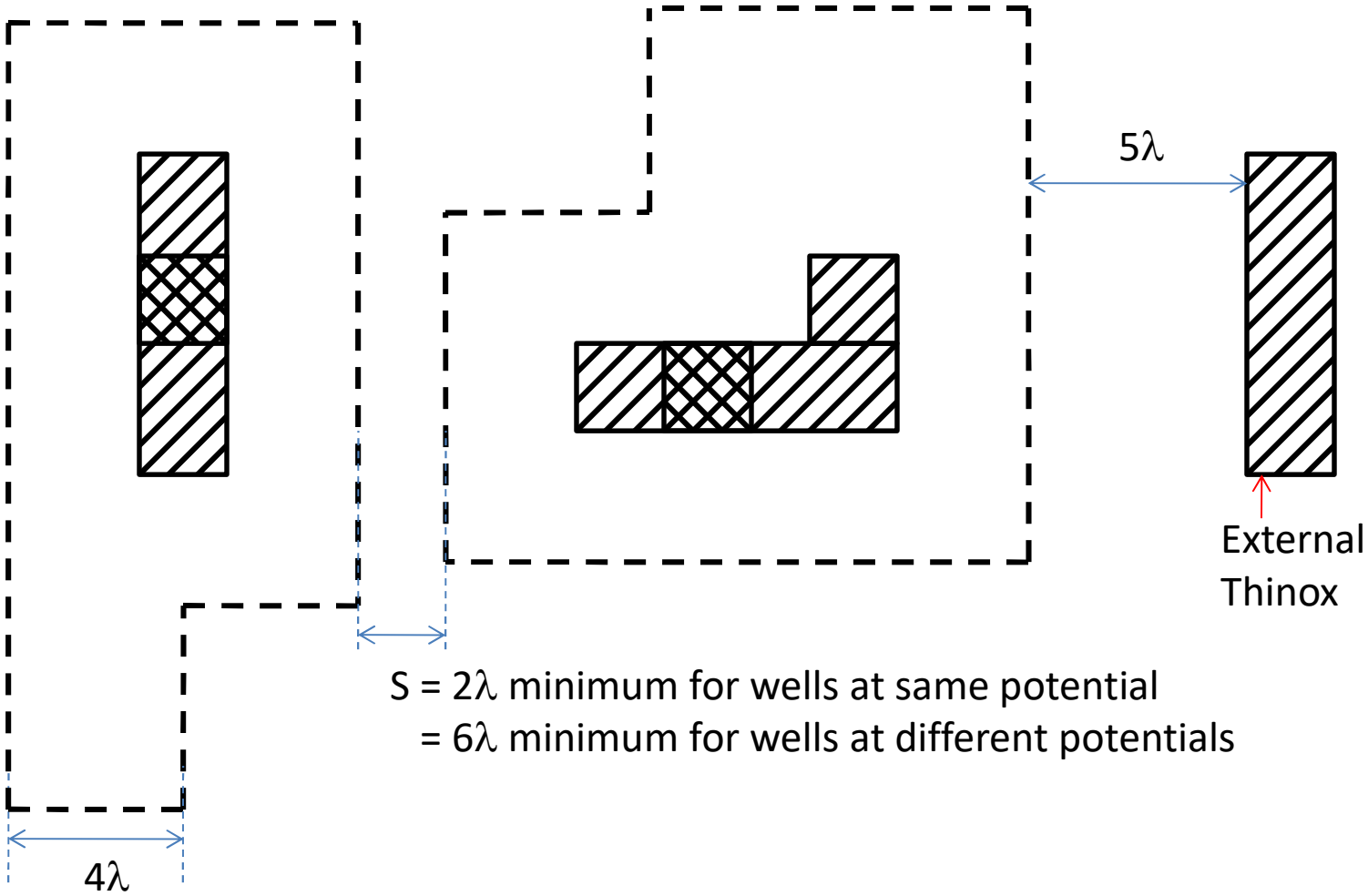


Design Rules: p-well CMOS

Split contacts may also be made with separate cuts



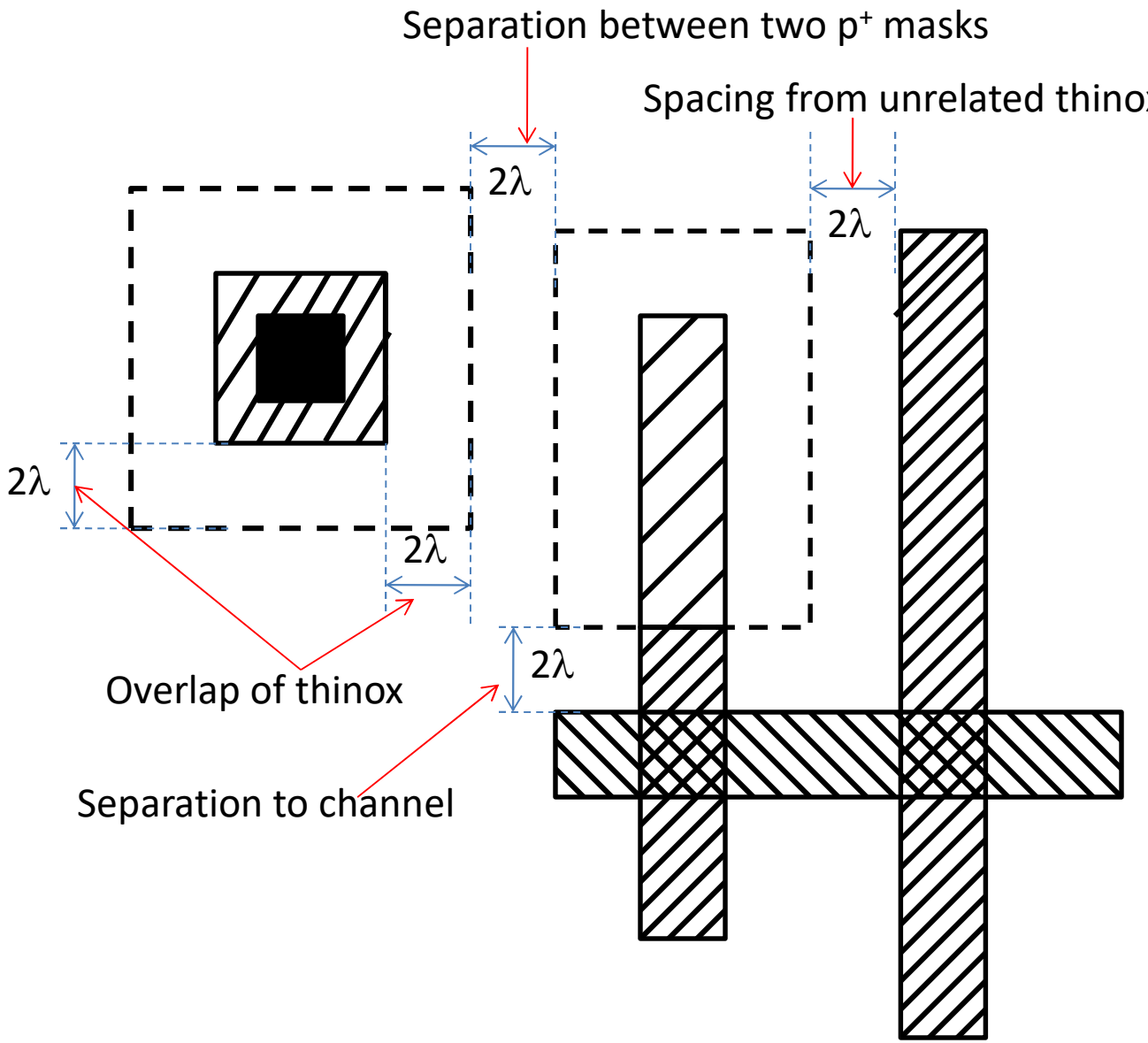
Design Rules: p-well CMOS



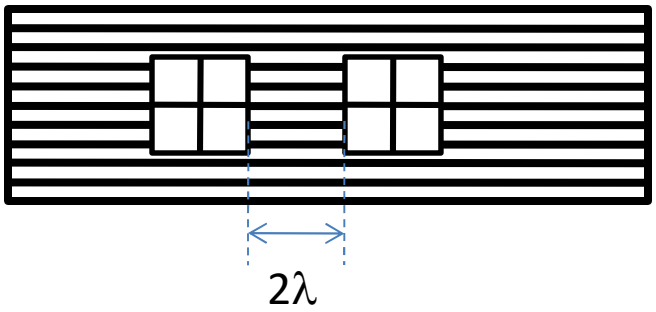
p-well must overlap all enclosed thinox by 3λ minimum

Thinox must not cross well boundary

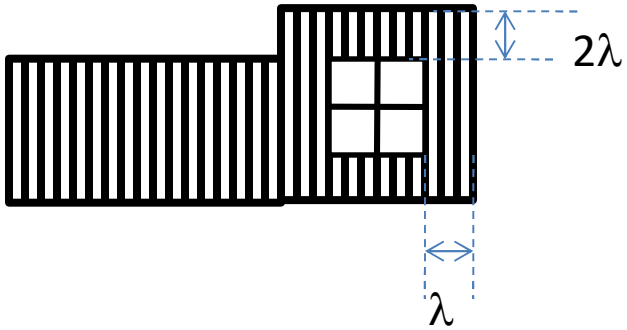
Design Rules: p-well CMOS



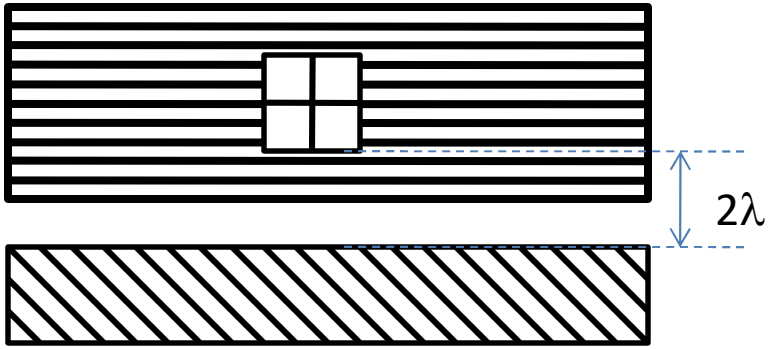
Aspects related to vias



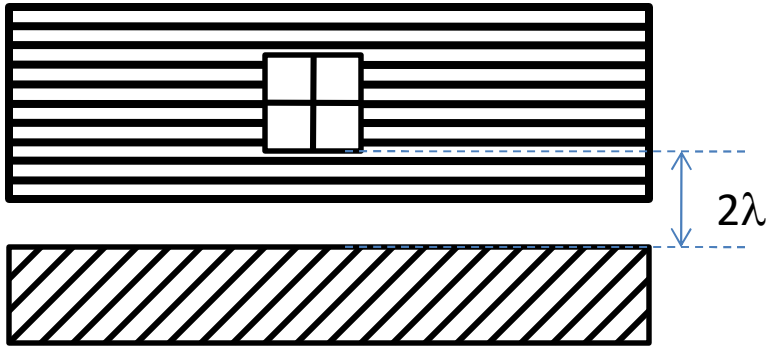
Separation via to via



Overlap by metal1

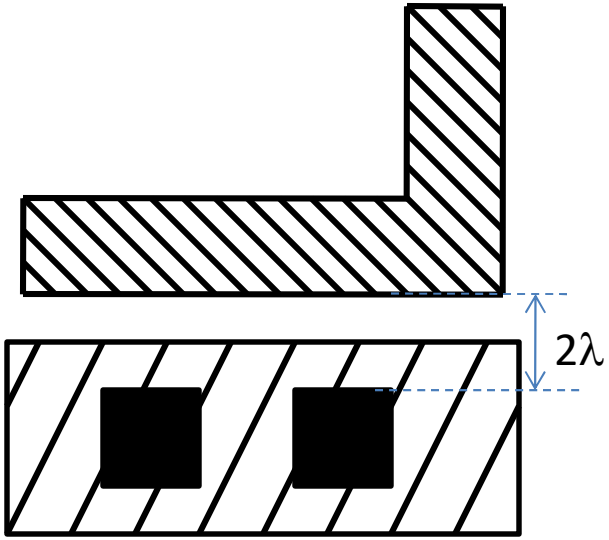


Separation via to polysilicon

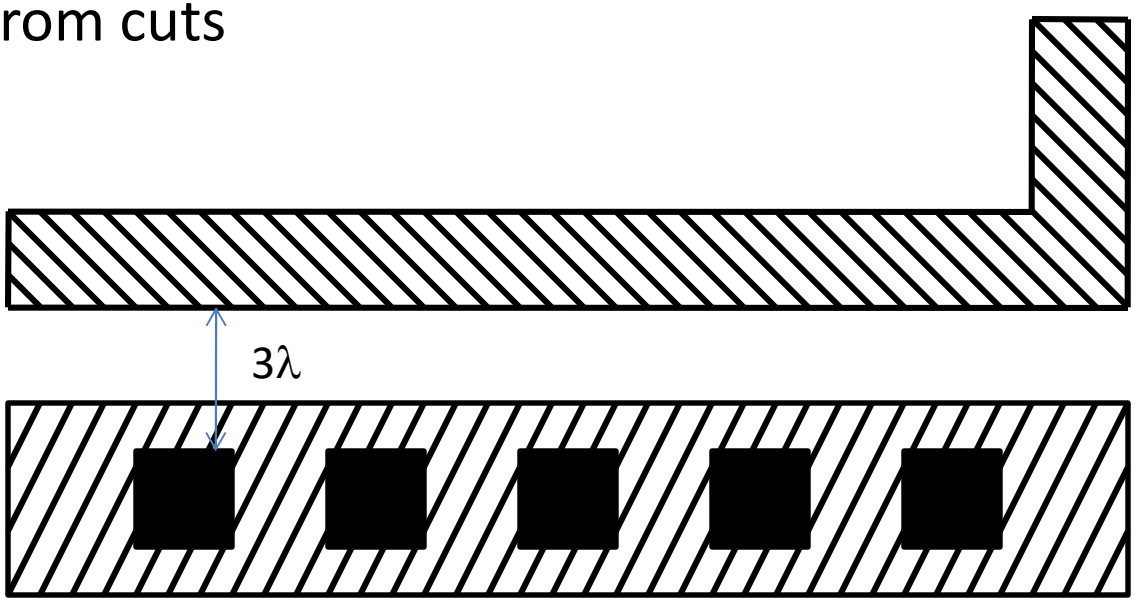


Separation via to thinox

Polysilicon wire separation from cuts

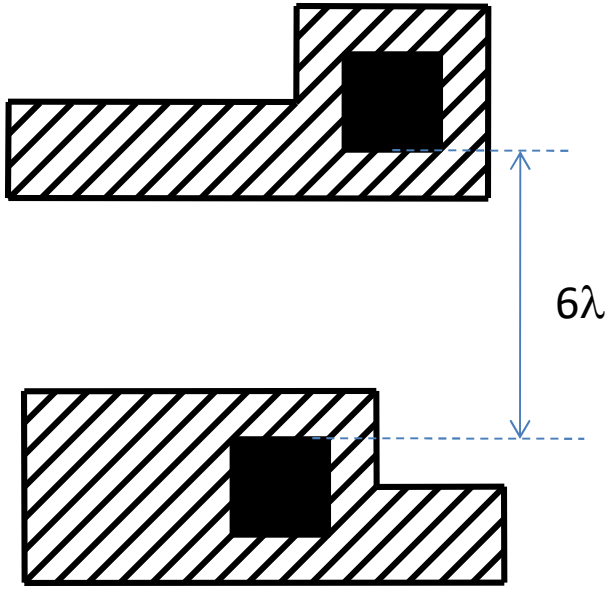


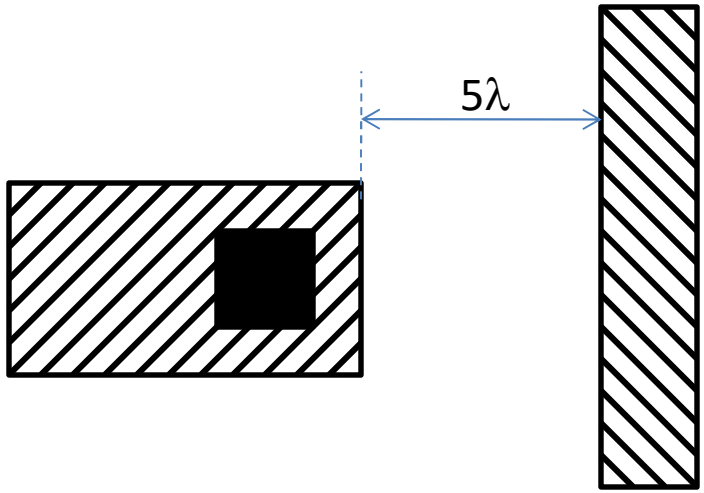
Short polysilicon run



Long polysilicon run

Diffusion wire separation from cuts



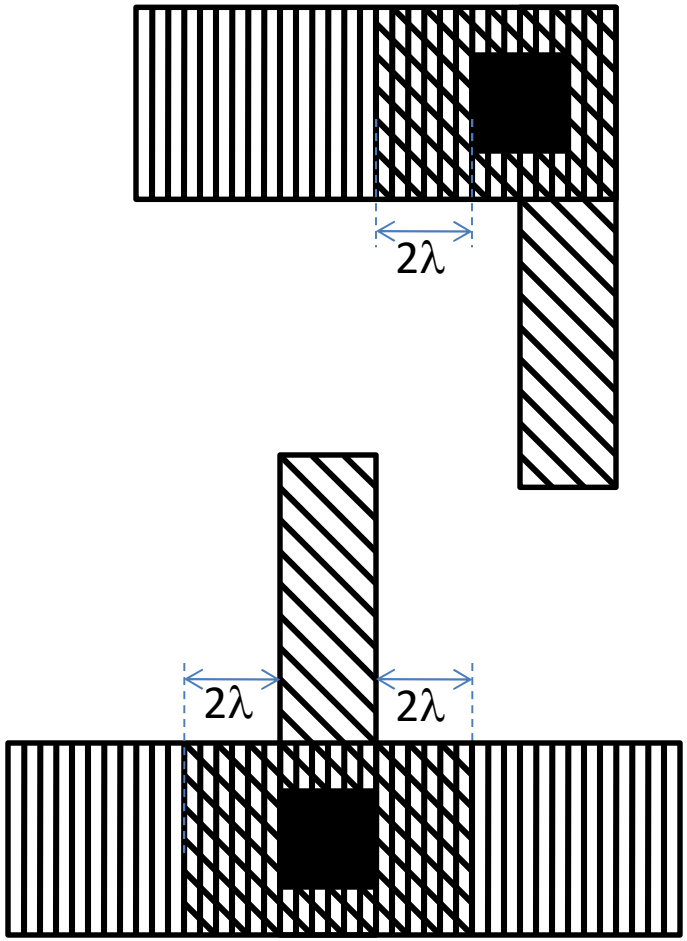


Separation between different active areas

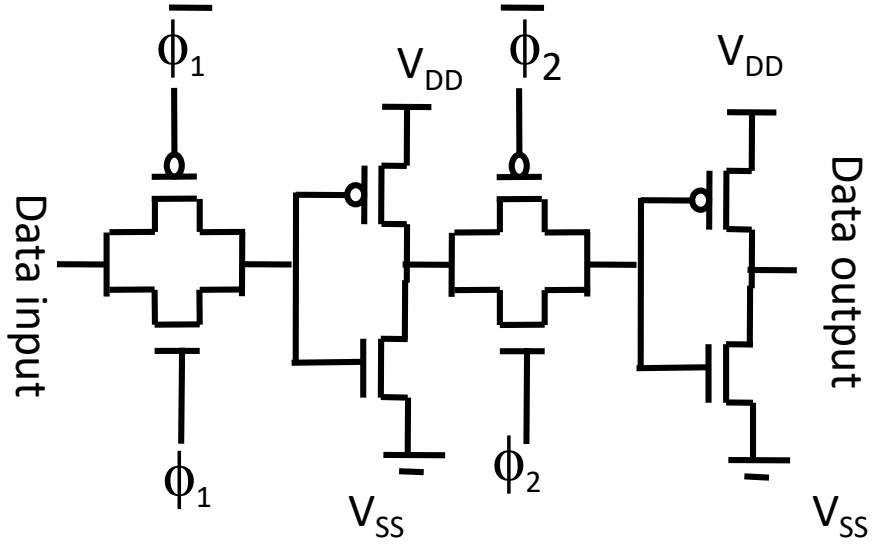
Polysilicon wire separation from cuts

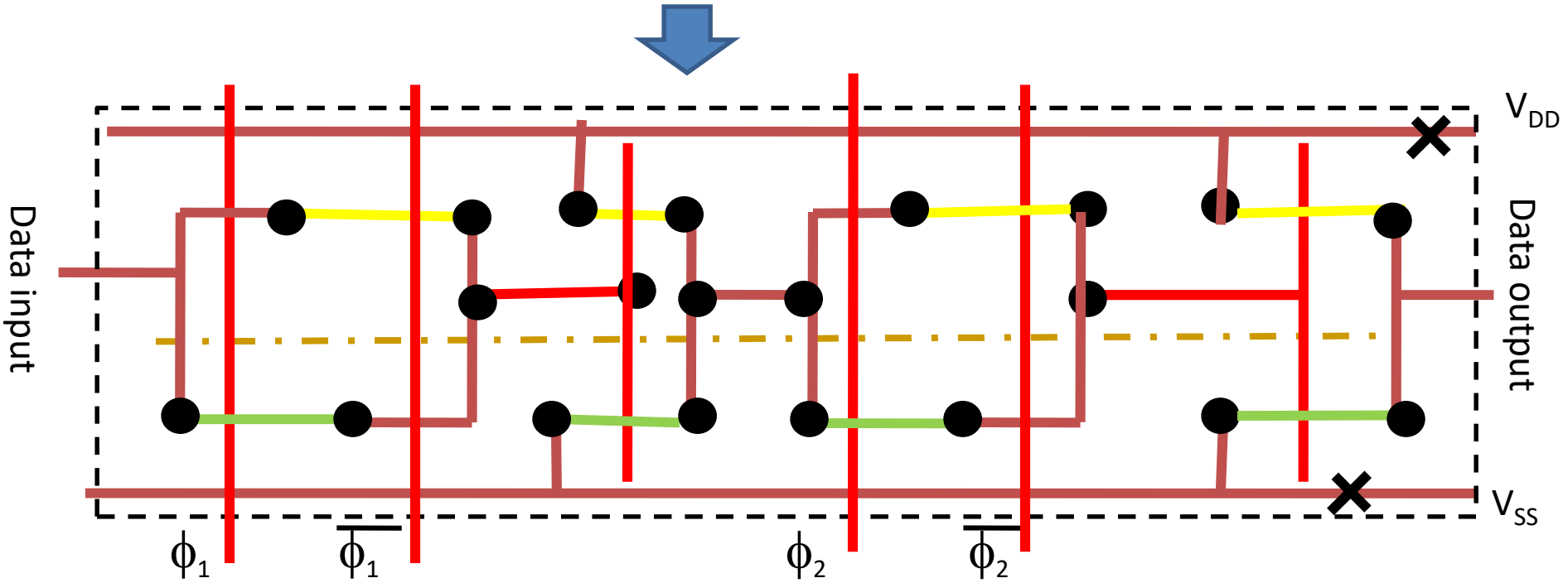
Increase in polysilicon overlap

Polysilicon is to be extended in direction of metal

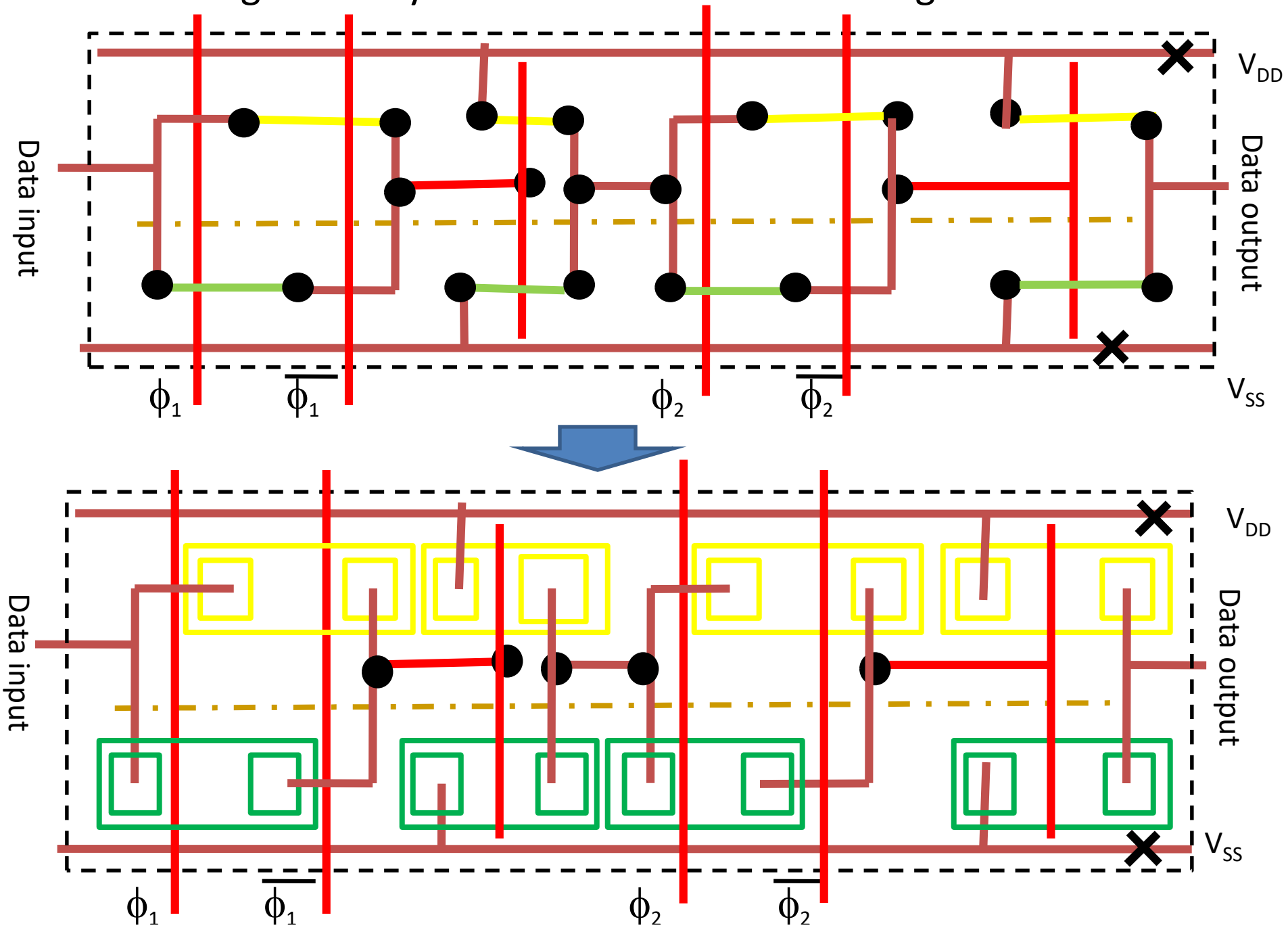


Example: 1 bit shift register: Circuit to stick diagram

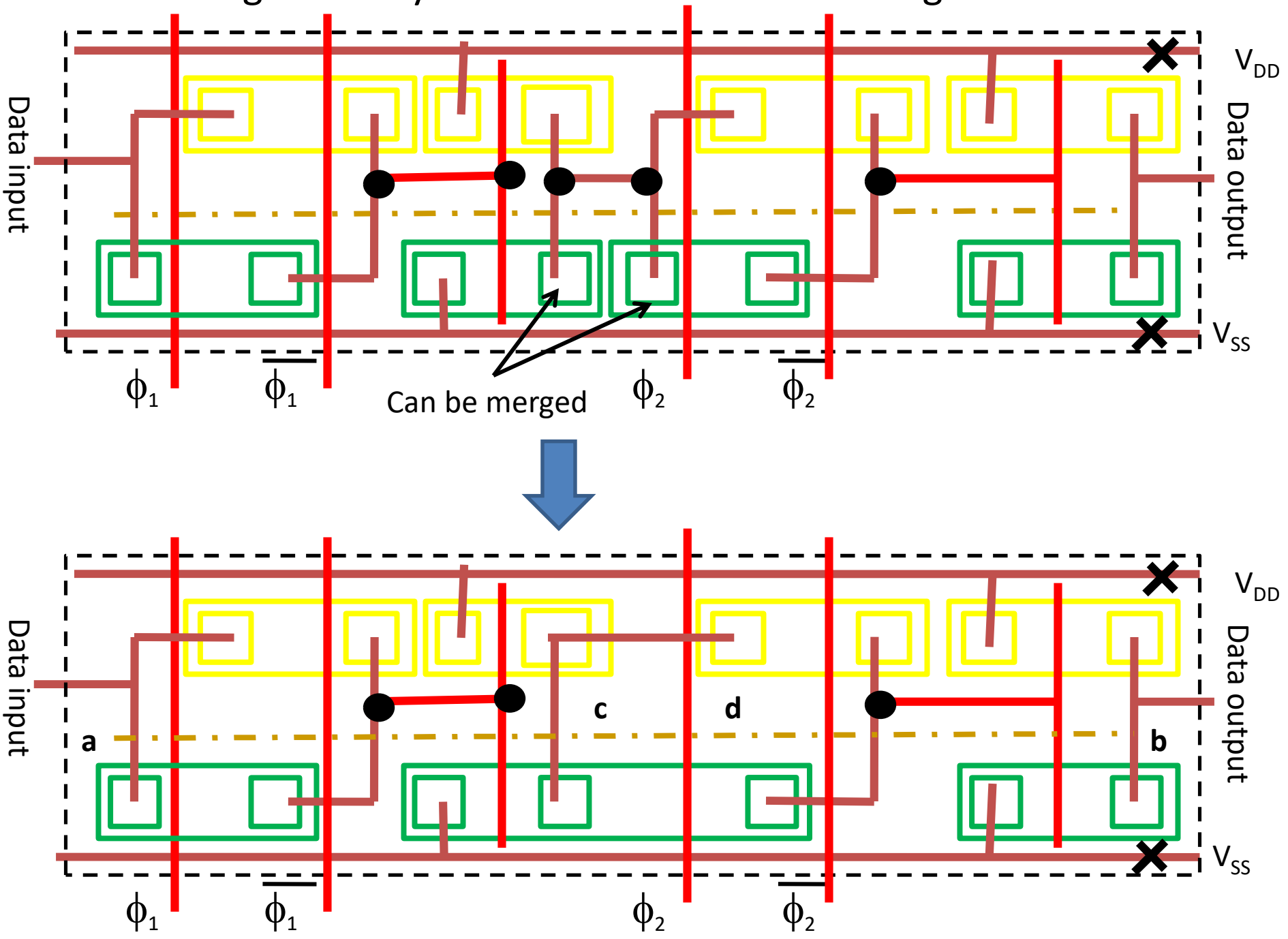




Stick Diagram to Symbolic Form: CMOS shift Register



Stick Diagram to Symbolic Form: CMOS shift Register



Symbolic Form to Mask form: CMOS shift Register