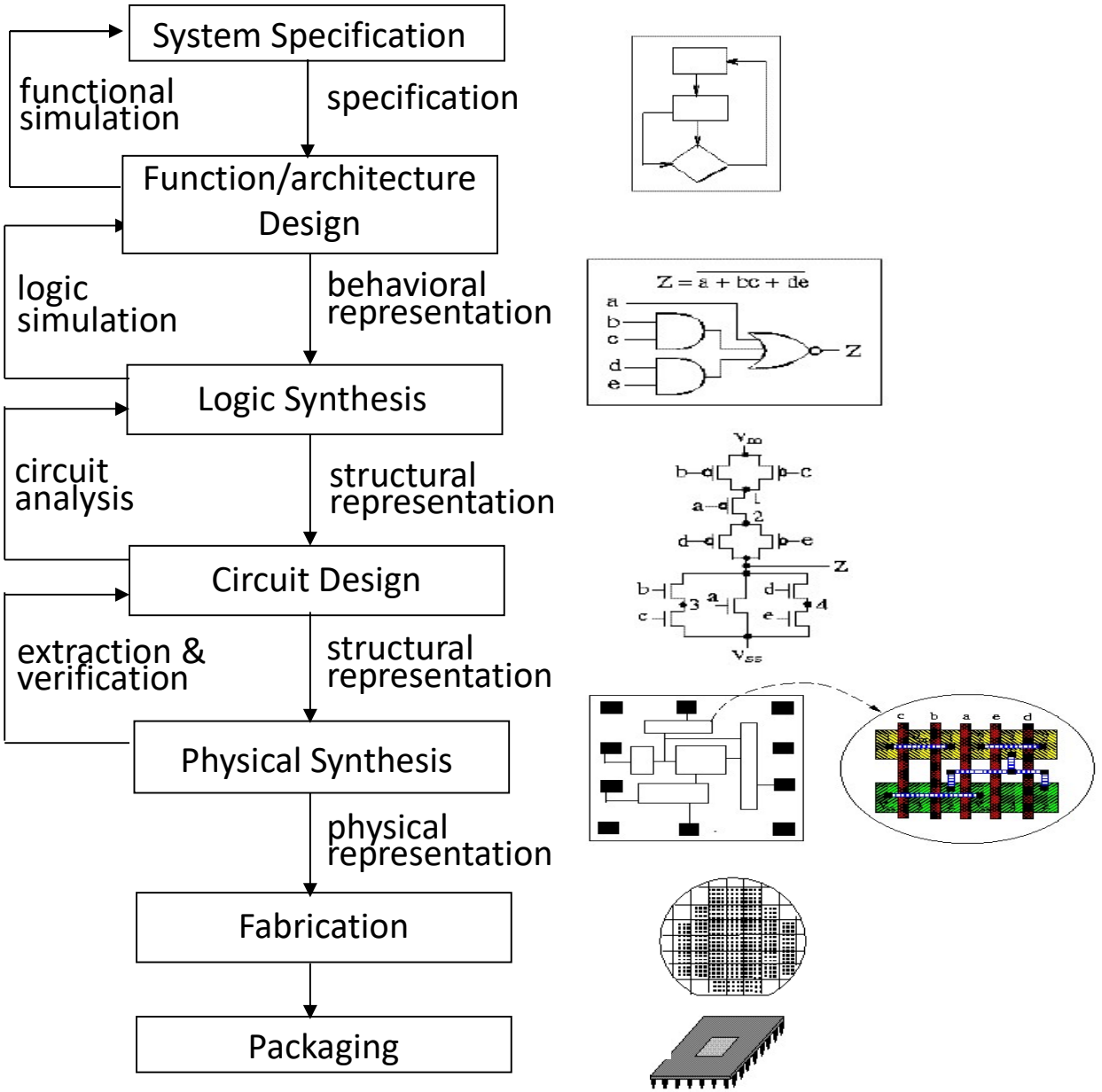
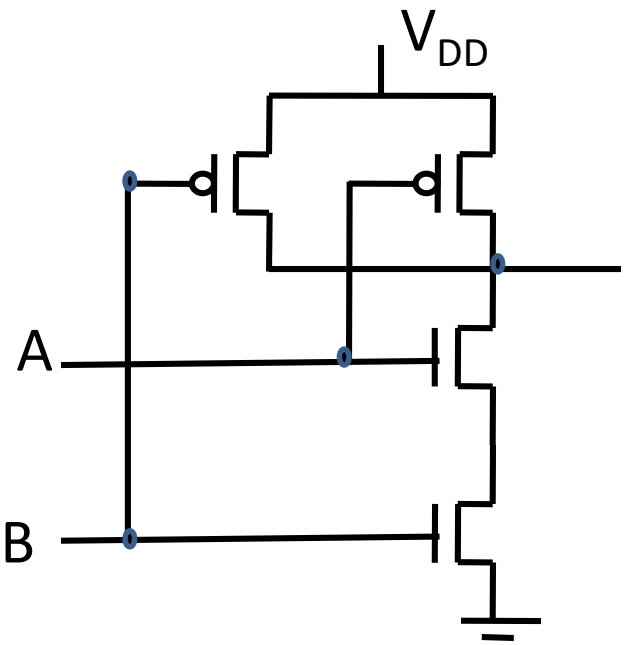
Logic Design by MOS Gates

VLSI Design Flow



Conduction Complement

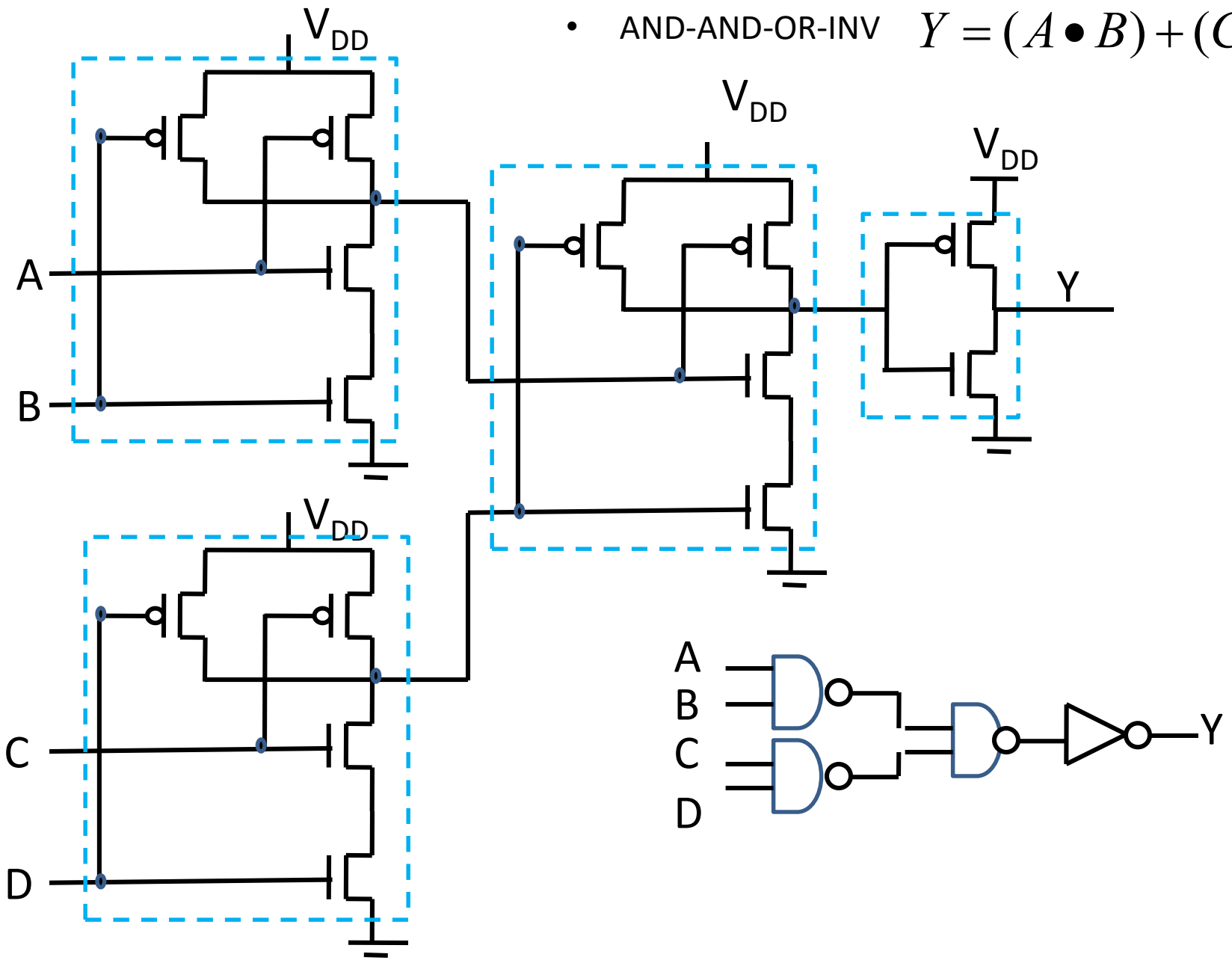
- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS



- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

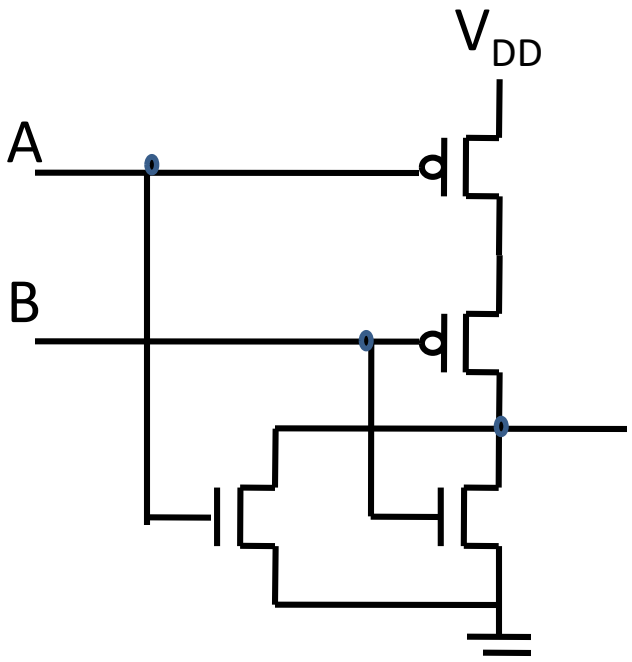
Realization by NAND Gates

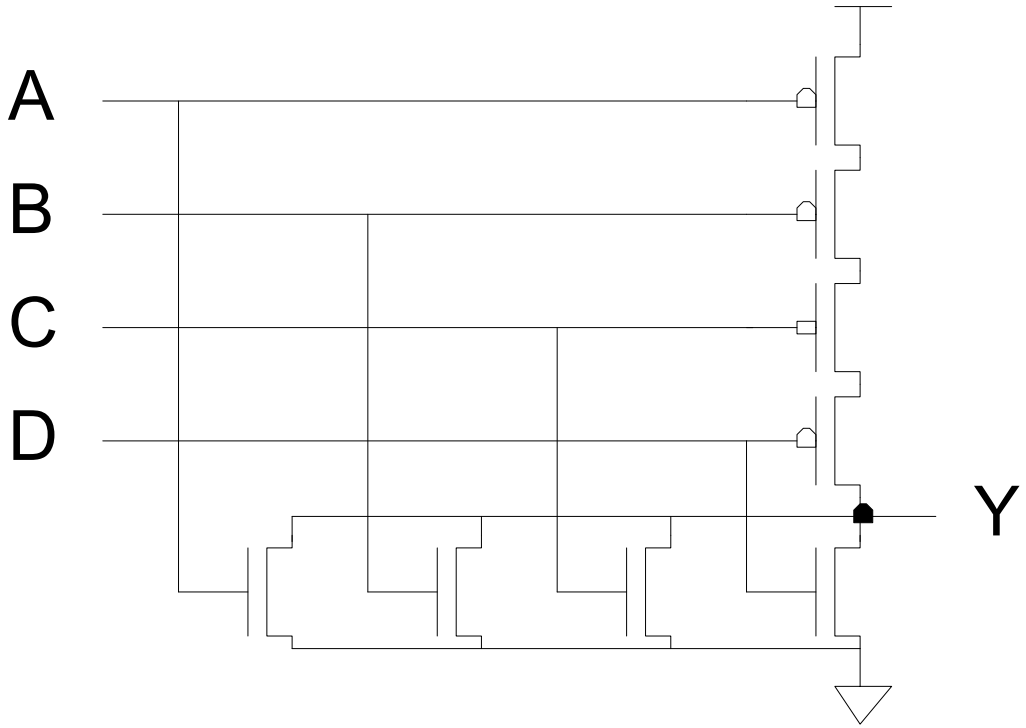
- AND-AND-OR-INV $Y = \overline{(A \bullet B) + (C \bullet D)}$



CMOS Gate Design

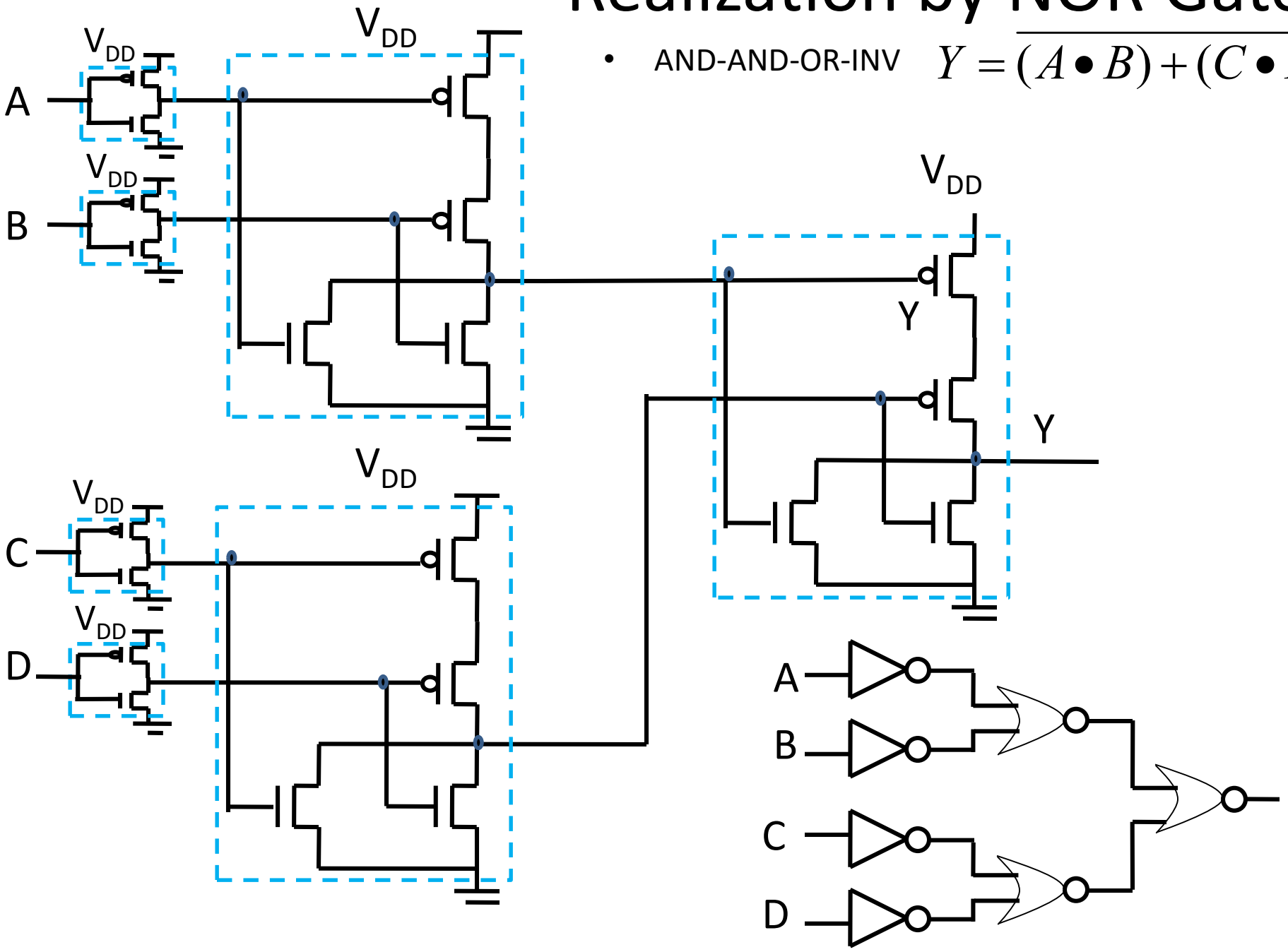
- CMOS NOR gate





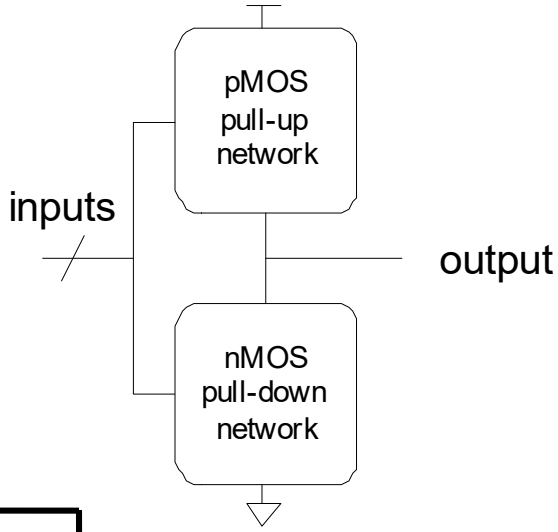
Realization by NOR Gates

- AND-AND-OR-INV $Y = \overline{(A \bullet B) + (C \bullet D)}$



Complementary CMOS (single complex cell)

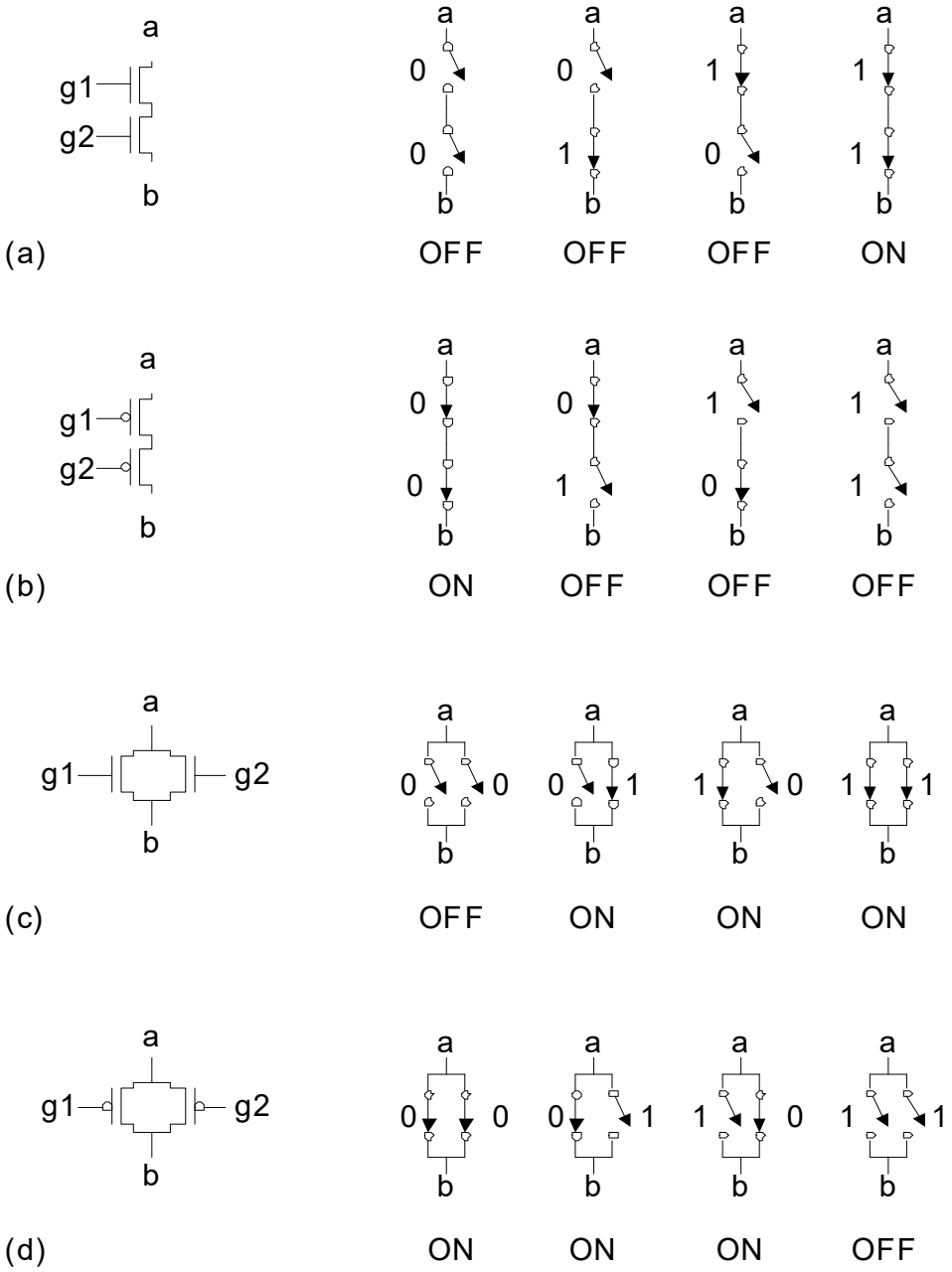
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

Series and Parallel

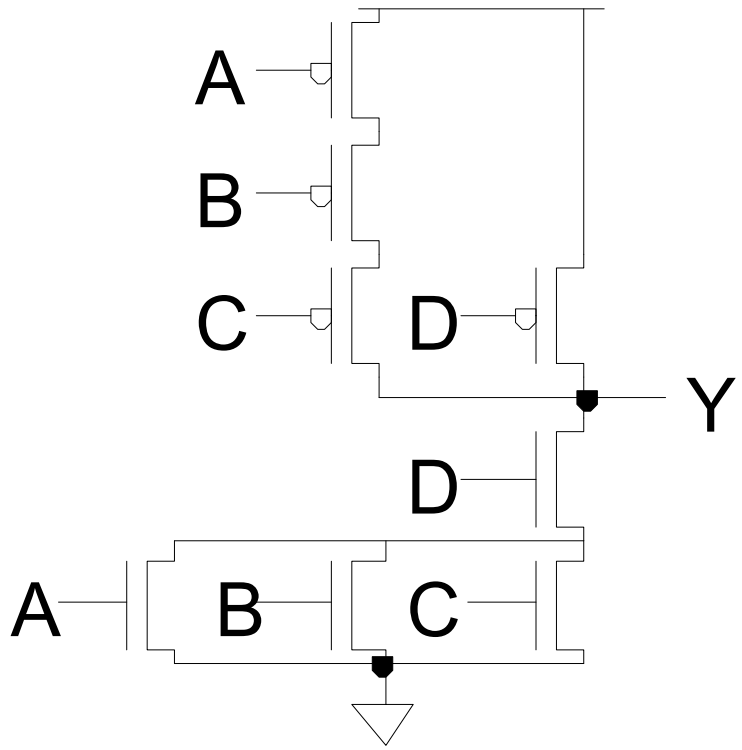
- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



Compound Gates

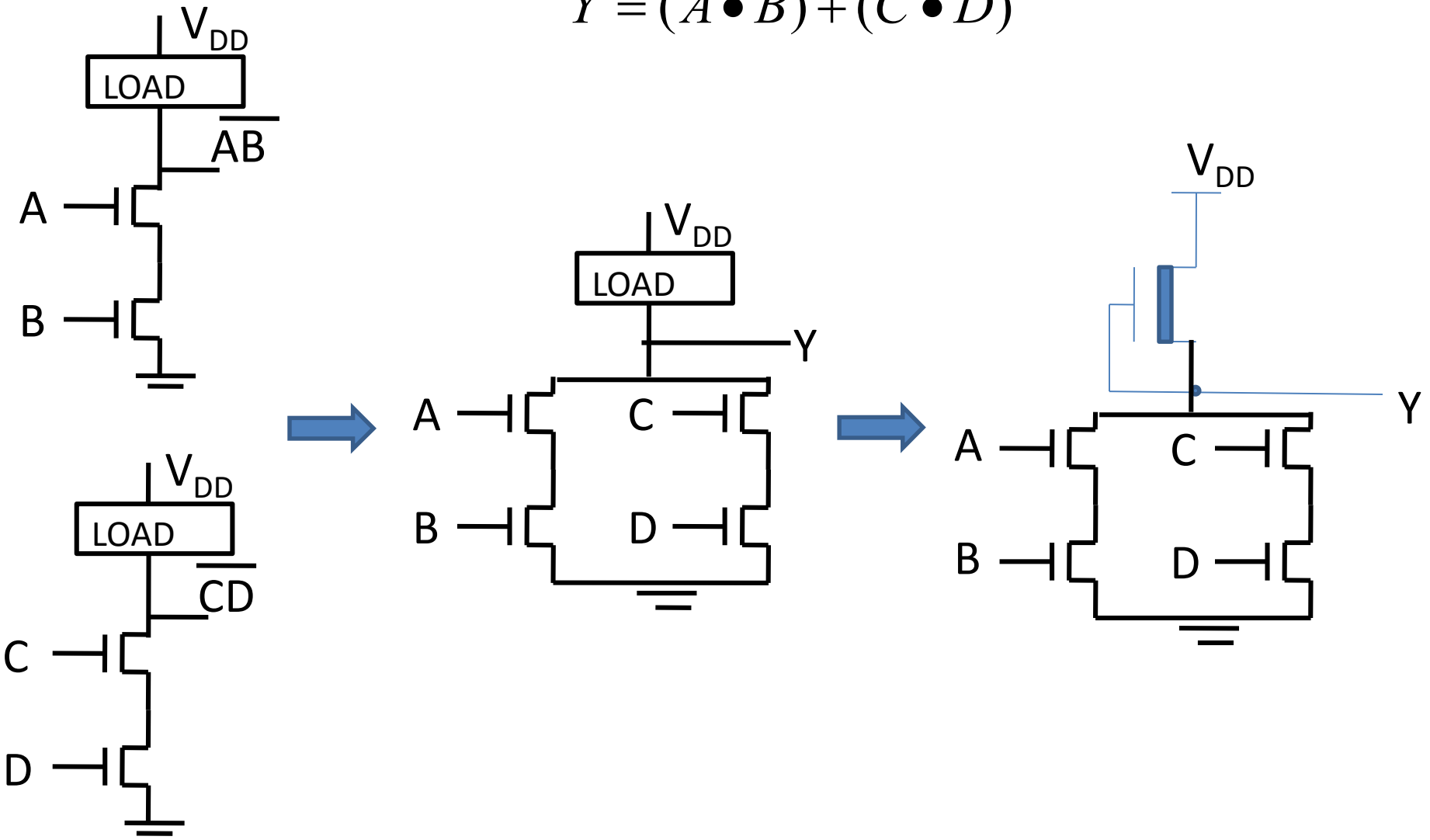
Compound gates can do any inverting function

- $Y = \overline{(A + B + C) \bullet D}$



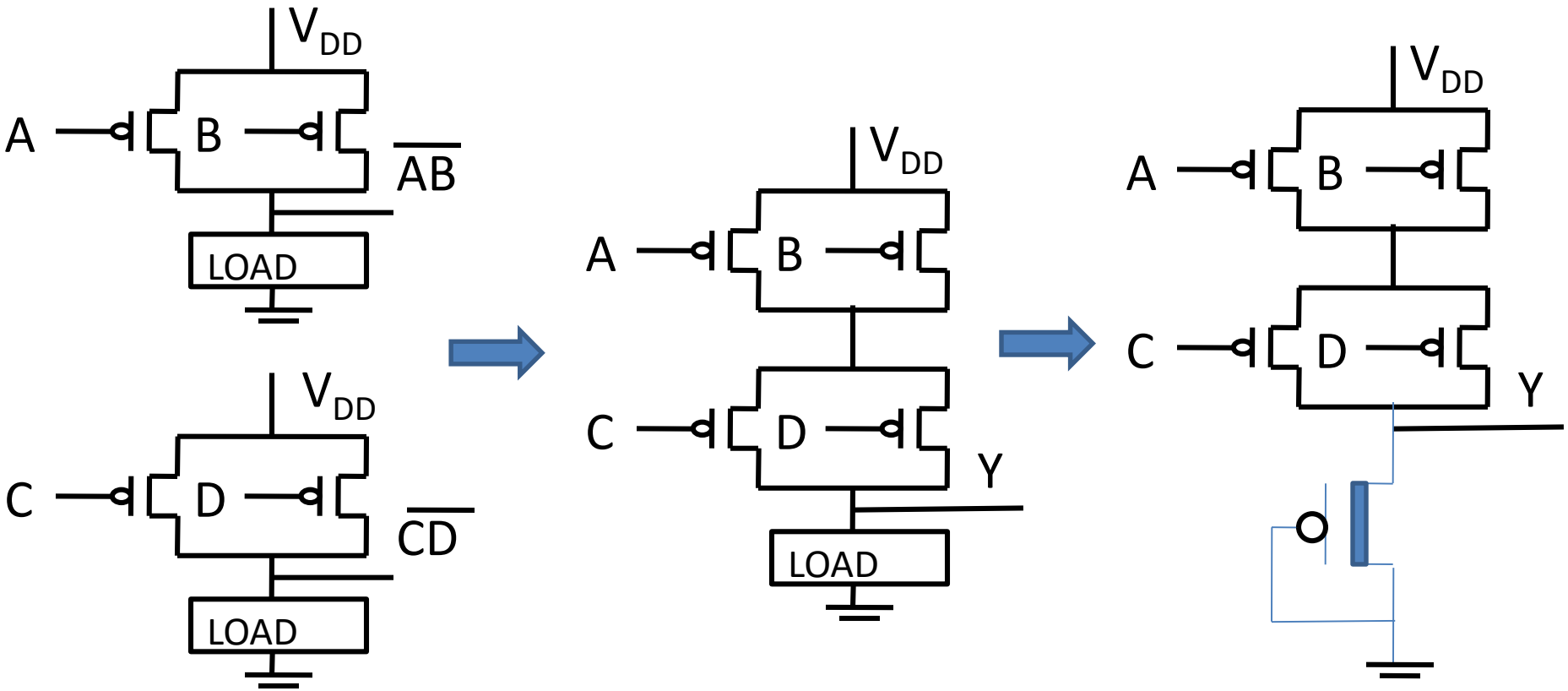
Example:

$$Y = \overline{(A \bullet B) + (C \bullet D)}$$



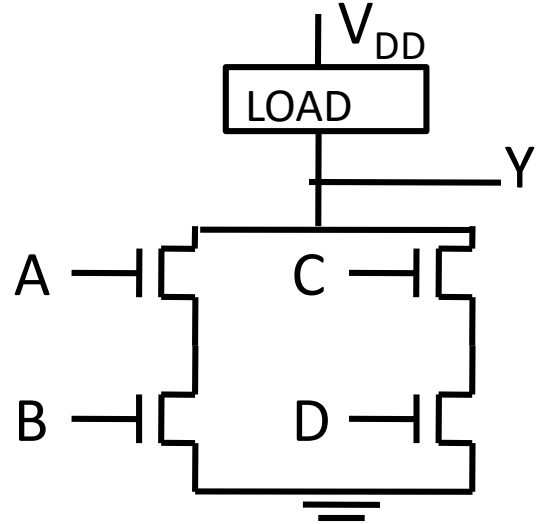
Example:

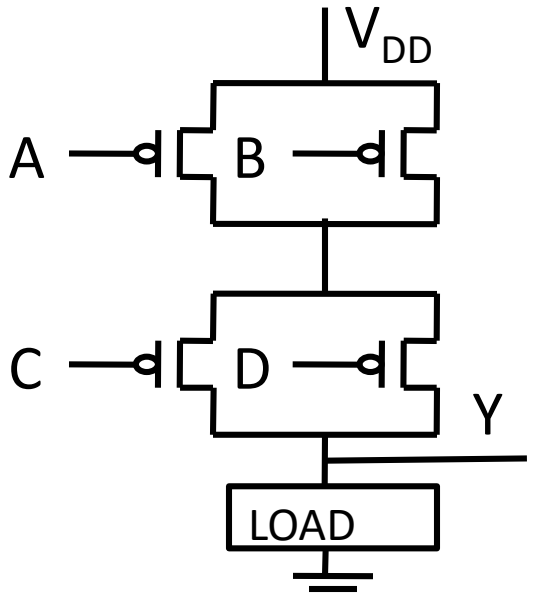
$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

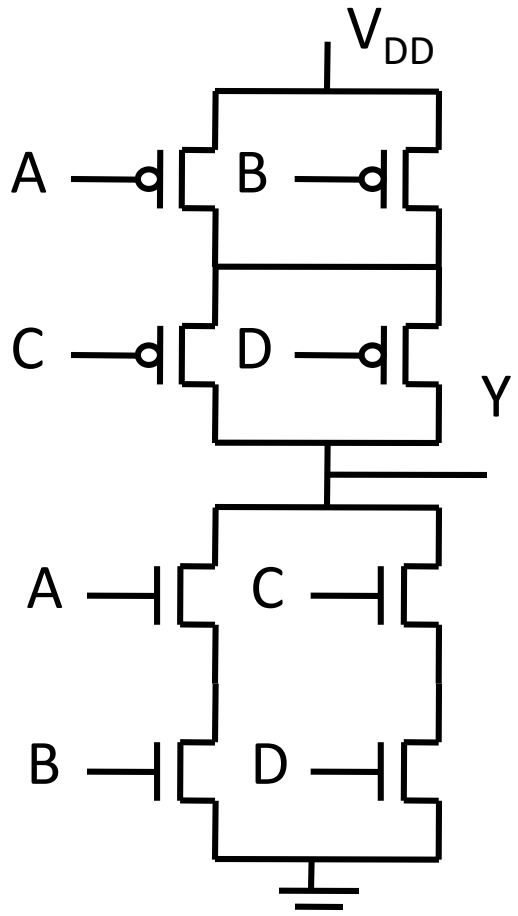


Example:

$$Y = \overline{(A \bullet B) + (C \bullet D)}$$



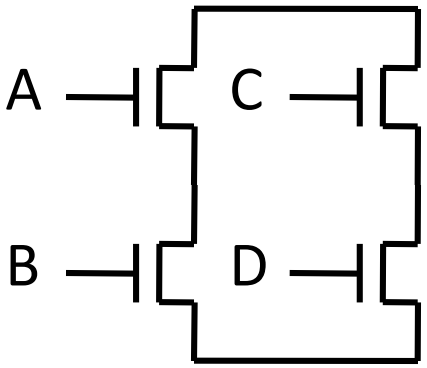




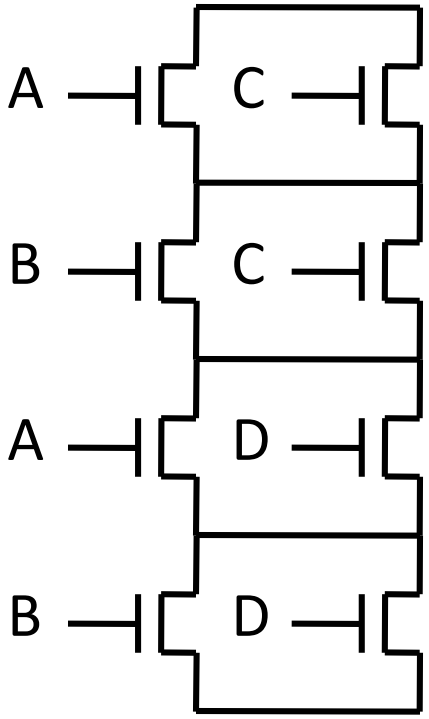
Several Realizations: NMOS

$$Y = \overline{AB + CD} = \overline{\overline{AB} + \overline{CD}} = \overline{(\overline{A}+\overline{B})(\overline{C}+\overline{D})} = \overline{\overline{A}\,\overline{C} + \overline{B}\,\overline{C} + \overline{A}\,\overline{D} + \overline{B}\,\overline{D}}$$

$$= \overline{(A+C)(B+C)(A+D)(B+D)}$$



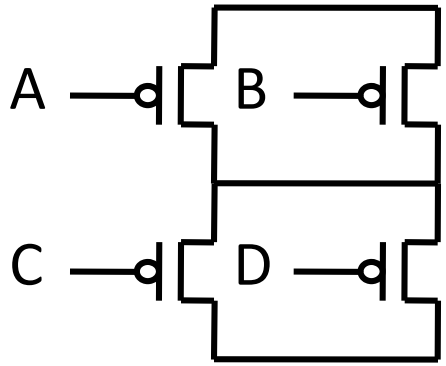
Series-Parallel (SP)



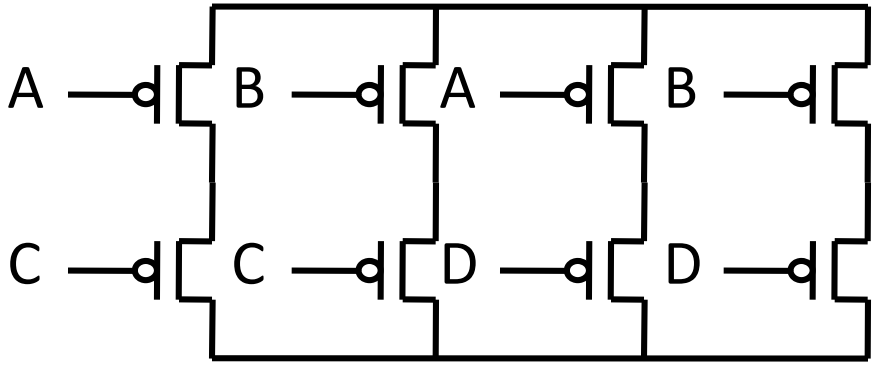
Parallel-Series (PS)

Several Realizations: PMOS

$$Y = \overline{AB + CD} = (\overline{A}+\overline{B})(\overline{C}+\overline{D}) = \overline{A}\,\overline{C} + \overline{B}\,\overline{C} + \overline{A}\,\overline{D} + \overline{B}\,\overline{D}$$

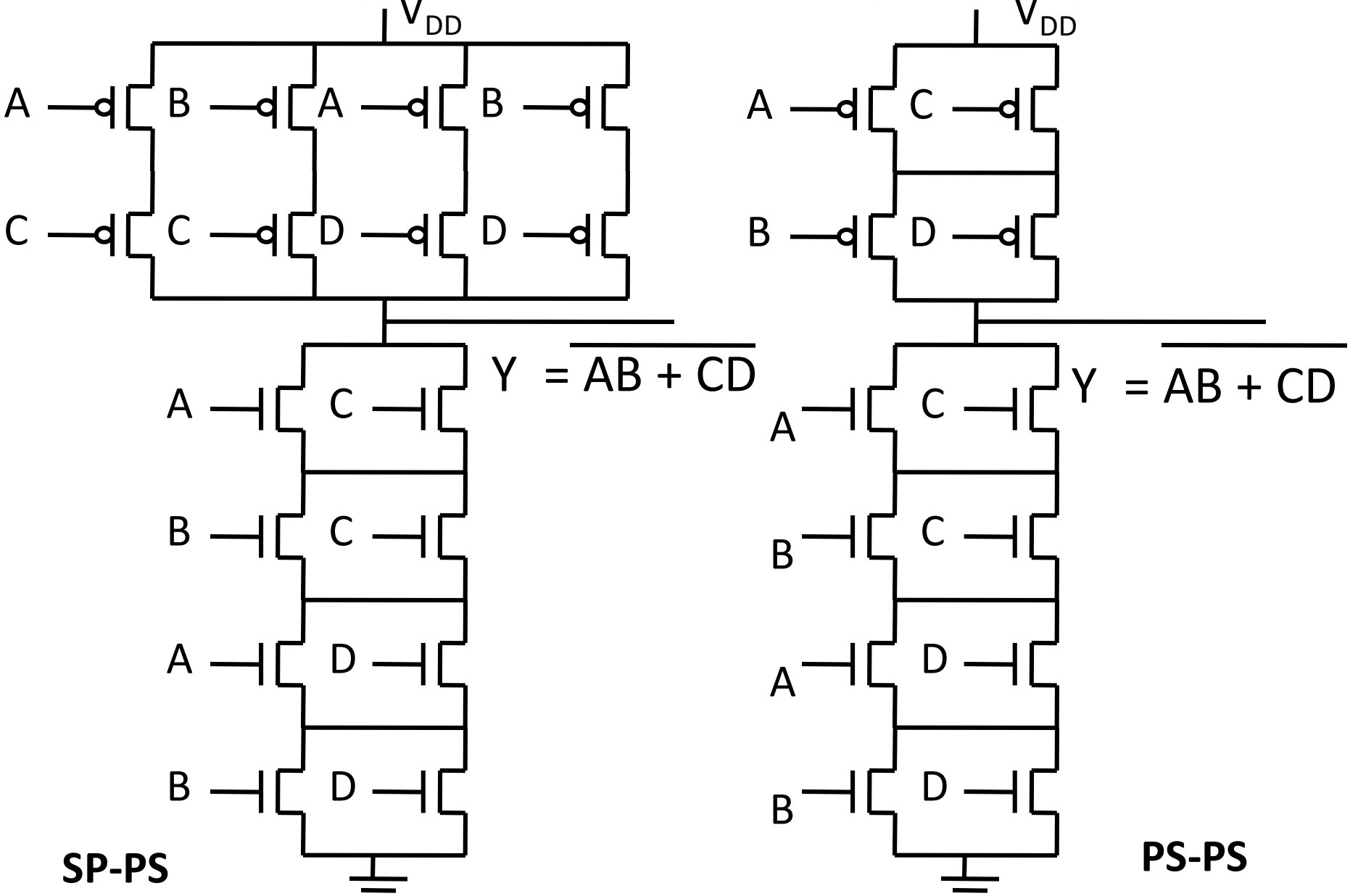


Parallel-Series (PS)

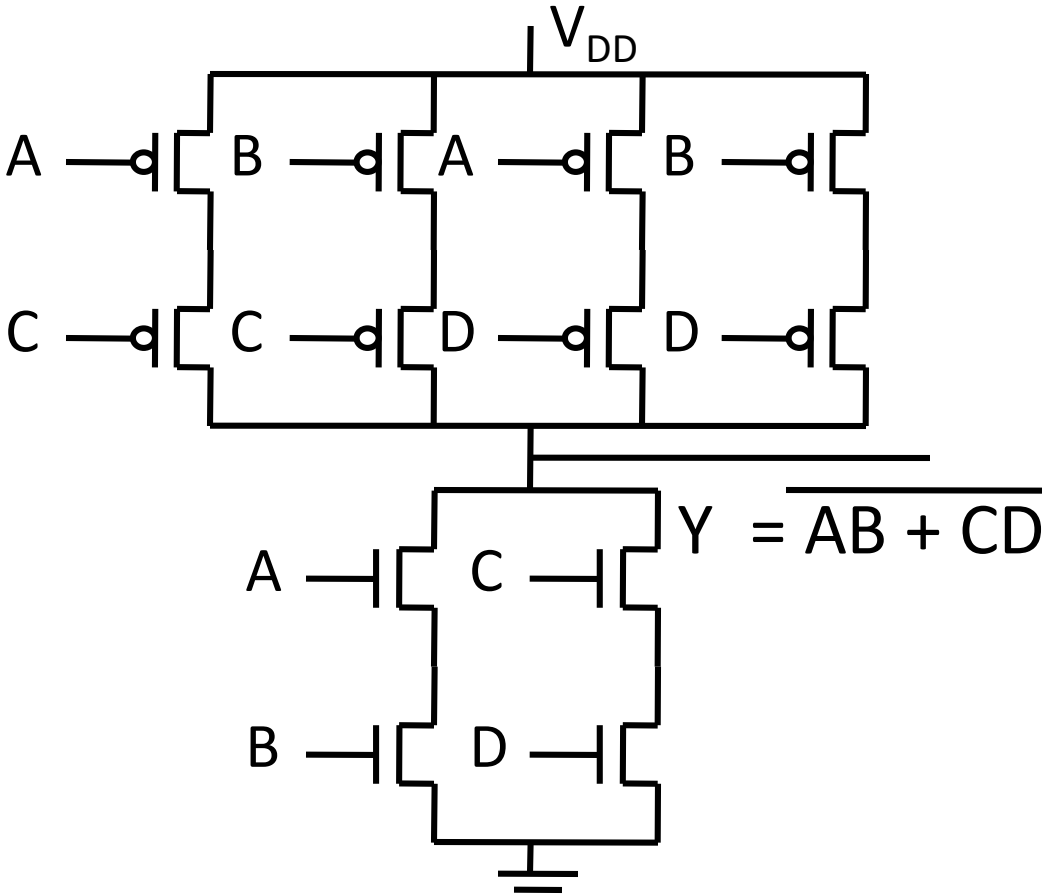


Series-Parallel (SP)

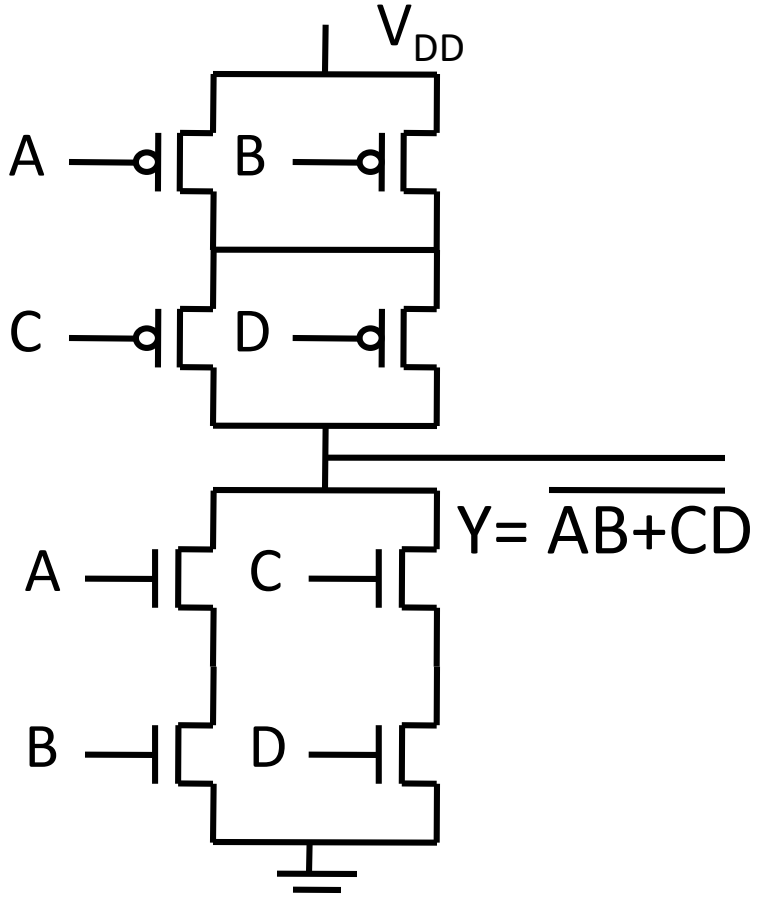
Different single complex cell designs using CMOS



Different single complex cell designs using CMOS



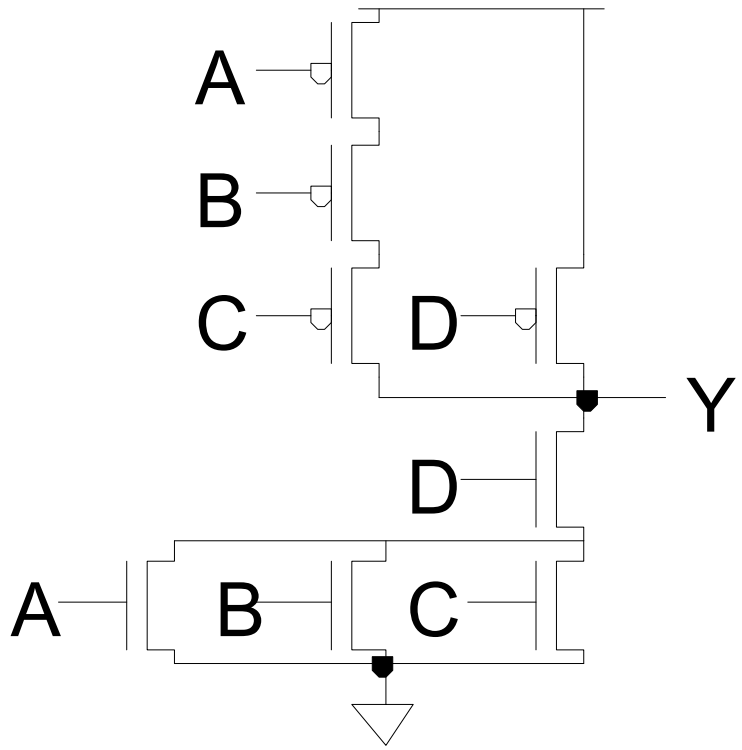
SP-SP



PS-SP

- $$Y = \overline{(AD + BD + CD)}$$

- $Y = \overline{(AD + BD + CD)}$



How to optimize the circuit ?

The question of delay, power, space

Two level gate level optimization

Multilevel gate level optimization

Optimization with respect to transistors

Optimization with respect to space in fabrication of Integrated circuits