BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2013

(3rd Year, 1st Semester)

VLSI DESIGN

Time : Three hours Full Marks : 100

Answer any ***five*** questions with at least ***one*** question from **Group-A**.

GROUP-A

1. a) What is semiconductor?
   b) Explain VLSI design Cycle?
   c) How the silicon wafer is prepared from sand? Explain the steps.
   d) What is the use of polysilicon in fabrication process?
   e) Explain the chemical vapour deposition technique.
   f) What is photoresist? Explain its uses in fabrication process.

   2+5+4+2+4+3

2. a) Deduce the pull-up to pull-down impedance ratio of an ideal CMOS inverter..
   b) Explain the functioning of nMOS inverter considering the load as depletion type transistor.
   c) An nMOS inverter is driven by another nMOS inverter having pull-up to pull-down ratio of 4·75 : 1, through three pass transistors each having threshold voltage of 0·275 VDD . Find the desired ratio of the pullup to pull-down impedance of the driven inverter.

   10+4+6

3. a) Implement the following Boolean function with the help of (i) nMOS (ii) pMOS (iii) CMOS NAND gates (iv) CMOS single complex cell design.

   $$f = A\bar{B} + \bar{A}C + \bar{C}D$$

   b) Draw the coloured stick and mask diagrams for implementing the Boolean function mentioned in question 3 (a) using (i) NMOS (ii) CMOS.

   10+10

GROUP-B

4. a) What are the different levels of partitioning?
   b) Consider a complete binary tree with n nodes. Apply Kernighan-Lin (K-L) algorithm to this graph. As the initial partition, let v_a, for all internal vertices, be in one set and v_b, for all leaves, be in the other set.
   c) What are the drawbacks of Kernighan-Lin algorithm?
   d) State the similarities between Fiduccia-Mattheyses algorithm and K-L algorithm.

   4+10+3+3

5. a) State with an example how a sliceable floorplan can be represented by a binary tree.
   b) Obtain a rectangular dual of the following adjacency graph (Fig.1).

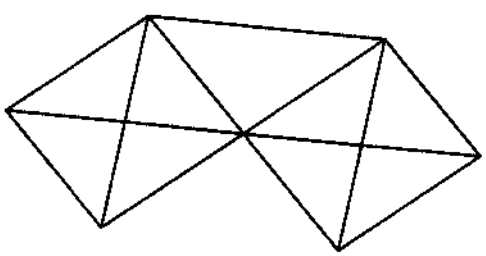

Fig.1

   c) How do you estimate the cost of floorplan. Consider the adjacency graph of Fig.2 where the edge weights are providing the distance between two vertices. Estimate the routing cost in different sliceable florplans for it.

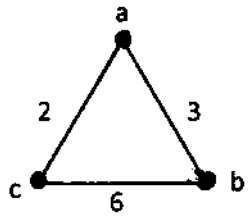

Fig. 2

d) State the advantages of integer linear programming technique in case in floorplanning.

3+7+7+3

6. a) Formulate the placement problem.
   b) State two different approaches in Force directed algorithm. What are pros and cons of Force directed algorithm?
   c) Explain the different procedures for Breuer's Algorithm. What are pros and cons of Breuer's algorithm?

3+7+10

7. a) Formulate the placement problem.
   b) State two different approaches in Force directed algorithm. What are pros and cons of Force directed algorithm?
   c) Explain the different procedures for Breuer's Algorithm. What are pros and cons of Breuer's algorithm?

3+7+10

8. a) Explain the different graph models used in Global Routing.
   b) Give an example or counter example as the case may be for the following statement: Soukup's maze router always produces the shortest path.
   c) Give an example for which Hightower line-probe algorithm does not find a path even when path exists between the source and the target.
   d) Explain the Steiner tree based routing for multi-terminal nets.
   e) Explain Detailed routing.

4+4+5+5+3

9. a) Route the following channel using any suitable algorithm.

   TOP = 3 4 0 1 2 4 3 5 2 1 0

   BOT = 1 0 3 0 4 0 5 2 1 4 5

   b) Get the solution for unconstrained via minimization for the following graph (Fig. 3).
   c) Constraints in placing modules are shown (Fig.4). How will you compact the design?

8+6+6

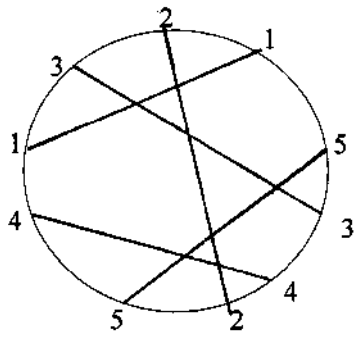

Fig. 3

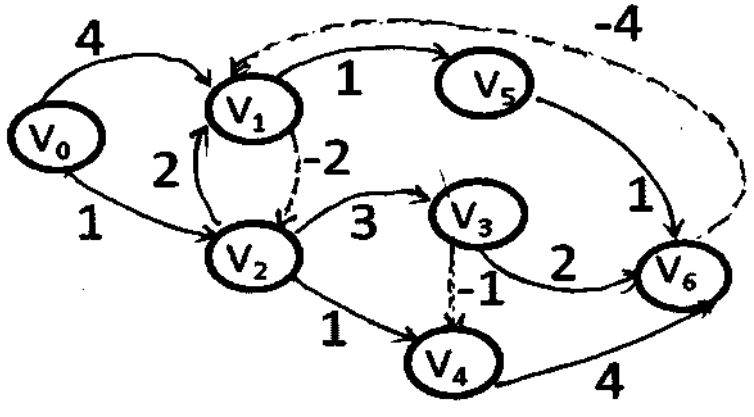

Fig. 4