Ex/CSE/T/314/13/2011

# BACHELOR OF COMPUTER SCIENCE ENGINEERING EXAMINATION, 2011

( 3rd Year, 1st Semester )

## VLSI DESIGN

Time : Three Hours Full Marks - 100

Answer any **Five** questions

1. a) Prove that the ratio of impedances of the pull-up to pull-down transistors of a MOS inverter is 4 : 1.

   b) What will be the actual value of $\frac{Z_{pu}}{Z_{pd}}$ of a MOS inverter driven by another MOS inverter leaving ratio of $\frac{Z_{pu}}{Z_{pd}}$ 4.75:1 through two pass transistors? The threshold voltage $V_{th}$ of a MOS transistor is 0.25 $V_{DD}$ and threshold voltage $V_{tp}$ of each pass transistor is 0.34 $V_{DD}$. 12+8

2. a) Discuss about the operations of precharge NMOS and CMOS logic gates.

   b) Implement the following Boolean functions with the help of a precharge NMOS circuit :

   $f(a,b,c,d) = a\bar{b}c + \bar{a}cd + \bar{b}\bar{d}$

   c) Implement the following Boolean function with the help of precharge CMOS circuit :

   $f(w,x,y,z) = \bar{w}xy + y\bar{z} + \overline{xy}$ 2x4+6+6

**[ Turn over**

3. a) Explain the operation of a 'DOMINO' logic.

b) Draw the coloured stick and mask diagrams (conforming to the λ-based design rules) for implementing the following Boolean functions, as per instruction given against each :

i) $f(w,x,y,z) = (x + y + \bar{z})(w + \bar{x} + \bar{y})$

[using precharge NMOS circuit].

ii)

[using CMOS circuit]

Note : Assume that the variables and their complements are availabnle. 6+2x4+2x3

4. a) State with colour diagrams the λ-based IC design rules of the following :

i) Implant dimension of a depletion mode NMOS transistor.

ii) Width and separation between two n diffusions.

iii) Separation between two wells having different potentials.

iv) Width and separation between two metal 1 layers.

b) Draw the circuit diagram of a 3 input BiCMOS MOR gate and explain its operation. (3x4+8)

5. a) What is the significance of a HDL in VLSI design?

b) Give the VHDL beleavovial and structural descriptions of the following :

$f(a,b,c,d) = a\bar{b}c + \bar{a}c\bar{d}$



i) A two-bit equality detector.

ii) A master-slave J-K flip-flop leaving present ($P_r$) and clear (Cl) facilities. 5+8+7

6. a) Discuss the following placement/routing algorithms used for VLSI design :

i) MAZE

ii) Dog-leg

iii) Min-cut

b) Draw and explain the operations of an inverting and a non-inverting 'super Buffers'. (5+4+5+2x3)

7. Write short notes on any **four** of the following :

i) Wafer preparation and cleaning.

ii) FPGA

iii) Silicon gate technology.

iv) Silicon on Insulator technology.

v) Testability.

v) Polysilicon etching. 4x5