

Question and answers

Class-Test 1

1. What is Moore's Law?

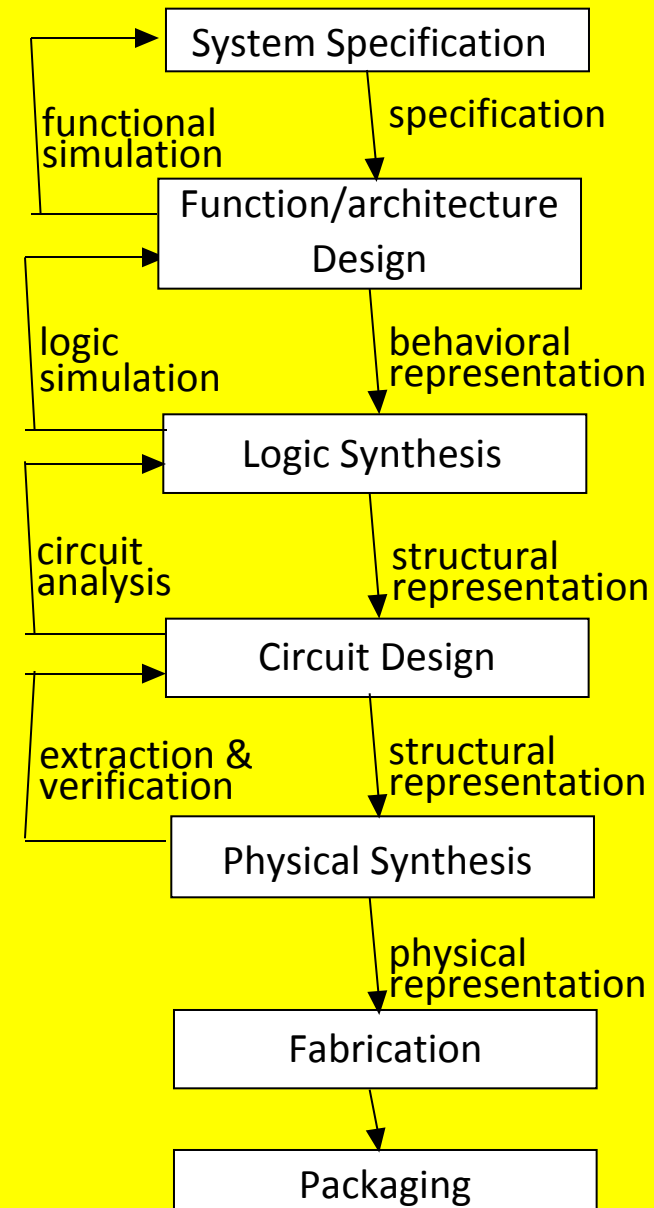
Gordon Moore: 1965

- Predicted that the number of transistors integrated on a die would grow exponentially (doubling every 12 to 18 months) **slide-19, lecture 1**

2. What is VLSI design Cycle?

Slide-8 , lecture-2

VLSI Design Flow



3. What is semiconductor? State one disadvantage of Silicon over Germanium in the use of chip designing.

semiconductors are materials which have a conductivity between conductors and nonconductors or insulators

slide-2, lecture 3

Silicon Disadvantages

Low carrier mobility

Indirect bandgap:

Weak absorption and emission of light

Most optoelectronic applications not possible

Slide-40, lecture-4

5. What is the use of polysilicon in fabrication process?

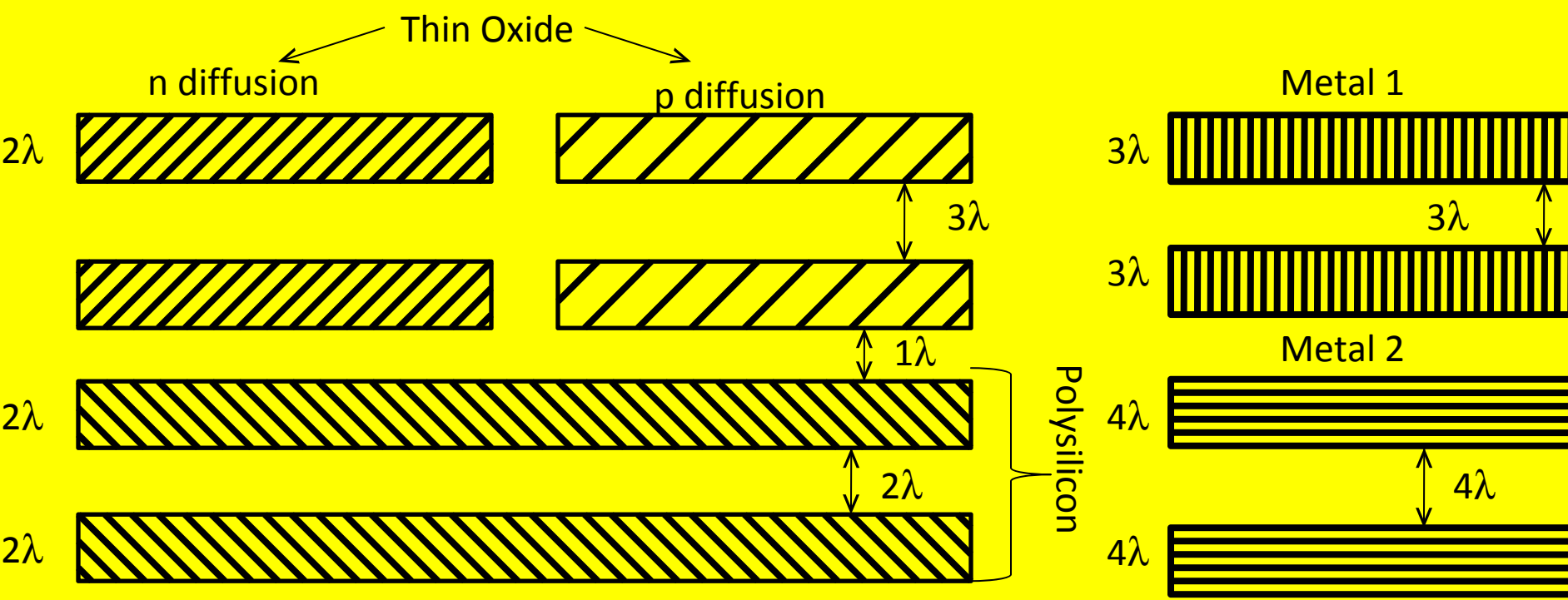
Polysilicon interconnects are used to connect Gates and other short-distance connections which have minimal currents. Polysilicon is a very stable material that rarely interacts with nearby materials.

Slide-19 Lecture-6

7. Compare CMOS versus bipolar technology

CMOS	Bipolar technology
<ul style="list-style-type: none"> - Low static power dissipation - High input impedance (low drive current) - High noise margin - Medium speed – high voltage swing - High packing density - High delay sensitivity to load (fan-out limitations) - Low output drive current - Low transconductance (output current changes slowly with change in V_{in}: $g_m \propto V_{in}$) - Bidirectional capability (drain and source interchangeable) - A near ideal switching device - Mask levels 12 to 16 	<ul style="list-style-type: none"> - High power dissipation - Low input impedance (high drive current) - Medium noise margin - High speed – low voltage swing - Low packing density - Low delay sensitivity to load - High output drive current - Low transconductance (output current changes rapidly with change in V_{in}: $g_m \propto e^{V_{in}}$) - Essentially unidirectional with hole as carrier - Not ideal switching device - Mask levels 12 to 20

9. State nMOS design rules



Basic nMOS design Rules

Different widths	Value
Diffusion Region width	2λ
Polysilicon region width	2λ
Diffusion-Diffusion spacing	3λ
Poly-Poly spacing	2λ
Polysilicon gate extension	2λ
Contact extension	λ
Metal width	3λ