Ex/CSE/T/314/13/2014

BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2014
(3rd Year, 1st Semester)
VLSI DESIGN

Time : Three hours Full Marks : 100

Answer any ***five*** questions

1. a) How do you define LSI and VLSI? What is Moore's law?
   b) Compare Silicon versus Germanium in the use of chip designing.
   c) Explain VLSI design Cycle.
   d) What are the advantages and disadvantages of CMOS over MOSFET?
   e) Explain lithography.

   3+3+6+3+5

2. a) Prove that the ratio of impedances Z_{pu} and Z_{pd} of the pull-up to pull-down transistors of an nMOS inverter is 4 : 1.
   b) What is the significance of finding the ratio Z_{pu}/Z_{pd}?
   c) An n MOS inverter is driven by another nMOS inverter having pull-up to pull-down ratio of 4.50:1, through 3 pass transistors each having threshold voltage of 0.265 V_{DD}. Find the desired ratio of the pull-up to pull-down impedance of the driven inverter.
   d) What is photoresist? Explain its uses in fabrication process.

   10+2+5+3

3. a) Implement the following Boolean function with the help of (i) nMOS (ii) pMOS (iii) CMOS NAND gates (iv) CMOS single complex cell design.

   $Y=ab+bd+cd$

   b) Draw the coloured stick and mask diagrams for implementing the Boolean function mentioned in question 3 (a) using (i) NMOS (ii) CMOS.

   10+10

4. a) Explain physical design cycle.
   b) Why do we need partitioning? What are the different levels of partitioning?
   c) Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices (Fig.1), starting with initial partition of $V_1= \{1,2,3,\ldots\ldots,n\}$, and $V_2=\{n+1,n+2,n+3,\ldots..,2n\}$. Consider n as odd.
   d) What are the drawbacks of Kernighan-Lin Heuristic.

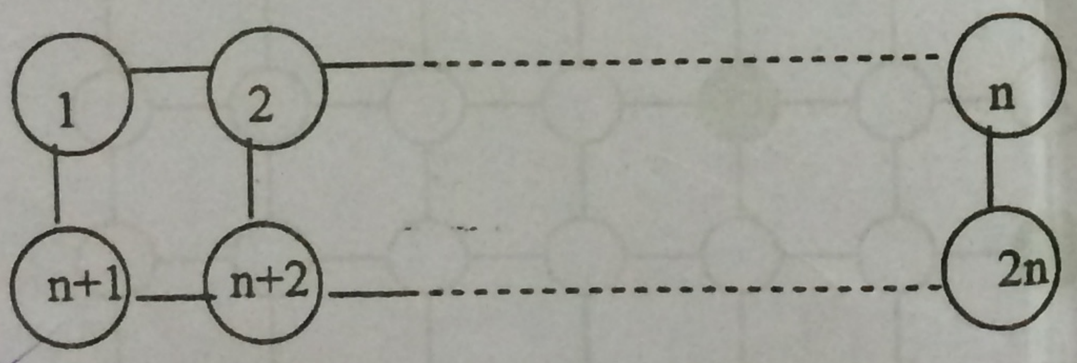

Fig.1

   5+4+8+3

5. a) State the floorplan optimization problem.
   b) Define sliceable and non-sliceable floorplan with examples. What are the advantages of sliceable floorplan?
   c) Explain the simulated annealing approach in Floorplanning problem.

d) Obtain a rectangular dual of the following adjacency graph (Fig. 2).

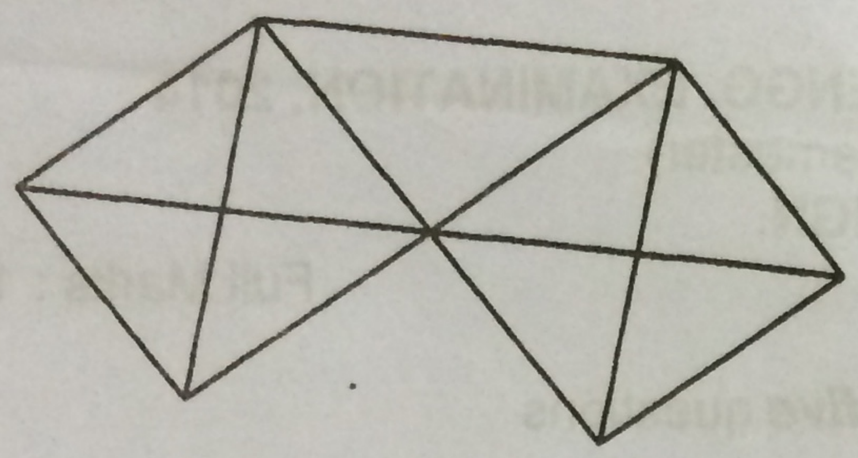

Fig.2

2+5+6+7

6. a) State the consequences and importance of placement in VLSI Design
   b) Explain the Force directed Placement algorithm with its prospects and consequences.
   c) Explain the different procedures for Breuer's Algorithm.

4+8+8

7. a) Explain Global Routing and Detailed Routing.
   b) Fig. 3 shows a grid graph with several blocked vertices. It also shows terminals s and t as source and target of a two-terminal net. Use Lee's algorithm to find the path for this net.
   c) Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty position. TOP = 3 4 0 1 2 4 3 5 2 1 0
   BOT = 1 0 3 0 4 0 5 2 1 4 5

4+8+8

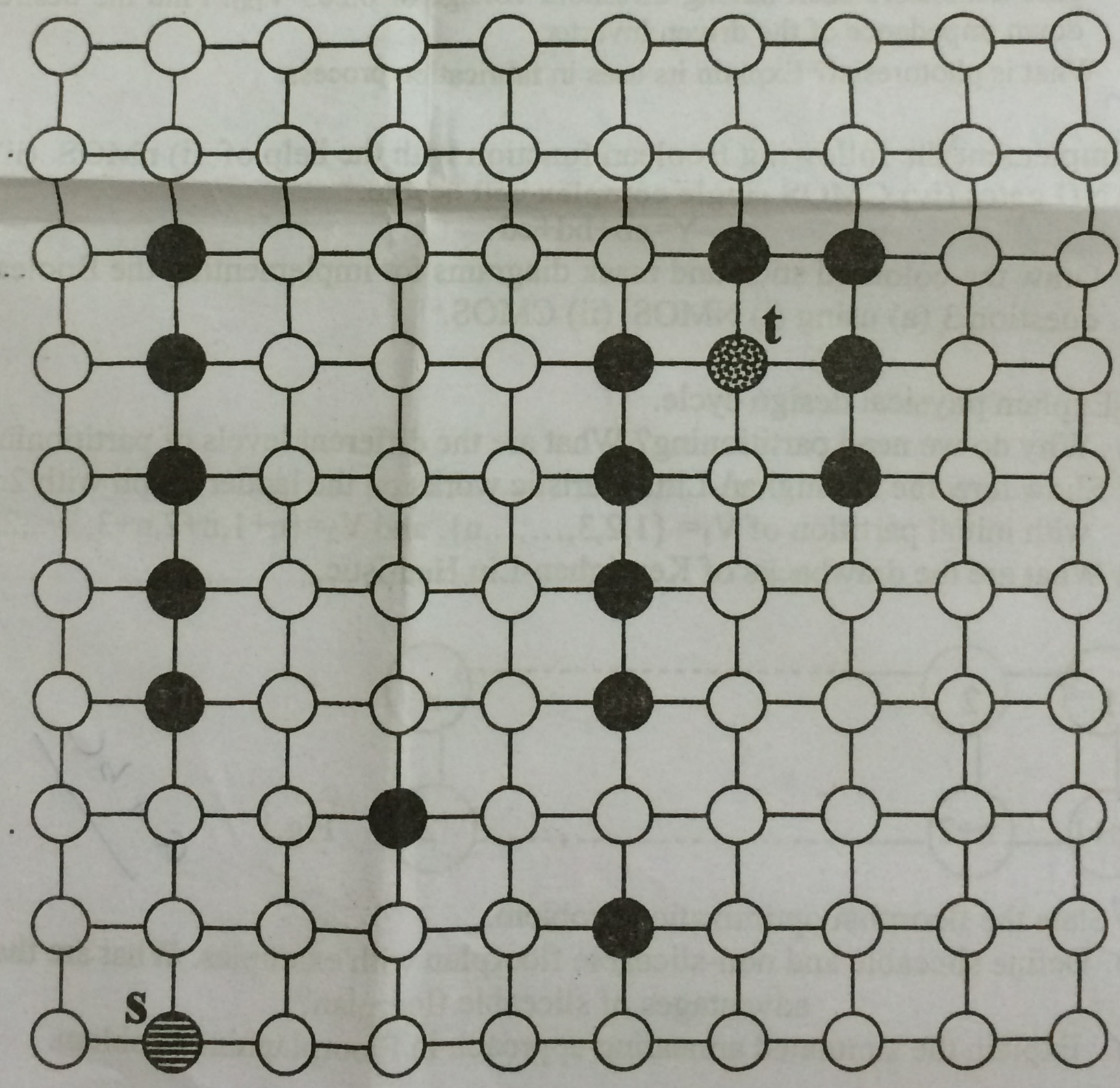

Fig. 3