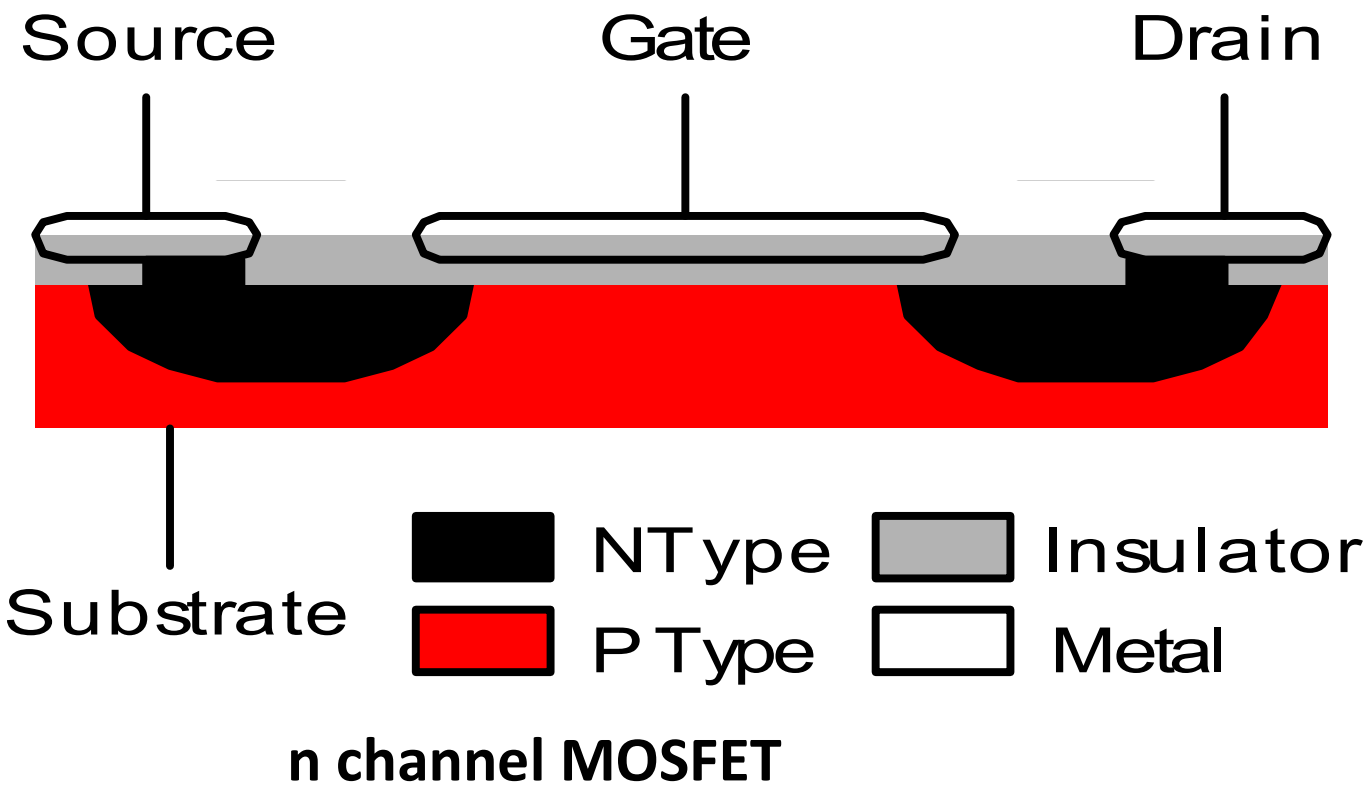
Metal Oxide Semiconductor Field-Effect Transistor

MOSFET: Metal Oxide Semiconductor Field-Effect Transistor



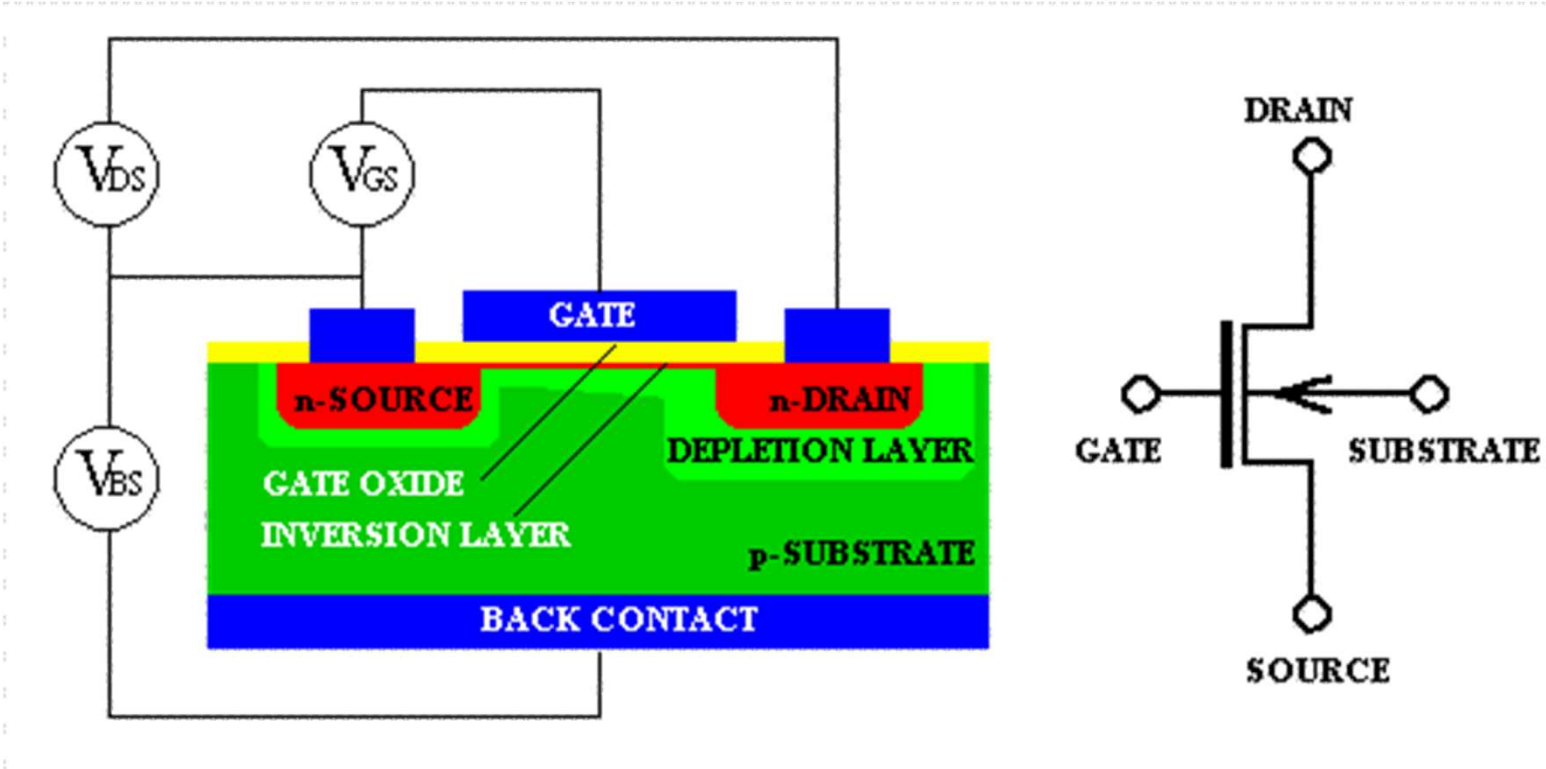
n channel MOSFET

In lightly doped p-type substrate, two highly doped n regions (source and drain) are diffused

Insulator is grown over surface and holes are cut into it to have contact with source and drain

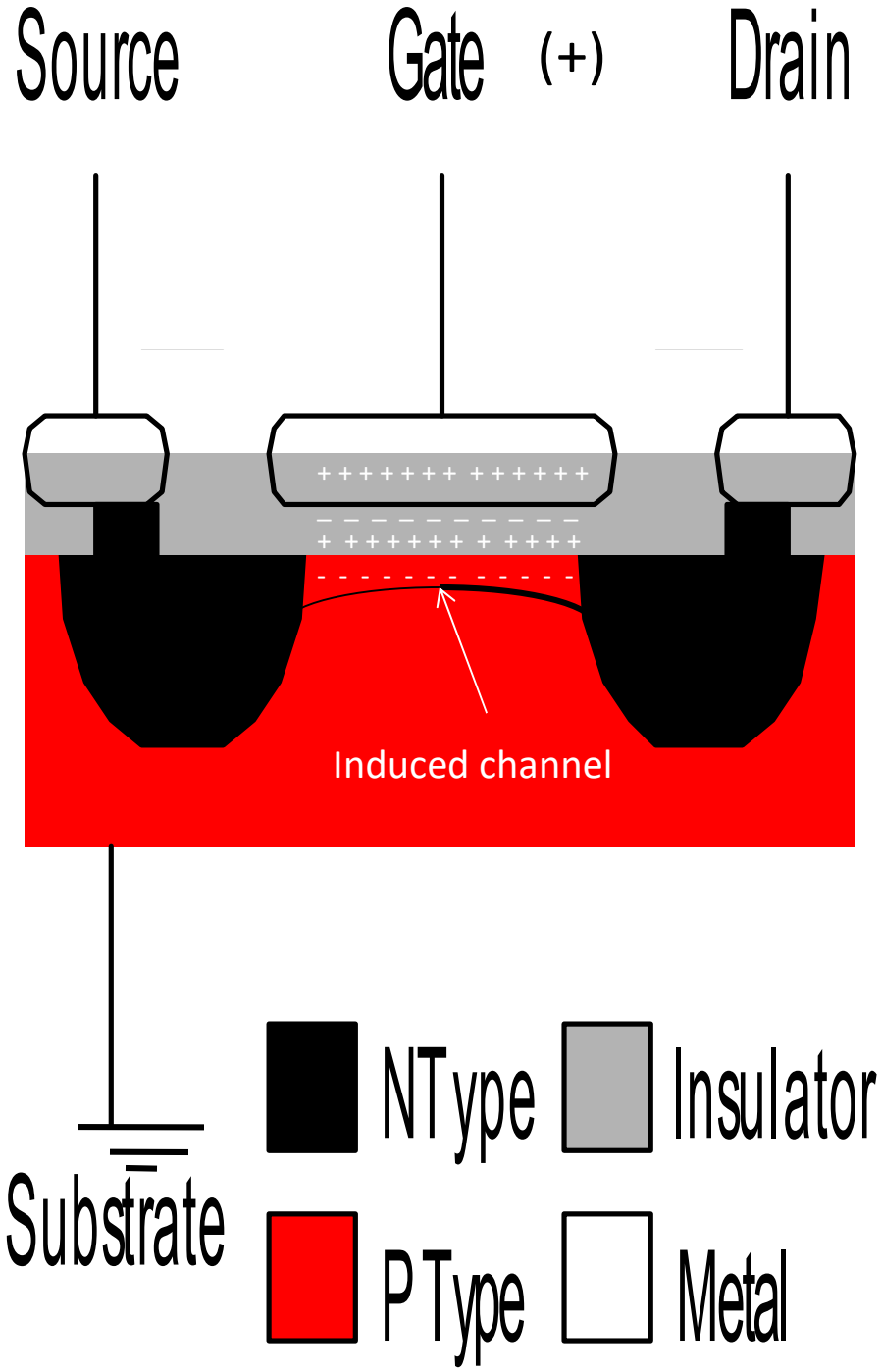
For Si substrate, SiO_2 is used as the Insulator

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)



n-channel

MOSFET operation



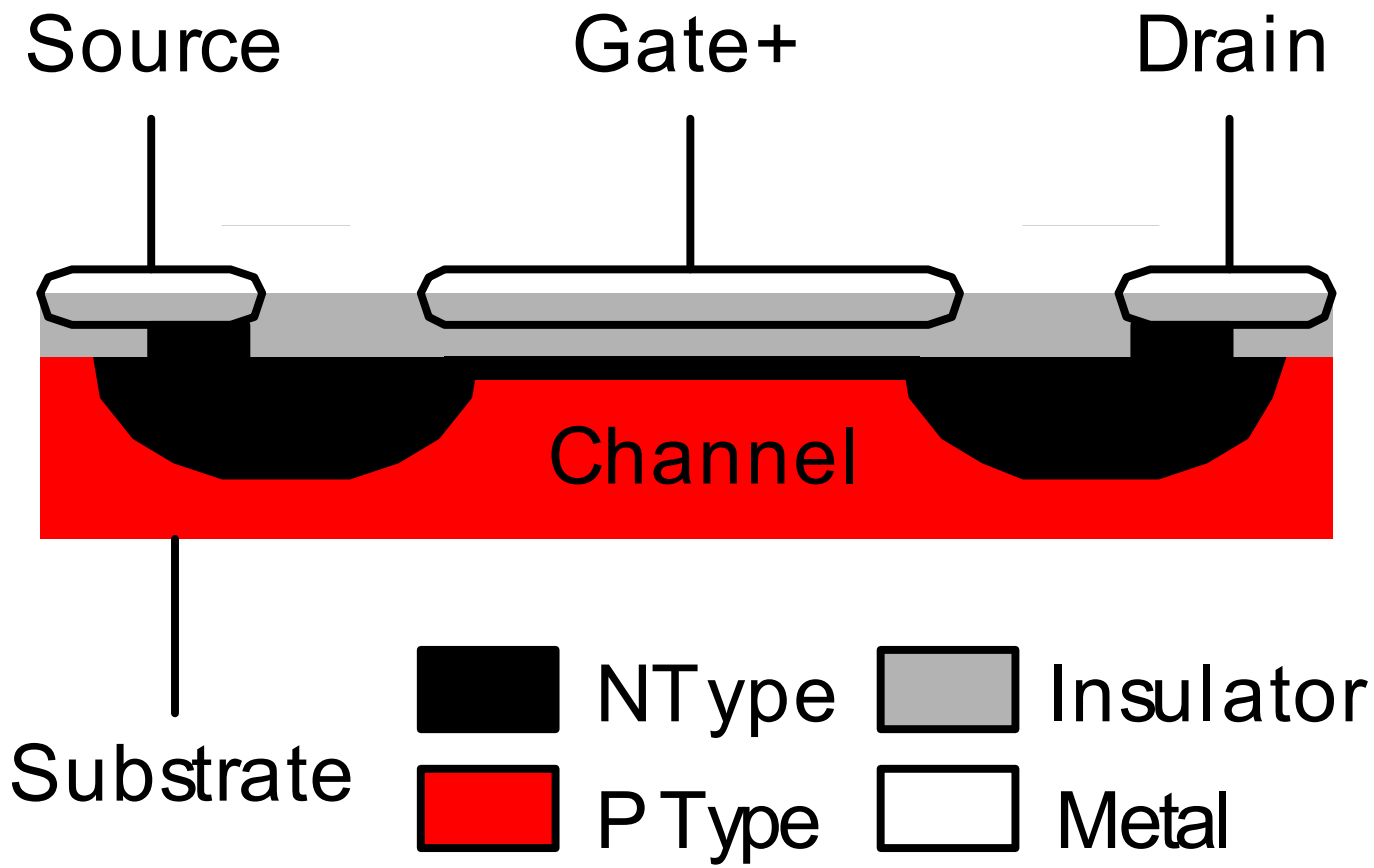
Substrate: Grounded
Gate : + ve voltage

An electric field is directed perpendicularly through oxide

Negative charge is induced on semiconductor

A channel is formed between drain and source

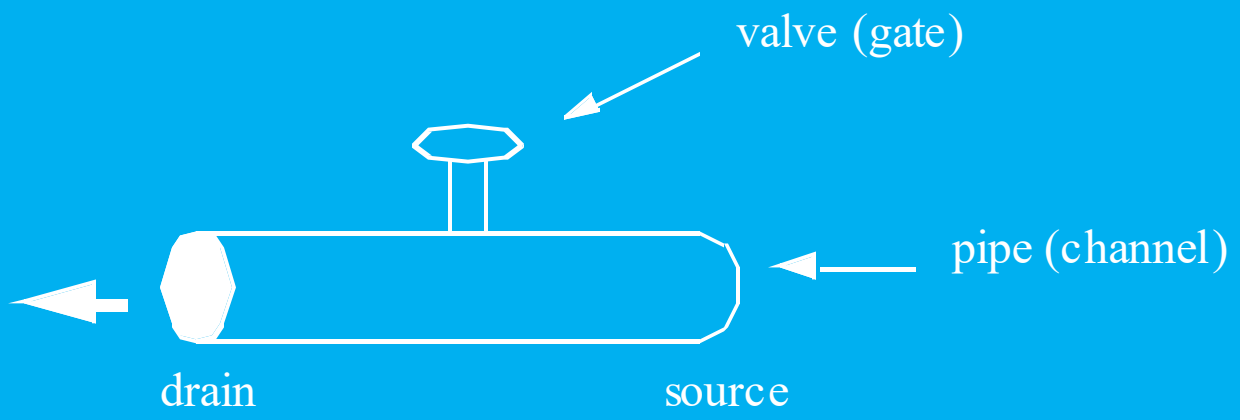
Width of channel depends on gate voltage



Electrons may flow through Channel

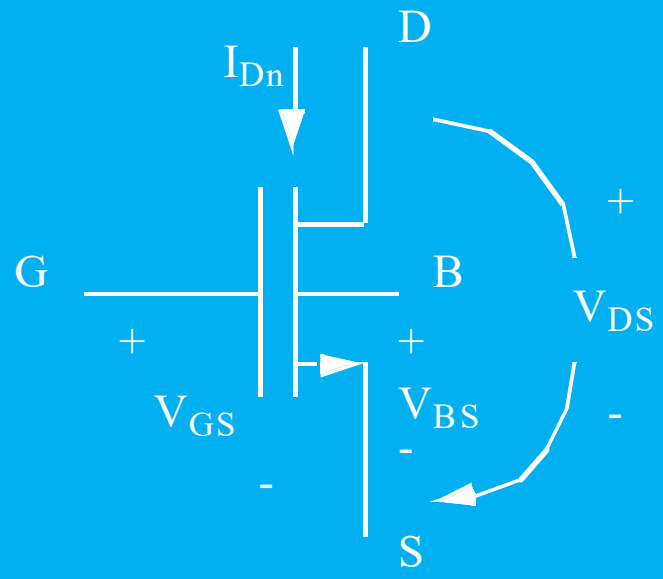
Basic Operation

1) Source and substrate grounded (zero voltage)
2) (+) voltage on the gate
   - Attracts e^-s to Si/SiO2 interface; forms channel
3) (+) voltage on the drain
   - e^-s in the channel drift from source to drain
   - current flows from drain to source

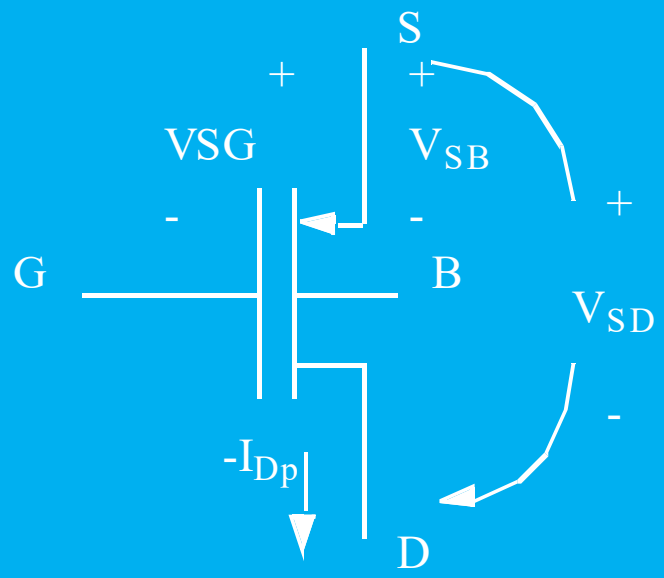


MOSFET

- Metal-oxide-semiconductor field-effect transistor



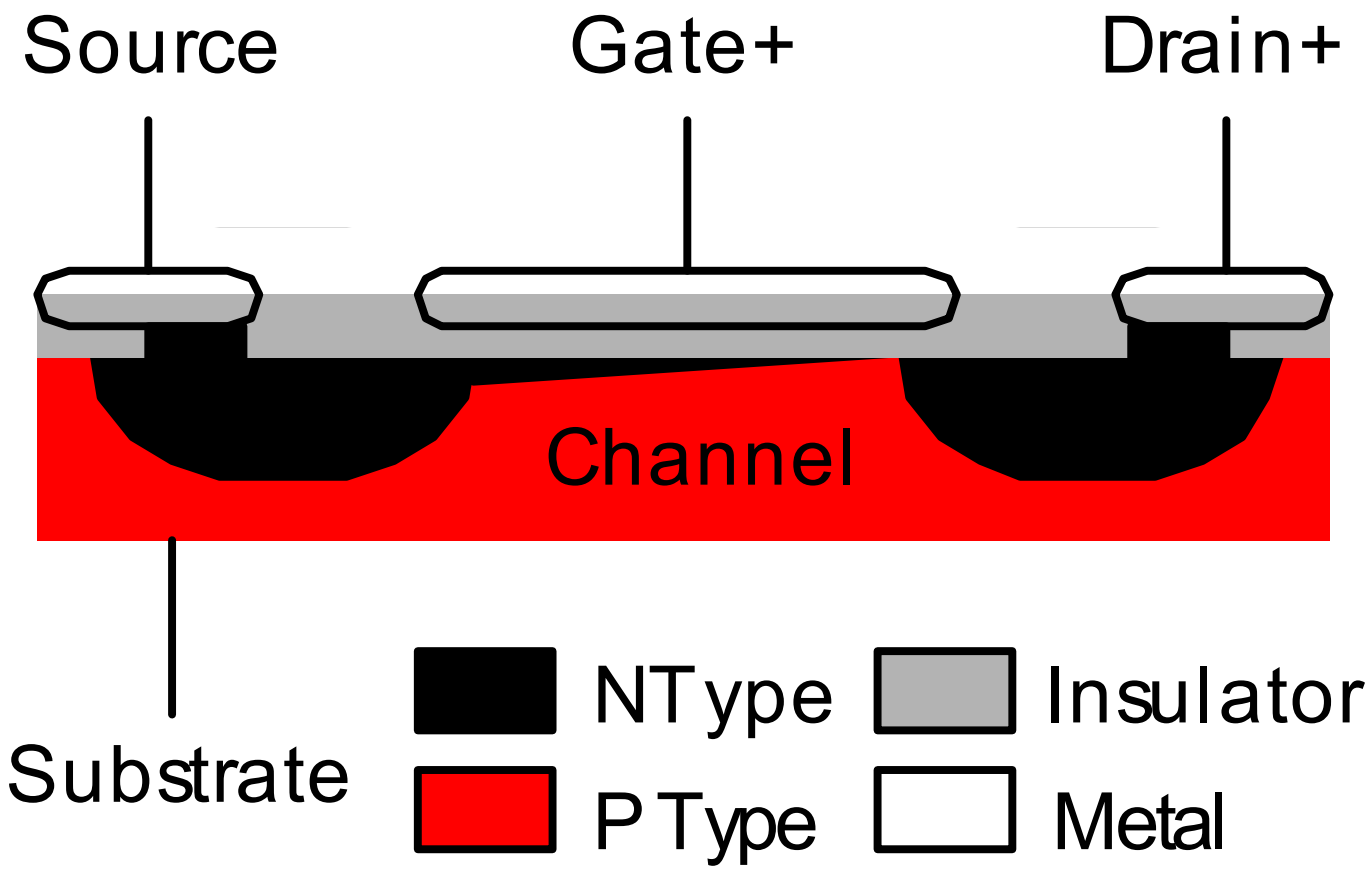
n-channel device



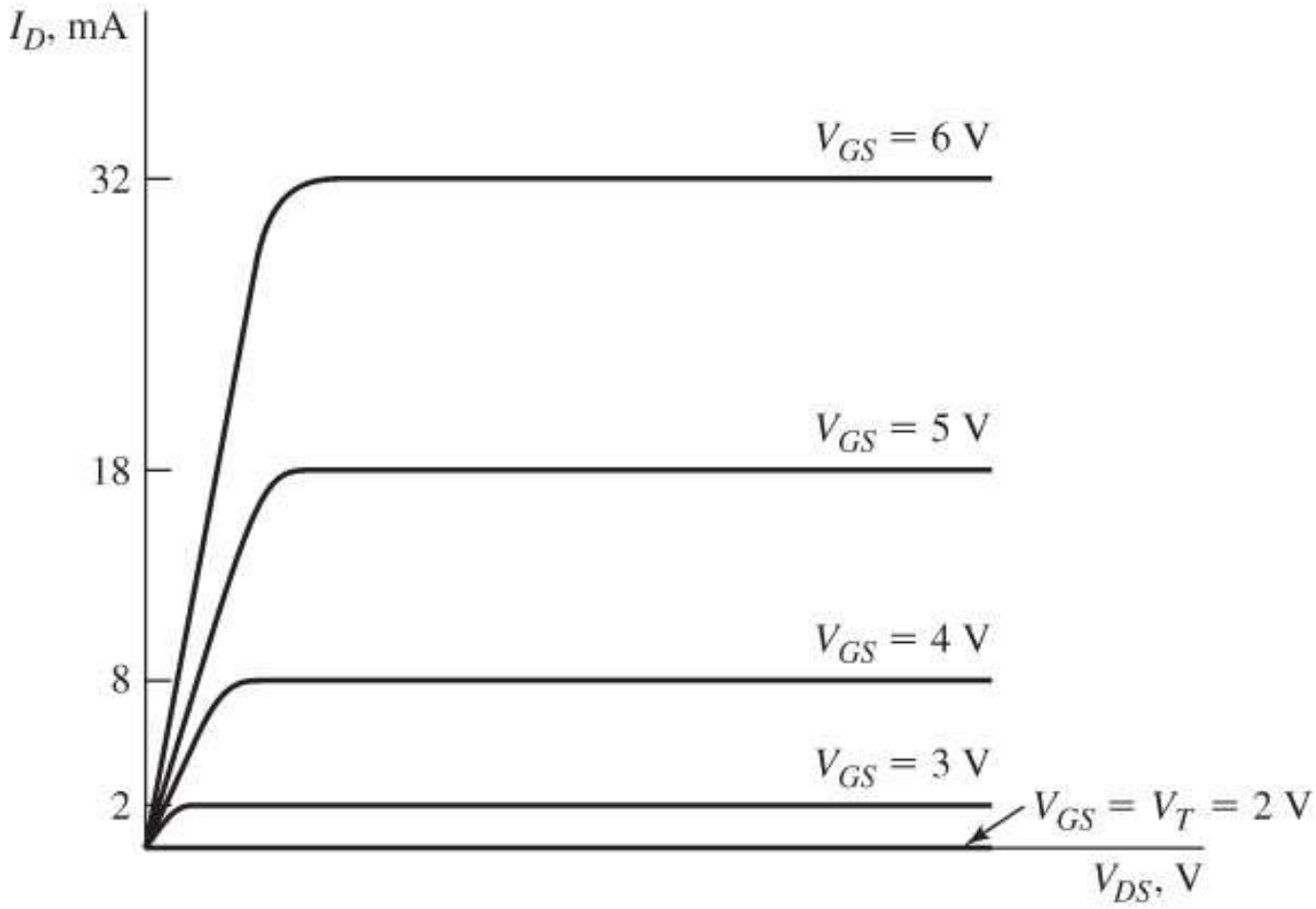
p-channel device

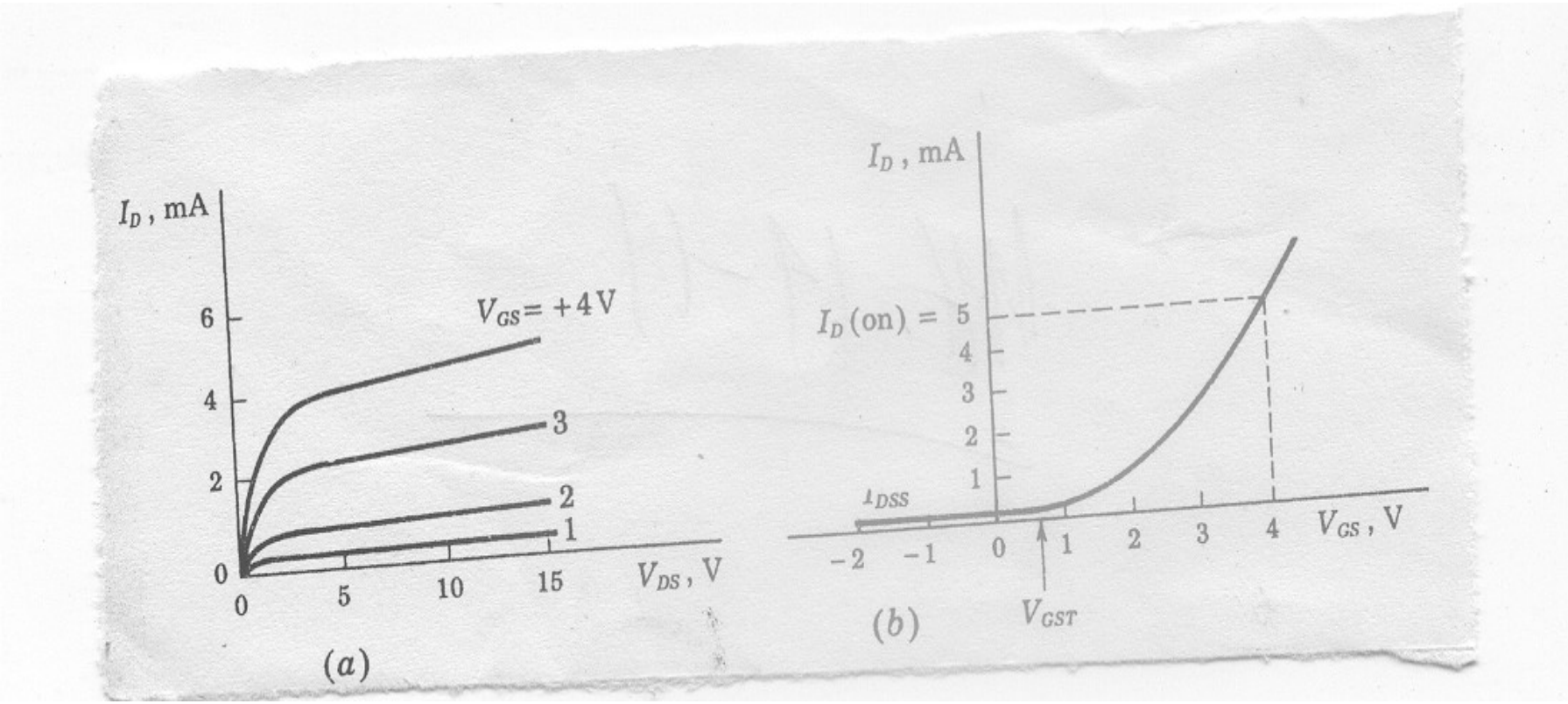
G = gate, D = drain, S = source, B = body (substrate)

N enhance FET at Pinchoff



Drain characteristics for an ideal representative N-channel enhancement-mode MOSFET.



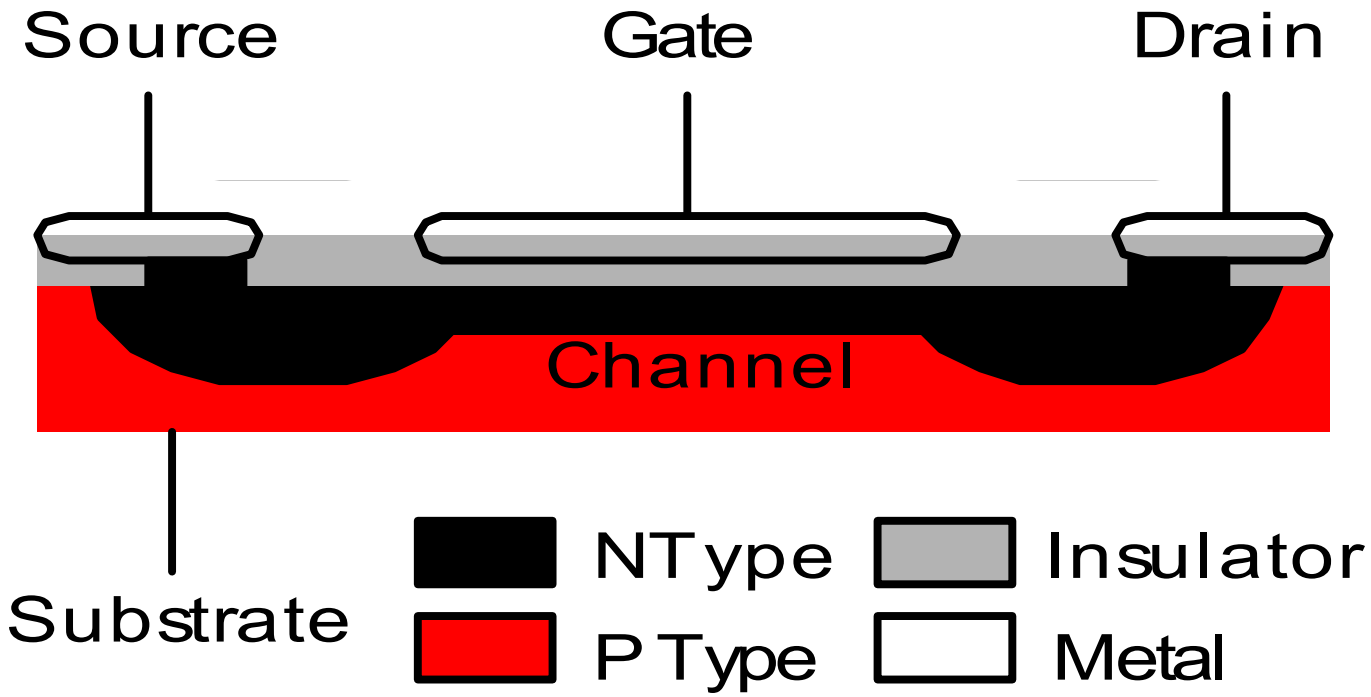


(a) I_D versus V_{DS} (b) I_D versus V_{GS} for a fixed V_{DS}

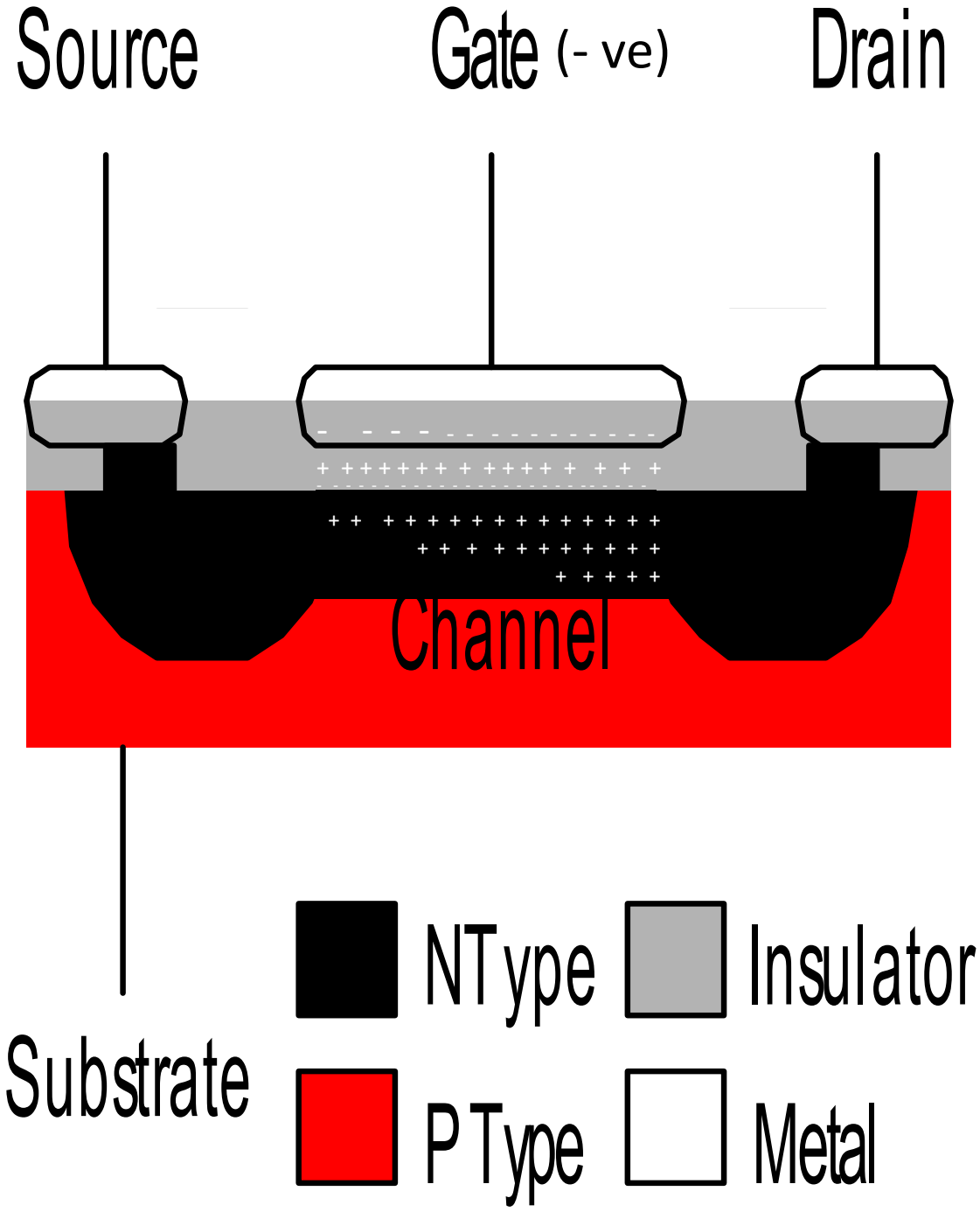
As V_{GS} is made positive I_D increases slowly at first and then much rapidly

I_D reaches significant value (some predefined small) at threshold voltage

N channel Depletion mode FET
ON – No gate bias



A channel is diffused between source and Drain



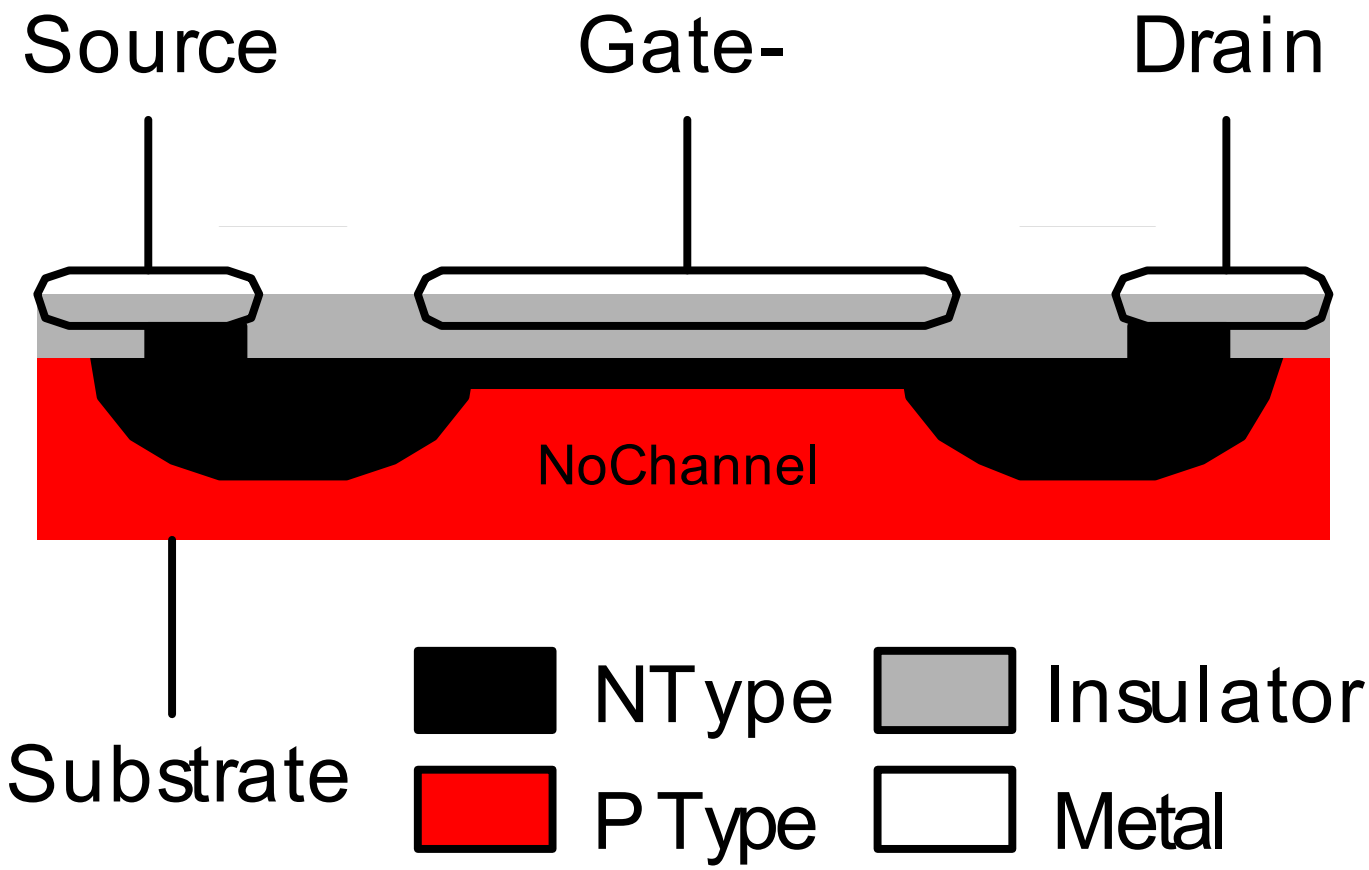
Channel Depletion with application of negative voltage

Induced +ve charge makes the channel less conductive

Causes effective depletion of majority carriers

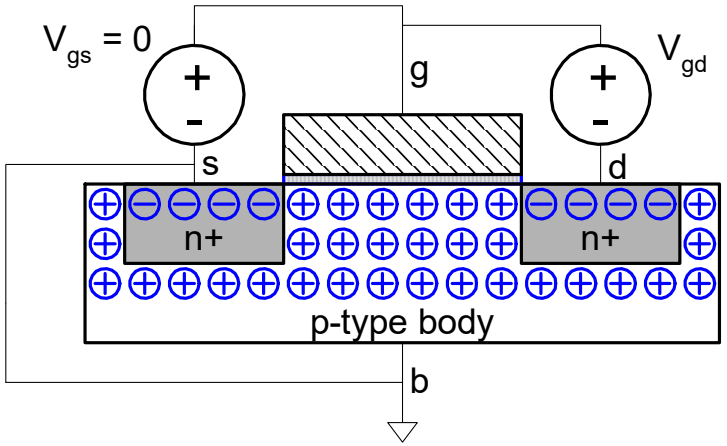
Analogous to JFET characteristics

N channel Depletion mode FET off



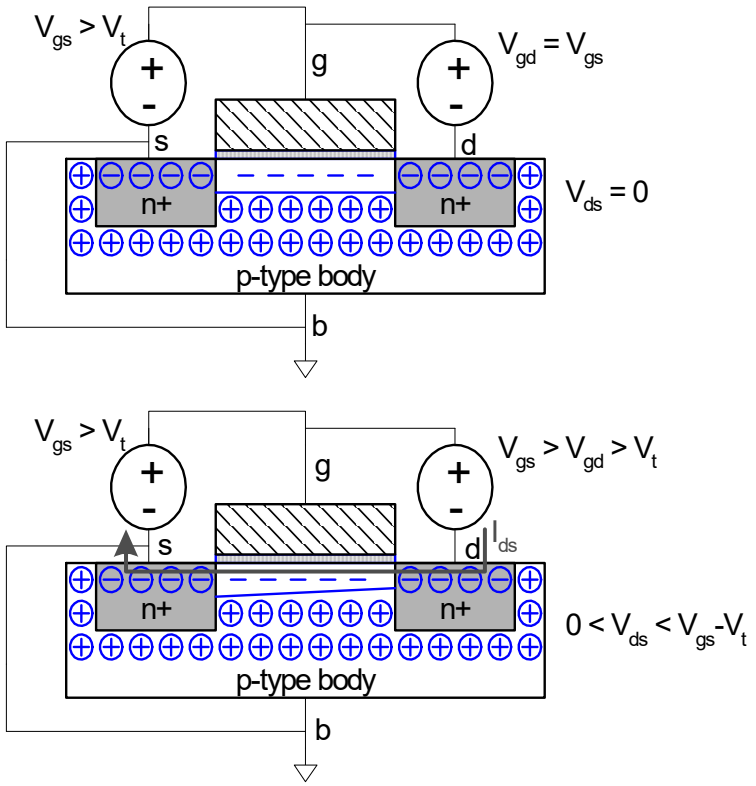
nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



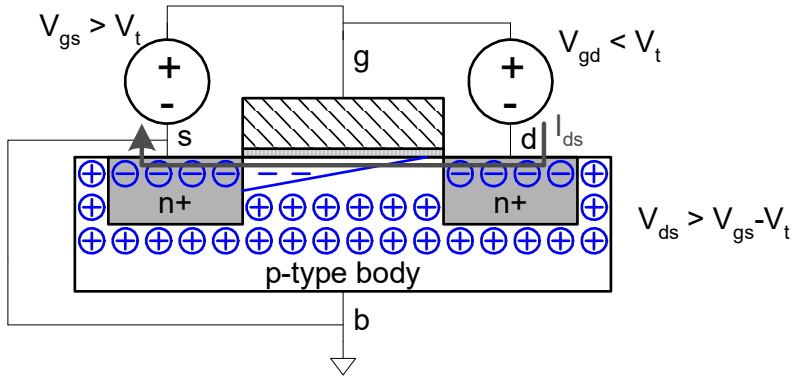
nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



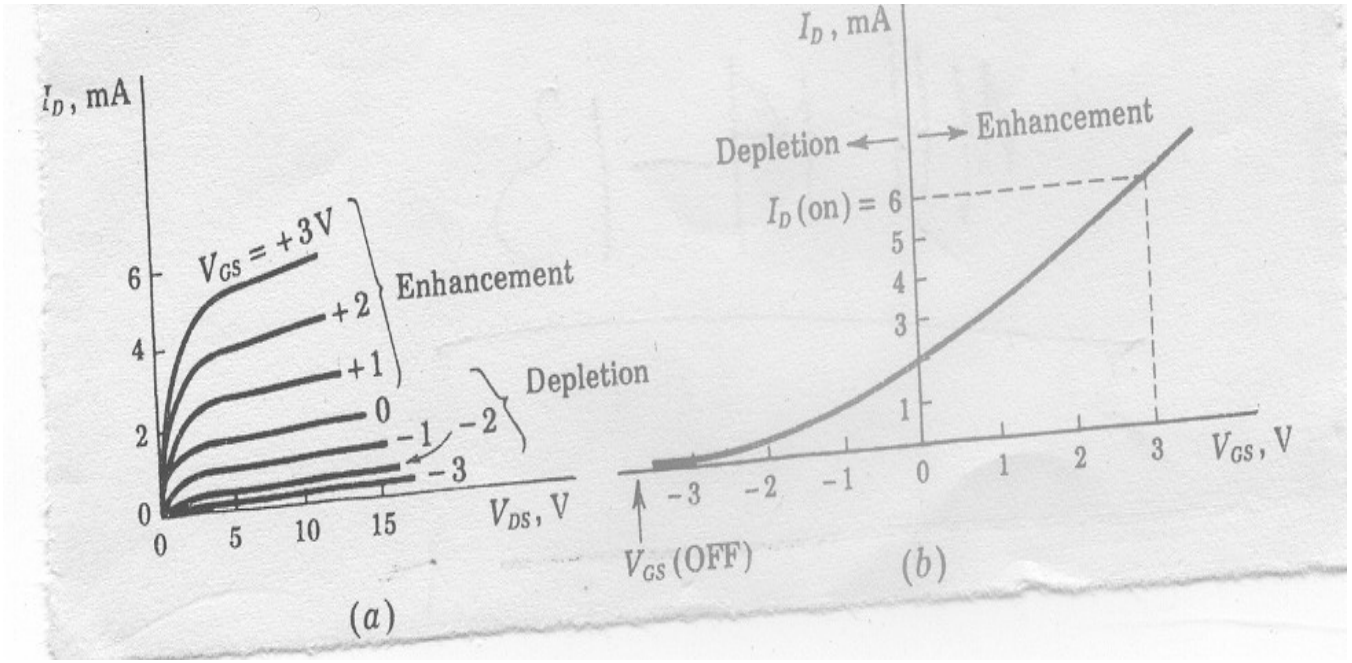
nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source



N channel Depletion mode MOSFET

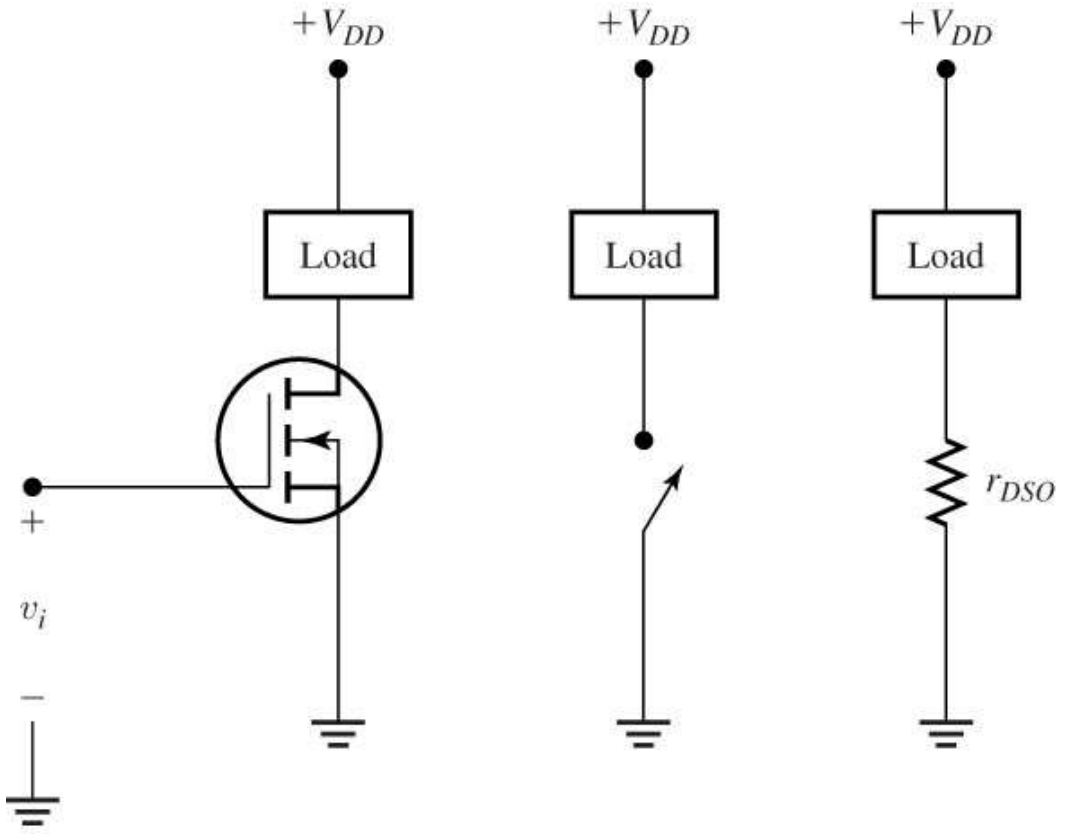
(a) I_D versus V_{DS} (b) I_D versus V_{GS} for a fixed V_{DS}



May be used for both enhancement and depletion mode

Lower threshold voltage than enhancement type

Switch using an N-channel enhancement-mode MOSFET.



(a)

(b) $v_i < V_{GS(\text{th})}$

(c) $v_i > V_{GS(\text{th})}$ ohmic region

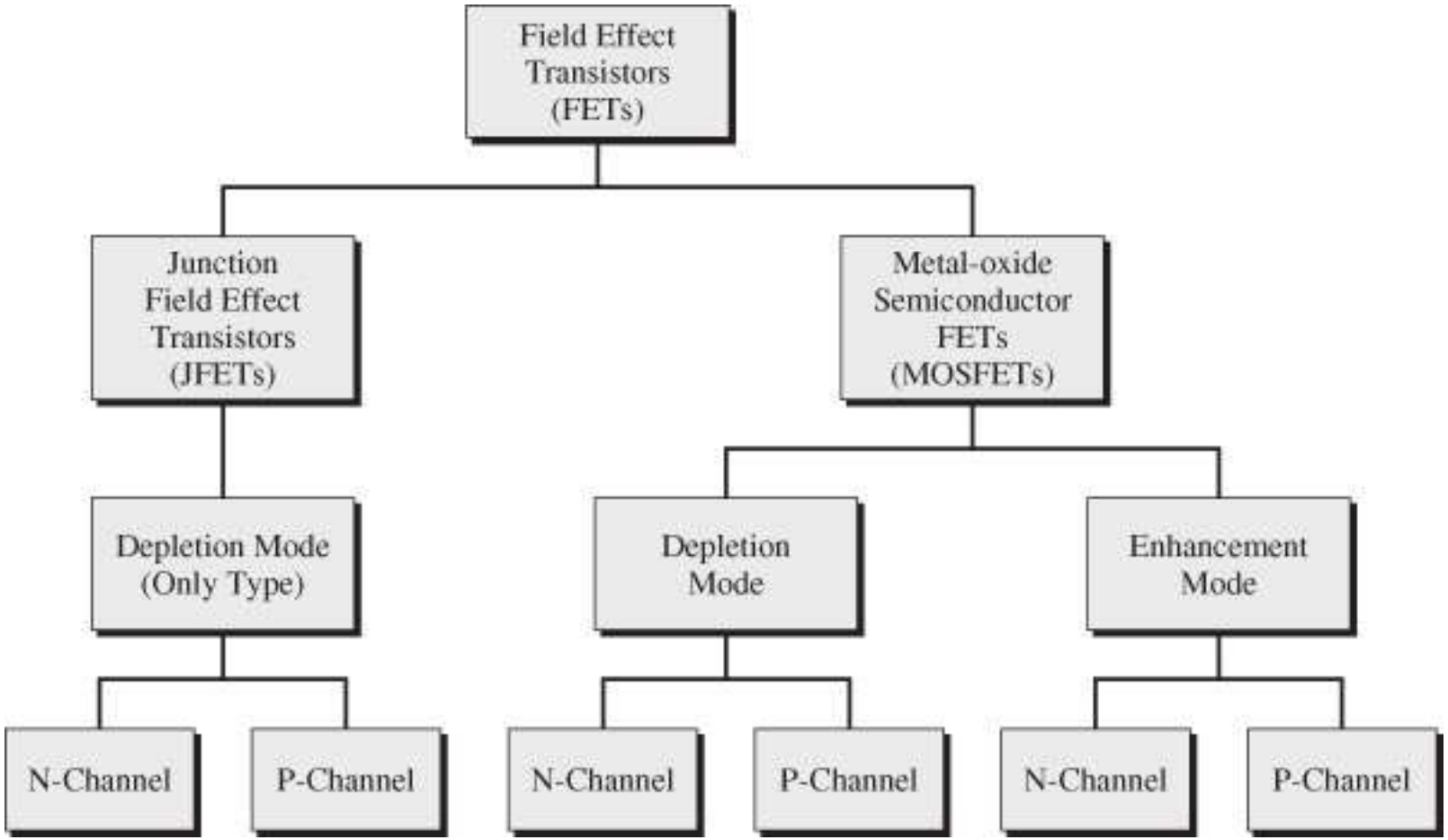
Comparison between p- with n-channel FET

p-channel is easier to fabricate

n-channel is faster as the mobility of electrons is 3 times greater than the mobility of holes

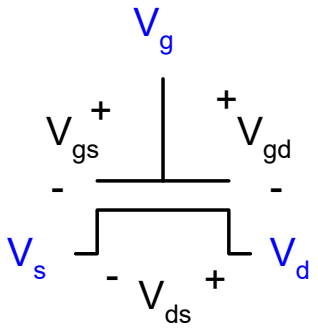
n-channel takes less space

Classification scheme for field effect transistors



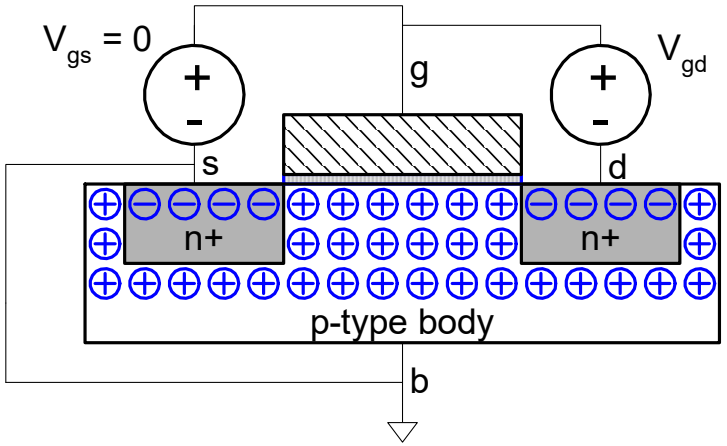
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



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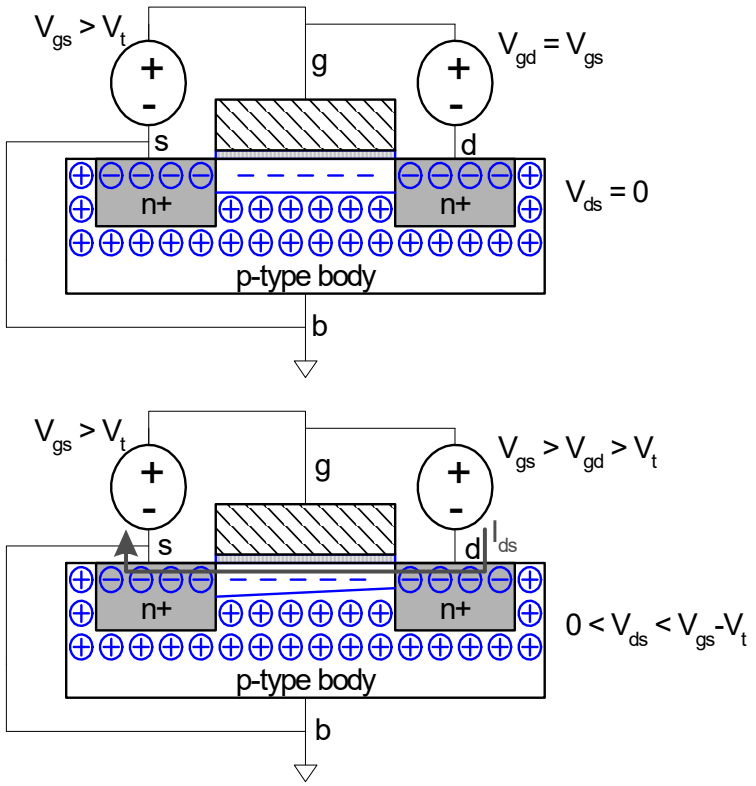

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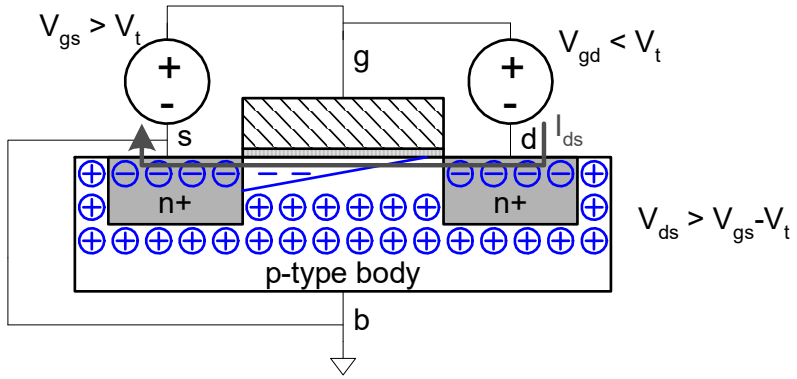
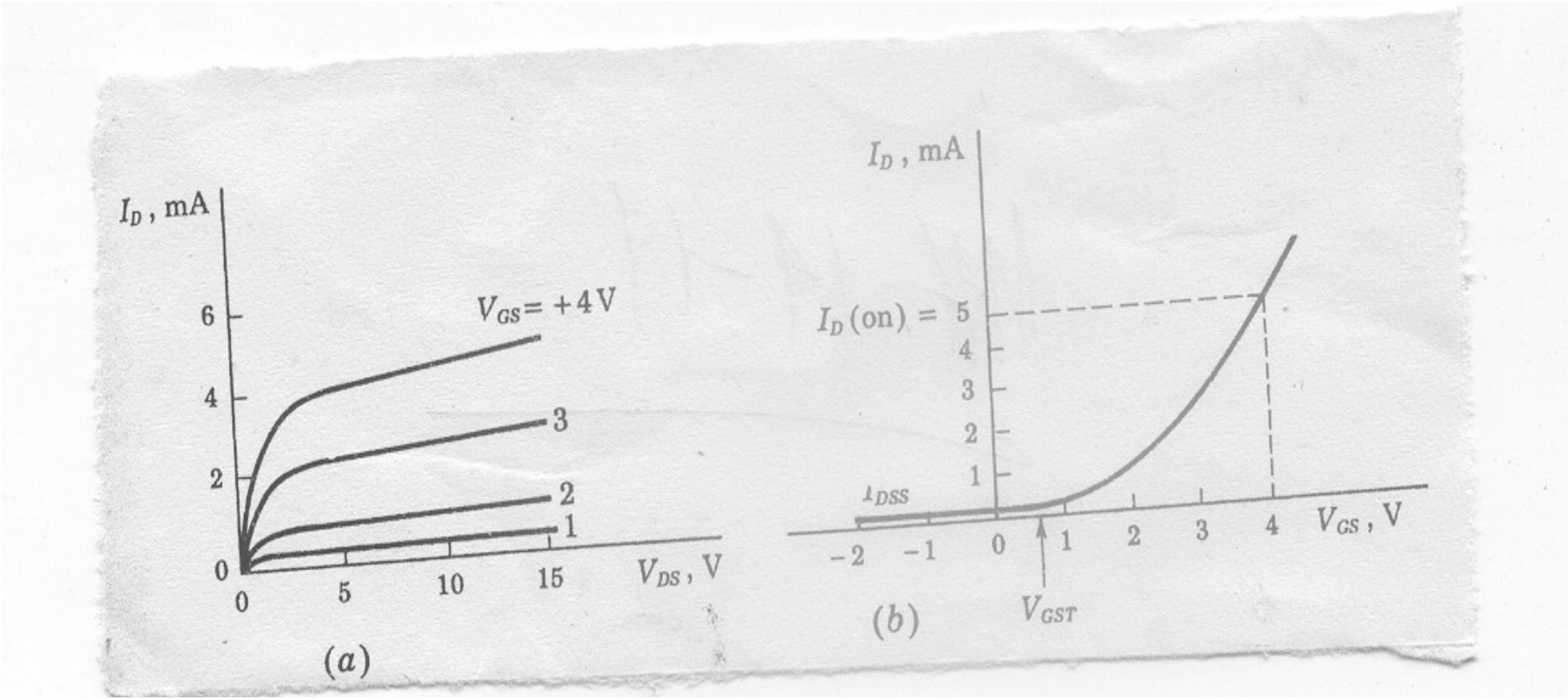


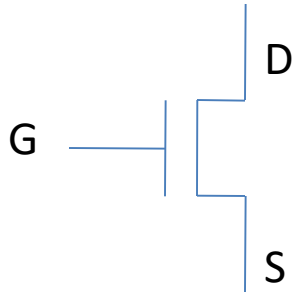
I-V Characteristics

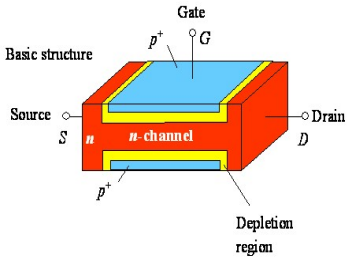
I_{ds} is dependent on both V_{ds} and V_{gs}

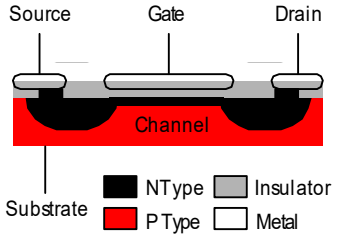


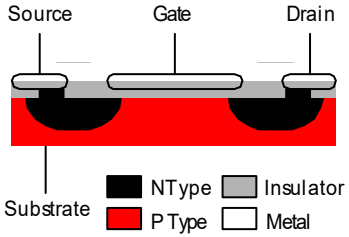
- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

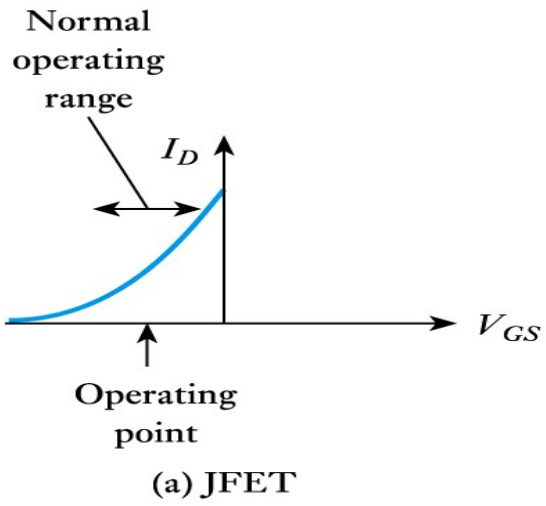
- **Transfer characteristics (n channel FET)**

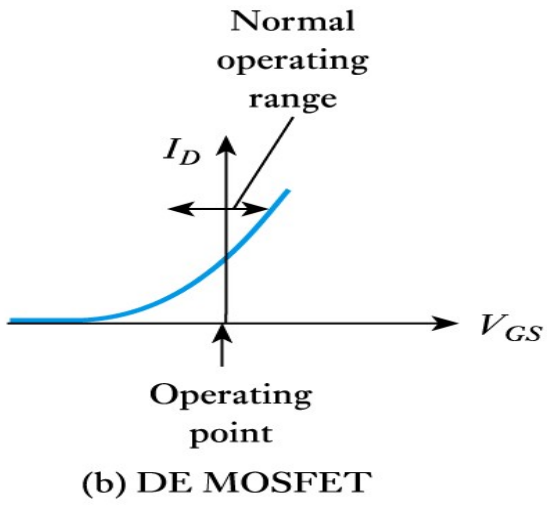


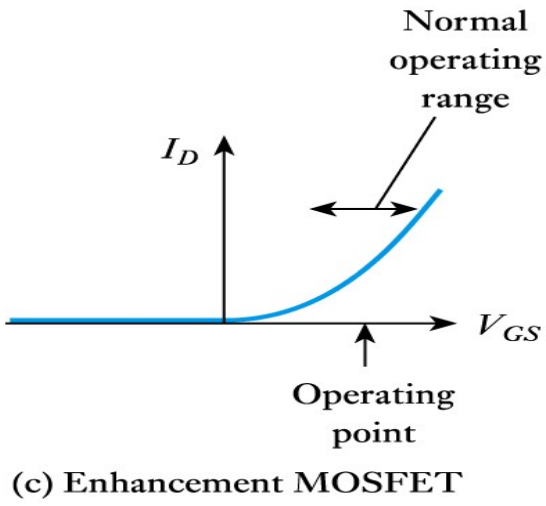






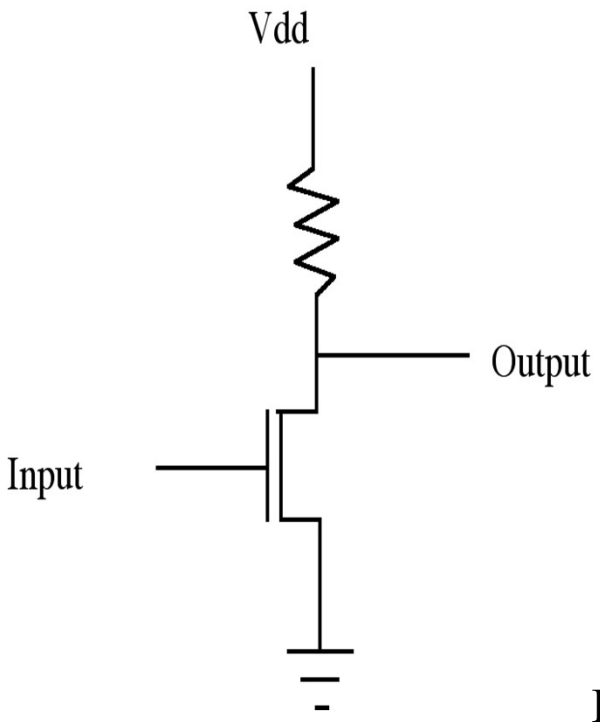


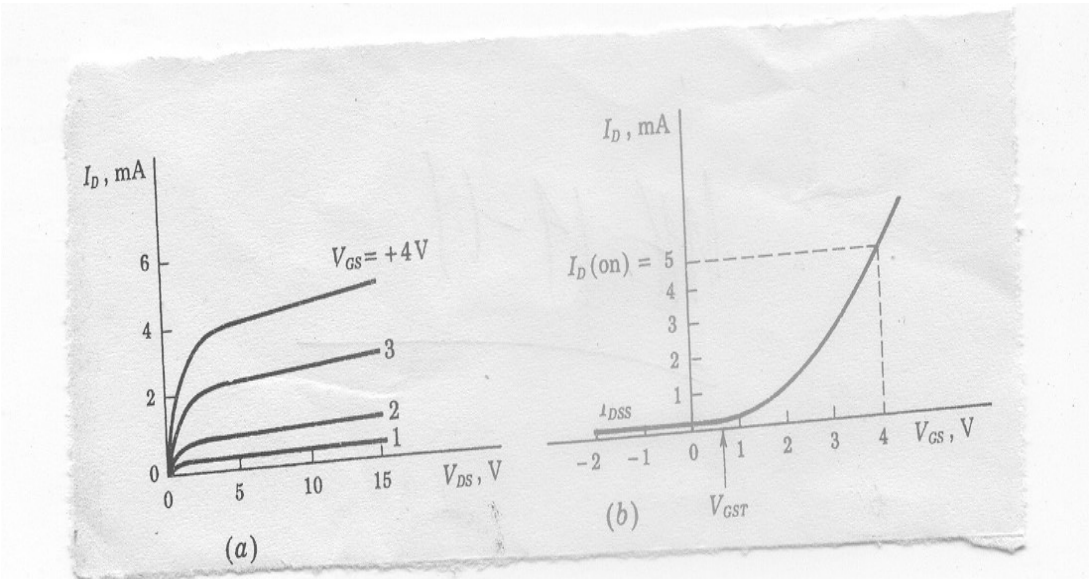




Operating range decides the type of FET

NMOS Inverter



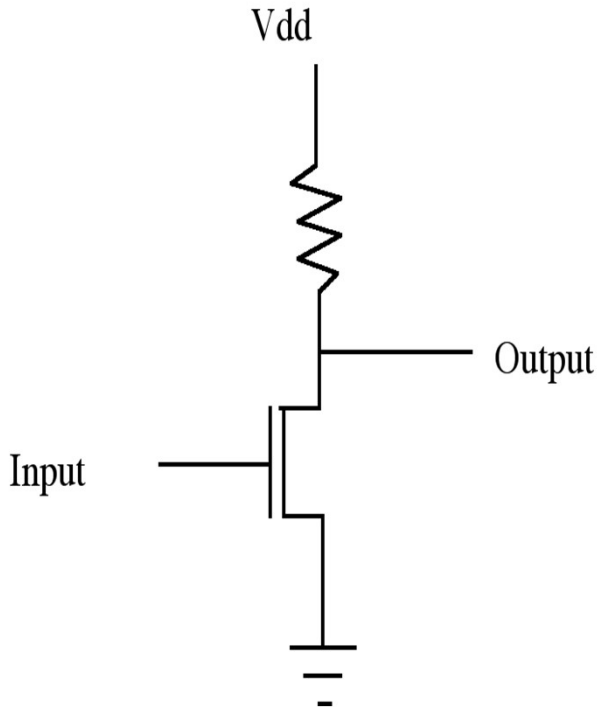


Enhancement NMOS: (a) I_D versus V_{DS} (b) I_D versus V_{GS}

Inverter Operation

- Plus signal input turns transistor on
- Ground is connected to output, thus a 1 (+) in gives 0 (Gnd) out
- A 0 input opens transistor and output is pulled high by resistor

NMOS Inverter

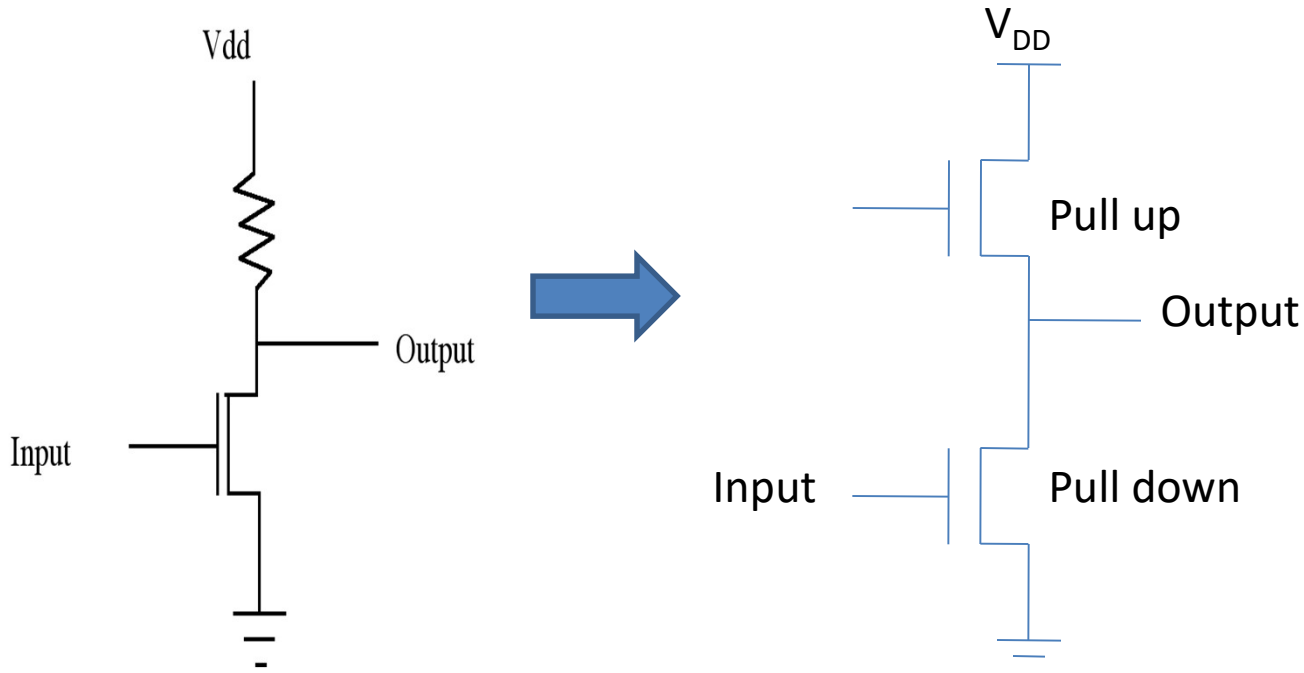


Resistor dissipates heat

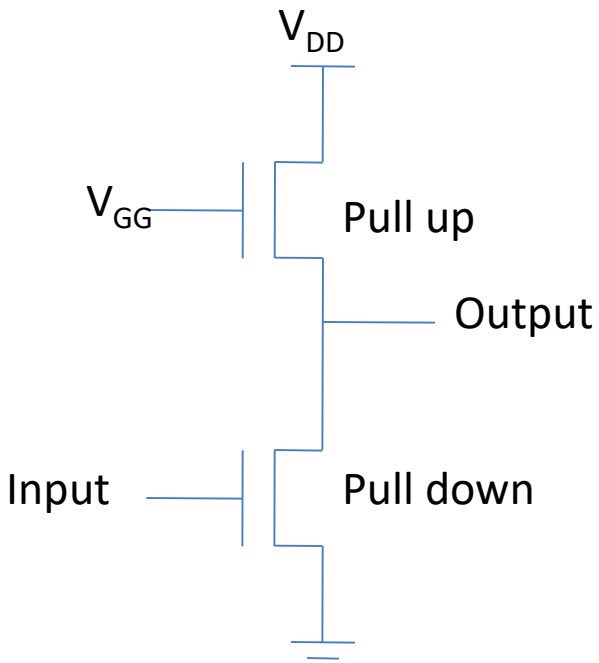
Fabrication of resistor is not easy

Even modest values of Resistors occupy excessively large areas in silicon substrate

A transistor may be used as a resistor

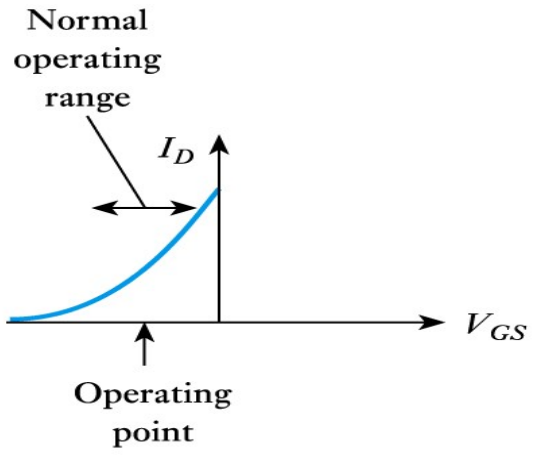


In Pull down NMOS
For input=1, Pull down conducts
For input =0, Pull down is off

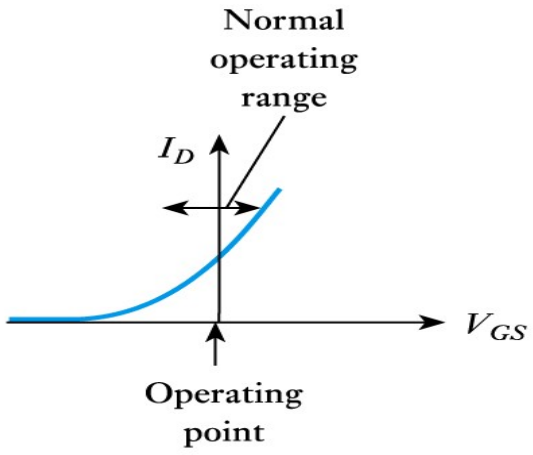


Pull up as an enhancement type NMOS

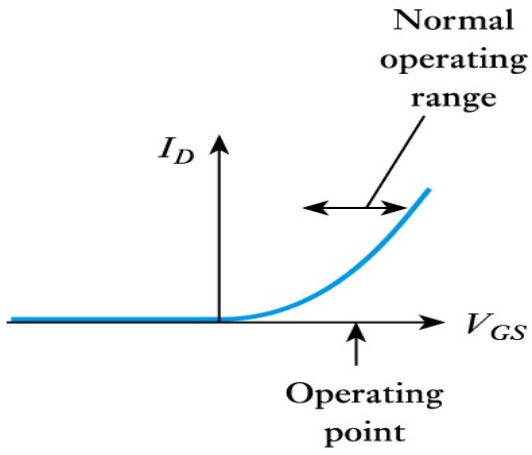
Pull up transistor input (V_{GG}) should be high



(a) JFET

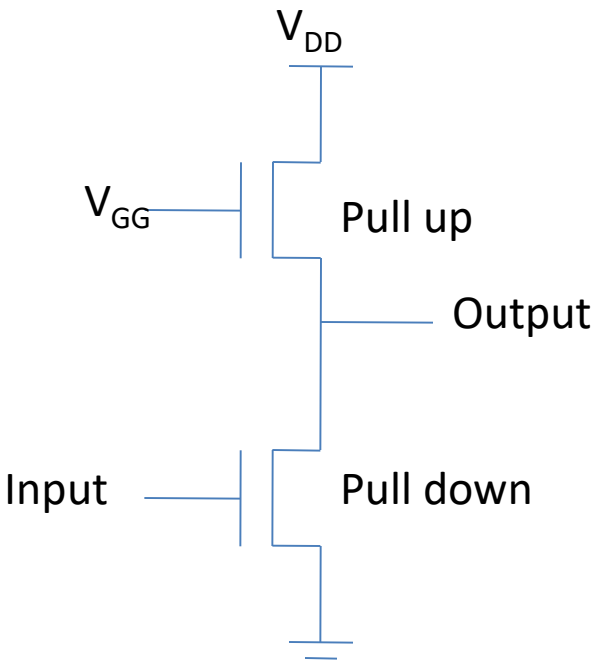


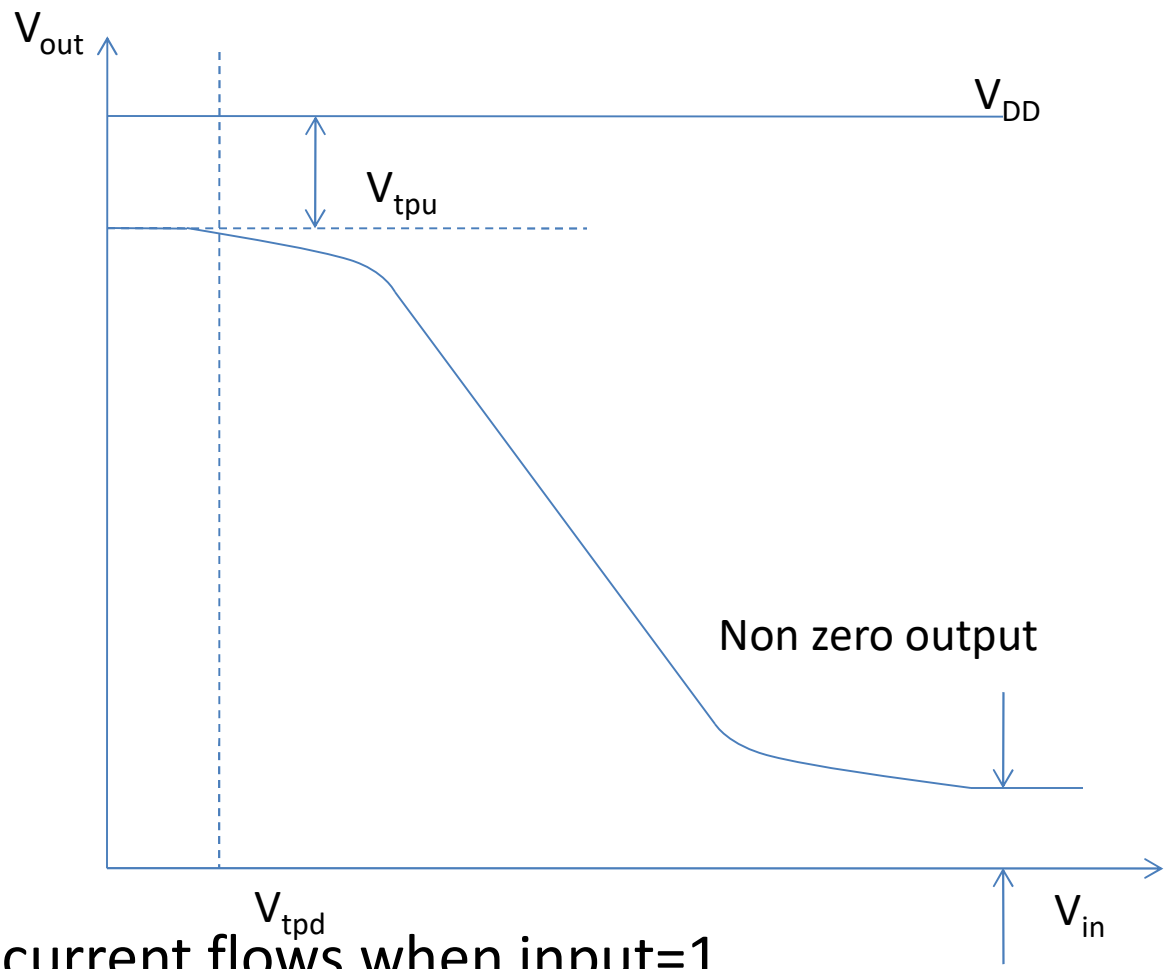
(b) DE MOSFET



(c) Enhancement MOSFET

Pull up as an enhancement NMOS





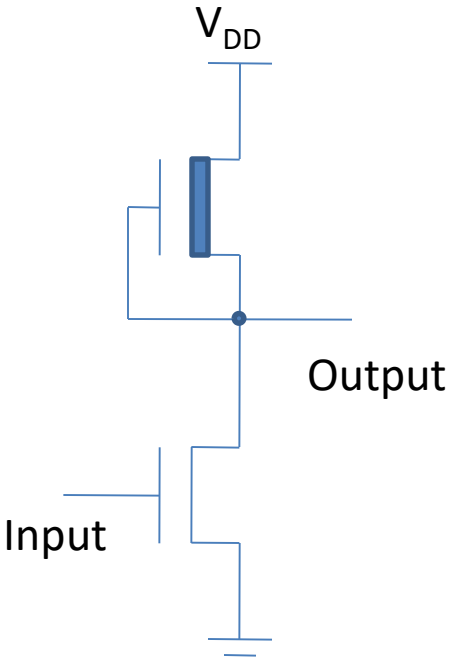
Dissipation is high since current flows when input=1

V_{out} can never be zero

V_{out} can never reach VDD (logical 1) if $V_{GG}=V_{DD}$ as is normally the case

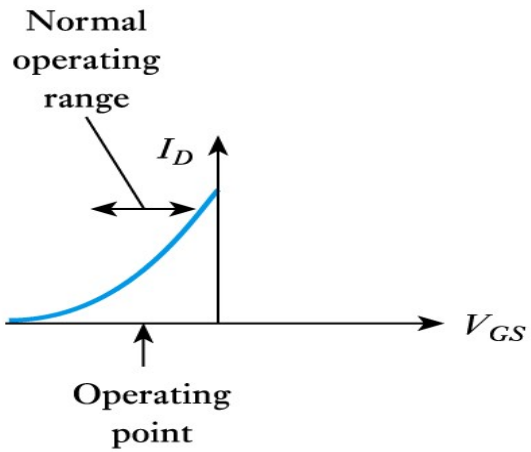
If V_{GG} is higher than V_{DD}, then an extra rail is required

Depletion type NMOS is used in pull up for better performance

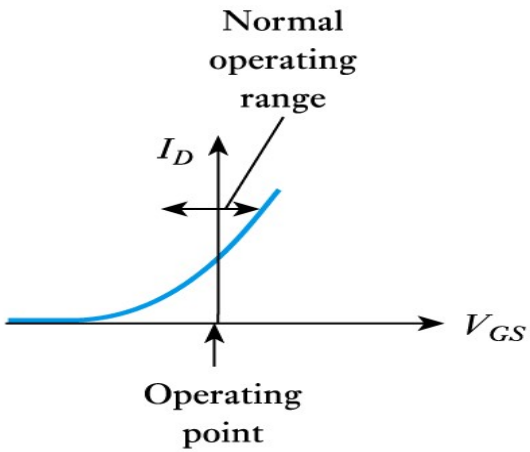


Gate and Source is shorted to achieve $V_{GS}=0$

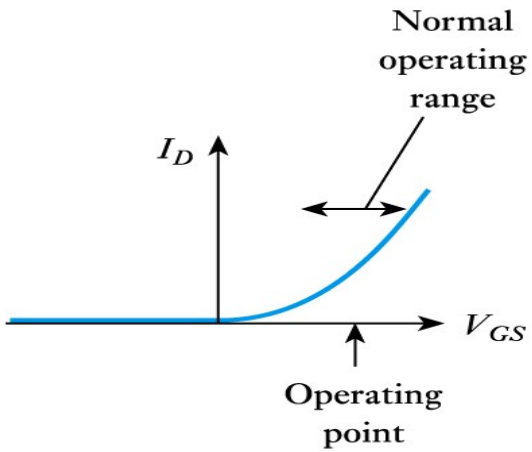
In Pull down NMOS
For input=1, Pull down is on
For input =0, Pull down is off
Pull up is always on



(a) JFET

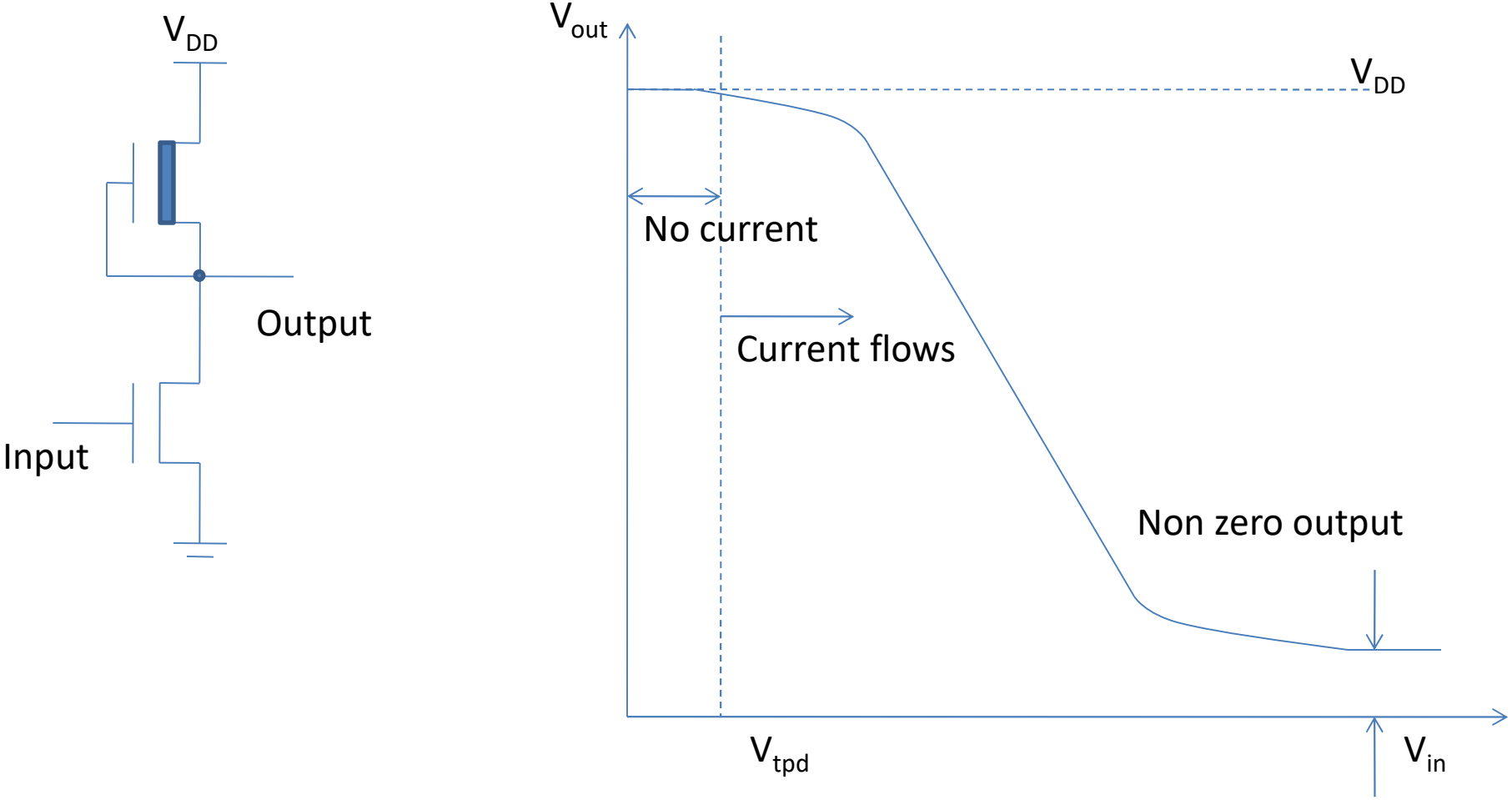


(b) DE MOSFET



(c) Enhancement MOSFET

Depletion type NMOS is used in pull up for better performance



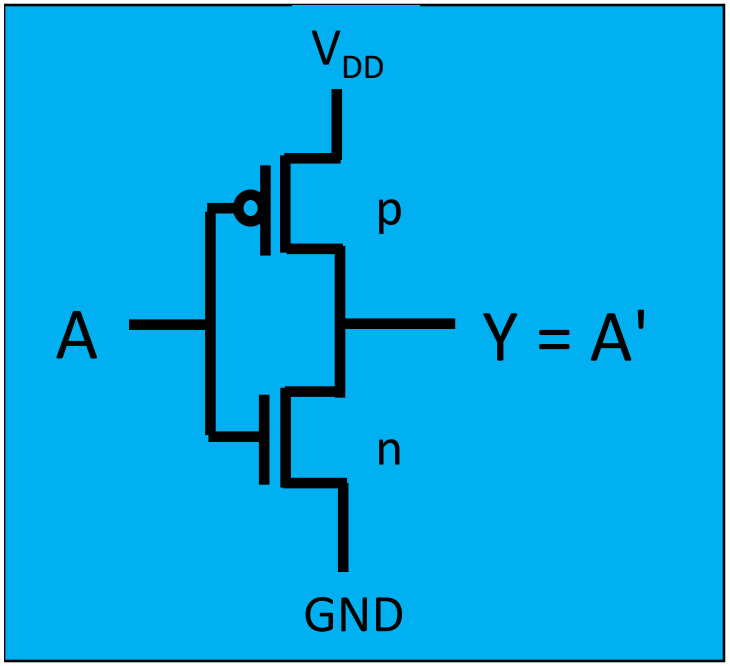
Dissipation is high since current flows when input=1

V_{out} can never be zero

Drawbacks of Metal-gate MOS Transistors

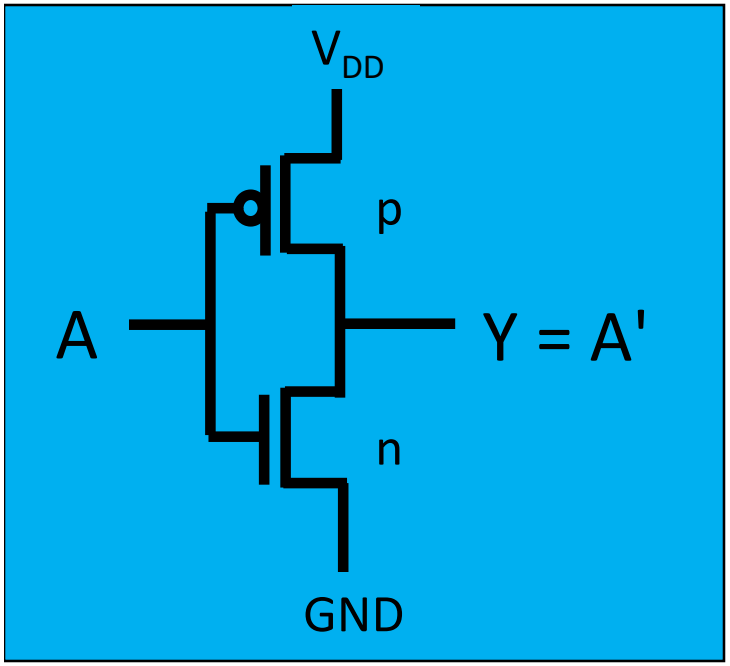
- High current flow for input at logic 1 in case of an inverter
- Excess surface state charges and mobile ion contamination cause the threshold variation.
- V_{out} never becomes exactly zero
- Suffer from excessive overlap capacitance.
- Parasitic capacitances C_{gs} and C_{gd} slow the transistor because they must be charged and discharged during switching.
- Aluminum is used as gate material which can erode completely causing contact spiking.

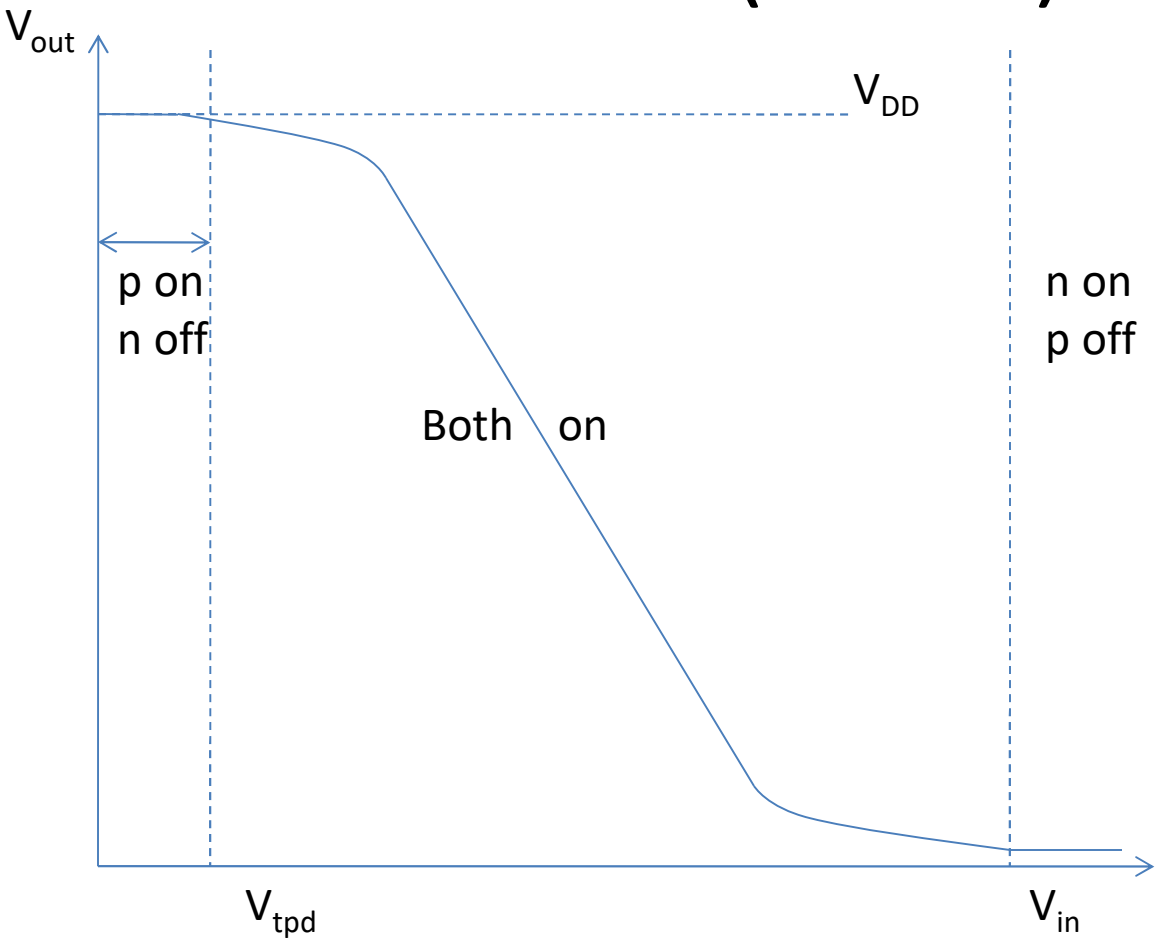
Complementary MOS Transistors (CMOS)



- When A is pulled high (V_{DD}), the PMOS inverter is turned off, while the NMOS is turned on pulling the output down to V_{SS}
- When A is pulled low (V_{SS}), the NMOS inverter is turned off, while the PMOS is turned on pulling the output up to V_{DD}

Complementary MOS Transistors (CMOS)



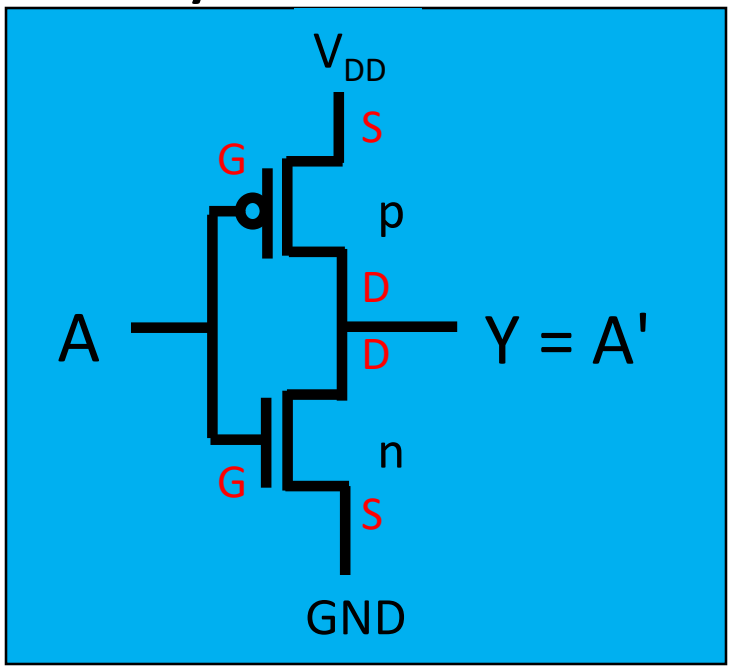


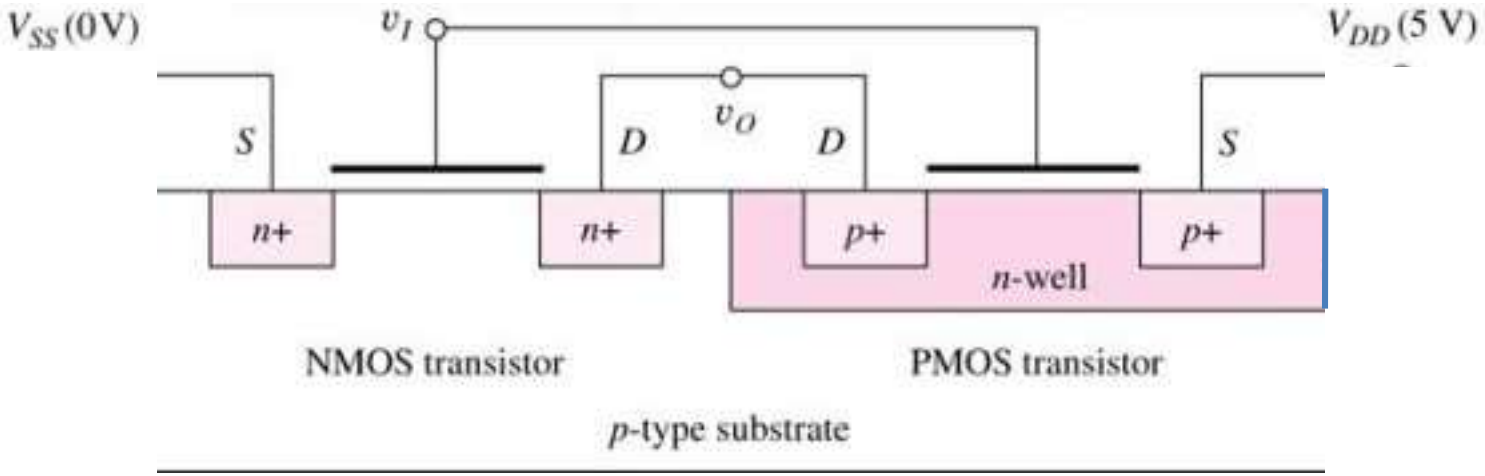
No current flow either for logical 0 or for logical 1 inputs

Full logical 1 and 0 levels are presented at output

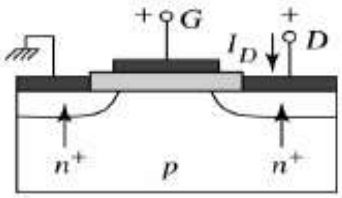
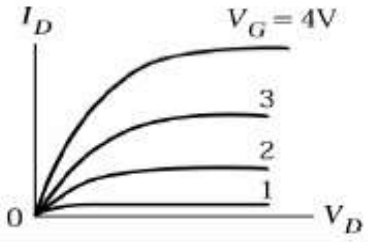
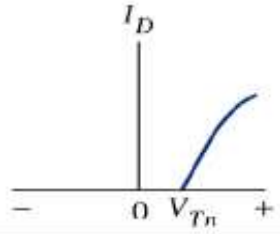
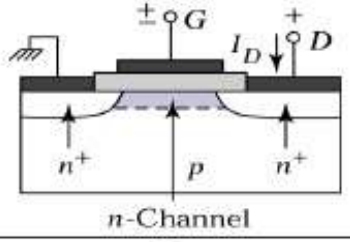
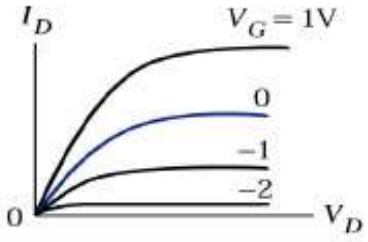
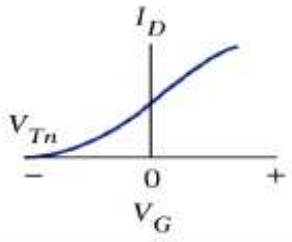
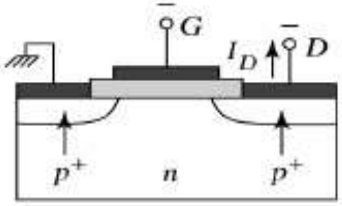
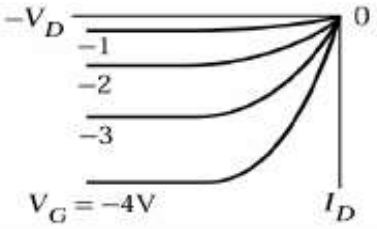
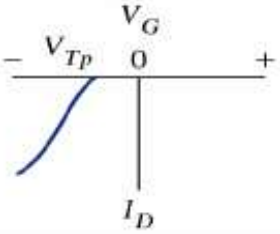
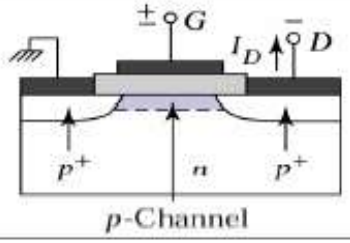
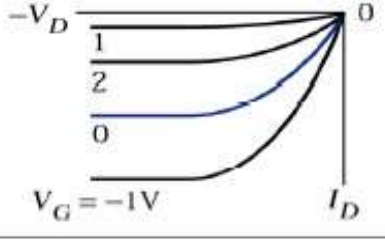
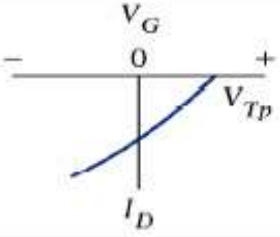
For devices of similar dimension p-channel is slower than n-channel device

Complementary MOS Transistors (CMOS)





Types of MOSFET

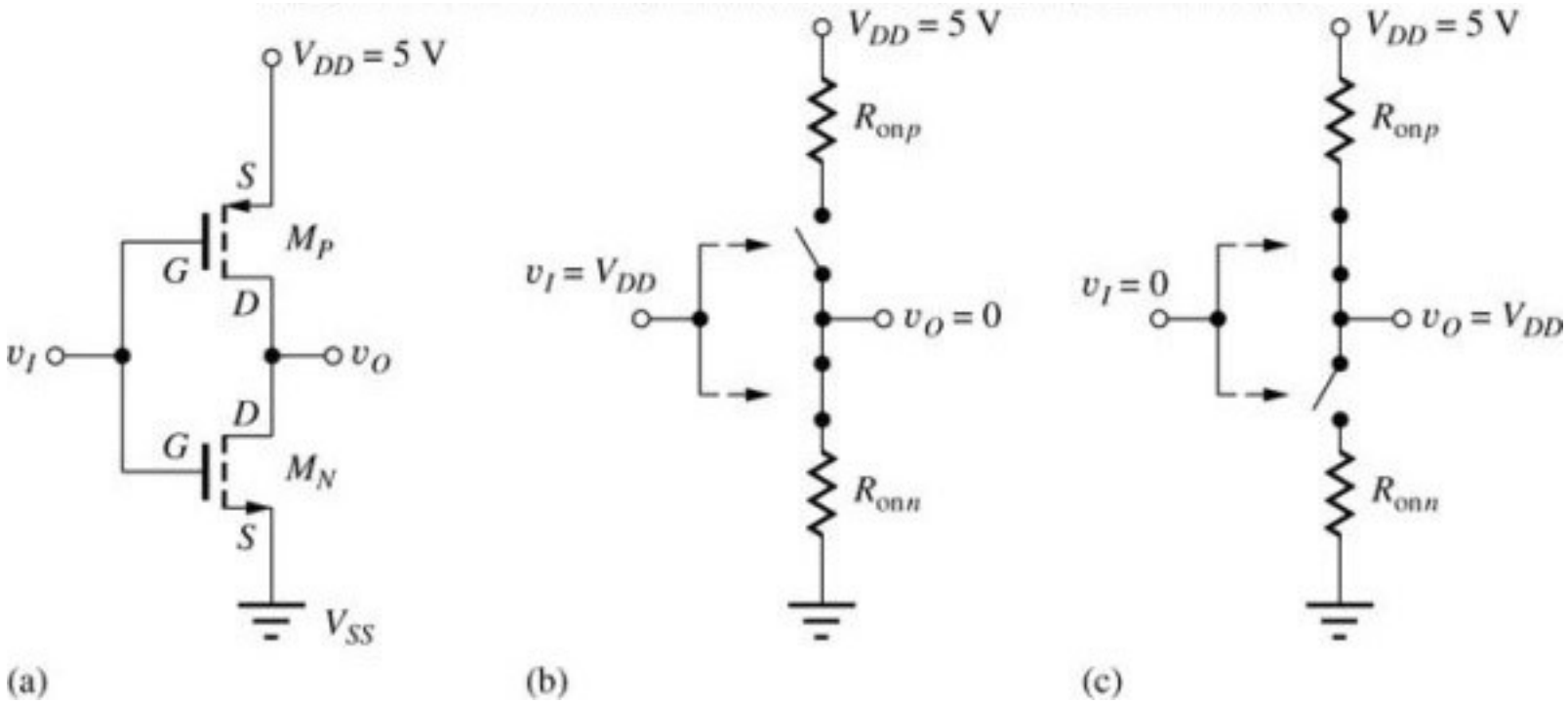
Type	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)			
n-Channel Depletion (Normally On)			
p-Channel Enhancement (Normally Off)			
p-Channel Depletion (Normally On)			

Pullup may be enhancement type PMOS

CMOS Inverter Technology

- Complementary MOS, or CMOS, needs both PMOS and NMOS devices for their logic gates to be realized
- The concept of CMOS was introduced in 1963 by Wanlass and Sah, but it did not become common until the 1980's as NMOS microprocessors were dissipating as much as 50 W and alternative design technique was needed
- CMOS still dominates digital IC design today

CMOS Inverter



(a) Circuit schematic for a CMOS inverter
(b) Simplified operation model with a high input applied
(c) Simplified operation model with a low input applied