VLSI LAB ASSIGNMENT

Encoder

1. Design a 4x2 Encoder using
    (a) structural modelling.
    (b) using behavioral modelling.
2. Design a 8x3 Encoder using
    (a) select statement.
    (b) case statement.
3. Design a decimal-to-BCD encoder.

Multiplexer

4. Design a 2x1 Multiplexer by
    (a)structural modelling.
    (b)process statement (using case statement and if else statement).
    (c)concurrent statement.
5. Design a 4x1 Multiplexer by
    (a)structural modelling.
    (b)process statement (using case statement and if else statement).
    (c)concurrent statement.
    (d)by component instantiation.
6. Design a 8x1 Multiplexer by
    (a) using only 2x1 Multiplexers.
    (b) using both 2x1 Multiplexers and 4x1 Multiplexers.
7. Design a 16x1 Multiplexer using component instantiation.

Decoder

8. Design 1x2 Decoder using
    (a) structural design.
    (b) sequential statement.
    (c) concurrent statement.
9. Design 2x4 Decoder using
    (a) structural design.
    (b) sequential statement.
    (c) concurrent statement.

10. Design a 3x8 decoder
    (a) by component instantiate.
    (b) by using procedural statement.

Demultiplexer

13. Design a 1x2 Demultiplexer and 1x4 Demultiplexer using structural design and behavioral design.

12. Design a 1x16 Demultiplexer
    (a) using only 1x4 Demultiplexers.
    (b) using only 1x2 Demultiplexers.
    (c) using only and both1x2 Demultiplexers and 1x8 Demultiplexers.
    (d) using only and both1x2 Demultiplexers and 1x4 Demultiplexers.

ADDER

14. Design Half Adder using gate level modelling.

15. Design Full Adder using
    (a) component instantiate.
    (b) using function or procedure.
16. Design 4-bit Ripple-Carry-Adder by
    (a) using generate statement.
    (b) using Loop statement.
17. Design BCD Adder.
18. Design Adder/Subtractor circuit.

Flip-Flop

19. Design SR Flipflop.
20. Design D Flipflop.
21. Design JK Flipflop.
22. Design T Flipflop.

Counter

23. Design a 4-bit synchronous Counter using JK Flipflop.