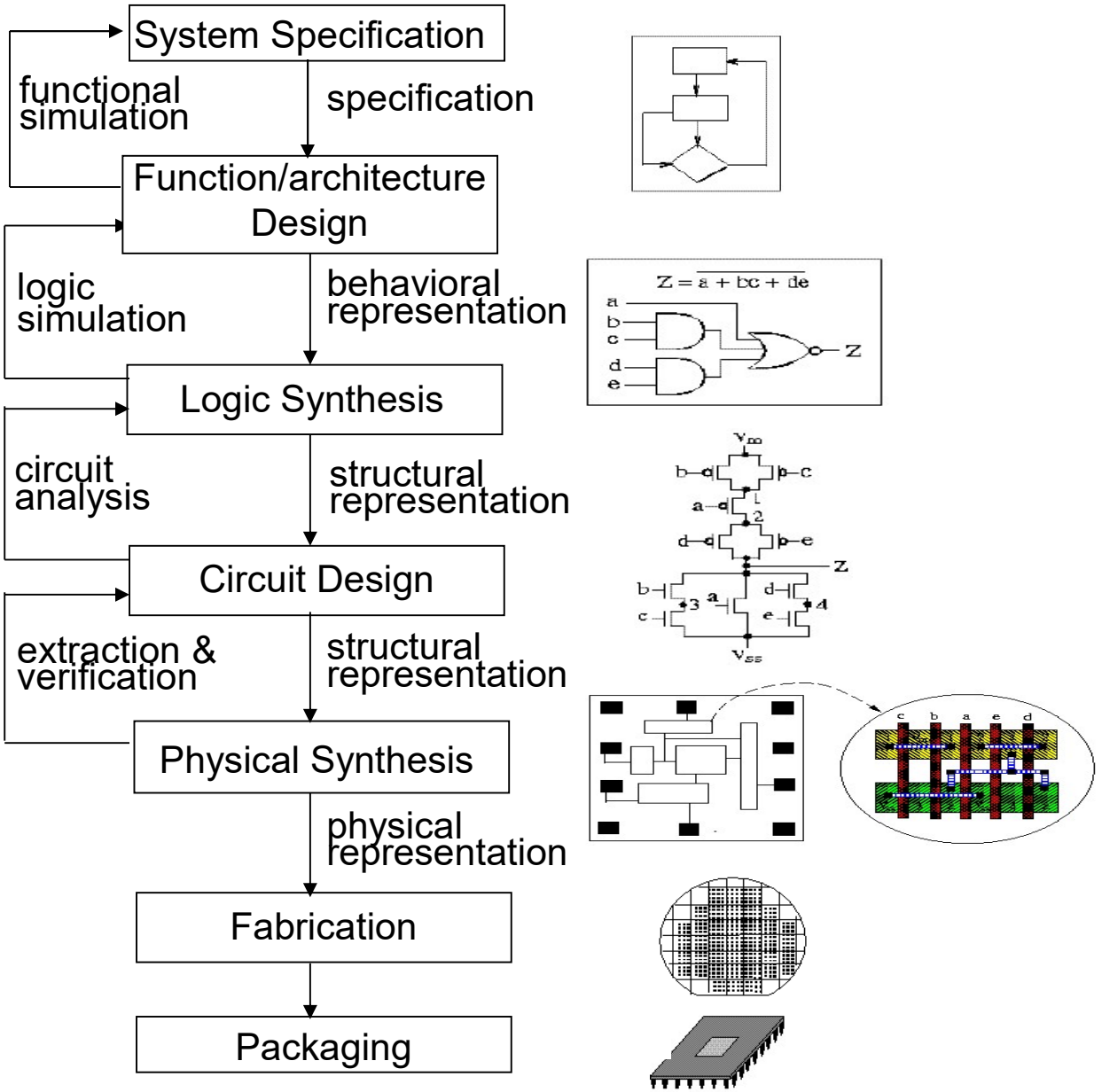
Layout and Stick Diagrams

VLSI Design Flow



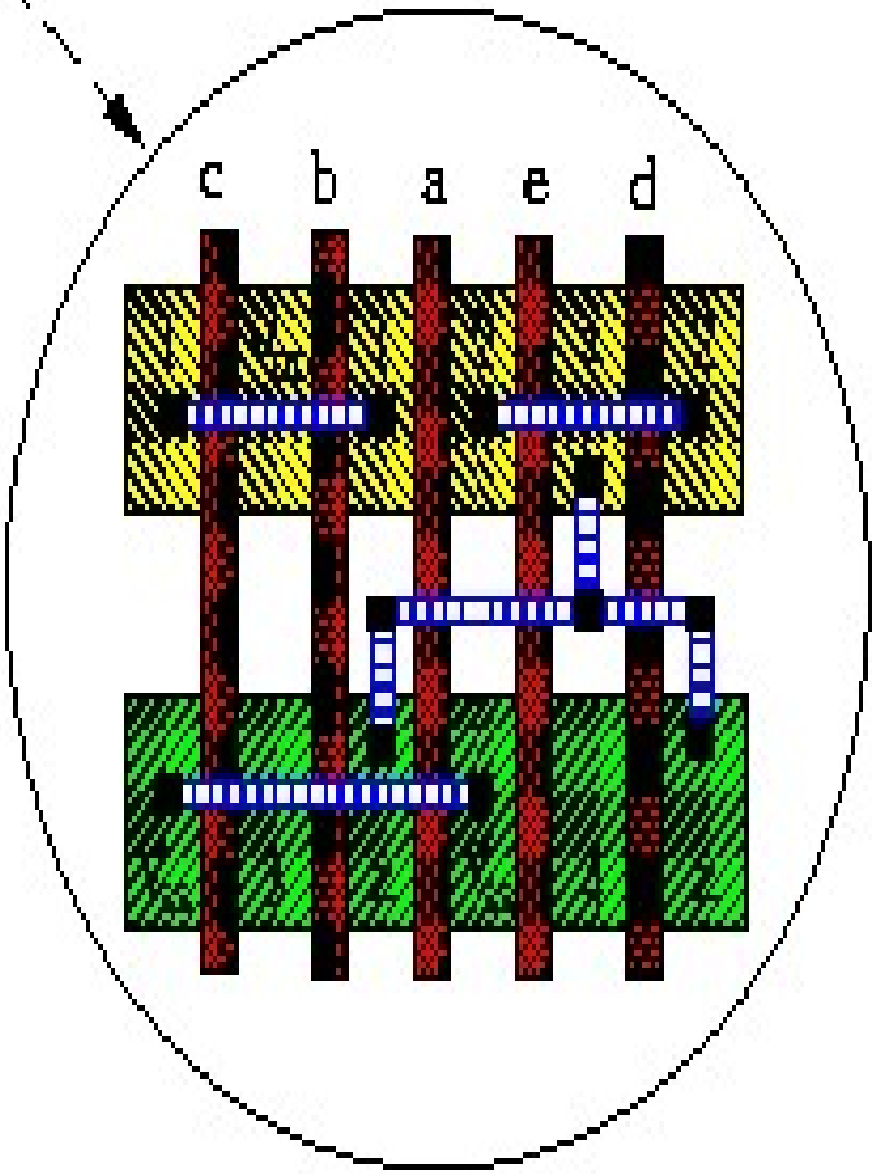
Layout

Layout consists of creating appropriate masks that define the sizes and locations of sources, drains, gates, and the necessary interconnections

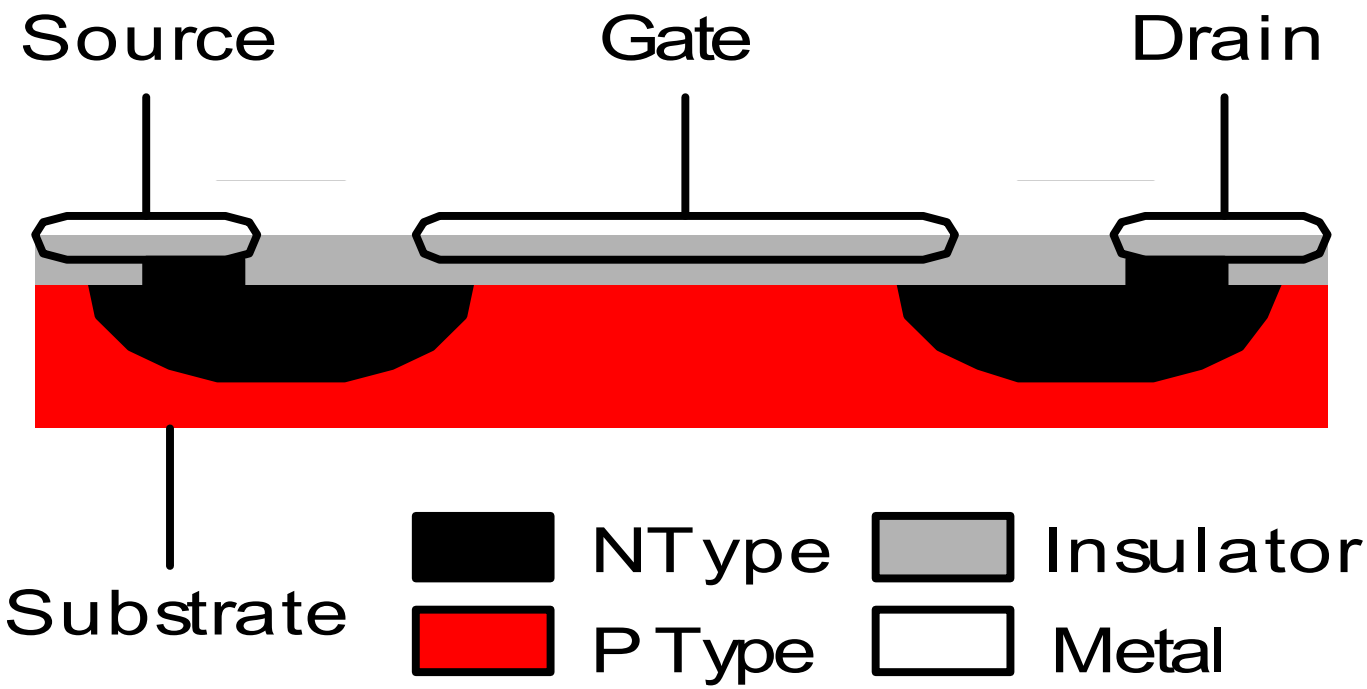
Layout is the lowest level of design abstraction for VLSI

Layout is directly sent to the manufacturer

Layout determines the circuit topology and the characteristics of components



MOSFET: Metal Oxide Semiconductor Field-Effect Transistor



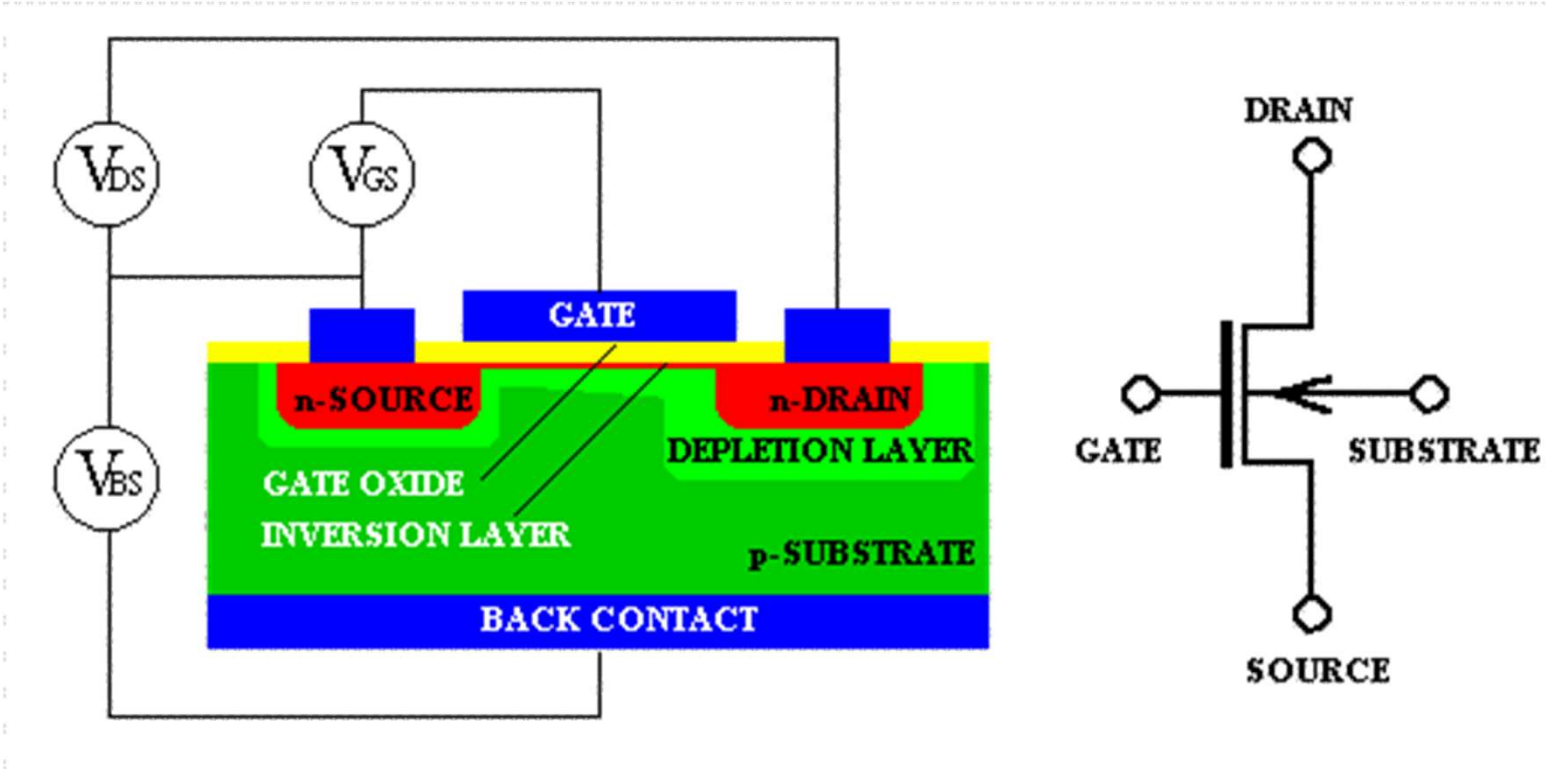
n channel MOSFET

In lightly doped p-type substrate, two highly doped n regions (source and drain) are diffused

Insulator is grown over surface and holes are cut into it to have contact with source and drain

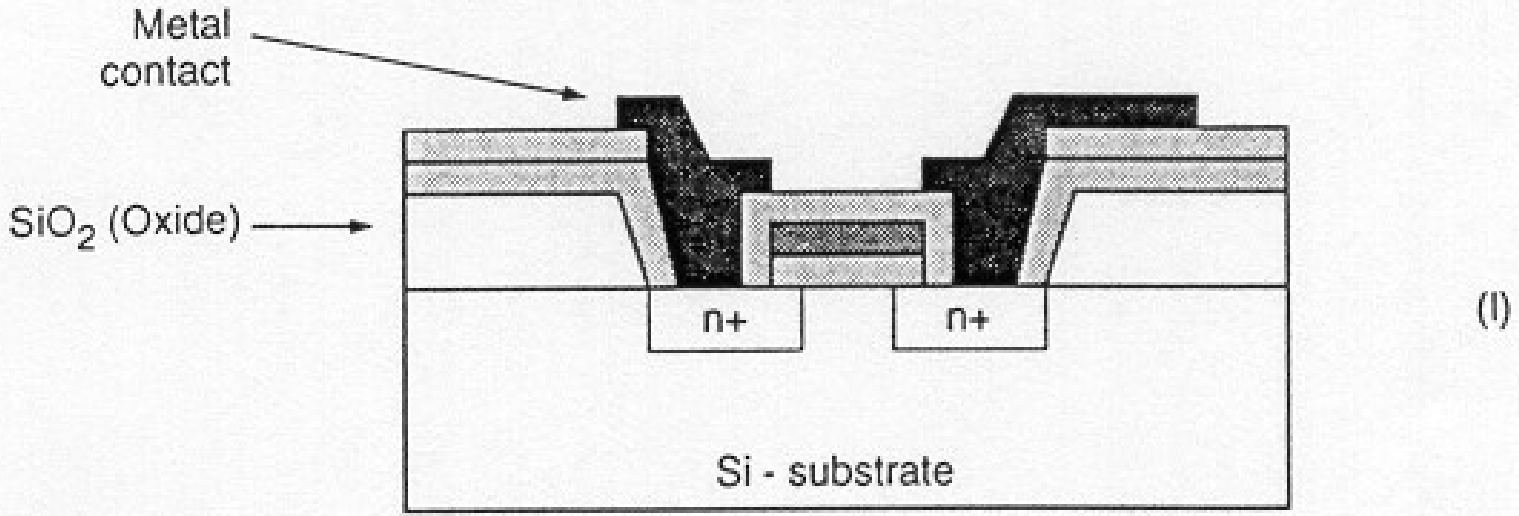
For Si substrate, SiO_2 is used as the Insulator

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)



n-channel

NMOS

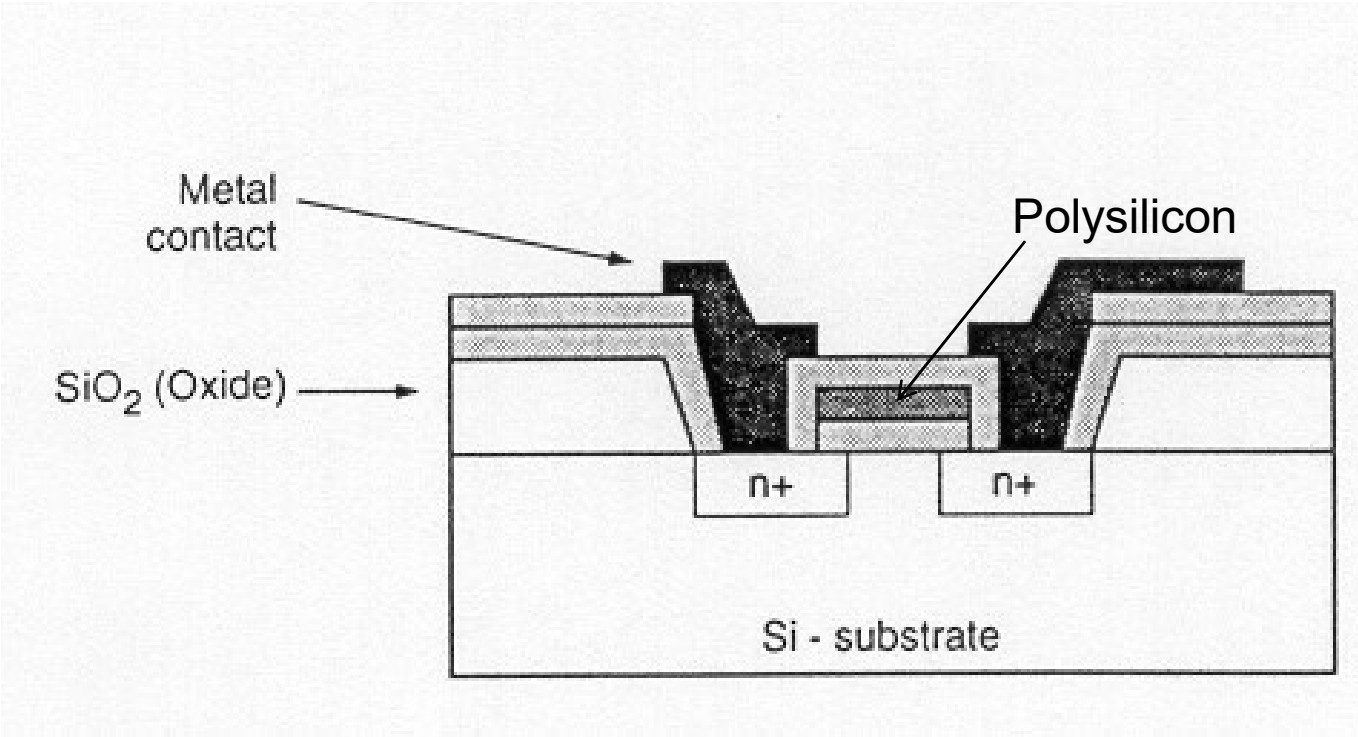


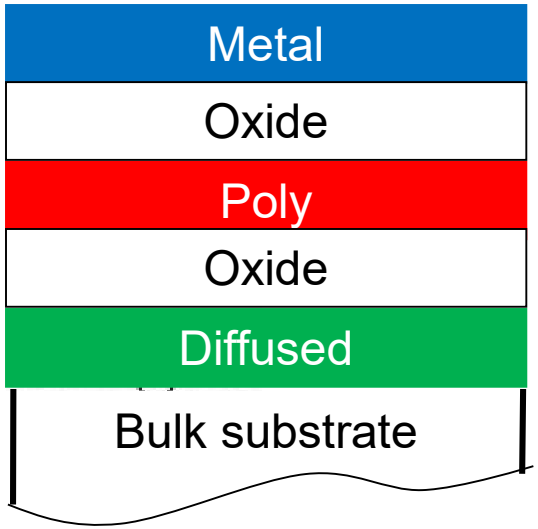
MOS Metalization process

It consists of three levels of conducting material (Diffused region, polysilicon, metal)

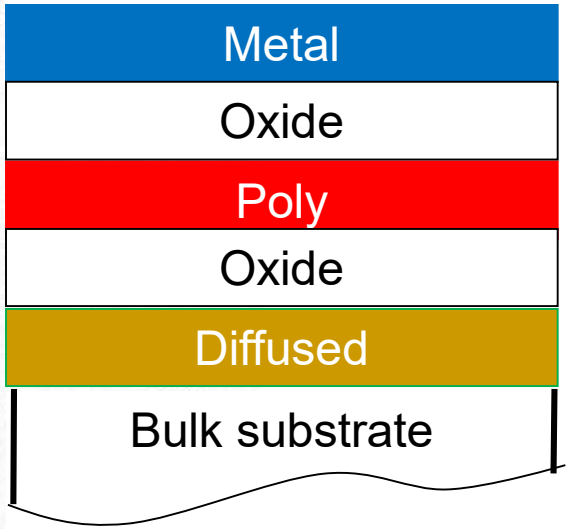
Each layer is isolated from the layers immediately above and below

Layers are color coded according to different photolithigraphic masks needed





NMOS



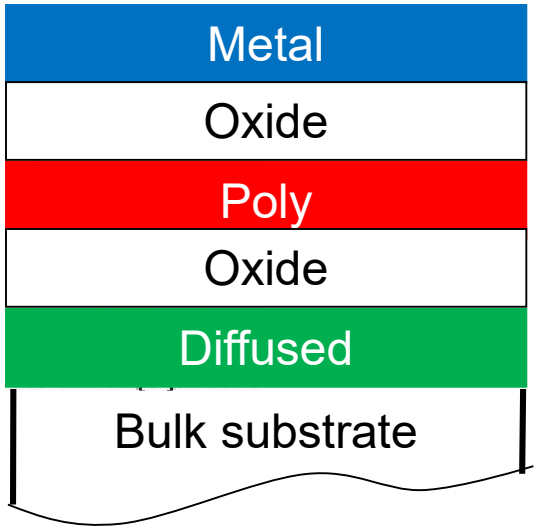
PMOS

MOS Metalization process

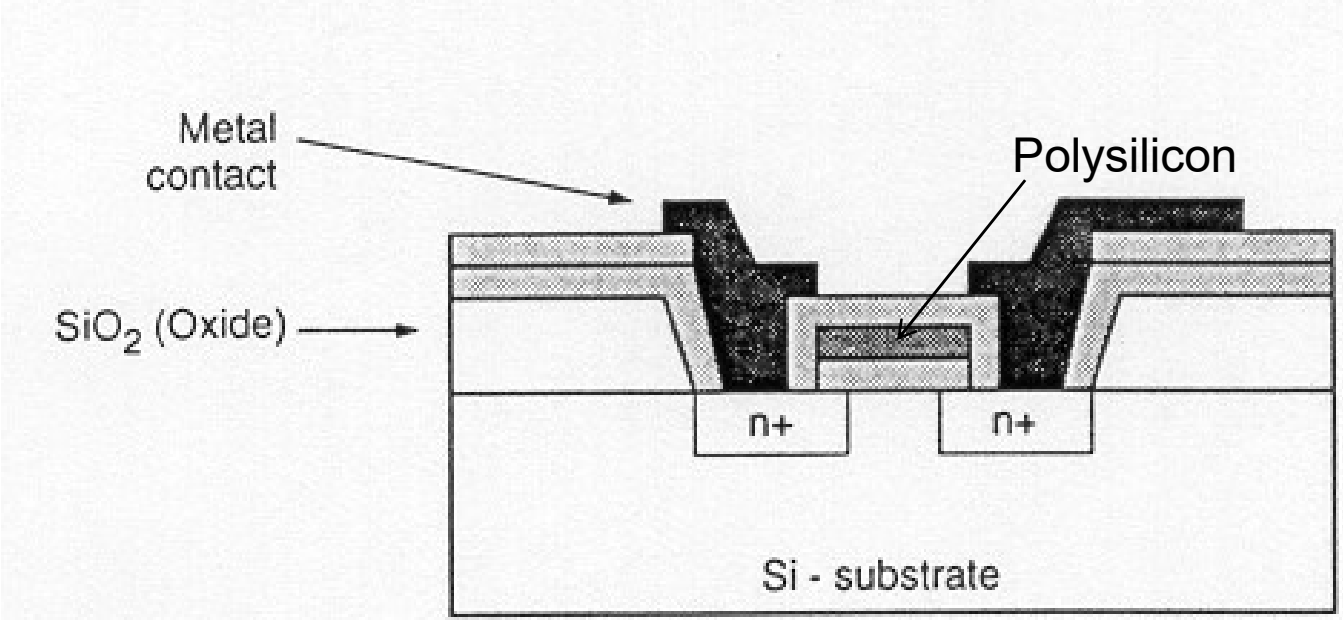
In some processes, there may be second metal layer

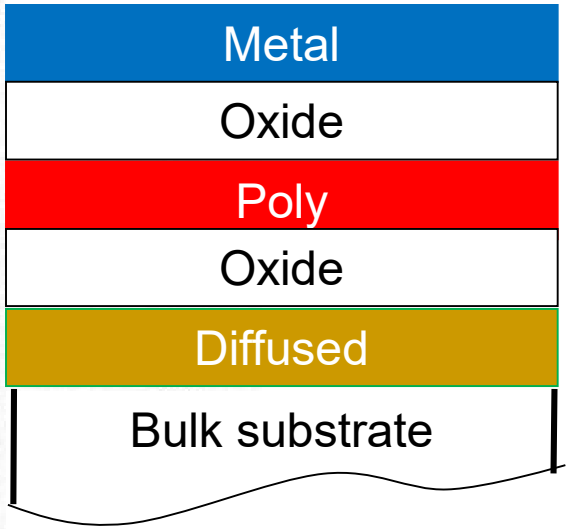
In some processes, a second polysilicon layer may exist

Layers may be joined together where contacts are formed



NMOS

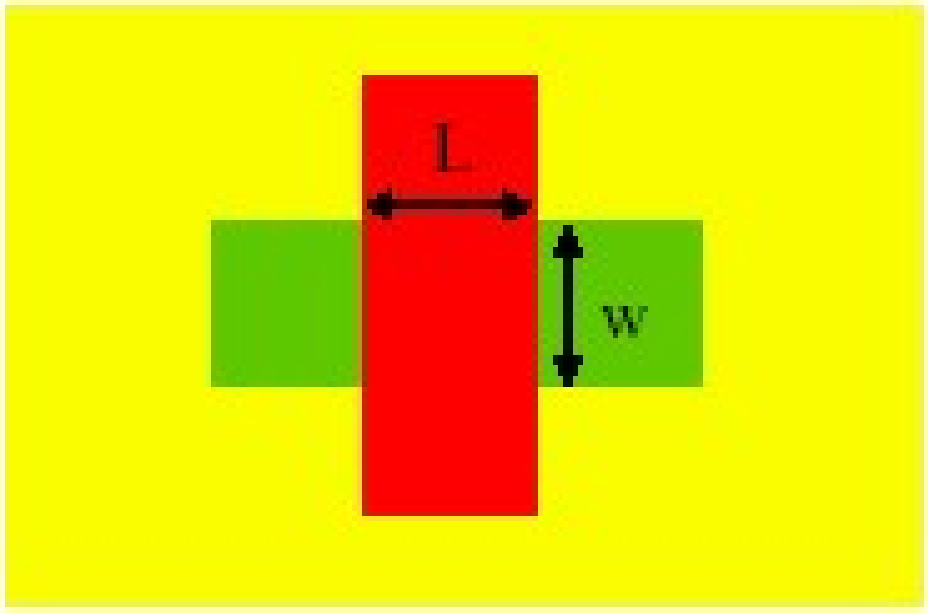




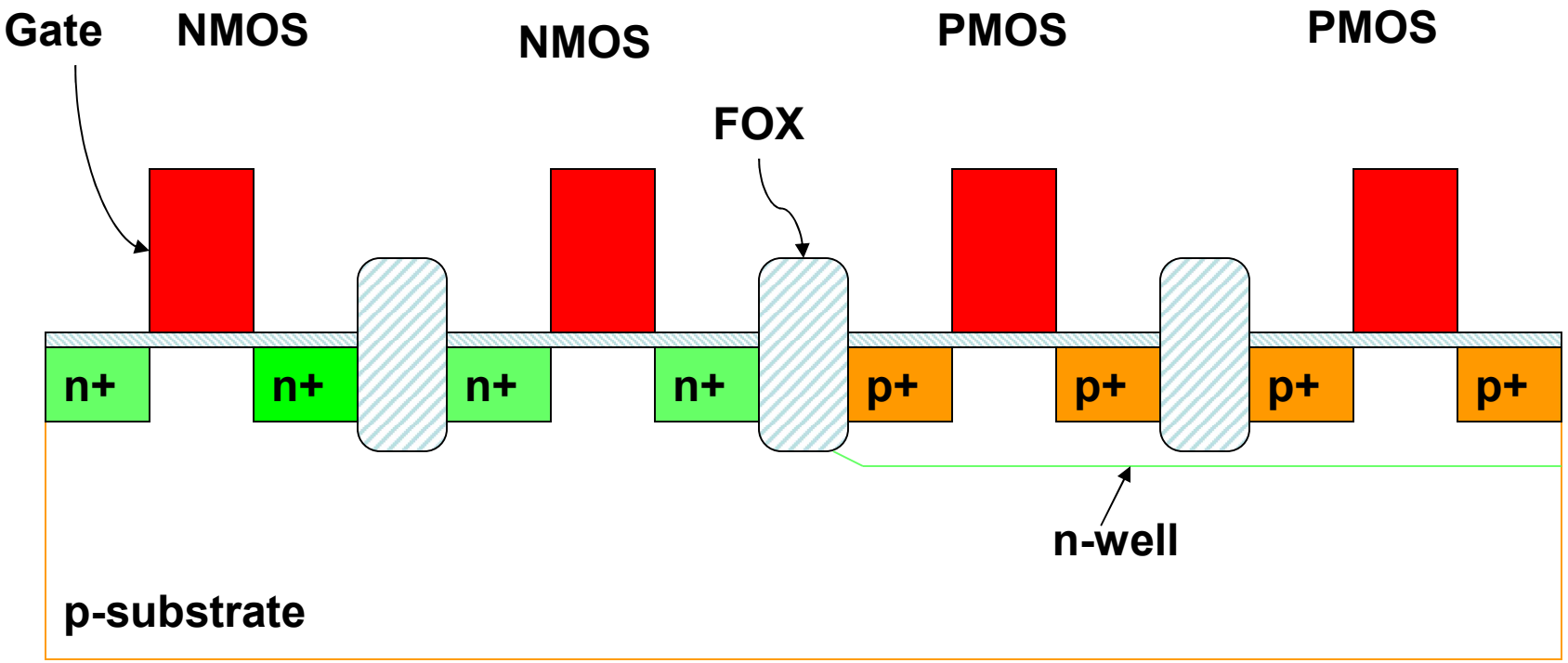
PMOS

Transistor Layout

n-type (tubs may vary):



n-well process

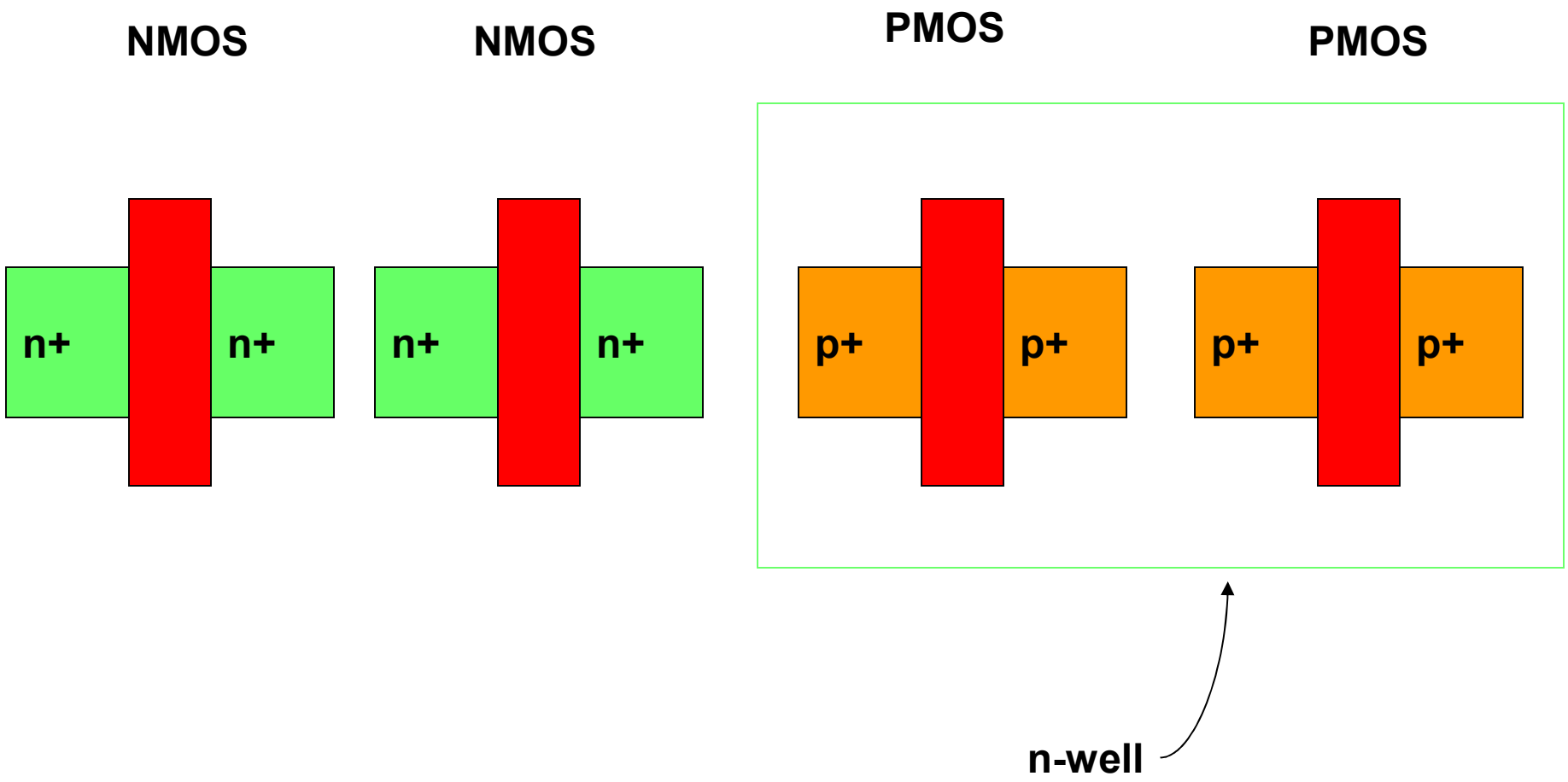


MOSFET Layers in an n-well process

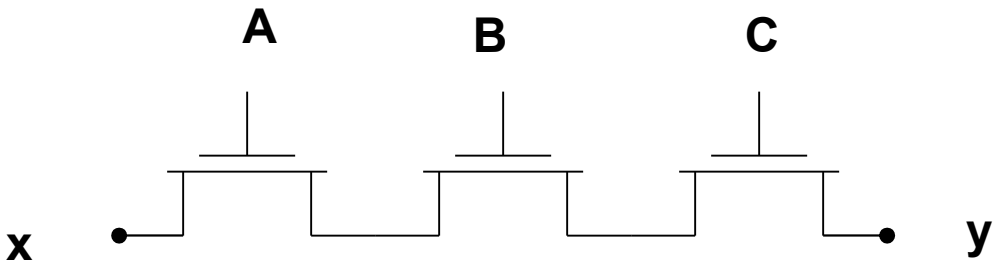
Layer Types

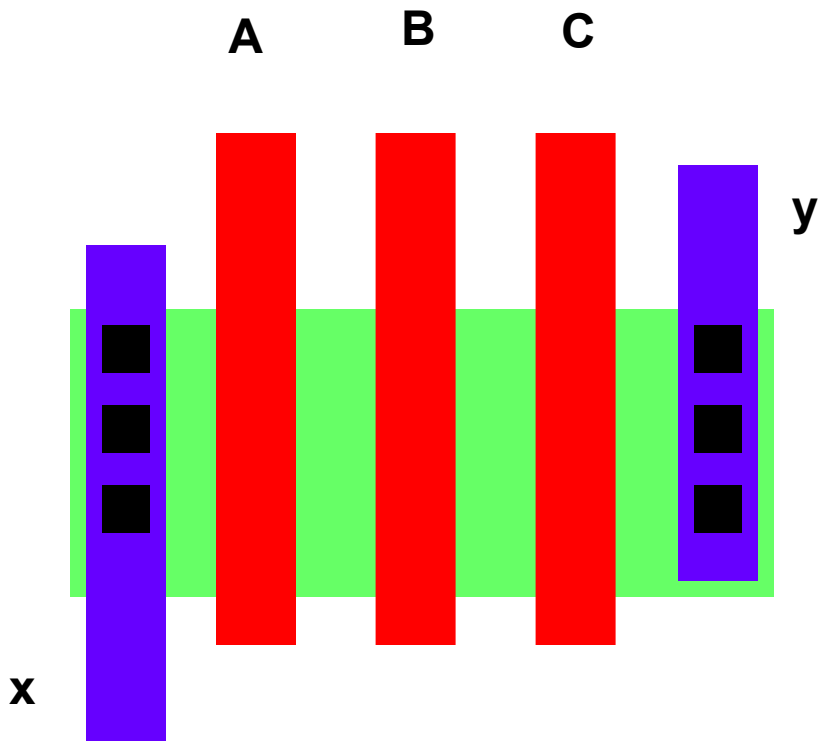
- p-substrate
- n-well
- n+
- p+
- Gate oxide
- Gate (polycilicon)
- Field Oxide
  - Insulated glass
  - Provide electrical isolation

Top view of the FET pattern

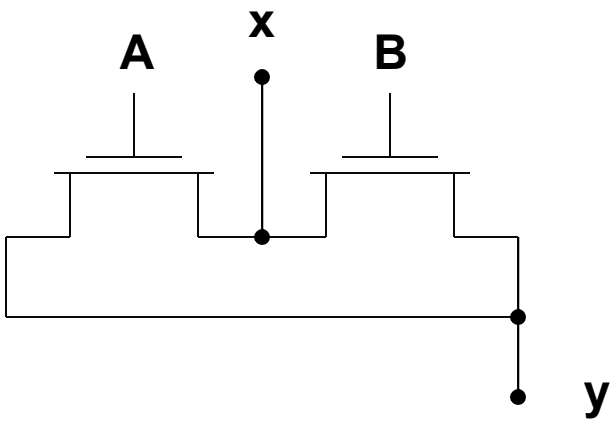


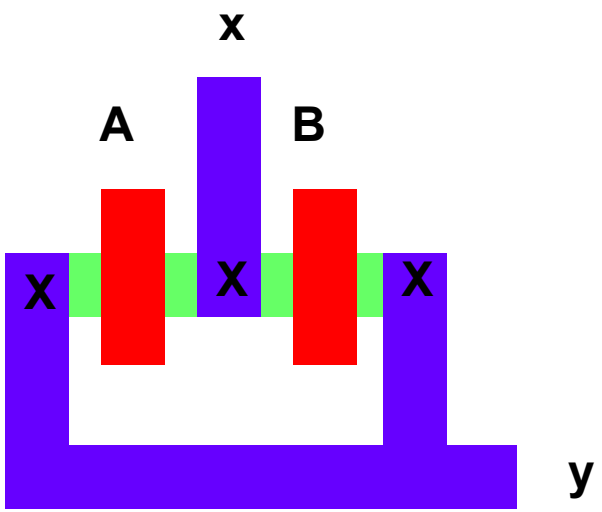
Designing MOS Arrays



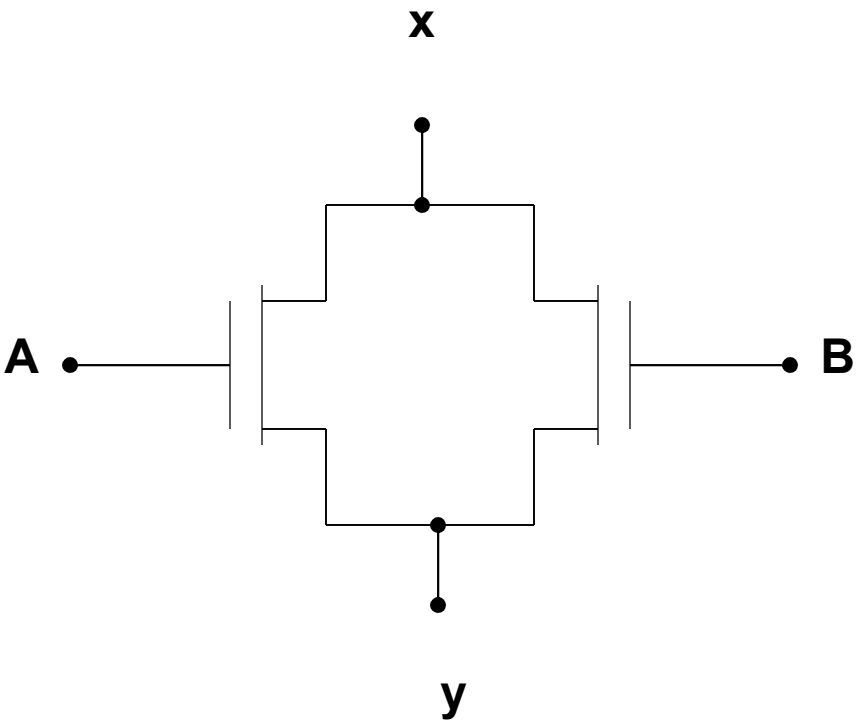


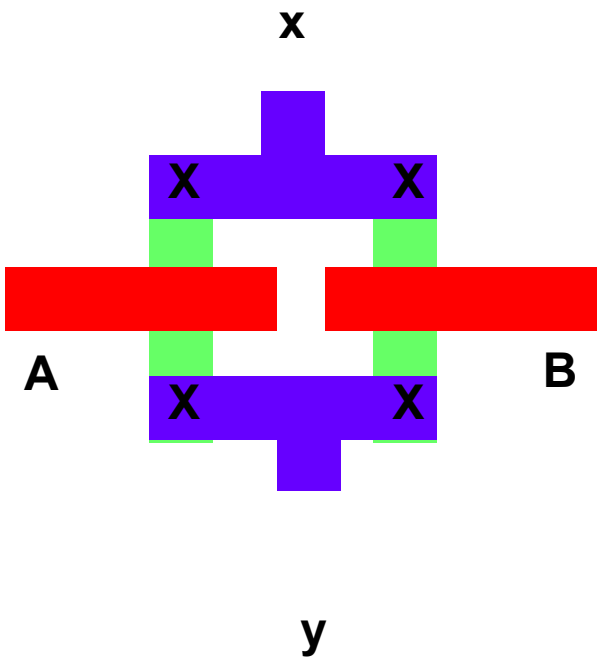
Parallel Connected MOS Patterning





Alternate Layout Strategy

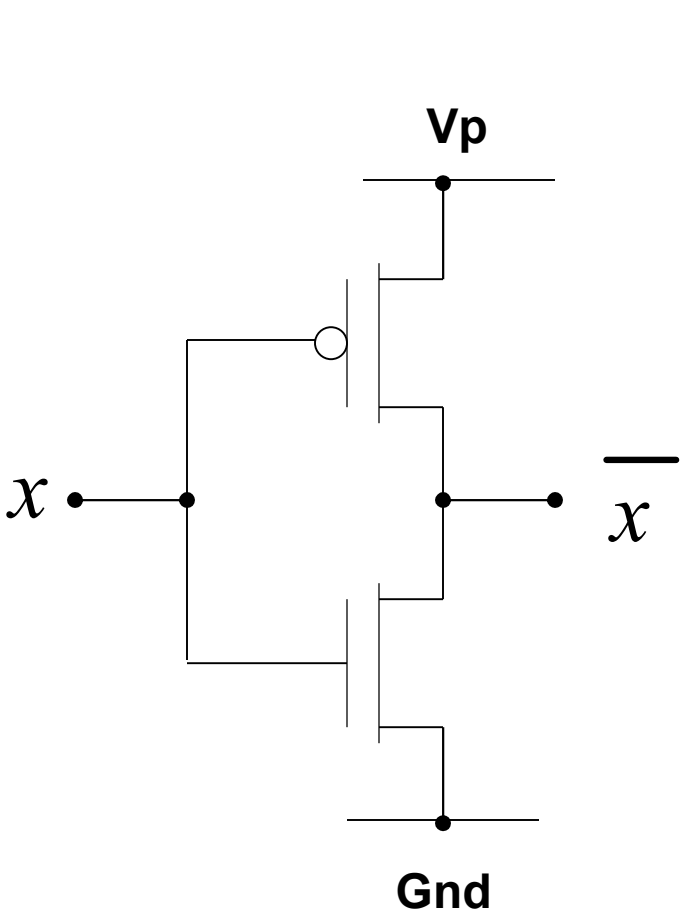


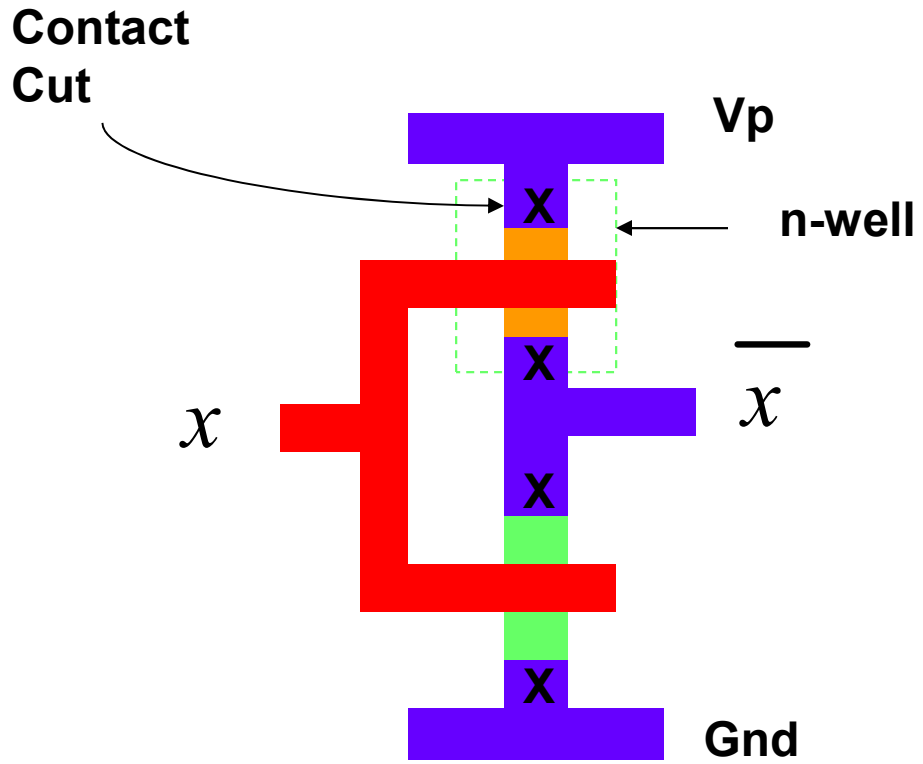


Basic Gate Design

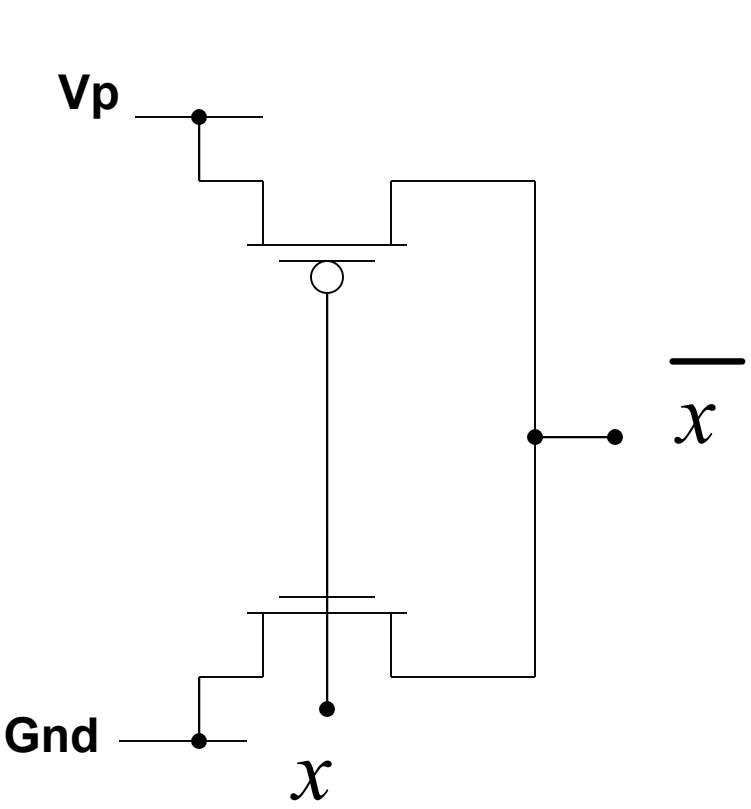
- Both the power supply and ground are routed using the Metal layer
- n+ and p+ regions are denoted using the same fill pattern. The only difference is the n-well
- Contacts are needed from Metal to n+ or p+

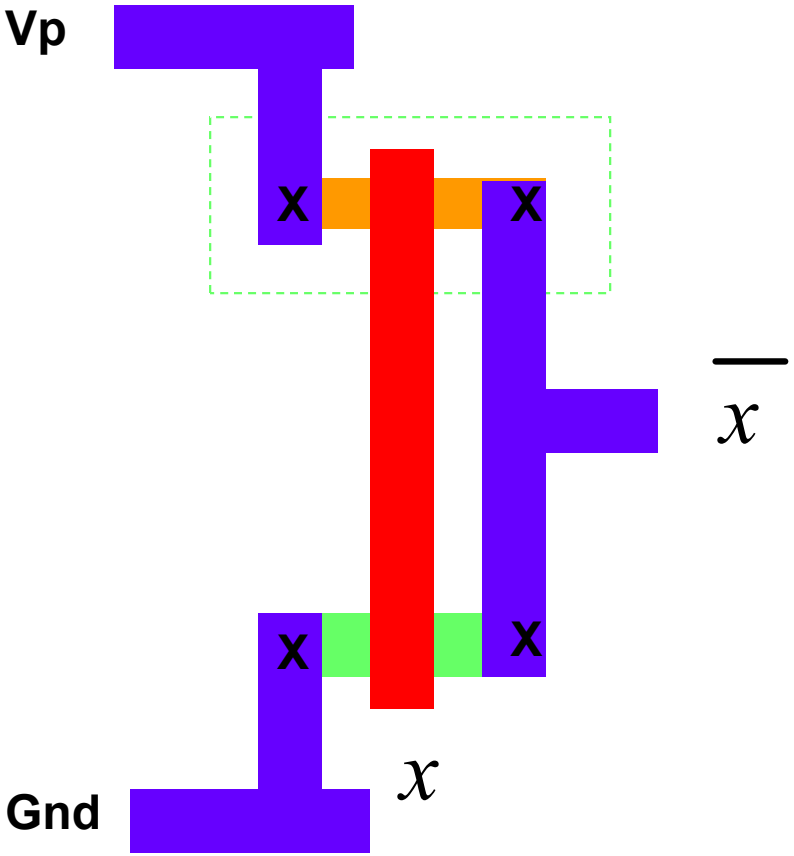
The CMOS NOT Gate



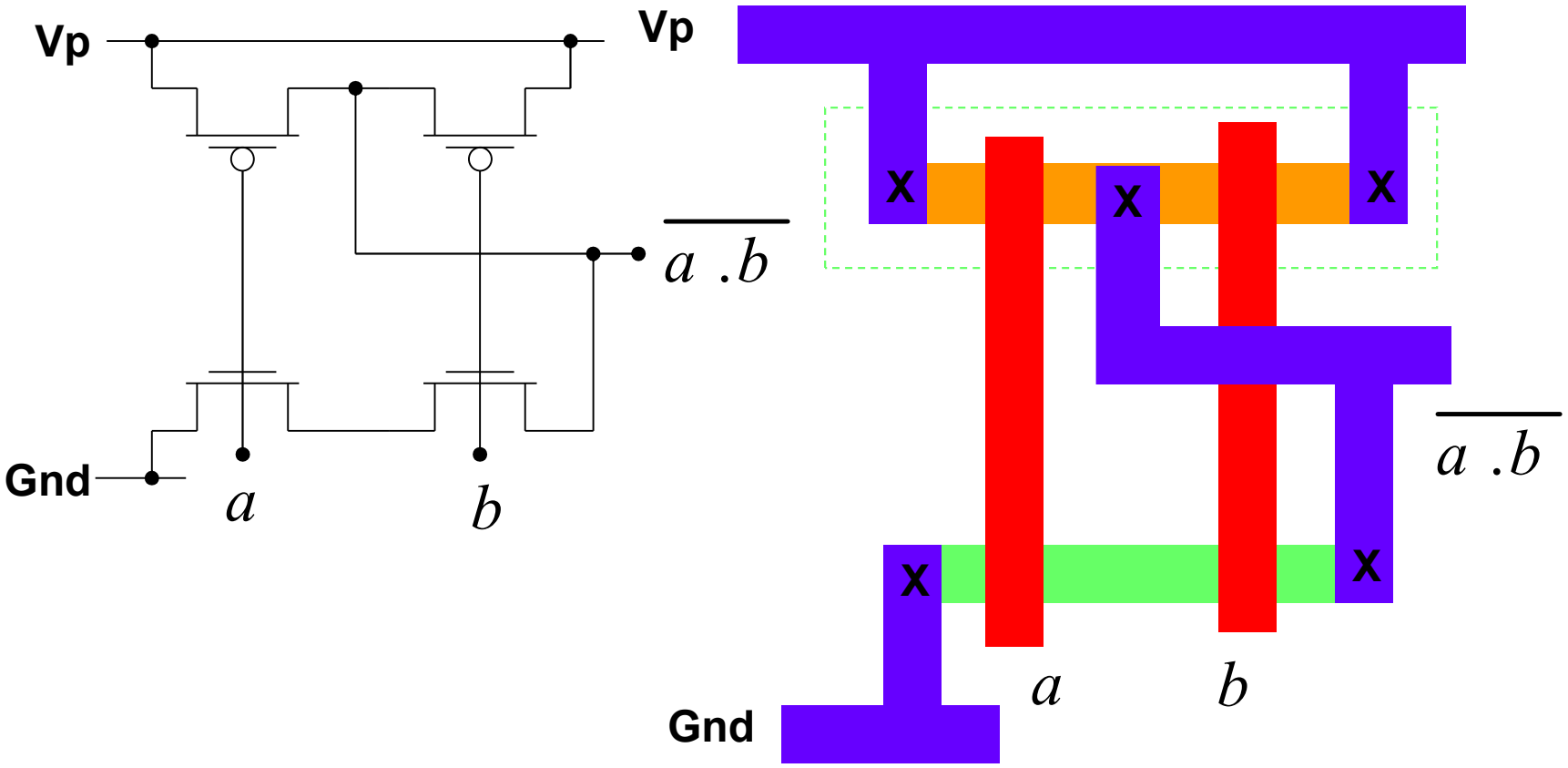


Alternate Layout of NOT Gate

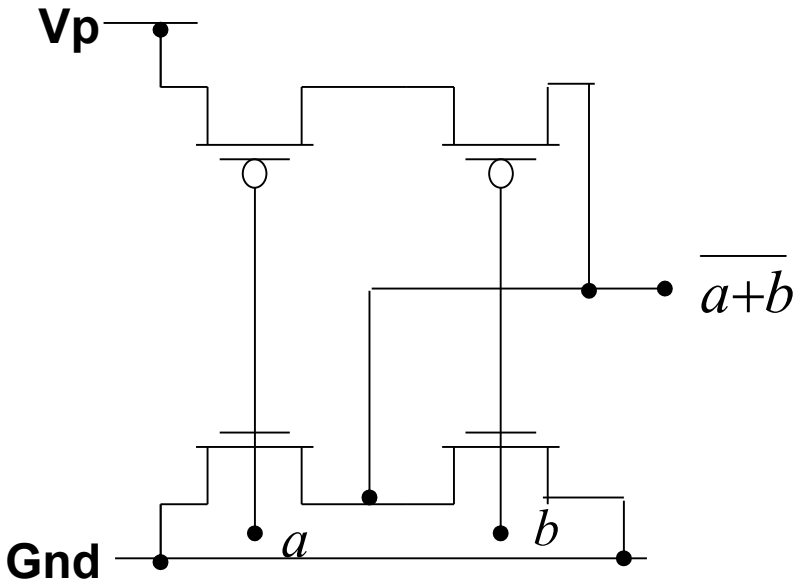


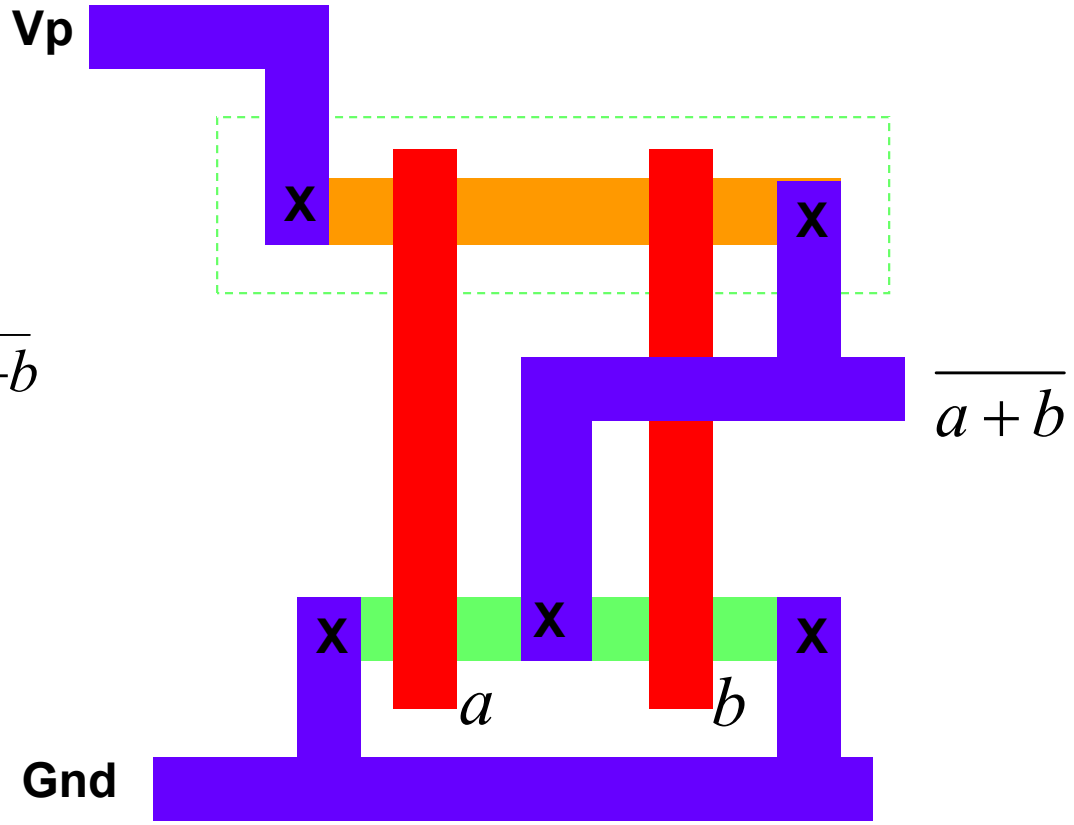


NAND2 Layout

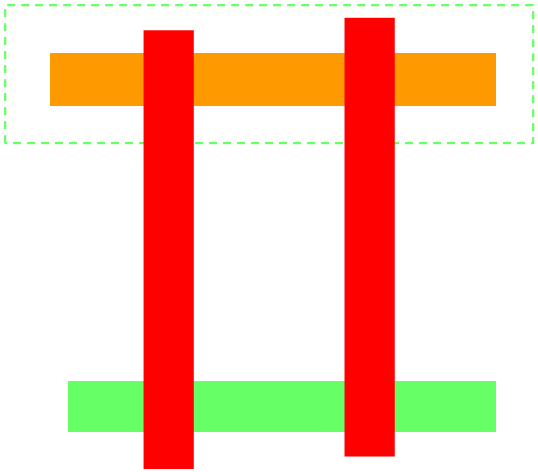


NOR2 Layout



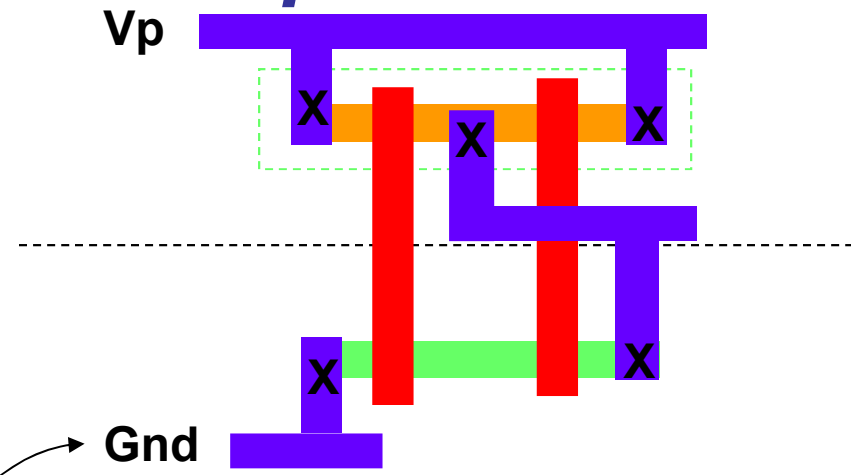


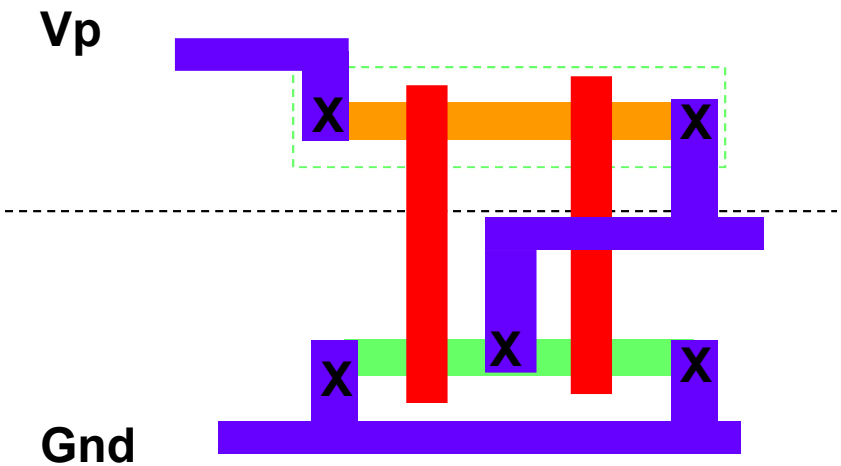
NAND2-NOR2 Comparison



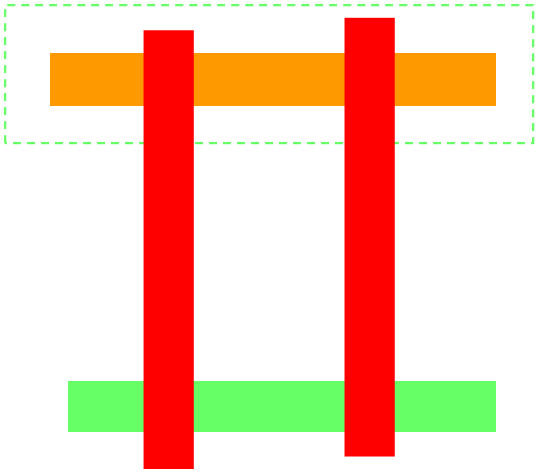
MOS Layout

Wiring



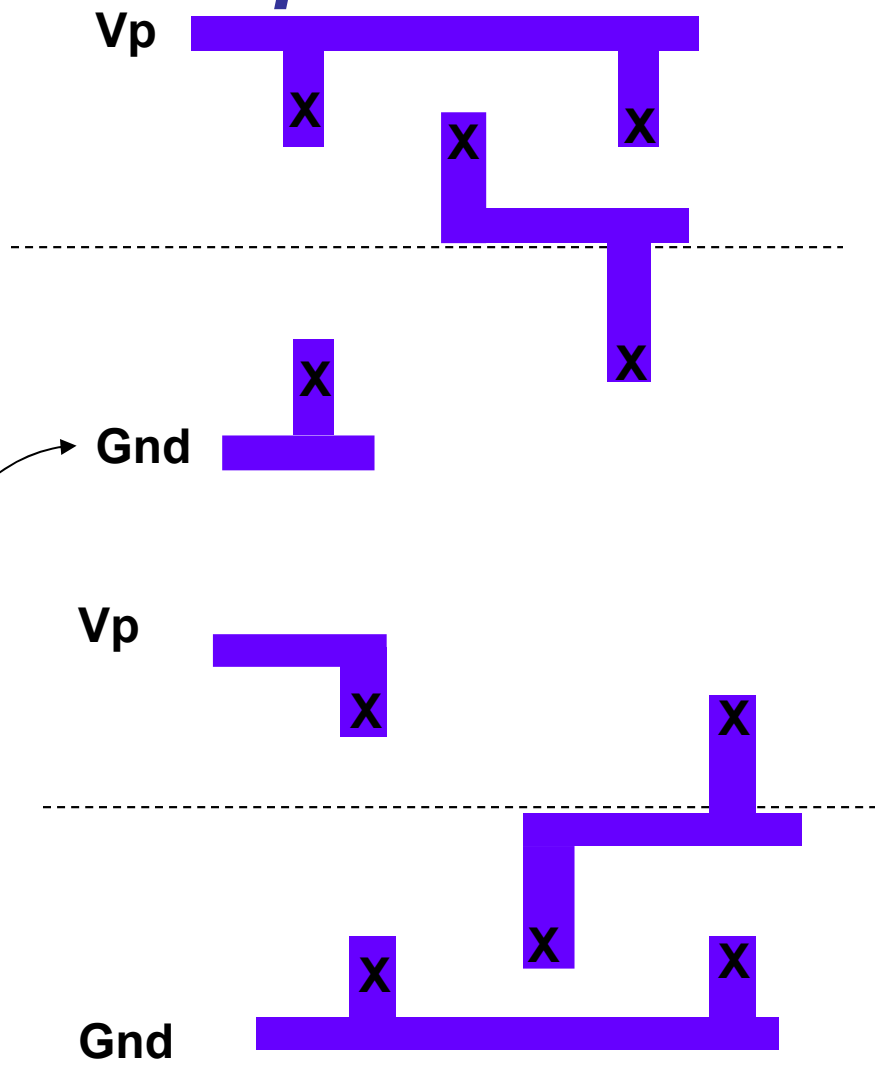


NAND2-NOR2 Comparison

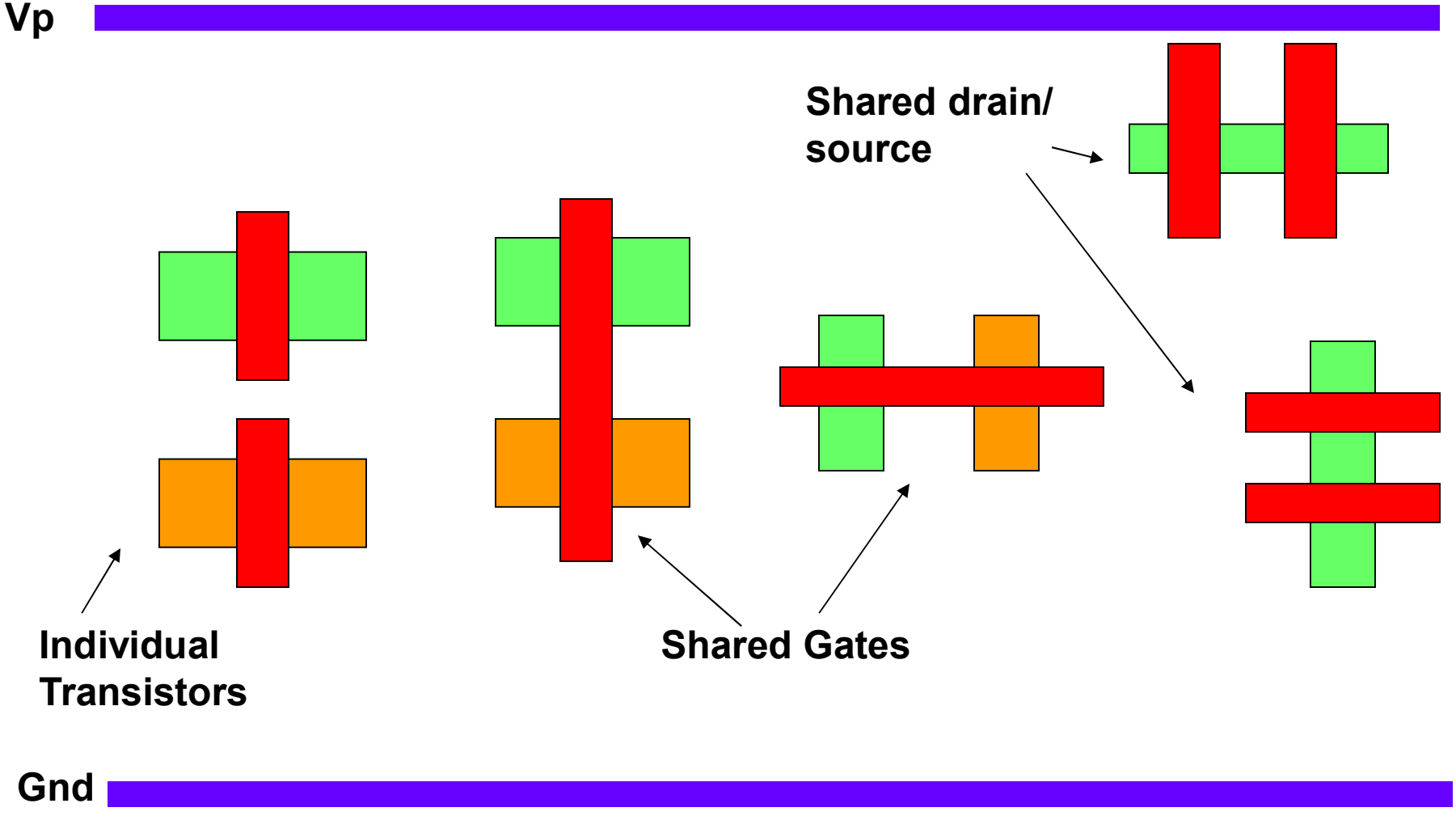


MOS Layout

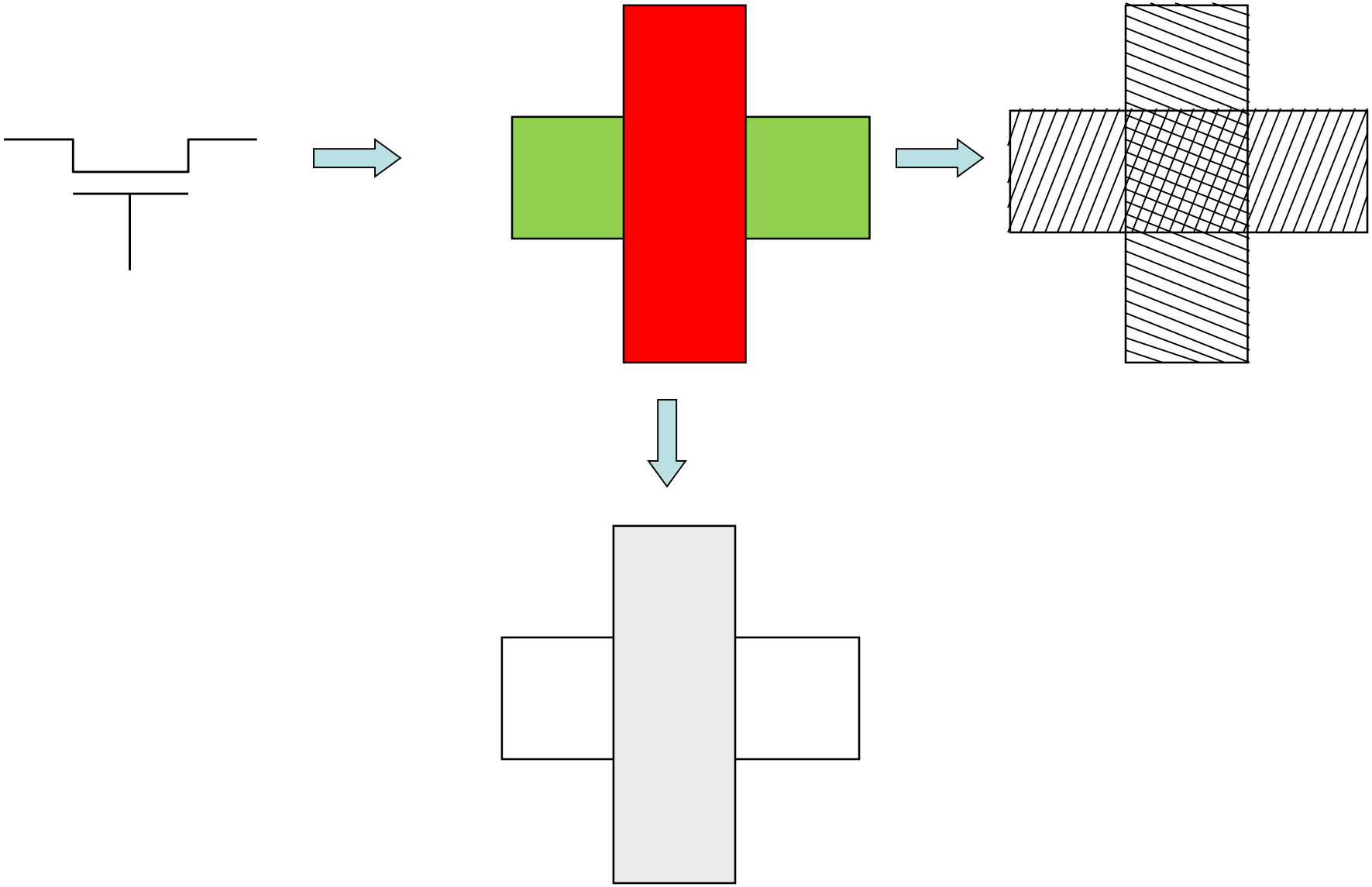
Wiring



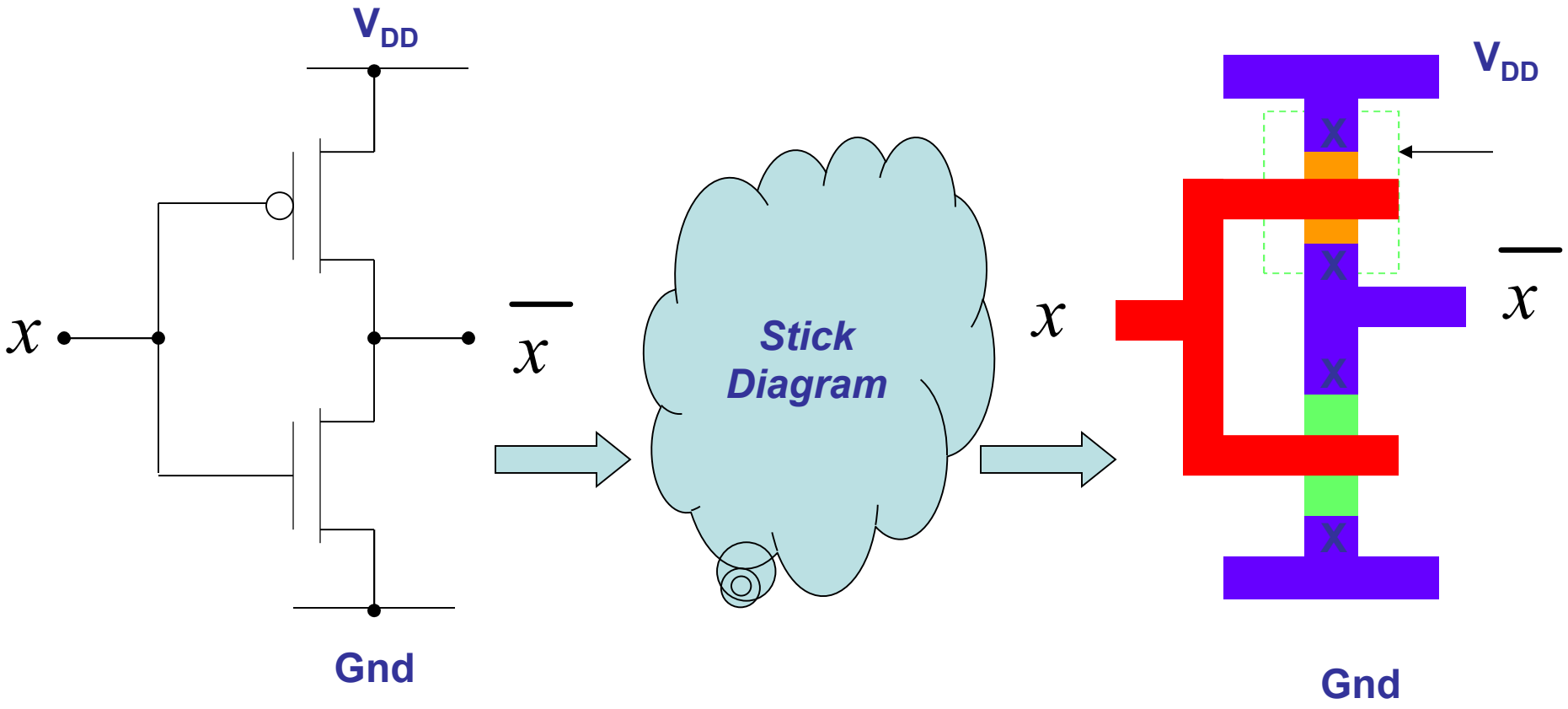
General Layout Geometry



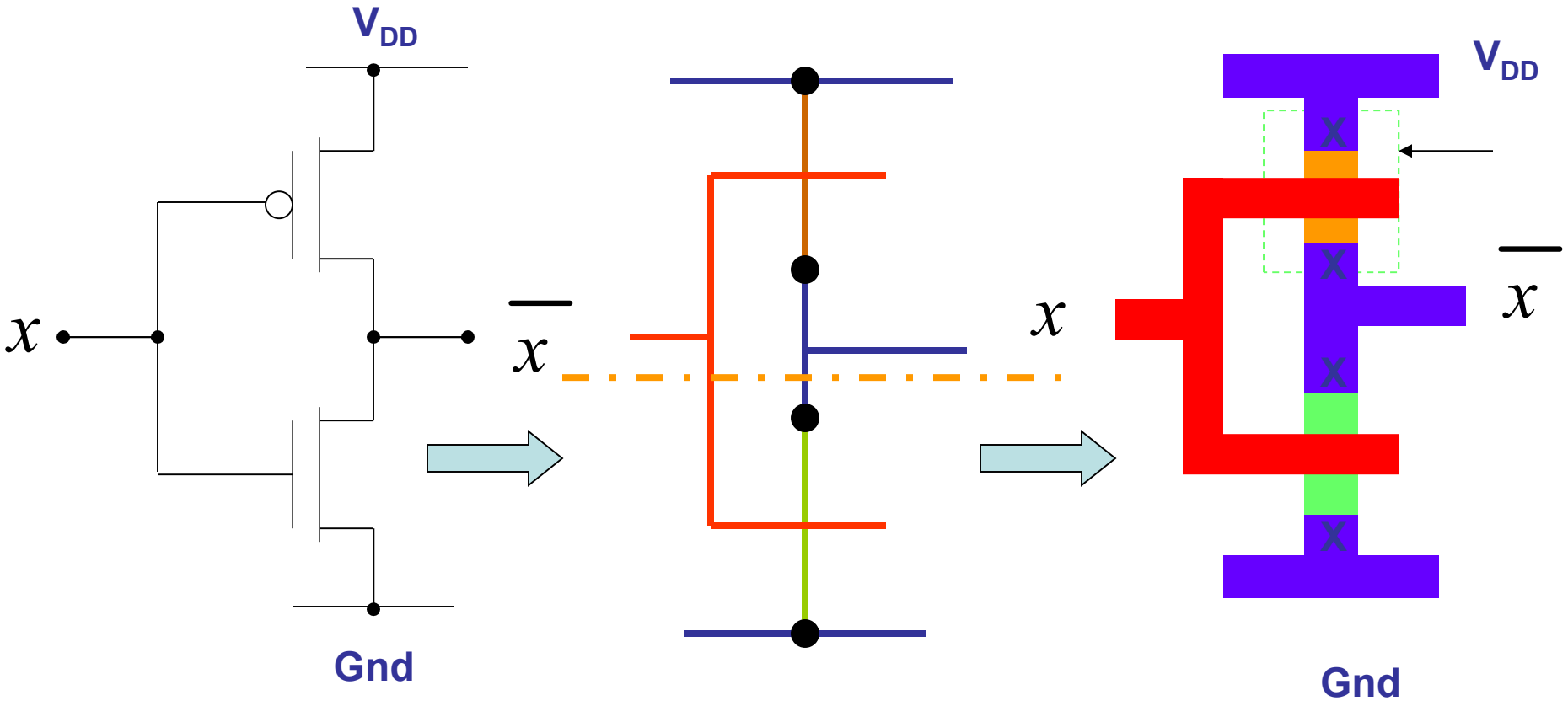
Layout



Stick Diagrams

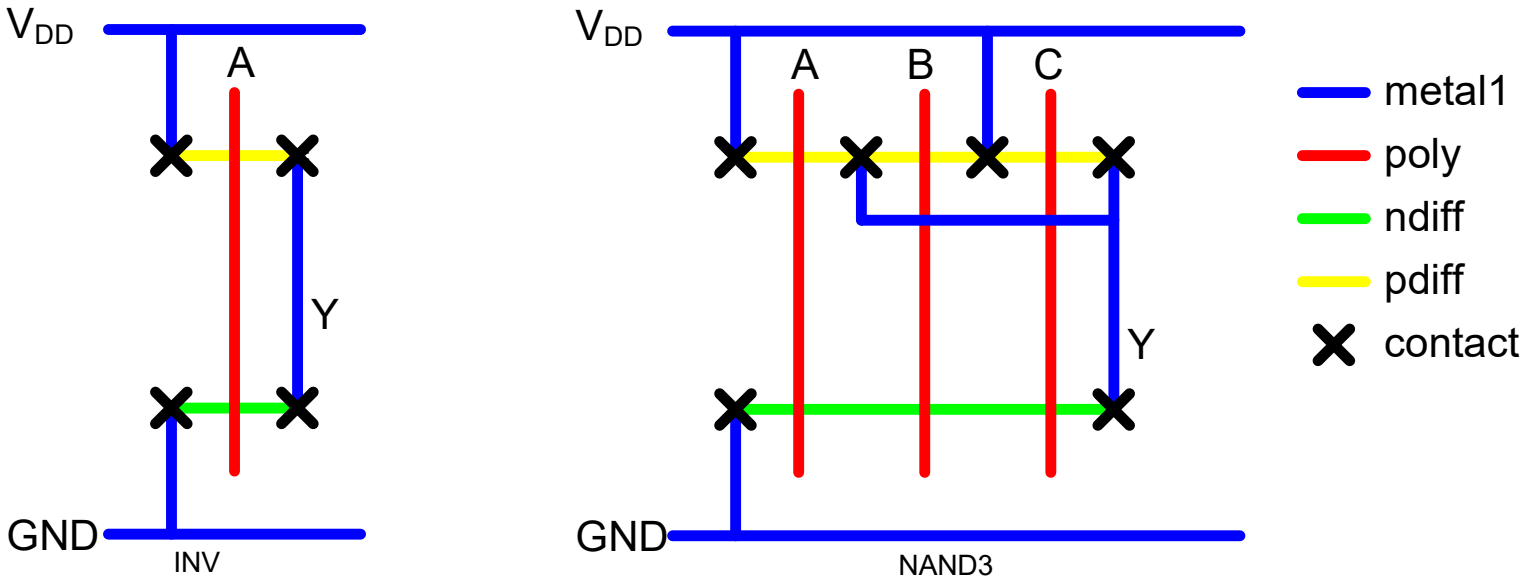


Stick Diagrams



Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers



Stick Diagrams

- VLSI design aims to translate circuit concepts onto silicon.
- stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through colour codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

Stick Diagrams

- Does show all components/vias.
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

A stick diagram is a cartoon of a layout.

Stick Diagrams

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries.
  - Any other low level details such as parasitics..

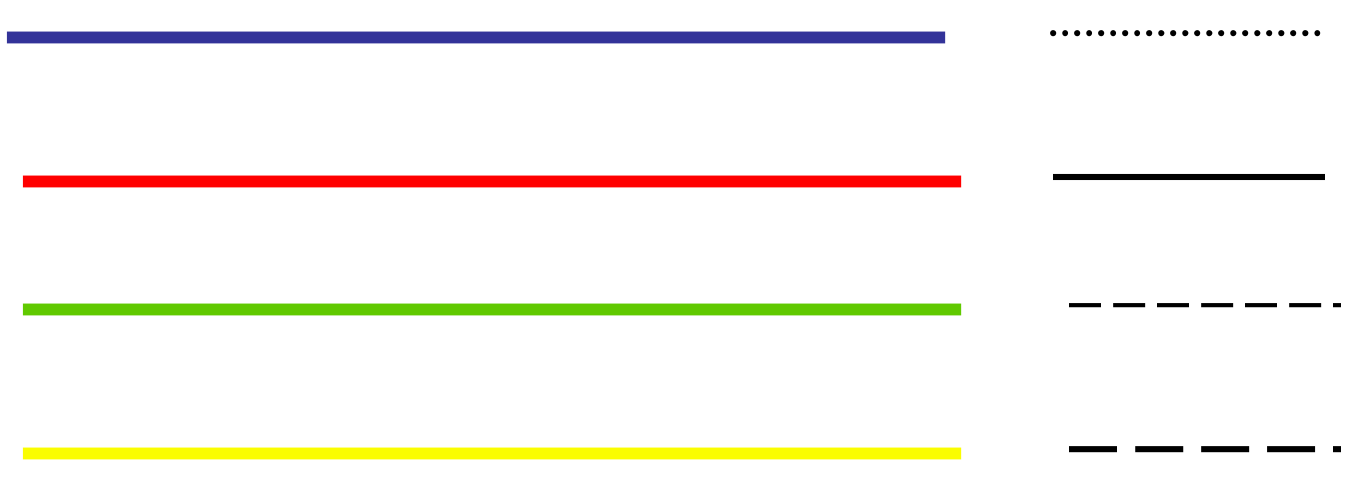
Stick Diagrams

Metal

poly

ndiff

pdiff



Can also draw in shades of gray/line style.

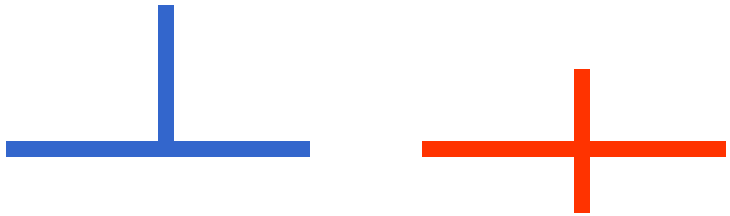
Buried Contact

Contact Cut

Stick Diagrams – Some rules

Rule 1.

When two or more ‘sticks’ of the same type cross or touch each other that represents electrical contact.

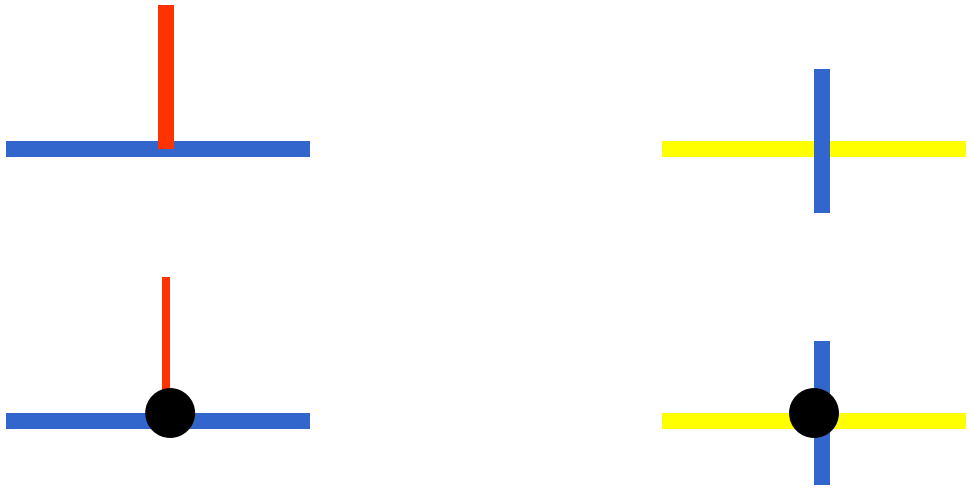


Stick Diagrams – Some rules

Rule 2.

When two or more ‘sticks’ of different type cross or touch each other there is no electrical contact.

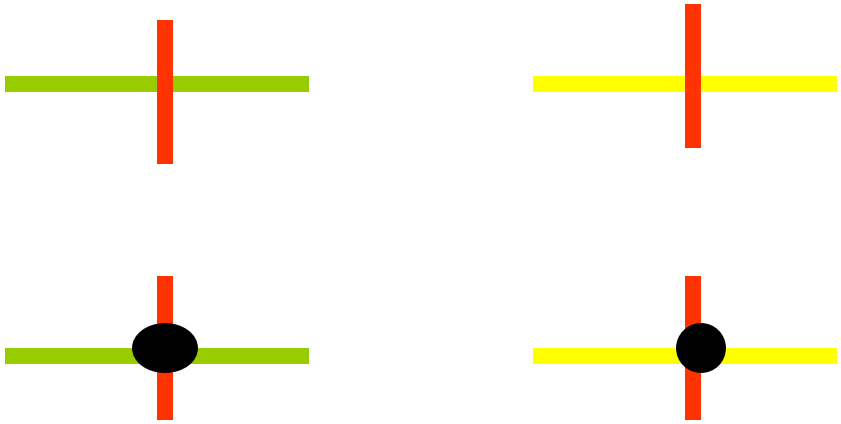
(If electrical contact is needed we have to show the connection explicitly).



Stick Diagrams – Some rules

Rule 3.

When a poly crosses diffusion it represents a transistor.

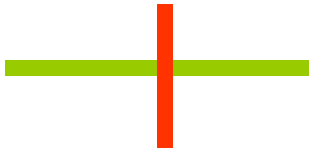


Note: If a contact is shown then it is ***not*** a transistor.

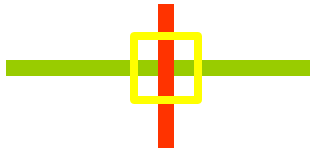
Stick Diagrams

Rule 4.

For depletion mode transistor put a yellow rectangle

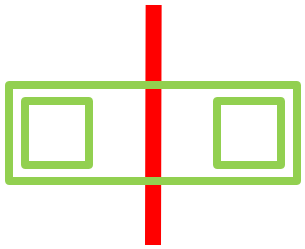


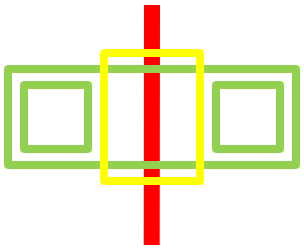
Enhancement type



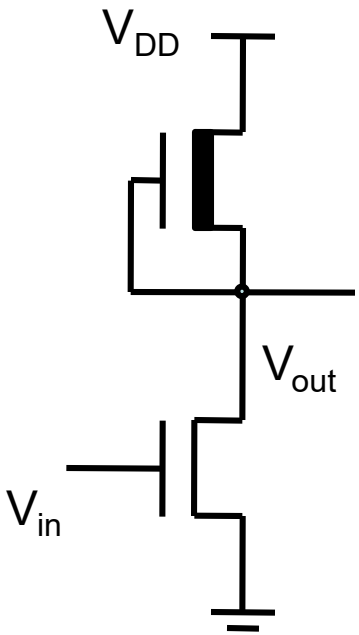
Depletion type

Feature Symbol:

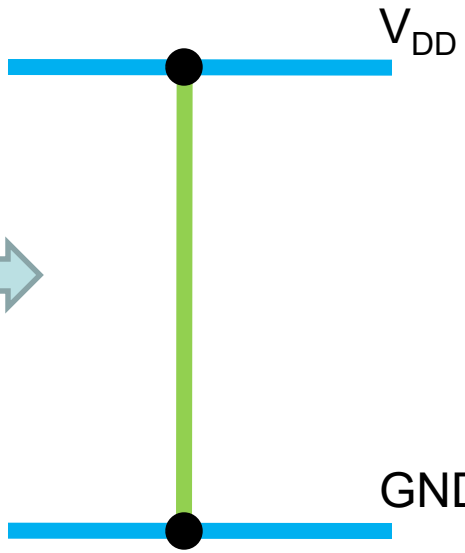


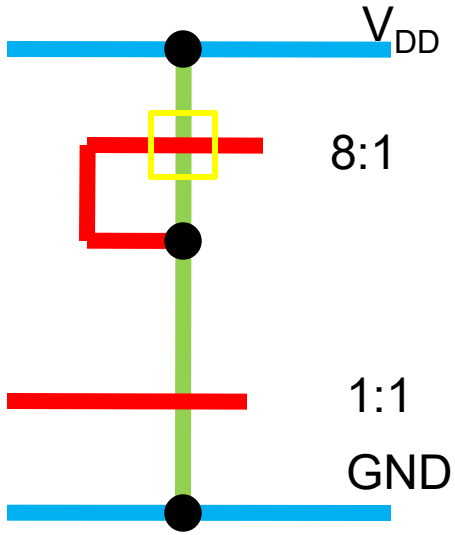


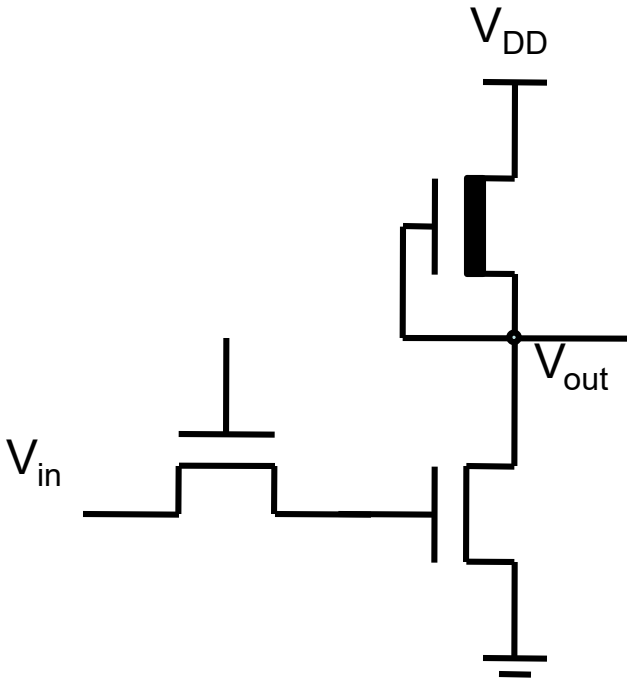
Examples of NMOS Stick layout Design Style

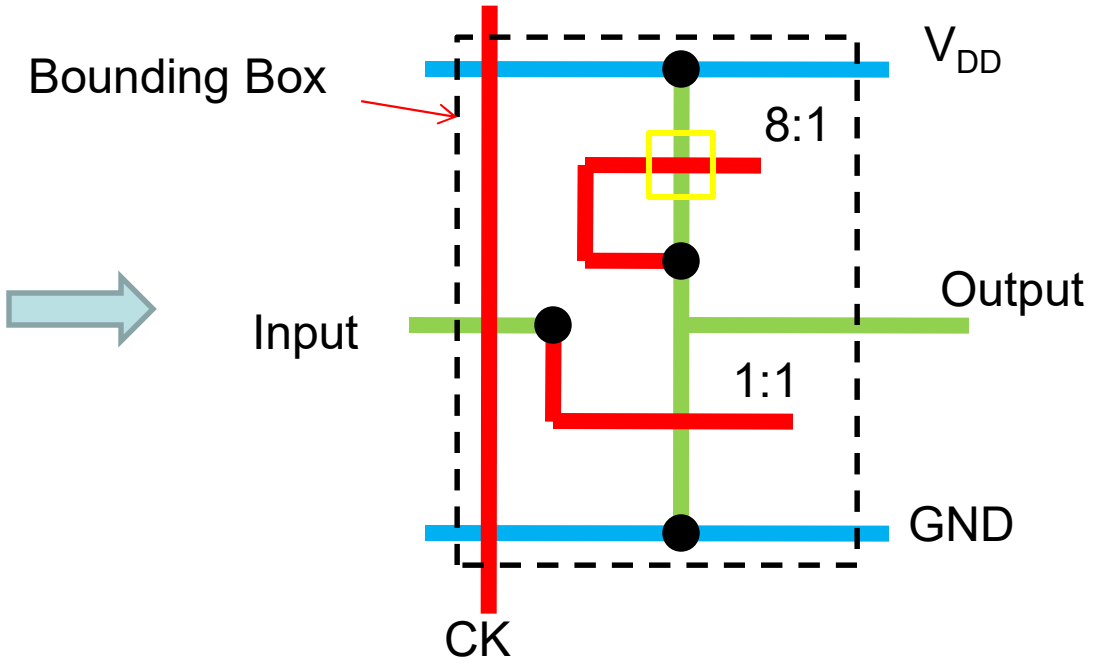


NMOS Inverter

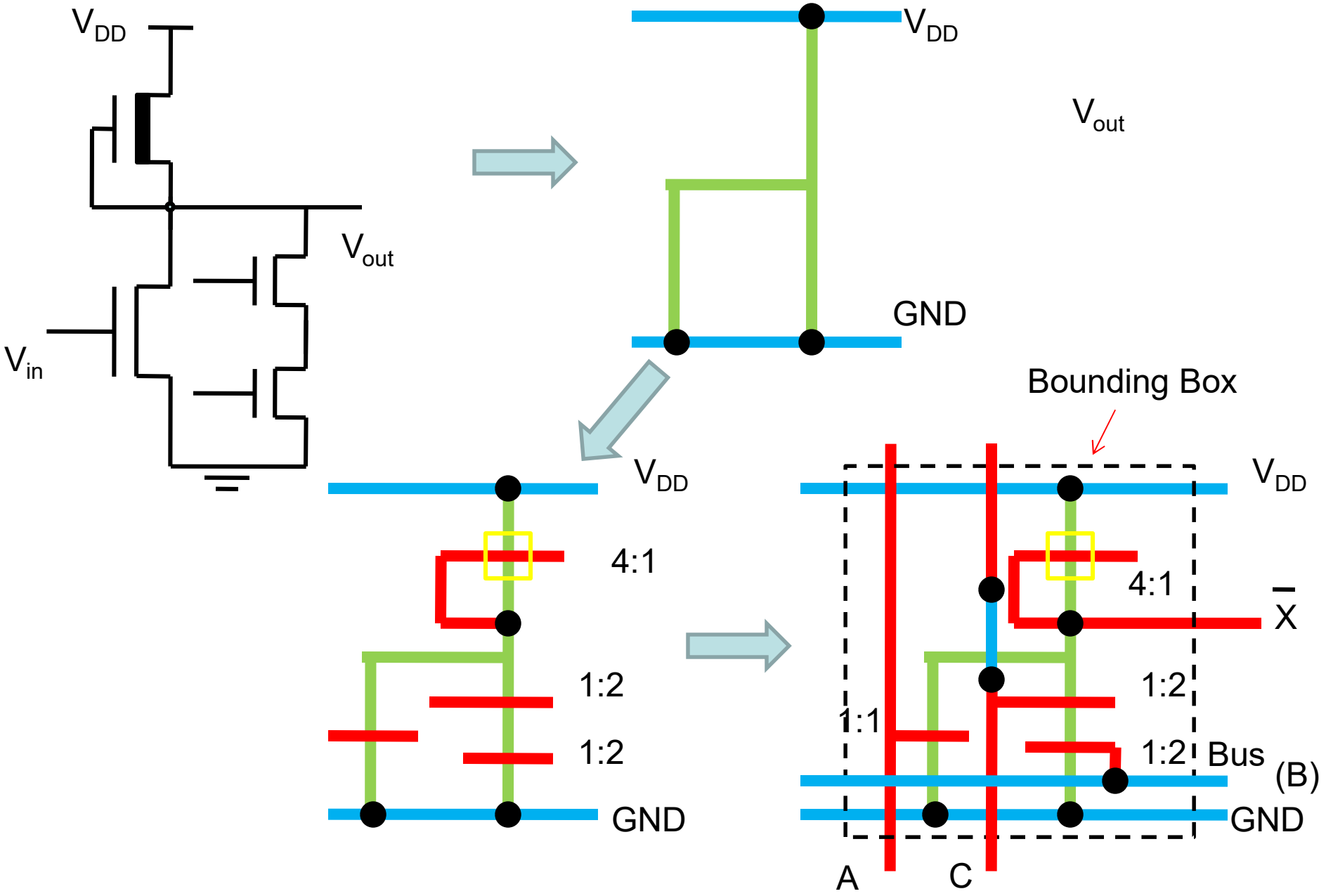








Examples of NMOS Stick layout Design Style: Realizing a logic function $\overline{X} = A + BC$

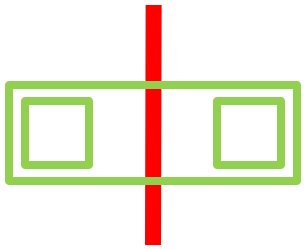


Stick Diagrams – Some rules

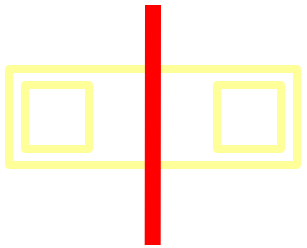
Rule 5.

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.

Feature Symbol:

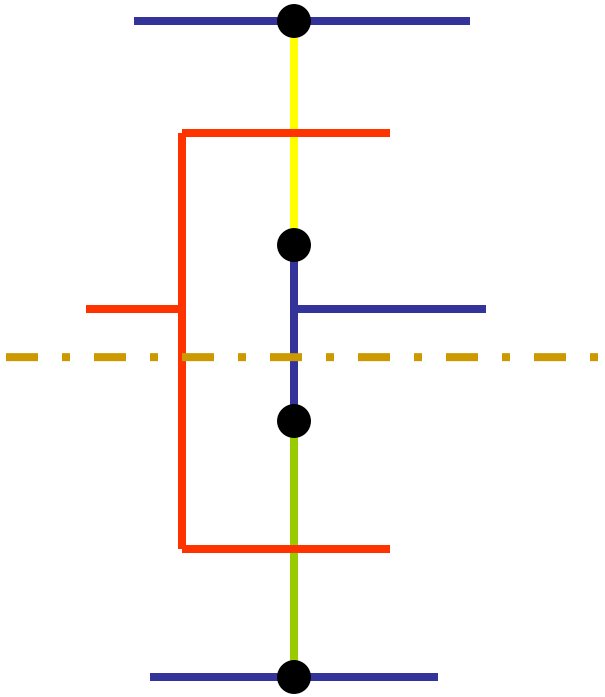


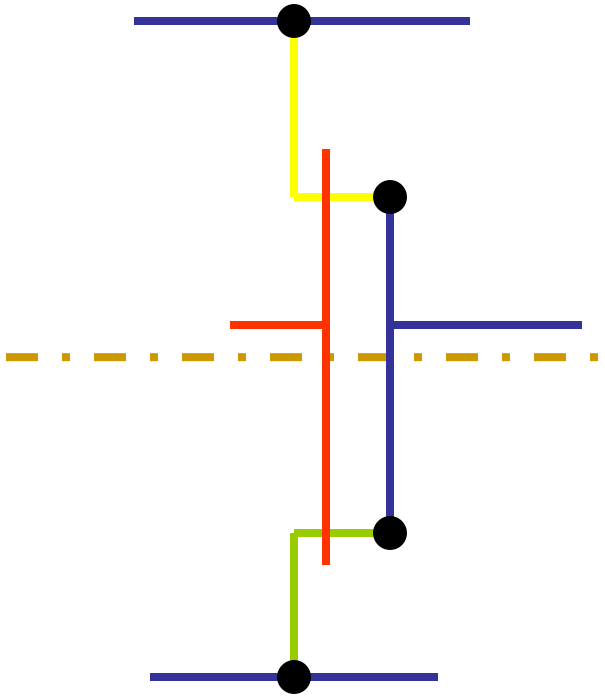
NMOS



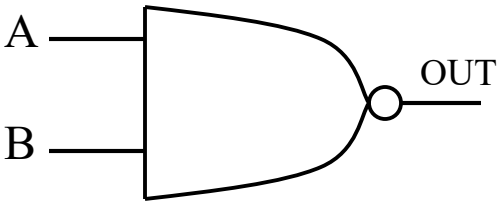
PMOS

How to draw Stick Diagrams

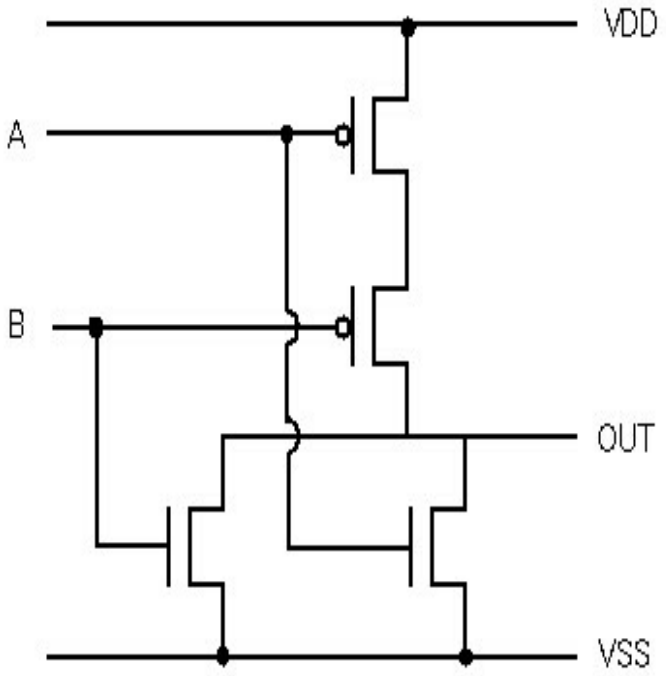




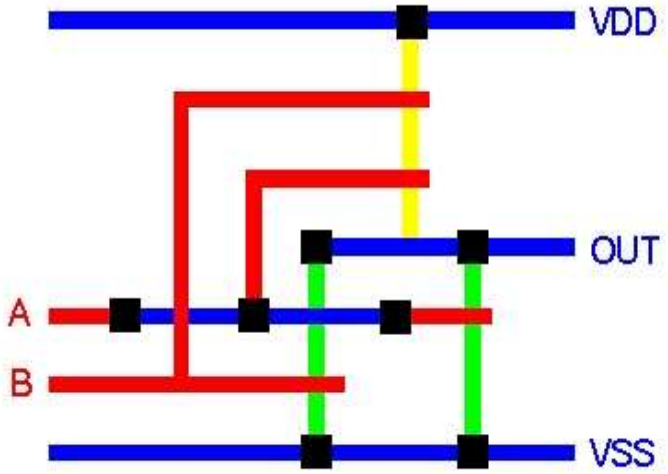
Stick Diagram – Example



NOR Gate

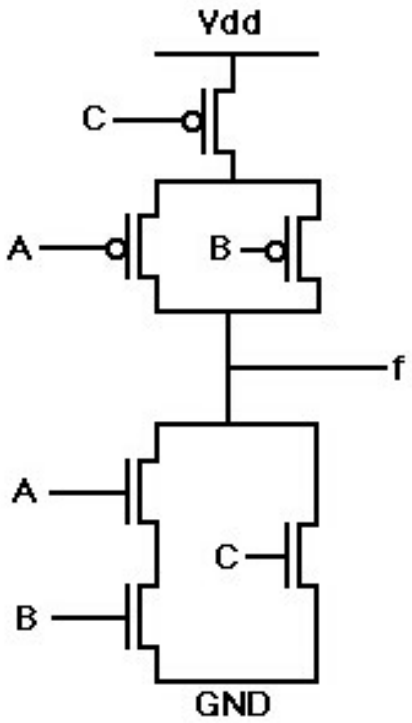


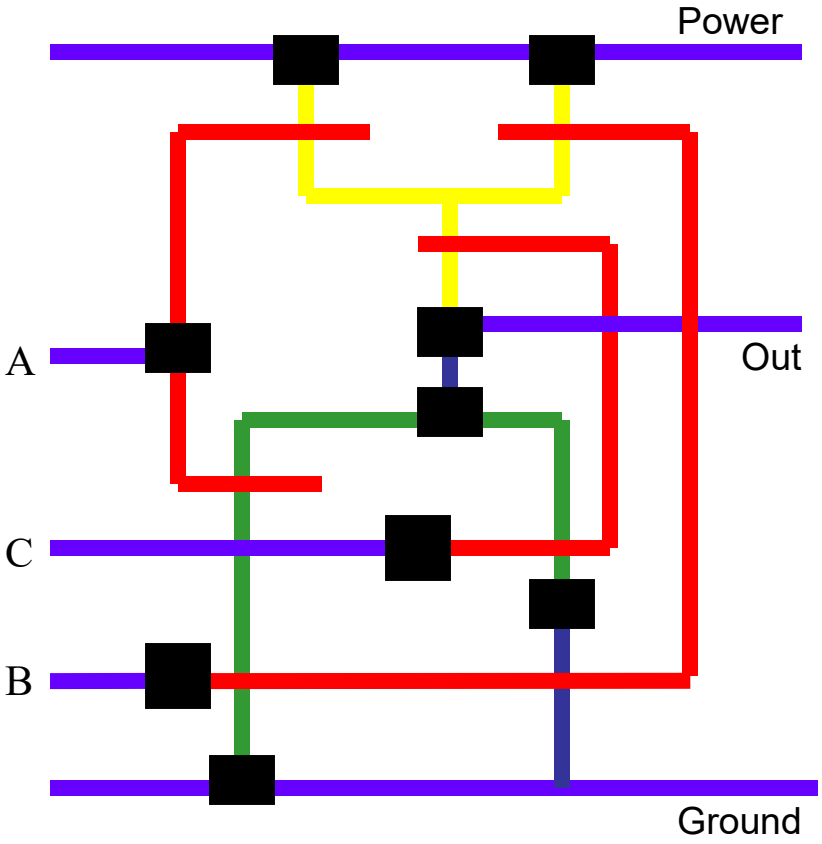
NOR gate in CMOS



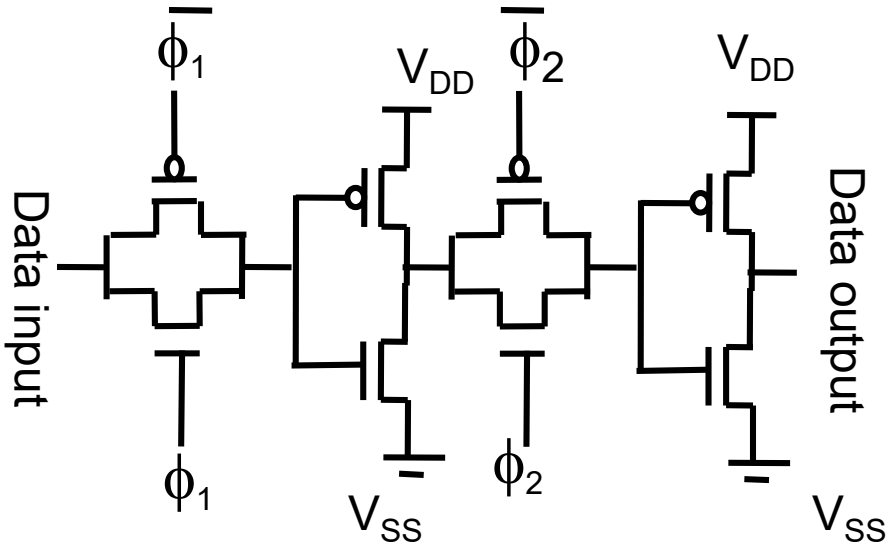
Stick Diagram - Example

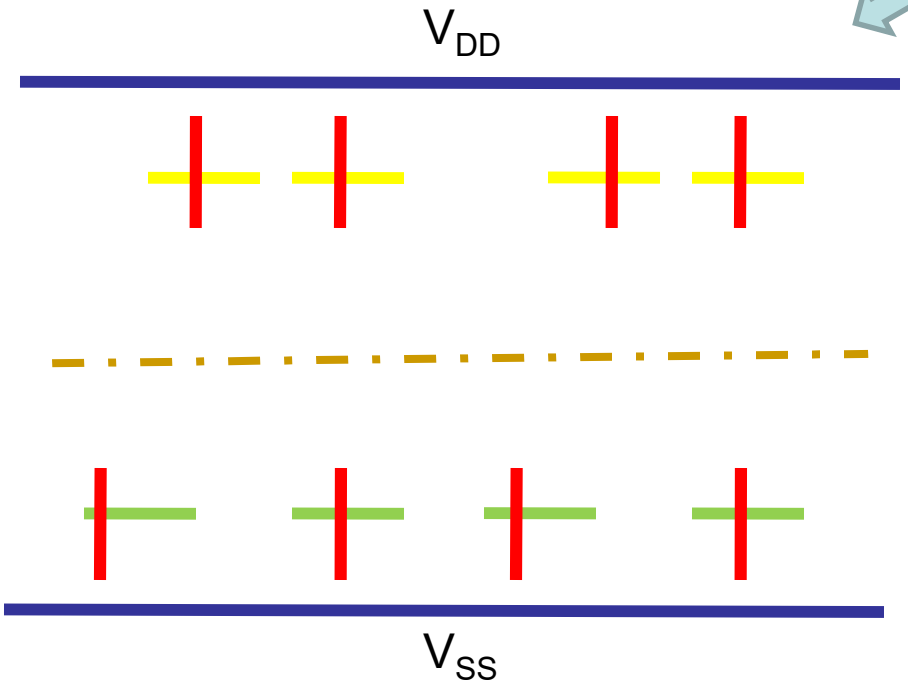
Example: $f = \overline{(A \bullet B) + C}$

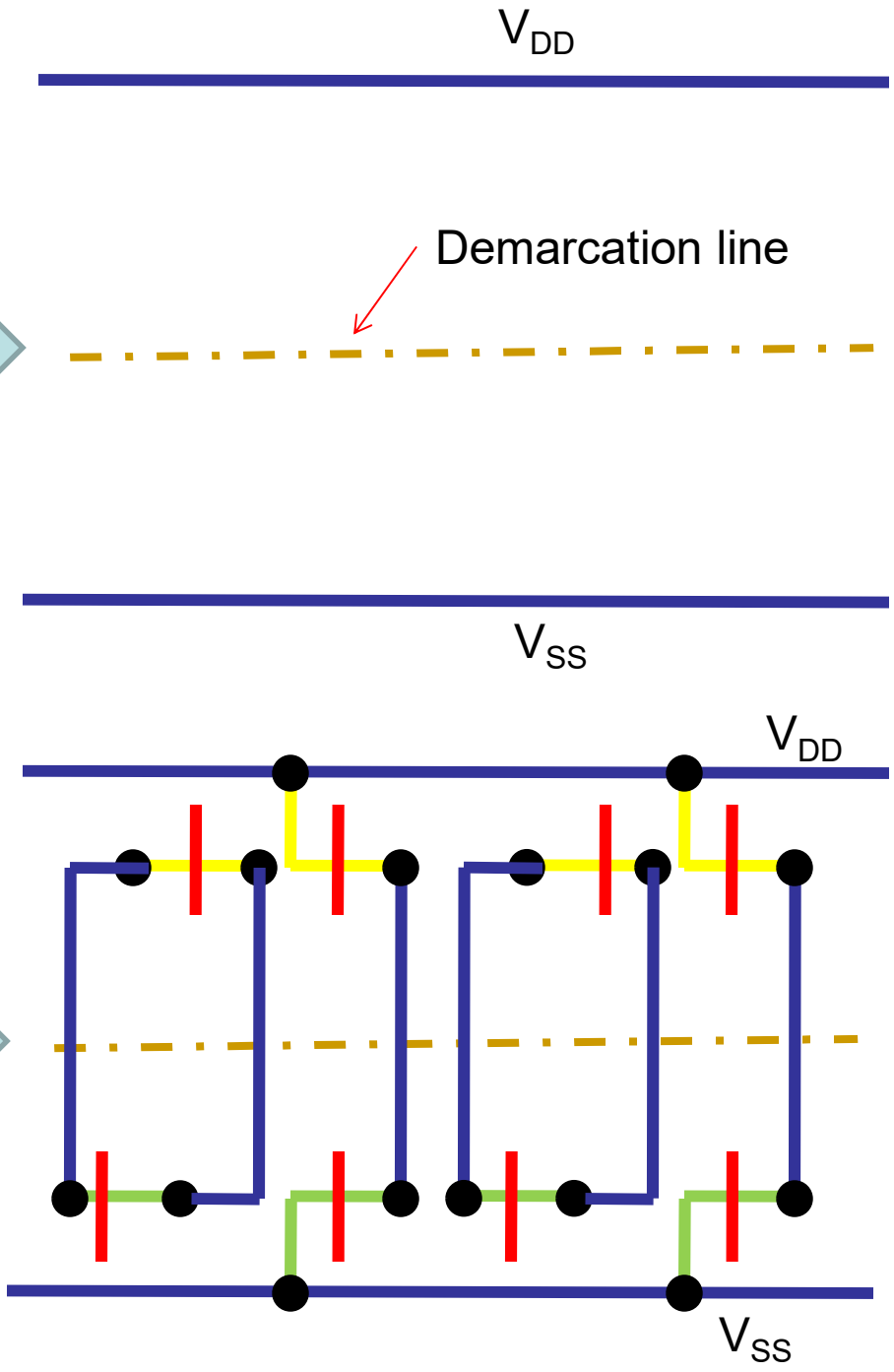




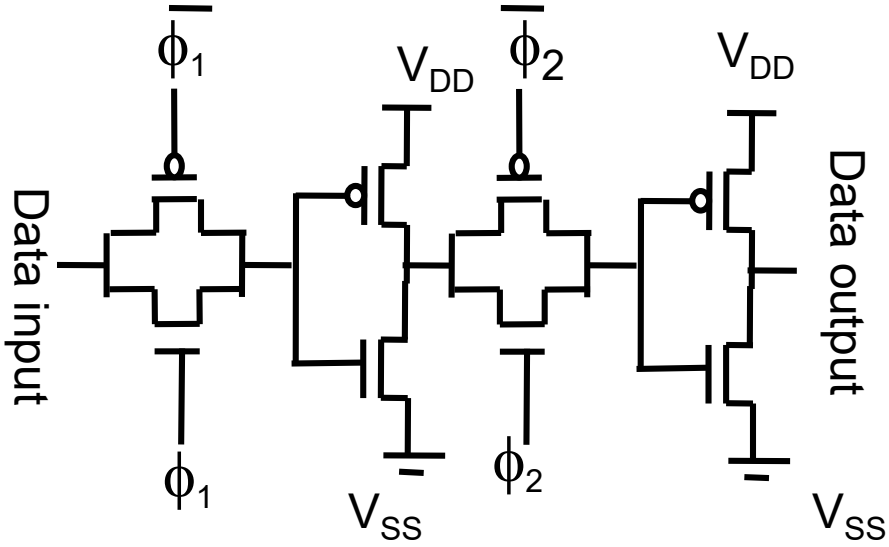
Example: 1 bit shift register

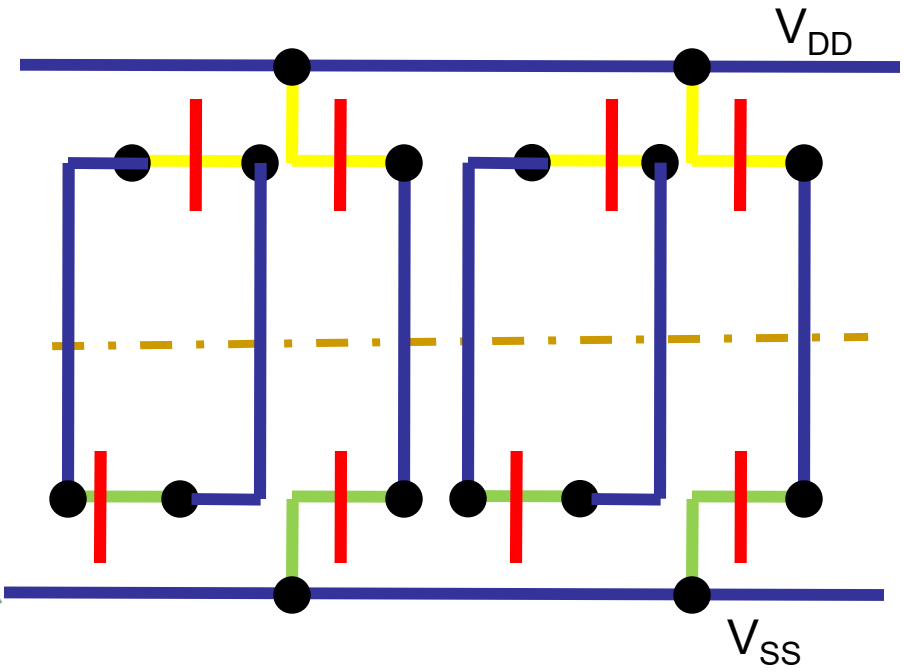


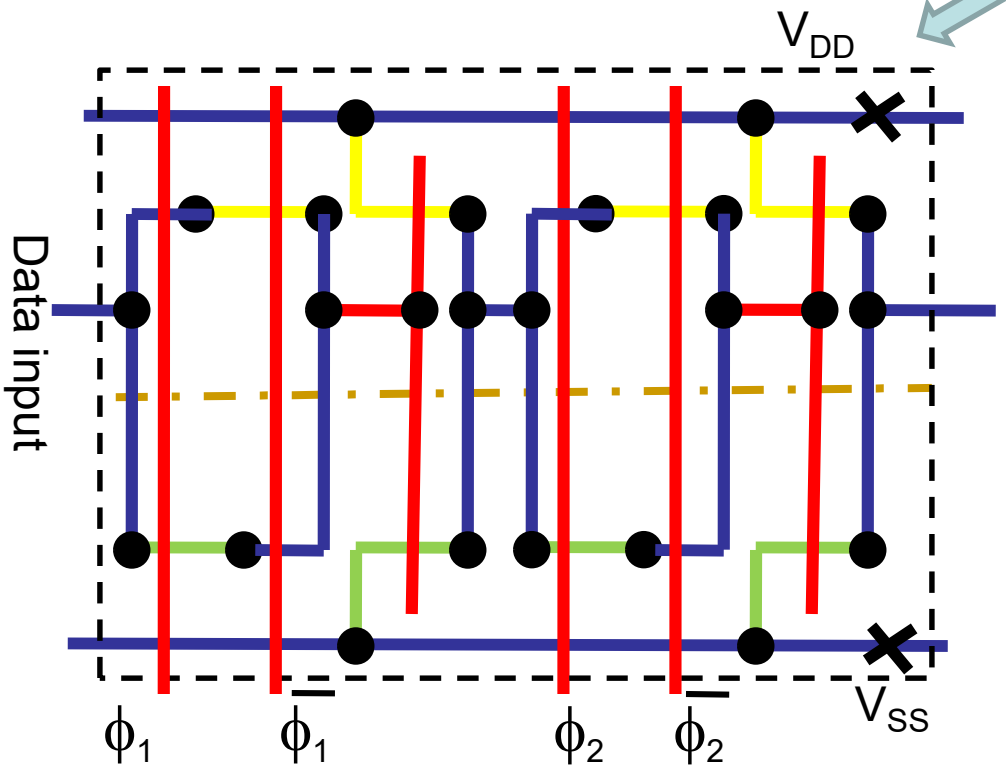




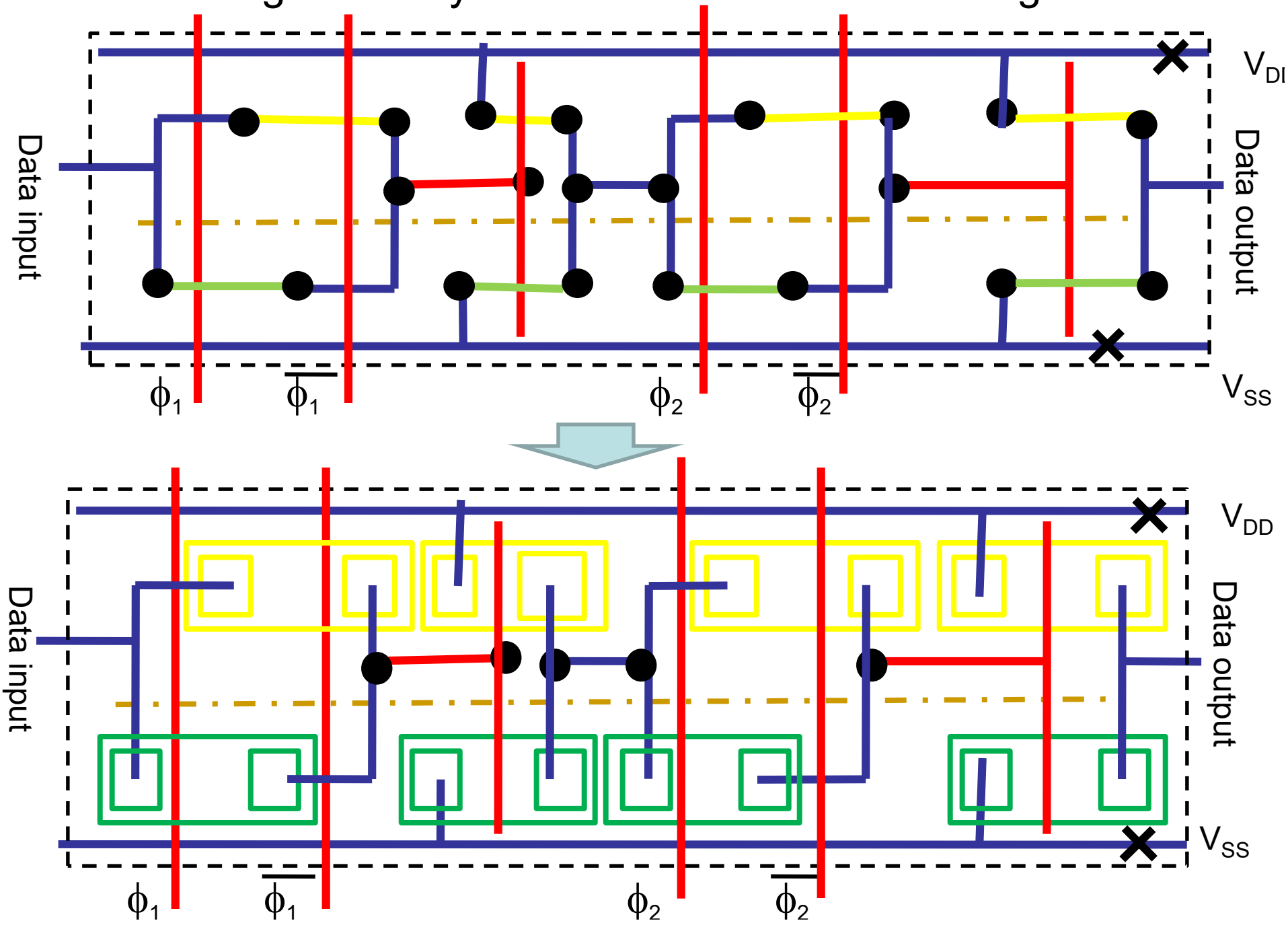
Example: 1 bit shift register



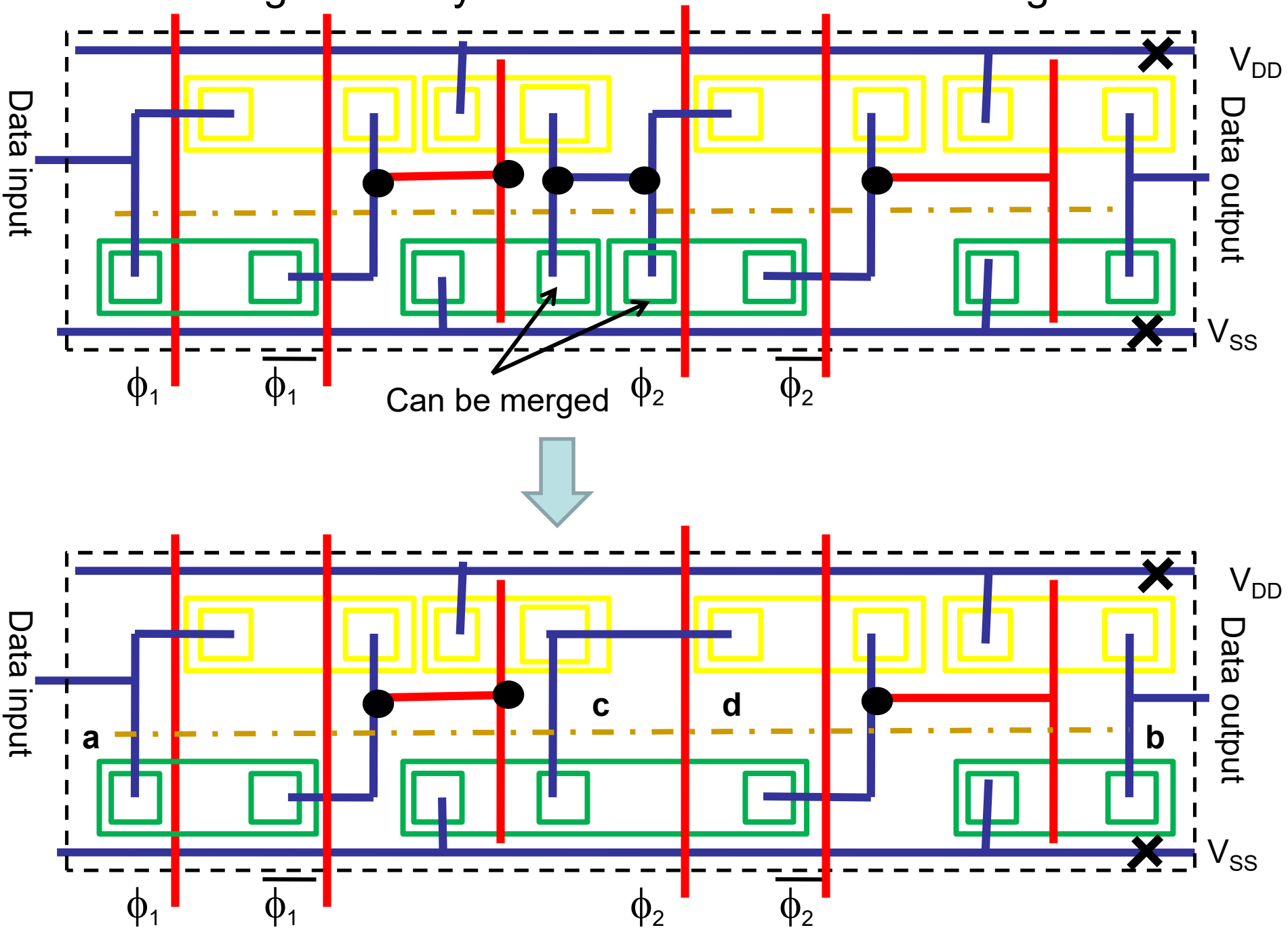




Stick Diagram to Symbolic Form: CMOS shift Register



Stick Diagram to Symbolic Form: CMOS shift Register



Points to Ponder

- be creative with layouts
- sketch designs first
- minimize junctions but avoid long poly runs
- have a floor plan plan for input, output, power and ground locations

Layout Comparison

- Which layout is better?