BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2010

(3rd Year, 1st Semester)

VLSI DESIGN

Time : Three hours Full Marks : 100

Answer any ***five*** questions.

1. a) What is Bi CMOS?
   b) Draw the Circuit diagram of a 3 inpuit Bi CMOS NOR gate and explain its operation.
   c) What is 'latch-up' problem inCMOS?
   d) How can time 'latch-up' problem be prevented?
   c) Draw and explain the operation of an inverting and a non-inverting super buffers. 2+7+2+3+6
2. a) What do you mean by λ- based IC design rules?
   b) Draw the coloured stick and mask diagrams, conforming to the λ- based design rules, for implementing the following Boolean functions, as per instruction given against each :
   i) $A\overline{B} + \overline{A}C + \overline{C}D$ (usingNMOS)
   ii) $(W + \overline{X}).(\overline{y} + Z)$ (usingCMOS) 4 + 2x4 + 2x4
3. a) Prove that the ratios of impedances of the pull-up to pull-down transistors of a standard MOS inverter is 4:1

b) Deduce the condition under which the change over between logic levels of a CMOS inverter is synmetrically disposed about the point at which

$V_{iN} = V_{OUT} = \frac{VDD}{2}$ 12+8

4. a) What will be the value of $\frac{Zpu}{Zpd}$ of a MOS inverter having the following parameters:

V_{the} = Threshold voltage of MOS transistor = 0.25 V_{DD},

Where V_{DD} is the inverter's supply volatge and V_{IMV} = Logic threshold voltage of the inverter = 0.475 V_{DD}.

b) Implement the following Boolean function with the help of a precharge n MoS circuit :

$\overline{W}\, x\, Y + W\, \overline{X} + W\, \overline{Y}\, Z$

c) Draw the diagram of a 3 input precharge CMOS NAND gate and explain its operation. 8+6+6

5. a) State with colour diagrams the λ besed IC design rules of the following :

i) Seperation between two n wells having name potential.

ii) Via Contact from metal 2 to metal 1 and trance to a polysilicon layer.

iii) Extension of polysilicon beyond diffusion boundaries and the distance from polysilicon layer where the diffusion layer can be shortened.

iv) Width and separation between two metal 2 layers.

v) Width and seperation between two polysilicon layers.

vi) Give the VHDL description of a master-slave J-K flip-flop. 3x5 + 5

6. a) Discuss the following algorithms for placement/ routing of VLSI components :

i) Min - cut

ii) Left edge.

b) Compare the relative merits and demerits of the customs, semicustoms and gate- array based IC design styles. 2x6 + 8

7. Write short notes on any four of the following :

i) Dry silicon etching

ii) Ga As MES FET

iii) SOI technology

iv) CMOS Domino logic

v) Silicon-gate technology

vi) Aluminium etching. 4x5

———————×———————