Cmos Project Report

Title: VLSI Design Project
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Submitted by:

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Table of contents:

Introduction:

Here this project mainly deals with how to design Combinational logics using cmos technology and then integrate them with Sequential circuits by taking consideration of the delays responsible in propagating the data correctly without any error.

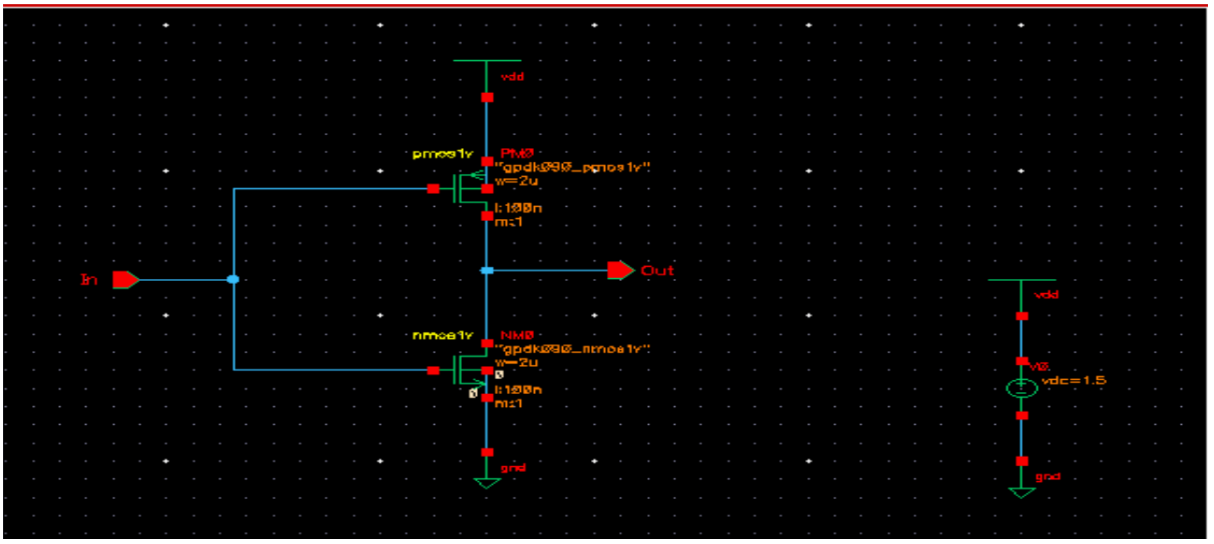
Software Used:
Cadence Virtuoso

Technology used:
90nm meter Technology.

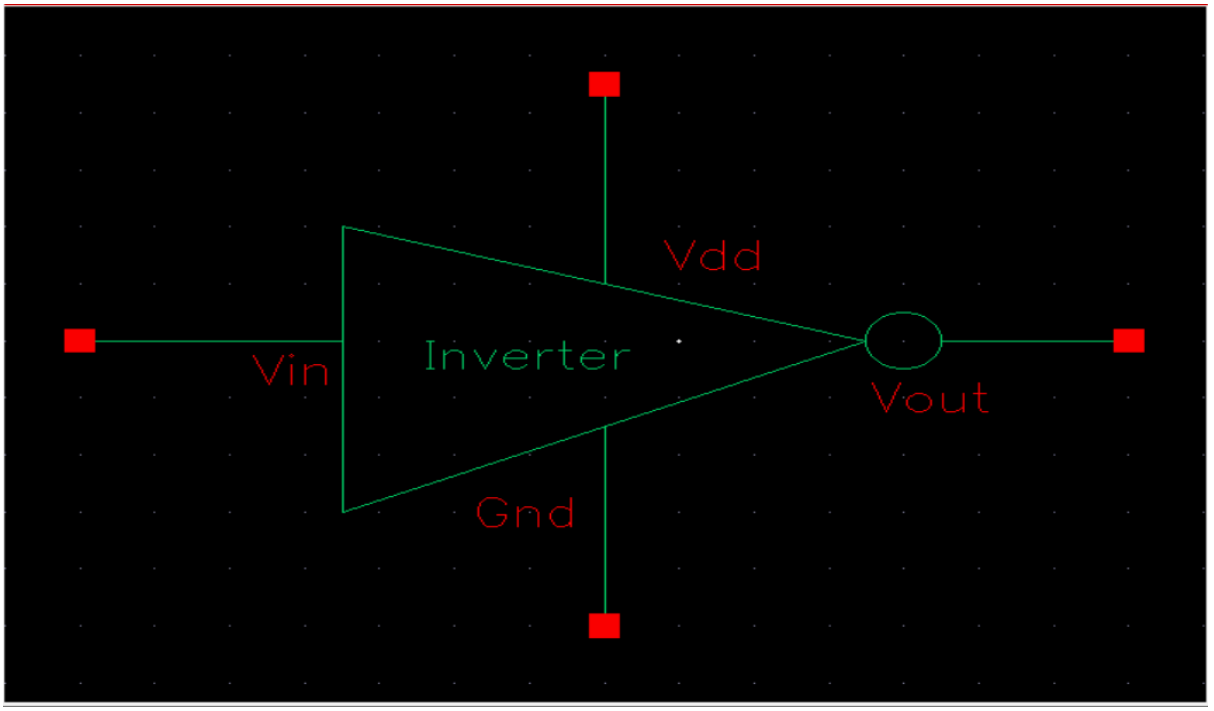
Parameters and Sizinges used:
Vdd = 1.5 V.
Width of channel (W) = 120 n meters.
Length of the channel used = 120 n meters.

Inverter :

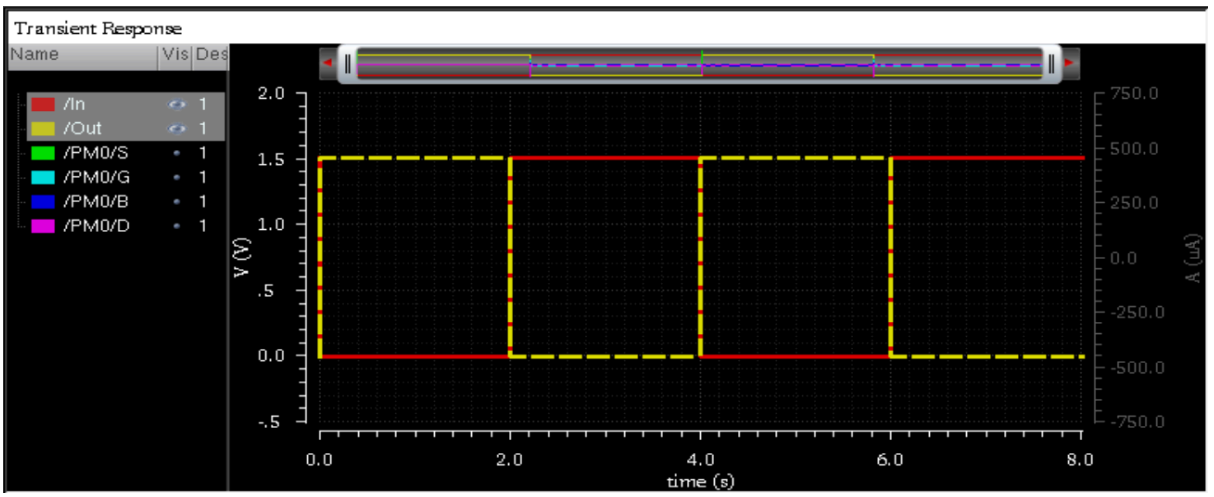
Schematic:



Symbol:



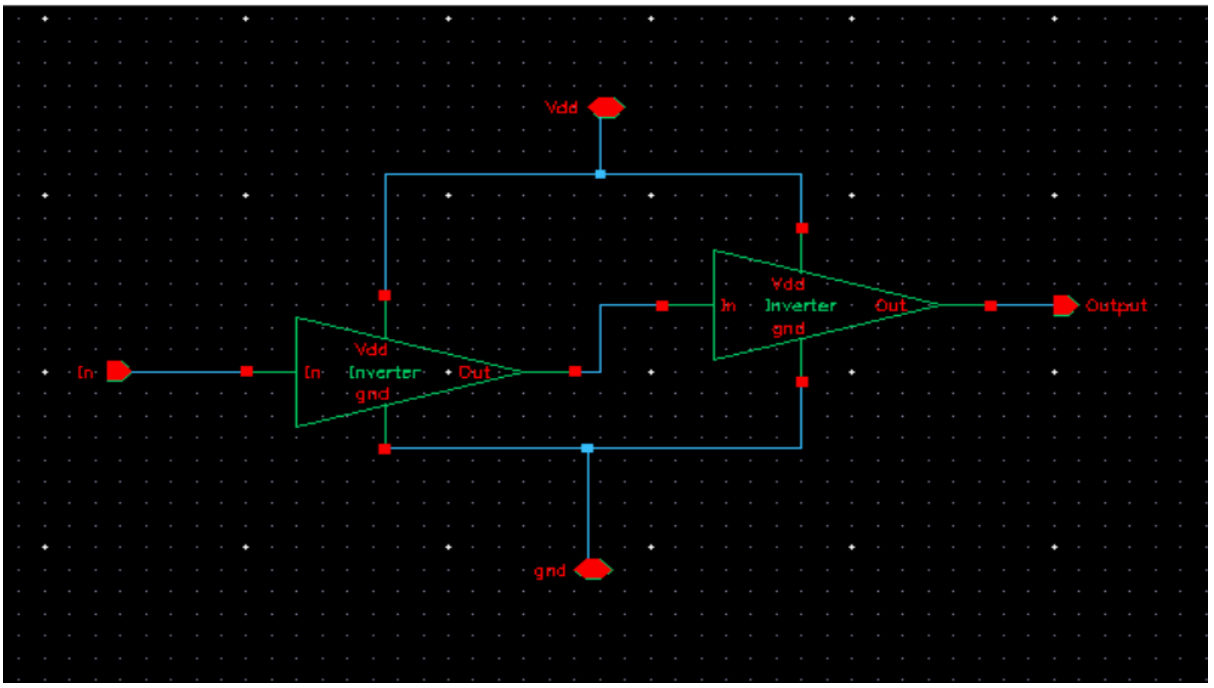
Output Waveform:



Buffer:

Here we use two back to back inverters to form a buffer which gives the same input data after some delay to avoid incorrect data captured and produced at the output side. And also used as a clock buffer to reduce the Clock Skew delay.

Schemantic:



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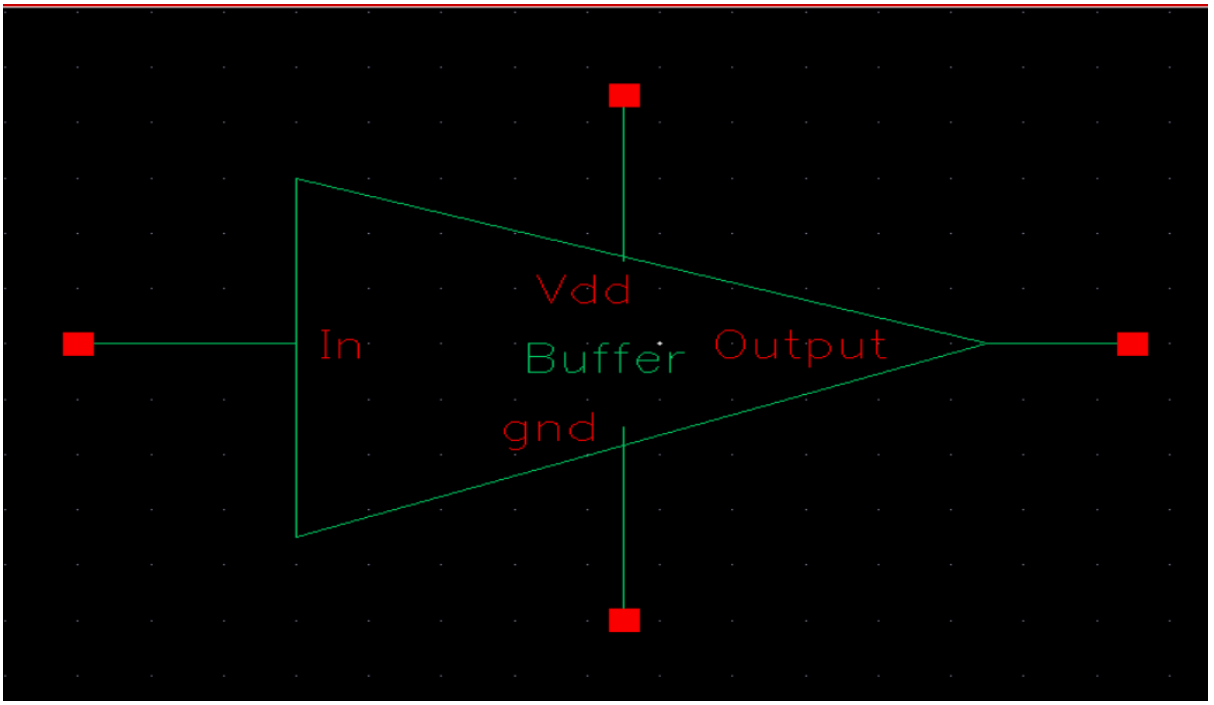
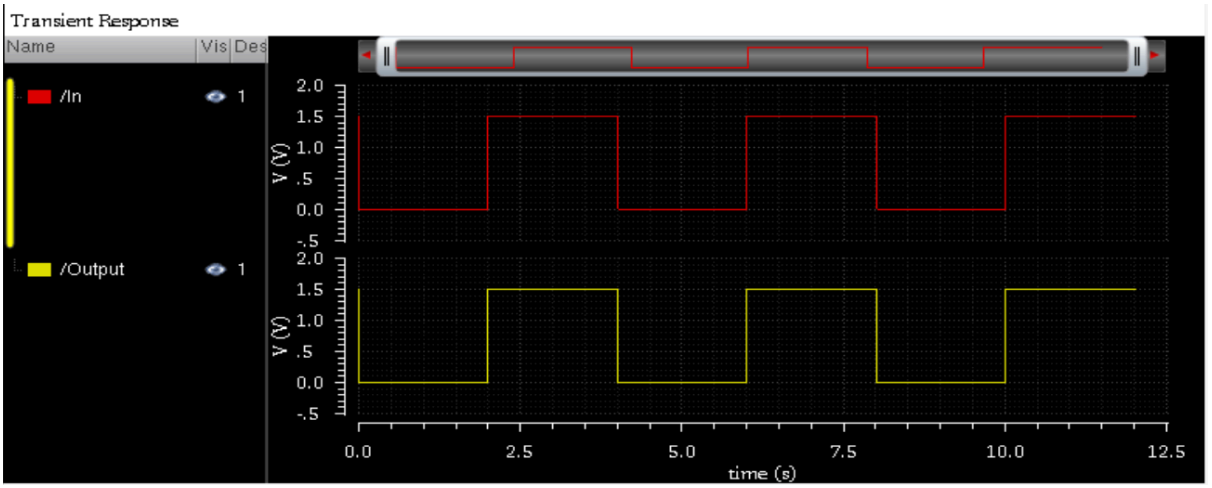


Output Waveform:

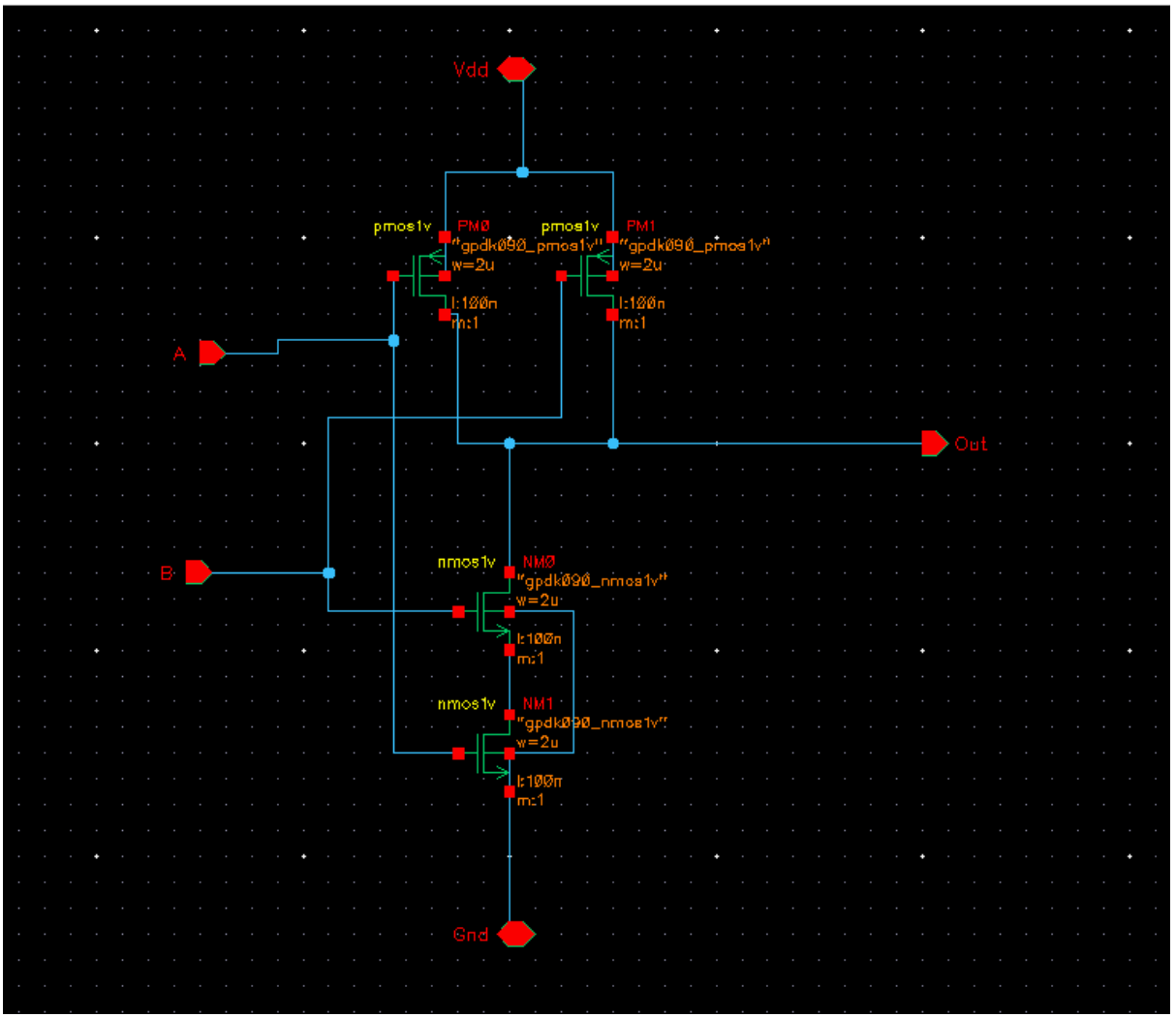


Nand Gate:

Truth Table:

INPUT (A)	INPUT (B)	OUTPUT (Z)
0	0	1
0	1	1
1	0	1
1	1	0

Schematic:



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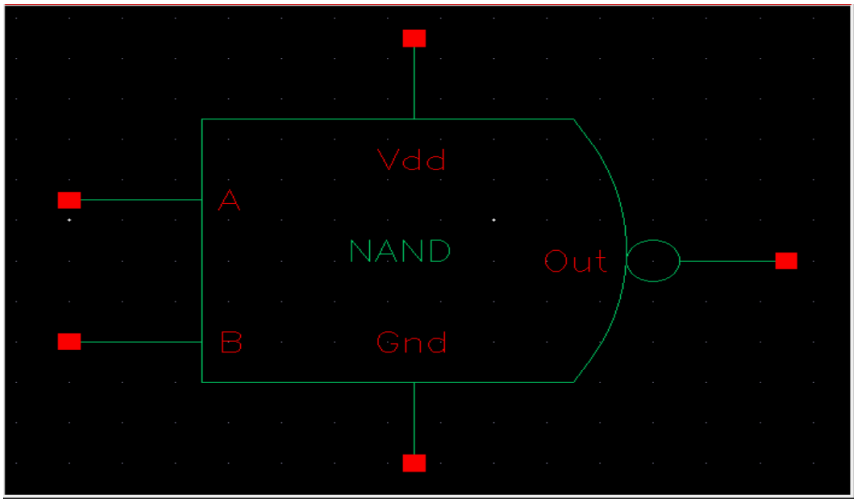
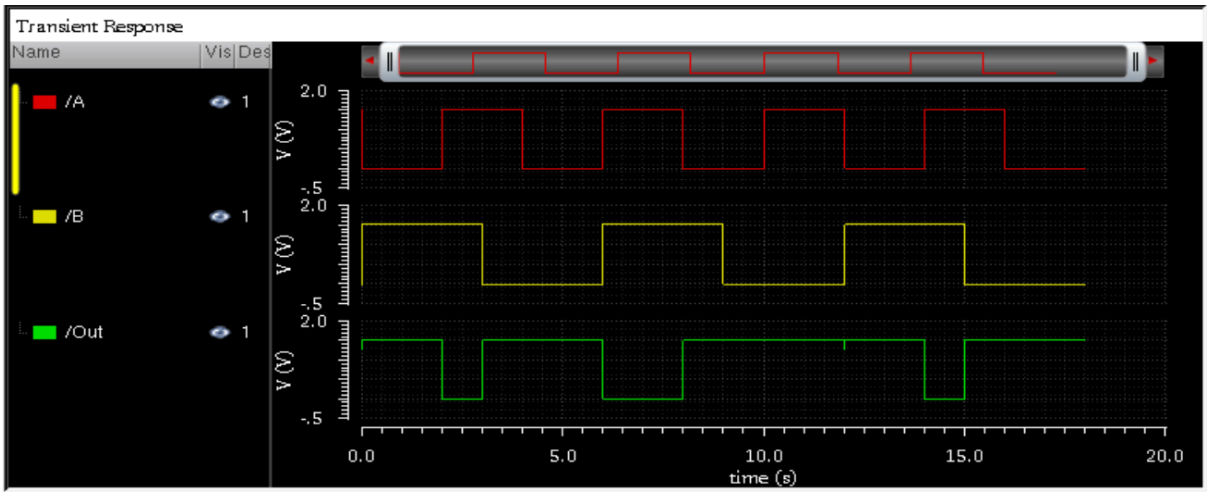


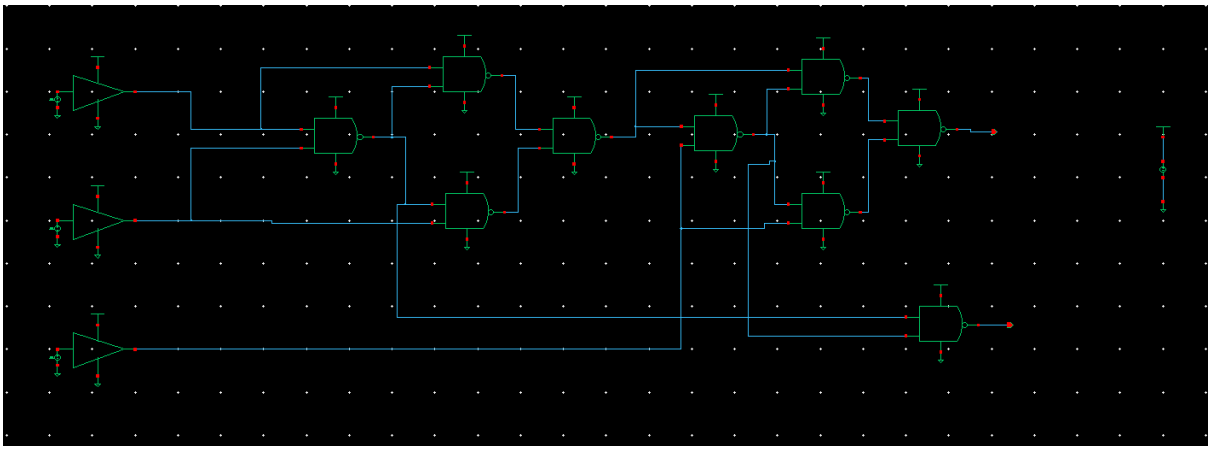
Output Waveform:



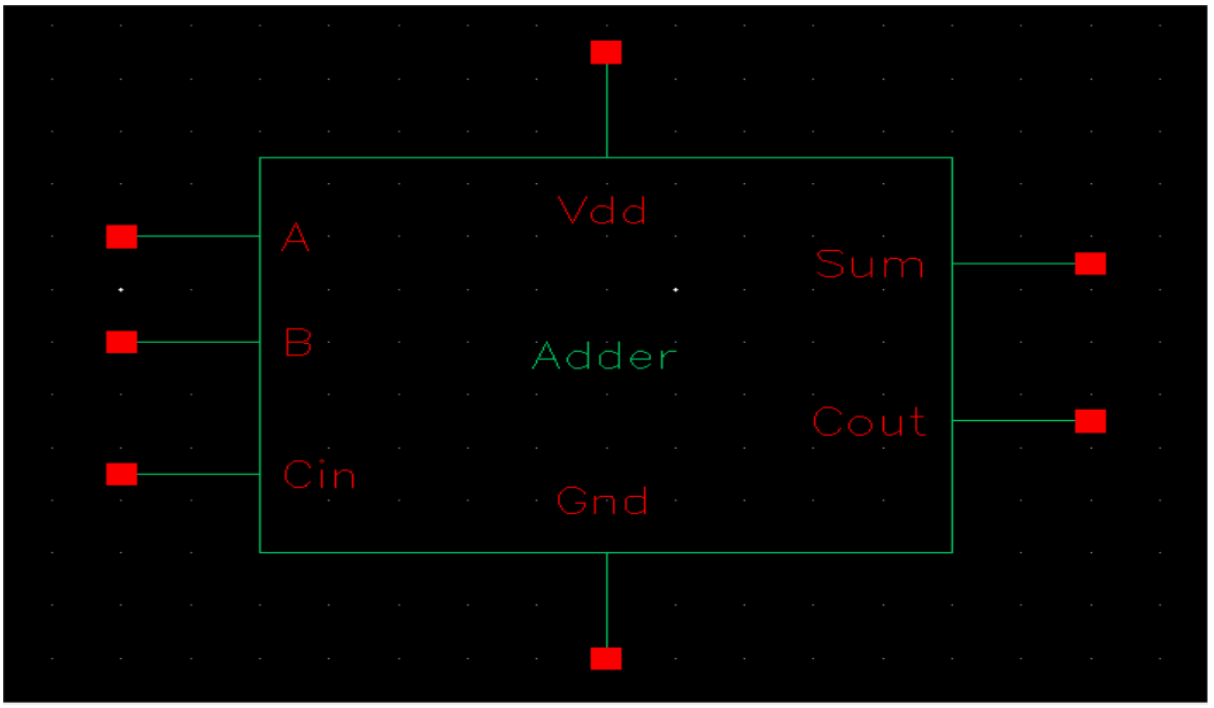
1 Bit Full Adder :

One bit Full Adder is now implemented using Nand gates.
It consists of Inputs: A, B, Cin which represents Two one bit numbers and a carry bit.
Has Outputs of Sum, Carry.
The logical equivalent of Sum is Sum = (A ⊕ B ⊕ Cin)
The logical equivalent of Carry is Cout = (AB + BCin + ACin)

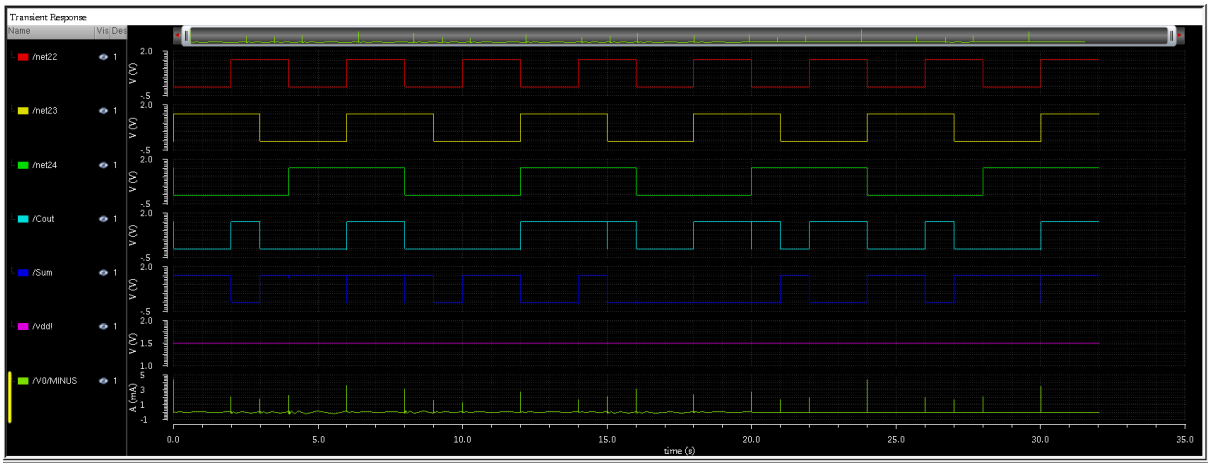
Schemetic:



Symbol:



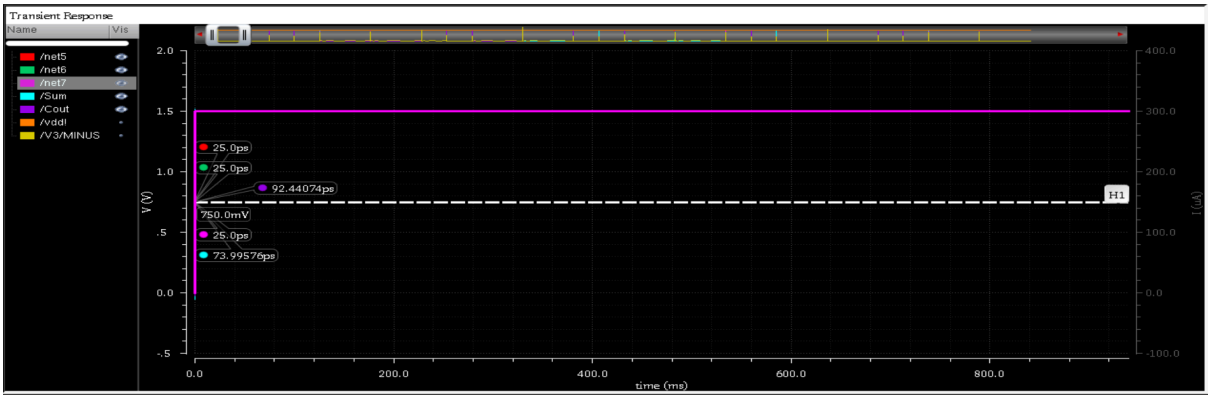
Output Waveform:



Delays:
We generally measure delays at 50 percent of input signal value.
We gave the raise and fall time delay as 50ps.

Create a marker at 50% of Vdd

Vdd 50% = 1.5*0.5
Vdd 50% = 0.75 V



Here if we observe that the input was changed at 25 ps
T1 = 25ps
The output Carry is changed at 92.44074 ps
T2 = 92.44074 ps
Tdelay = T2 - T1
= 92.44074 ps - 25 ps

Tdelay = 67.44074 ps

Power :

Generally the power is calculated by taking the average of all current samples.

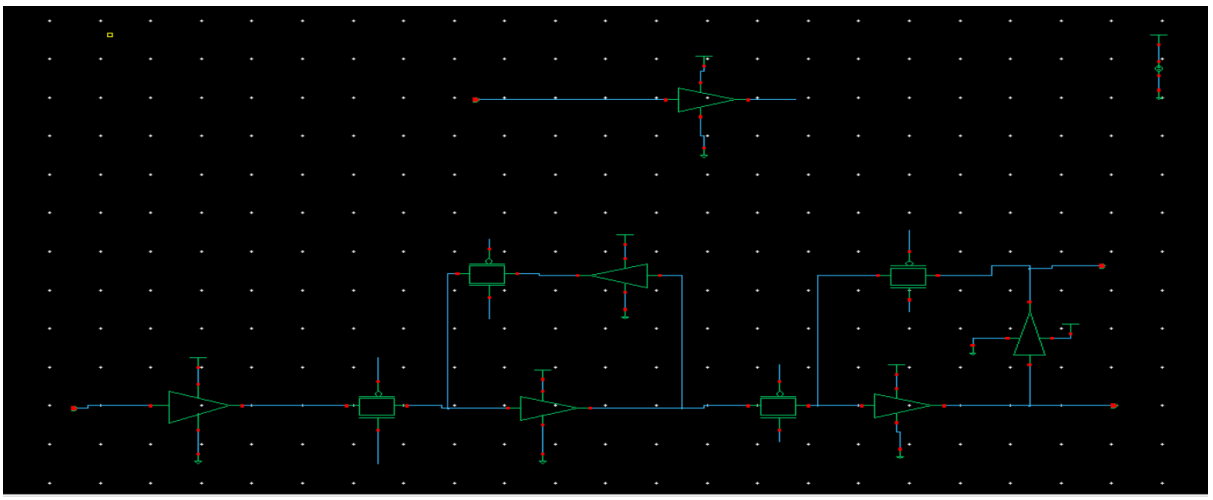
	Expression	Value
1	average(v("/v...	1.307E-6

So the Average power obtained is Pavg = 1.307 uWatt.

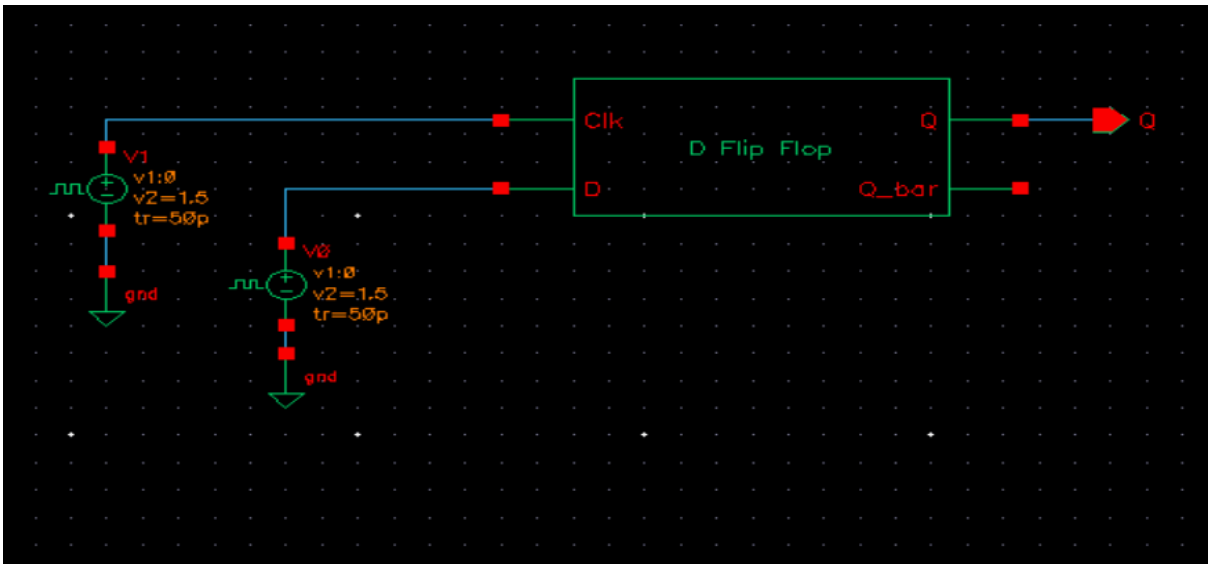
Edge Triggered D-Flip Flop:

Here the Flip flop is a sequential circuit where the clock is present for Synchronization.
When the positive edge occurs the data is stored in a flip flop and produced as output until the next clock edge.

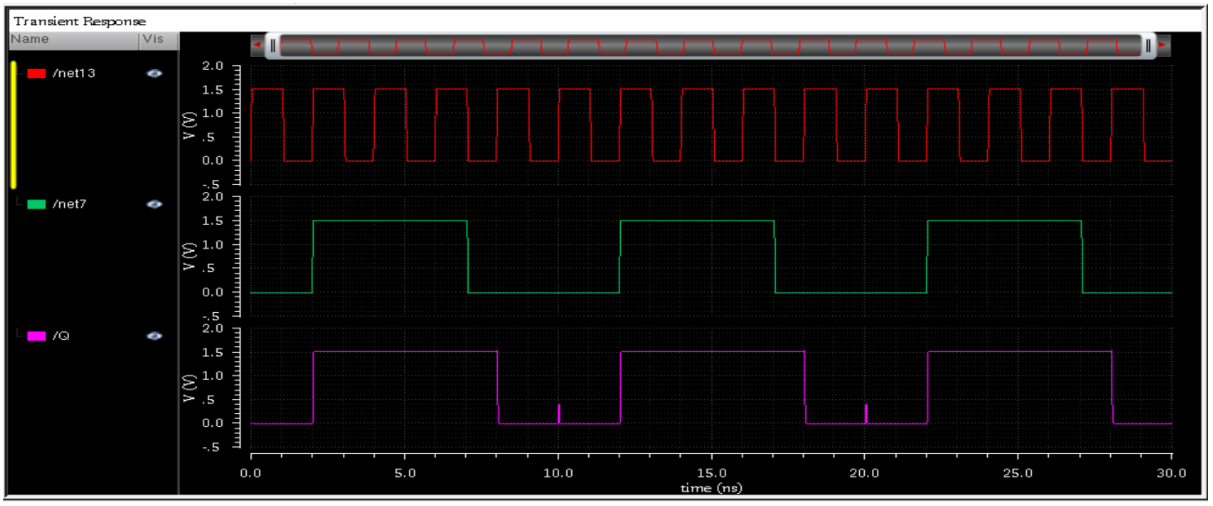
Schematic:



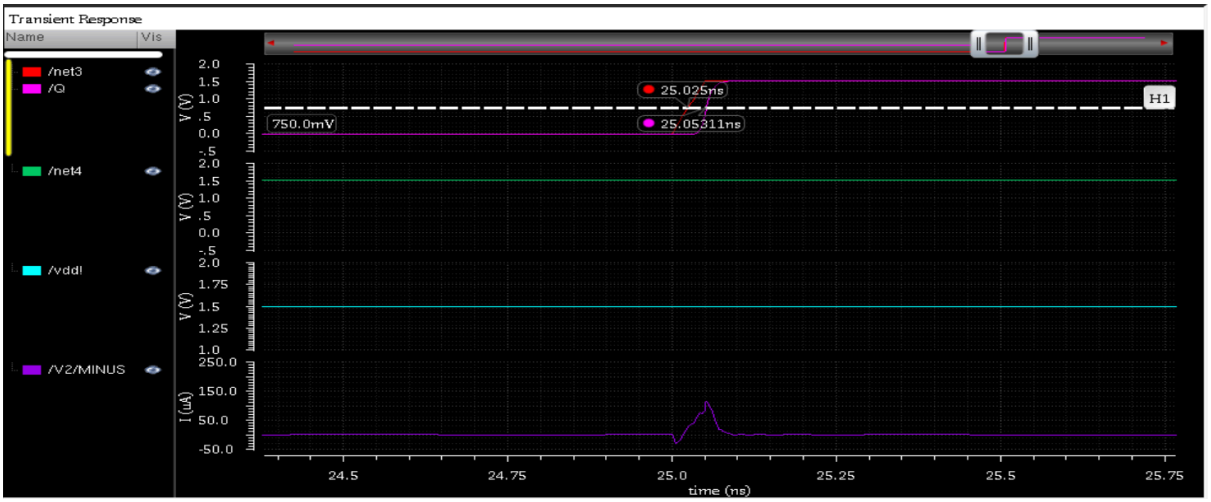
Symbol:



Output Waveform:



Clock to q delay:

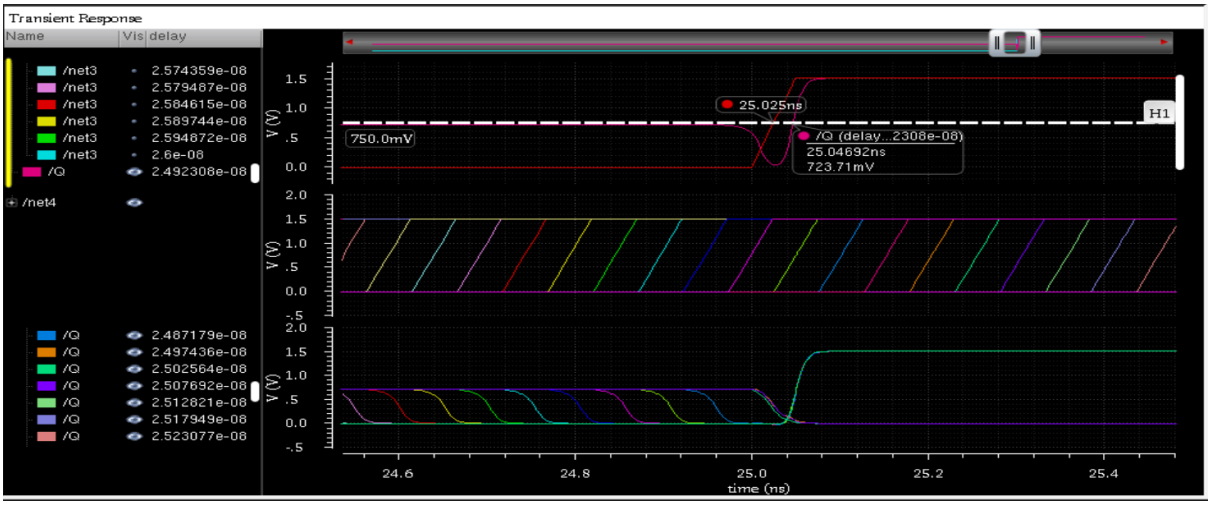


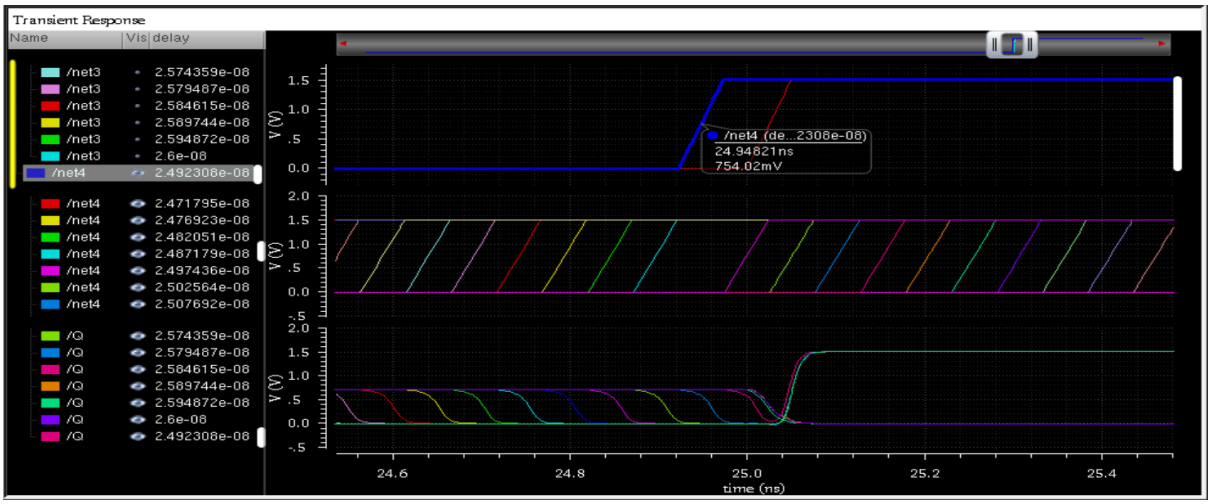
Tc-q = Tclk - Tq
Tclk = 25.025 ns
Tq = 25.05311 ns

Tc-q = 25.05311 - 25.025 ns
Tc-q = 0.02811 ns
Tc-q = 28.11 ps

Setup Time: The minimum time at which the data should be available to the flip flop so that the data can be propagated into the flip flop properly.
Now to find the setup time, we should perform parametric analysis.

At last, raising edge of q you will get 5 % more than Tclk-q delay so we use that value of d and measure setup time.





Td = 24.94821 ns
Tclk = 25.025 ns
Tsu = Tclk - Td
= 25.025 ns - 24.94821 ns
Tsu = 76.79 ps

Power:

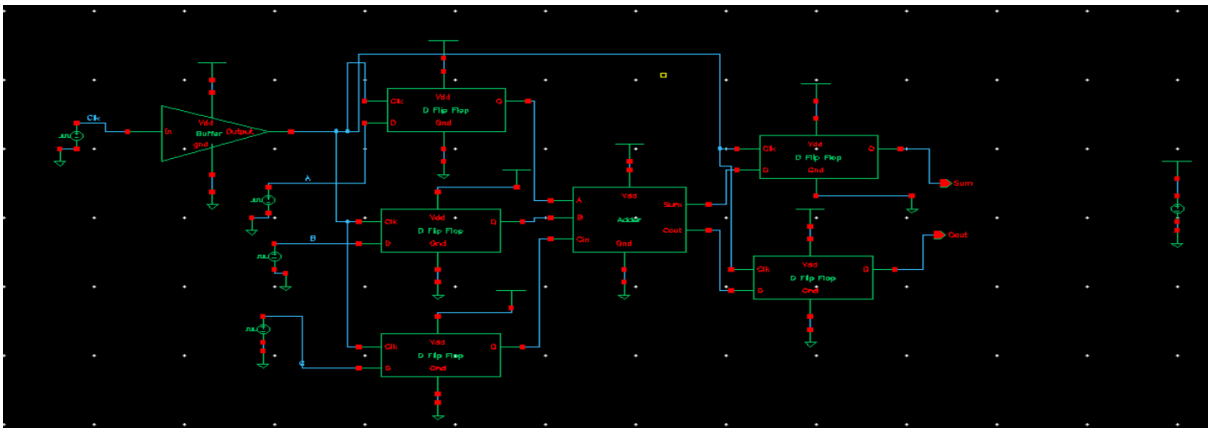
	Expression	Value
1	average(v("/v...	9.366E-6

The average power obtained is Pavg = 9.366 uWatt

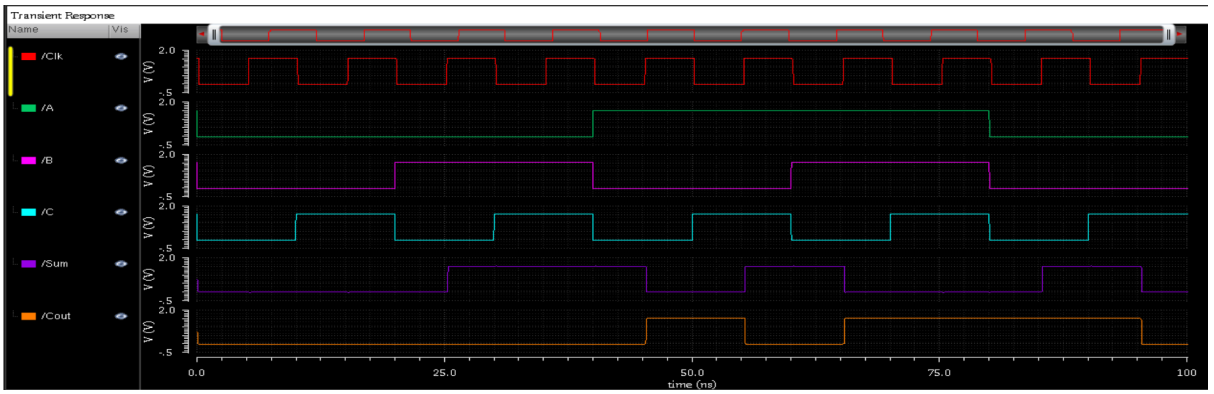
Integration of Flip Flop and Adder:

Now we will integrate the flip flop and adder so that the result can be stored for a clock cycle in the flip flop.

Schematic:



Output waveform:



Now the max clock frequency it can be operated is

Tclk=Tsu+Tc-q+Tcomb

= 76.79 + 28.11 + 67.44 ps

Tclk = 172.34 ps

F_max = 1 / Tclk

= 1 / 172.34 ps

F_max = 5.802 GHz

It can operate at a maximum clock speed of 5.802 GHz.

Simulation Results:

S.No	Design	No. TXs	Total Area	Max Delay	Avg power	PDP
1.	Full Adder	36	0.648 pm^2	67.44 ps	8.511 uWatt	0.5739 fWattS
2.	Flip Flop	20	0.324 pm^2	28.11 ps	9.366 uWatt	0.2632 fWattS
3.	Integrated	136	2.268 pm^2	172.34 ps	20.40 uWatt	3.5157 fWattS

Conclusion:

This project has provided a comprehensive exploration into the design and implementation of fundamental digital circuits using CMOS technology, emphasizing both combinational and sequential logic elements. Through the effective use of Cadence Virtuoso and 90nm technology, we have successfully designed, simulated, and analyzed essential circuits including the CMOS inverter, buffer, NAND gate, 1-bit full adder, edge-triggered D flip-flop, and the integration of the full adder with a flip-flop.

The design phase focused on understanding the role of transistor sizing, power consumption, propagation delays, and circuit reliability. Careful attention was paid to voltage thresholds and sizing parameters like a 1.5V supply, channel width of 120nm, and length of 120nm to ensure optimal performance under the set technological constraints.

Simulation results validated the theoretical behavior of each component, confirming correct logic outputs and expected delay characteristics. Specifically, the 1-bit full adder demonstrated efficient logic performance with minimal power consumption and delay, while the edge-triggered D flip-flop showed precise data synchronization, essential for sequential circuit design. The integration of the flip-flop with the full adder not only verified functional correctness but also highlighted the practical challenges of timing constraints, which were addressed by calculating setup time, clock-to-Q delay, and maximum operating frequency — which reached an impressive 5.802 GHz.

Overall, this project reinforced the importance of accurate modeling, layout planning, and simulation verification in modern VLSI design. It also showcased the delicate trade-offs between speed, power, and area that designers must manage in real-world chip design.

The End