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A High-Speed Low-Power Two-Stage Comparator with Regeneration Enhancement and Through Current Suppression Techniques

Chia-Wei Pai, and Hiroki Ishikuro
Department of Electronics and Electrical Engineering, Keio University, Yokohama, Japan
Email: paicw@iskr.elec.keio.ac.jp

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***Abstract*—This paper presents a high-speed low-power two-stage dynamic comparator for SAR ADC. The pre-amplifier of the proposed comparator uses the dynamic bias technique to save power. To increase the output voltage difference of the pre-amplifier, the StrongARM latch is inserted. The proposed latch keeps a cross-coupled inverter to ensure good positive feedback ability. The tail current source is replaced by the input pair to save power. The auxiliary input pair speeds up the regeneration of the latch. Simulation results demonstrate that the proposed comparator with V_{DD} = 1.8 V achieved a clock-to-Q delay of 228 ps and an input-referred noise of 479 μV at V_{id} = 1 mV and V_{CM} = 0.9 V. The proposed comparator consumes 196.3 fJ per comparison with 1.024 GHz.**

Keywords—Dynamic comparator, two-stage comparator, double-tail latch-type comparator, dynamic bias, charge steering, StrongARM, analog-to-digital converter (ADC), SAR ADC.

I. INTRODUCTION

Dynamic comparators, also called regenerative comparators, are the widely used core block for ADC and determine the performance of ADC. In recent years, SAR ADC has become the most popular choice because of its low power consumption, medium to high resolution, and medium conversion speed. Many applications require high-speed and low-power ADC, such as ultra-wideband radios [1]. To realize high-speed and low-power ADC, improving the speed and power consumption of the comparator is straightforward.

The StrongARM latch-type comparator [2] is one of the most popular dynamic comparators because it has almost no static power consumption. However, its design degree of freedom is limited.

Two-stage dynamic comparator consists of the pre-amplifier stage (1st stage) and the latch stage (2nd stage). By separating each stage, it is more suitable for lower supply voltage because of the more headroom margin. Isolation between the amplifier and latch provides better amplification and reduces the kickback noise. Also, it allows the input common-mode voltage can be up to near the supply voltage V_{DD} because there is no need to consider the gate-source voltage V_{GS} of the latch like the StrongARM latch-type comparator. Therefore, the two-stage dynamic comparator has more design degree of freedom.

The double-tail dynamic comparator shown in Fig. 1 [3] is a two-stage comparator designed for high-speed operation. Two tail current sources allow determining the speed of each stage independently. However, as shown in Fig. 1, the direct current from the power supply V_{DD} to the ground GND causes the through current and thus more power consumption before the regeneration is completed. This is a severe problem especially when the input voltage is small. The smaller the input voltage, the time the through-current flowing longer. Therefore the power consumption increases.

The dynamic bias comparator shown in Fig. 2 [4] has attracted much attention in recent years because of its low power consumption. By inserting a capacitor under the tail current source of the pre-amplifier stage, the discharging current of the drain node ON and OP of input pair M_1 and M_2 charges the capacitor C_t and reduces the tail current in the amplification phase. The drain node ON and OP of input pair M_1 and M_2, therefore, discharge partially and thus save energy. Although the power consumption is low, it suffers a speed decrease.

The StrongARM latch-type comparator using the dynamic bias technique is presented in [5] for low power consumption. However, the output voltage is not rail-to-rail due to the partial discharging. To guarantee the correct logic level, [5] applies a clock whose duty cycle is more than 50% which means it needs more time to obtain the correct comparison result. From the viewpoint of designing the SAR ADC, it spends more time to convert each bit because each conversion of SAR ADC starts when the previous comparison result is determined. The non-rail-to-rail output voltage also made the conversion time longer due to the not enough overdrive voltage of logic circuits. Therefore, it is not suitable for high-speed SAR ADC.

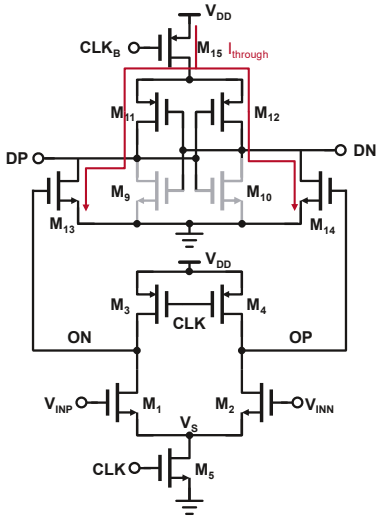


Fig. 1. Double-tail dynamic comparator [3].

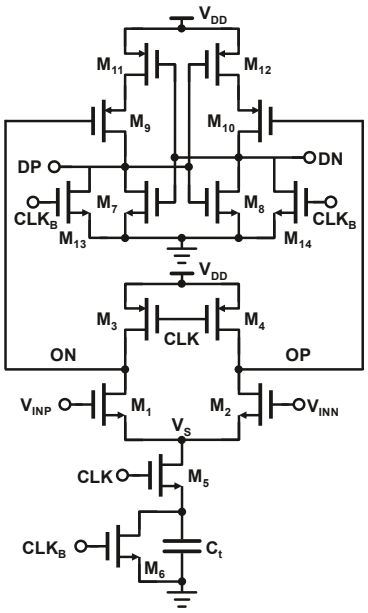


Fig. 2. Dynamic bias comparator [4].

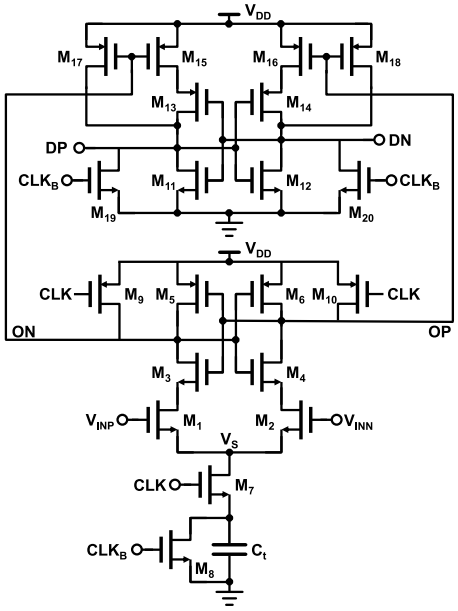


Fig. 3. Proposed two-stage dynamic comparator.

To lower the power consumption of SAR ADC, a lot of switching schemes have been proposed, such as a monotonic switching scheme [6], and a bidirectional switching scheme [7]. However, those suffer the common-mode voltage variation of the comparator. The common-mode voltage variation causes the power consumption, speed, and noise of the comparator to change. To guarantee the best performance of SAR ADC, it is important to determine if the comparator is operating at the best performance.

This paper proposed a high-speed and low-power two-stage dynamic comparator. The pre-amplifier stage applied the dynamic bias technique [4] to save power consumption and used the positive feedback of StrongARM latch to enhance speed, the architecture same as [5]. The proposed 2nd stage has gain-enhancement input pair to speed up and save power consumption by suppressing the through current.

The rest paper is organized as follows. In Section II, the operation and design of the proposed comparator are described. Section III describes the simulation results. Section IV concludes this paper.

II. Proposer Two-Stage Dynamic Comparator

Fig. 3 presents the proposed high-speed and low-power two-stage dynamic comparator. The speed-enhancement pre-amplifier stage applied the dynamic bias technique for saving power. The positive feedback of StrongARM latch speeds up not only the amplification speed but also the regeneration speed of the latch in the 2nd stage. The low-power gain-enhancement latch in the 2nd stage has two input pairs $M_{15,\ 17}$ ($M_{16,\ 18}$) to sense the output voltage of the 1st stage. Instead of the tail current source, the two input pairs not only enhance input gain but also suppress the through current, therefore, saving power.

A. Operation of the Proposed Comparator

The operation of a dynamic comparator has two phases: the reset phase and the comparison phase. In the proposed dynamic comparator, during the reset phase ($CLK = GND$, $CLK_B = V_{DD}$), M_8 turns ON. The capacitor C_t discharges through M_8. M_9 (M_{10}) turns ON and ON (OP) is charged to V_{DD}, ensuring the initial state is determined. M_{19} (M_{20}) turns ON, and DP (DN) discharges to GND. In this paper, the comparison phase is further divided into two phases: the amplification phase and the regenerative phase. During the amplification phase ($CLK = V_{DD}$, $CLK_B = GND$), M_7 turns ON, and M_1 and M_2 start to sense and amplify the input signal. When the voltage difference between the OP/ON and the drain node of M_1/M_2 is greater than the threshold voltage V_{thN}, the StrongARM latch is active and rapidly amplifies the voltage difference between ON and OP. When ON/OP is below $V_{DD} - |V_{thP}|$, the input pair $M_{15,\ 17}$ ($/M_{16,\ 18}$) of the 2nd stage amplifies the output voltage ON (OP) of the 1st stage. Then, when DP/DN is greater than V_{thN}, the regeneration starts and finally decides whether V_{INP} is greater than V_{INN}.

B. Design of the Proposed Pre-amplifier Stage

The timing waveform of the proposed dynamic comparator is shown in Fig. 4(a). Fig. 4(b) is the timing waveform of the dynamic bias comparator for comparison.

As shown in Fig. 4(b), the voltage difference between ON and OP is very small. The dynamic bias technique saves power consumption by decreasing the tail current and therefore the ON (OP) discharges partially. The gradually decreasing tail current attenuates the voltage difference between ON and OP. In other words, the amplification is also attenuated. This is the reason that the dynamic bias technique slows down the comparison. The regeneration of the latch in the 2nd stage suffers from the small voltage difference of ON and OP.

The proposed pre-amplifier improves the amplification by inserting the StrongARM latch. As shown in Fig. 4(a), this results in not only a greater voltage difference in the output of the 1st stage and also the speed enhancement of comparison. The voltage difference becomes larger thanks to the positive feedback of the StrongARM latch. This also accelerates the regeneration of the next latch stage because the more the

difference is, the more effective the positive feedback of the latch in the 2nd stage.

C. Design of the Proposed Latch Stage

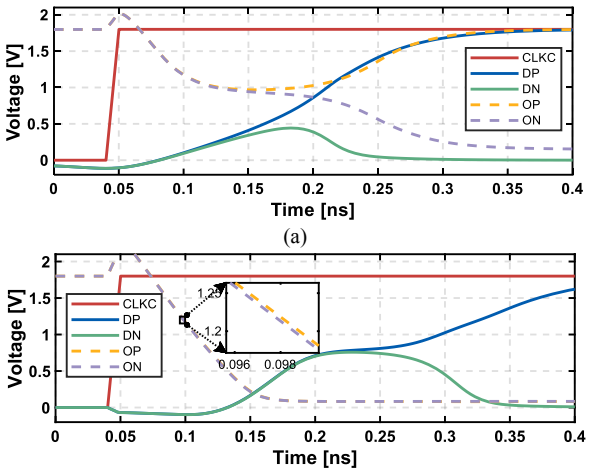
As mentioned before, the double-tail comparator (Fig. 1) uses a high-speed latch though it has a large through current and thus more power consumption. During the comparison, this through current still flows from V_{DD} to GND until the voltage of ON/OP $V_{ON}/V_{OP} < V_{thN}$. The dynamic bias comparator (Fig. 2) uses a low-power latch. By inserting the PMOS input pair M_9 and M_{10} into the middle of the path and removing the tail current source, the through current is suppressed. At the beginning of the regeneration phase ($V_{ON}/V_{OP} < V_{DD} - |V_{thP}|$), the regeneration, also means the positive feedback, is weakened due to the overdrive voltage V_{ov} being very small and the current being also very small. And the small output voltage difference of the 1st stage further degrades the regeneration. This, however, results in the slow operation of the latch in the 2nd stage. The power consumption is also increased due to the time both NMOS and PMOS turning ON becoming longer and thus the through current flows more.

The proposed latch keeps the cross-coupled inverter so that it does not weaken the positive feedback. Therefore, unlike the latch of the dynamic bias comparator (Fig. 2), the latch keeps high-speed operation. By replacing the tail current source with an input pair M_{15} and M_{16}, there is no through current path. However, this also damages the speed because at the beginning the V_{ov} of the input pair is small, and the current is also small. To speed up the regeneration, M_{17} and M_{18} are added as auxiliary input pairs. M_{17} (M_{18}) also senses the ON (OP). And, connecting the output of M_{17} (M_{18}) to DP (DN) accelerates the turn-on speed of M_{11} (M_{12}). Although M_{17} and M_{18} make another through current path, the through current flows very short time, and therefore the power consumption is not a severe problem. Fig.5(a) shows that the current of the proposed comparator is smaller than the current of the dynamic bias comparator. As shown in Fig. 4(a), the difference between ON and OP becomes larger during the regeneration phase. This also helps to speed up the regeneration. Therefore, the proposed latch achieved high-speed operation and low power consumption.

III. Simulation Results

All three comparators have been designed and simulated using 180-nm CMOS technology with V_{DD} = 1.8 V. For a fair comparison, the size of the input pair of all comparators is the same in order to have similar characteristics. The bias point of the dynamic bias and proposed pre-amplifier is also designed at a similar point. Fig. 5(b) shows the voltage V_S of the proposed comparator and the dynamic bias comparator. They are almost the same value at the amplification phase so both the transconductance (gm) of the input pair are the almost same value and thus they have similar performances. And the latch in the 2nd stage of the different comparators is designed at the same aspect ratio, although the latch architecture is different.

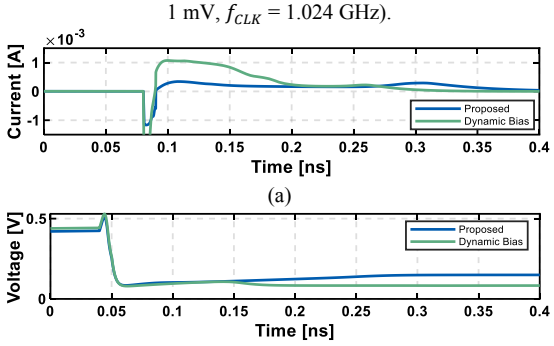
From the viewpoint of designing the SAR ADC, the common-mode voltage V_{CM} variation of the comparator affects the performance of SAR ADC, for example, large variation results in large SNDR variation [8]. Another conclusion from [8] is that the best FoM of the comparator is obtained at about



(a)

(b)

Fig. 4. (a) Timing waveform of the proposed dynamic comparator and (b) timing waveform of the dynamic bias comparator (V_{CM} = 0.9 V, $V_{INP} - V_{INN}$ = 1 mV, f_{CLK} = 1.024 GHz).



(a)

(b)

Fig. 5. (a) Current waveform (b) bias voltage waveform of the proposed dynamic comparator and the dynamic bias comparator (V_{CM} = 0.9 V, $V_{INP} - V_{INN}$ = 1 mV, f_{CLK} = 1.024 GHz).

$V_{DD}/2$ ($= V_{CM}$). Therefore, it is important to design a switching scheme that has less V_{CM} variation or even no V_{CM} variation. Considering the design of a comparator for a specific SAR ADC, it must match the structure of the SAR ADC in order to achieve the best performance.

Assuming that a 10-bit 100 MHz SAR ADC, the LSB is about 1.75 mV with V_{DD} = 1.8 V. The input differential voltage of the comparator, therefore, is set at 1 mV which is smaller than 1 LSB. The clock frequency is 1.024 GHz.

Fig. 6 shows the Energy/comparison as a function of V_{CM}. The proposed comparator has the smallest energy from V_{CM} = 0.7 V to V_{DD}.

The Clock-to-Q delay (CLK-Q delay) is defined as the time from the rising edge of the clock reaching $V_{DD}/2$ to the output difference reaching $V_{DD}/2$. Fig.7 shows the CLK-Q delay as a function of V_{CM}. Although the proposed comparator is slower than the double-tail comparator, it is faster than the dynamic bias comparator thanks to the proposed techniques. At V_{CM} = 0.7 V, Both the proposed comparator and the dynamic comparator can not have a rail-to-rail output. The results at V_{CM} = 0.7 V are just for reference.

Fig. 8 shows the input-referred noise as a function of V_{CM}. All comparators have been designed to have similar noise at $V_{DD}/2 = V_{CM} = 0.9\,V$, which satisfied the required SNDR of

TABLE I. PERFORMANCE COMPARISON

	This Work (Simulation results)			Dynamic Bias JSSC'18 [4]	TVLSI'14 [9]	Access'19 [10]
	Proposed	Dynamic Bias	Double-tail			
Technology [nm]	**180**	180	180	65	180	180
Supply Voltage [V]	**1.8**	1.8	1.8	1.2	1.2	1.2
Frequency [GHz]	**1.024**	1.024	1.024	0.05	0.5	2
Energy/Comparison [fJ]*	**196.3**	227.7	356.3	34	660	112.5
Clock-to-Q Delay [ps]*	**228**	270	173	1200	550	>800
Noise 1σ [uV]*	**479**	477.4	474.8	400	7800	–
FoM $[(\text{fJpsuV})^{-1}10^{9}]$*	**46.65**	34.07	34.16	61	0.35	–
FoM w/o Noise $[(\text{fJps})^{-1}10^{5}]$*	**2.18**	1.59	1.58	2.45	0.28	<1.11

*Under this situation: $V_{CM} = V_{DD}/2$, $V_{id} = 1\ mV$

the assuming SAR ADC. The proposed comparator has lower input-referred noise than the dynamic bias comparator.

For comparison, [8] defined an FoM expressed as

$$FoM = \frac{1}{Power \cdot Delay \cdot Noise}. \quad (1)$$

Fig. 9 shows the FoM as a function of V_{CM}. The proposed comparator has better FoM than the dynamic bias comparator. Compared to the double-tail comparator, the proposed comparator has a better FoM below V_{CM} = 1.1 V. Above V_{CM} = 1.1 V, it also has a competitive performance. From the viewpoint of designing SAR ADC, for example, a bidirectional switching scheme [7] results in the input common-mode voltage of the comparator goes to near $V_{DD}/2$ during the conversion cycle. The voltage difference at LSB-side is smaller than MSB-side, spending more time to complete the conversion. It is more desirable to make the comparator operate at a high FoM region. Therefore, the proposed comparator can improve the performance of the bidirectional switching scheme SAR ADC because, at LSB-side, the proposed comparator can operate at the highest FoM.

This paper defined another FoM for speed orientation, just removing the input-referred noise from (1). Fig. 10 shows the speed orientation FoM. The proposed comparator achieved the best speed-power performance. It is very suitable for medium-resolution high-speed SAR ADC.

Table I compared the proposed comparator and the other comparators. The original dynamic bias comparator [4] has the best FoM. However, its speed is very slow. If speeding up the dynamic bias comparator, our results show that the proposed comparator has the best FoM, not the dynamic bias comparator. Therefore, the proposed comparator has the best balance between power consumption and speed. It is more suitable for high-speed high-performance ADC.

IV. CONCLUSION

In this paper, a high-speed low-power dynamic comparator is presented. The simulation results show that the proposed comparator achieved the best FoM thanks to the proposed positive feedback enhancement pre-amplifier and the low-power high regeneration ability latch. The proposed comparator is suitable for realizing high-speed and low-power SAR ADC. It will achieve the best performance if the common-mode voltage of the comparator is lower than $V_{DD}/2$.

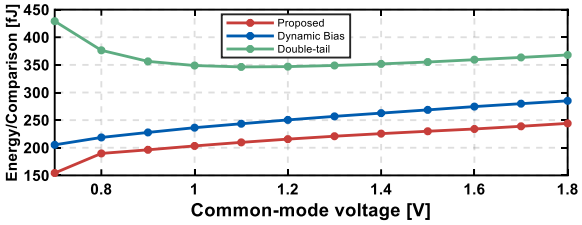


Fig. 6. Energy per comparison versus common-mode voltage

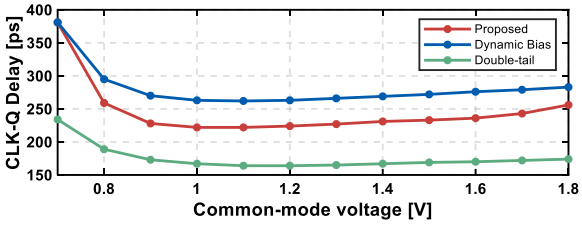


Fig. 7. Clock-to-Q delay versus common-mode voltage.

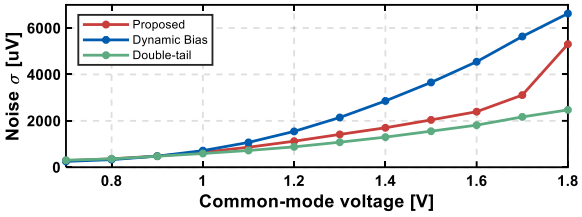


Fig. 8. Input-referred noise versus common-mode voltage.

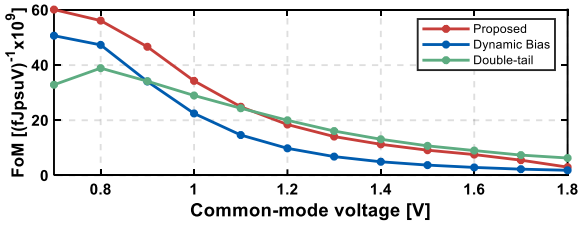


Fig. 9. FoM versus common-mode voltage.

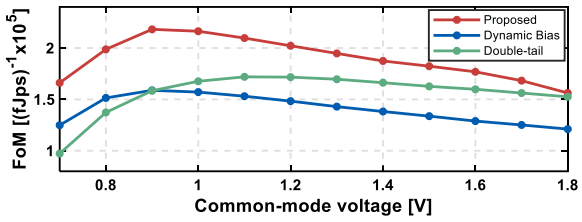


Fig. 10. Speed orientation FoM versus common-mode voltage.

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